

M5M5Y416CWG -70HI, -85HI

Preliminary

*Notice: This is not a final specification.
Some parametric limits are subject to change.*

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

Those are summarized in the part name table below.

DESCRIPTION

The M5M5Y416C is a family of low voltage 4-Mbit static RAMs organized as 262144-words by 16-bit, fabricated by Mitsubishi's high-performance 0.18µm CMOS technology.

The M5M5Y416C is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5Y416CWG is packaged in a CSP (chip scale package), with the outline of 7.0mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

FEATURES

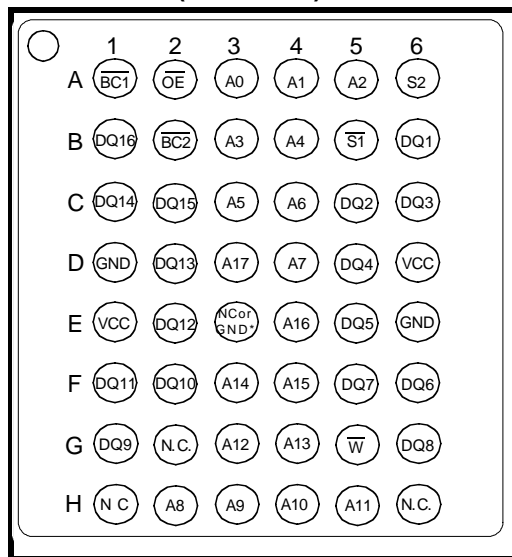
- Single 1.65~2.3V power supply
- Small stand-by current: 0.2µA (2.0V, typ.)
- No clocks, No refresh
- Data retention supply voltage =1.3V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by $\overline{S1}$, $\overline{S2}$, $\overline{BC1}$ and $\overline{BC2}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Process technology: 0.18µm CMOS
- Package: 48ball 7.0mm x 8.5mm CSP

Version, Operating temperature	Part name	Power Supply	Access time max.	Stand-by current (µA)						Active current I _{cc1} (2.3V, max)
				* Typical		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
I-version -40 ~ +85°C	M5M5Y416CWG -70HI	1.65 ~ 2.3V	70ns	0.2	0.4	1	2	8	15	30mA (10MHz) 3mA (1MHz)
	M5M5Y416CWG -85HI	1.65 ~ 2.3V	85ns							

* Typical parameter indicates the value for the center of distribution at 2.0V, and not 100% tested.

PIN CONFIGURATION

(TOP VIEW)



Pin	Function
A0 ~ A17	Address input
DQ1 ~ DQ16	Data input / output
$\overline{S1}$	Chip select input 1
$\overline{S2}$	Chip select input 2
\overline{W}	Write control input
\overline{OE}	Output enable input
$\overline{BC1}$	Lower Byte (DQ1 ~ 8)
$\overline{BC2}$	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply

Outline: 48FJA

NC: No Connection

*Don't connect E3 ball to voltage level more than 0V



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FUNCTION

The M5M5Y416CWG is organized as 262144-words by 16-bit. These devices operate on a single +1.65~2.3V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs $\overline{BC1}$, $\overline{BC2}$, $\overline{S1}$, $S2$, \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write operation is executed whenever the low level \overline{W} overlaps with the low level $\overline{BC1}$ and/or $\overline{BC2}$ and the low level $\overline{S1}$ and the high level $S2$. The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{BC1}$ and/or $\overline{BC2}$ and $\overline{S1}$ and $S2$ are in an active state($\overline{S1}=L, S2=H$).

When setting $\overline{BC1}$ at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting $\overline{BC2}$ at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

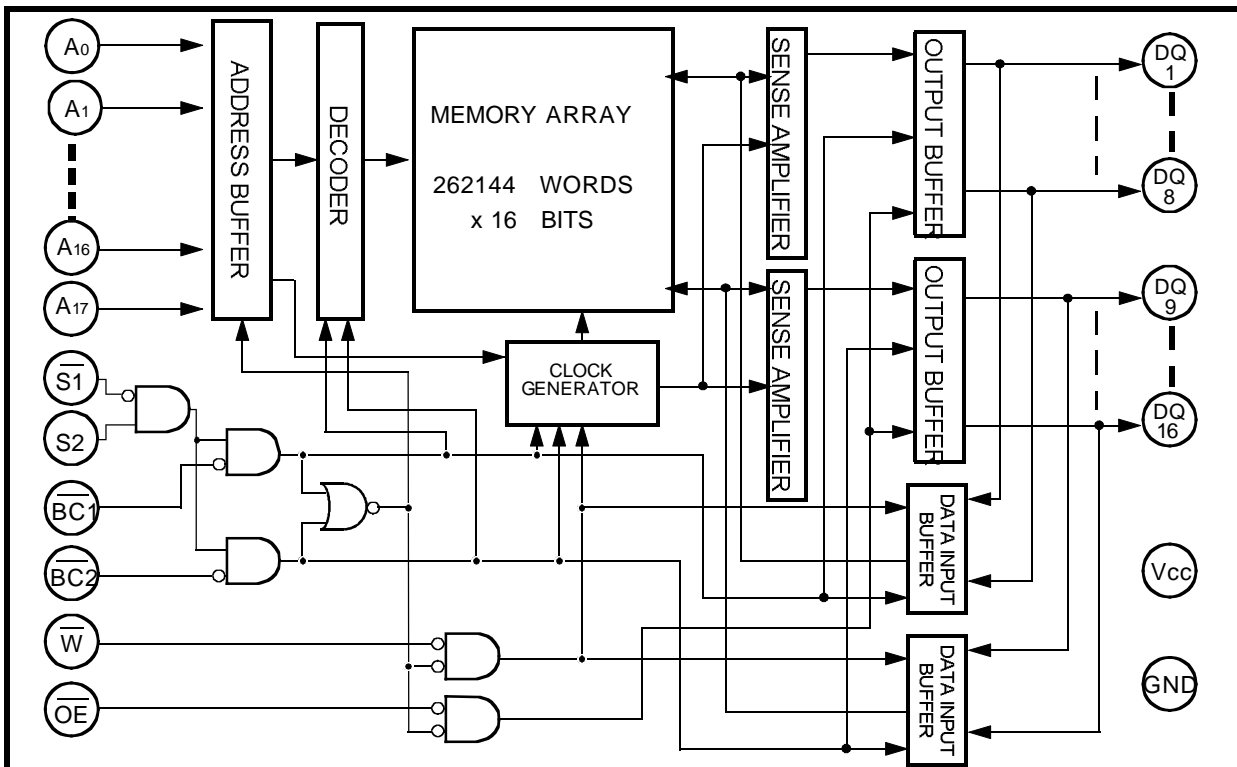
When setting $\overline{BC1}$ and $\overline{BC2}$ at a high level or $\overline{S1}$ at a high level or $S2$ at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC1}$, $\overline{BC2}$ and $\overline{S1}$, $S2$.

The power supply current is reduced as low as 0.2 μ A(25°C, typical), and the memory data can be held at +1.3V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	$S2$	$\overline{BC1}$	$\overline{BC2}$	\overline{W}	\overline{OE}	Mode	DQ1~8	DQ9~16	Icc
H	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
L	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	————	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	————	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	————	High-Z	High-Z	Active

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V _{CC}	Supply voltage	With respect to GND	-0.5* ~ +2.7	V
V _I	Input voltage	With respect to GND	-0.2* ~ V _{CC} + 0.2 (max. 2.7V)	
V _O	Output voltage	With respect to GND	0 ~ V _{CC}	
P _d	Power dissipation	T _a =25°C	700	mW
T _a	Operating temperature	I-version	- 40 ~ +85	°C
T _{stg}	Storage temperature		- 65 ~ +150	°C

* -0.7V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=1.65~ 2.3V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units	
			Min	Typ	Max		
V _{IH}	High-level input voltage		0.7 x V _{CC}		V _{CC} +0.2	V	
V _{IL}	Low-level input voltage		-0.2 *		0.4		
V _{OH}	High-level output voltage	I _{OH} = -0.1mA	1.3			V	
V _{OL}	Low-level output voltage	I _{OL} =0.1mA			0.2		
I _I	Input leakage current	V _I =0 ~ V _{CC}			±1	µA	
I _O	Output leakage current	BC1 and BC2=V _{IH} or S1=V _{IH} or S2=V _{IL} or OE=V _{IH} , VI/O=0 ~ V _{CC}			±1	µA	
I _{CC1}	Active supply current (AC,MOS level)	BC1 and BC2 ≤ 0.2V, S1 ≤ 0.2V, S2 ≥ V _{CC} -0.2V other inputs ≤ 0.2V or ≥ V _{CC} -0.2V Output - open (duty 100%)	f = 10MHz	-	18	30	mA
			f = 1MHz	-	1.5	3	
I _{CC2}	Active supply current (AC,TTL level)	BC1 and BC2=V _{IL} , S1=V _{IL} , S2=V _{IH} other pins =V _{IH} or V _{IL} Output - open (duty 100%)	f = 10MHz	-	18	30	mA
			f = 1MHz	-	1.5	3	
I _{CC3}	Stand by supply current (AC,MOS level)	(1) S1 ≥ V _{CC} - 0.2V, S2 ≥ V _{CC} - 0.2V, other inputs = 0 ~ V _{CC} (2) S2 ≤ 0.2V, other inputs = 0 ~ V _{CC} (3) BC1 and BC2 ≥ V _{CC} - 0.2V S1 ≤ 0.2V, S2 ≥ V _{CC} - 0.2V other inputs = 0 ~ V _{CC}	~ +25°C	-	0.2	1	µA
			~ +40°C	-	0.4	2	
			~ +70°C	-	-	8	
			~ +85°C	-	-	15	
I _{CC4}	Stand by supply current (AC,TTL level)	BC1 and BC2=V _{IH} or S1=V _{IH} or S2=V _{IL} Other inputs=0 ~ V _{CC}	-	-	0.5	mA	

* -0.7V in case of AC (Pulse width ≤ 30ns)

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

Note 2: Typical parameter indicates the value for the center of distribution at 2.0V, and not 100% tested.

CAPACITANCE

(V_{CC}=1.65 ~ 2.3V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			10	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	



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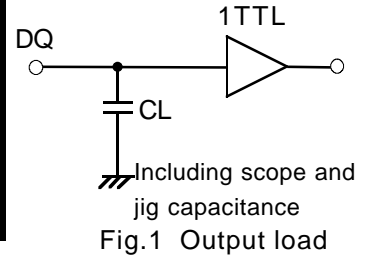
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AC ELECTRICAL CHARACTERISTICS (V_{CC}=1.65 ~ 2.3V, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	1.65~2.3V
Input pulse	V _{IH} =0.7 x V _{CC} +0.2V, V _{IL} =0.2V
Input rise time and fall time	5ns
Reference level	V _{OH} =V _{OL} =0.9V <small>Transition is measured ±200mV from steady state voltage.(for ten,tdis)</small>
Output loads	Fig.1,CL=30pF CL=5pF (for ten,tdis)



(2) READ CYCLE

Symbol	Parameter	Limits				Units
		70HI		85HI		
		Min	Max	Min	Max	
t _{CR}	Read cycle time	70		85		ns
t _{a(A)}	Address access time		70		85	ns
t _{a(S1)}	Chip select 1 access time		70		85	ns
t _{a(S2)}	Chip select 2 access time		70		85	ns
t _{a(BC1)}	Byte control 1 access time		70		85	ns
t _{a(BC2)}	Byte control 2 access time		70		85	ns
t _{a(OE)}	Output enable access time		35		45	ns
t _{dis(S1)}	Output disable time after $\overline{S1}$ high		25		30	ns
t _{dis(S2)}	Output disable time after $\overline{S2}$ low		25		30	ns
t _{dis(BC1)}	Output disable time after $\overline{BC1}$ high		25		30	ns
t _{dis(BC2)}	Output disable time after $\overline{BC2}$ high		25		30	ns
t _{dis(OE)}	Output disable time after \overline{OE} high		25		30	ns
t _{en(S1)}	Output enable time after $\overline{S1}$ low	10		10		ns
t _{en(S2)}	Output enable time after $\overline{S2}$ high	10		10		ns
t _{en(BC1)}	Output enable time after $\overline{BC1}$ low	10		10		ns
t _{en(BC2)}	Output enable time after $\overline{BC2}$ low	10		10		ns
t _{en(OE)}	Output enable time after \overline{OE} low	5		5		ns
t _{v(A)}	Data valid time after address	10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits				Units
		70HI		85HI		
		Min	Max	Min	Max	
t _{cw}	Write cycle time	70		85		ns
t _{w(W)}	Write pulse width	55		60		ns
t _{su(A)}	Address setup time	0		0		ns
t _{su(A-WH)}	Address setup time with respect to \overline{W}	65		70		ns
t _{su(BC1)}	Byte control 1 setup time	65		70		ns
t _{su(BC2)}	Byte control 2 setup time	65		70		ns
t _{su(S1)}	Chip select 1 setup time	65		70		ns
t _{su(S2)}	Chip select 2 setup time	65		70		ns
t _{su(D)}	Data setup time	30		35		ns
t _{h(D)}	Data hold time	0		0		ns
t _{rec(W)}	Write recovery time	0		0		ns
t _{dis(W)}	Output disable time from \overline{W} low		25		30	ns
t _{dis(OE)}	Output disable time from \overline{OE} high		25		30	ns
t _{en(W)}	Output enable time from \overline{W} high	5		5		ns
t _{en(OE)}	Output enable time from \overline{OE} low	5		5		ns



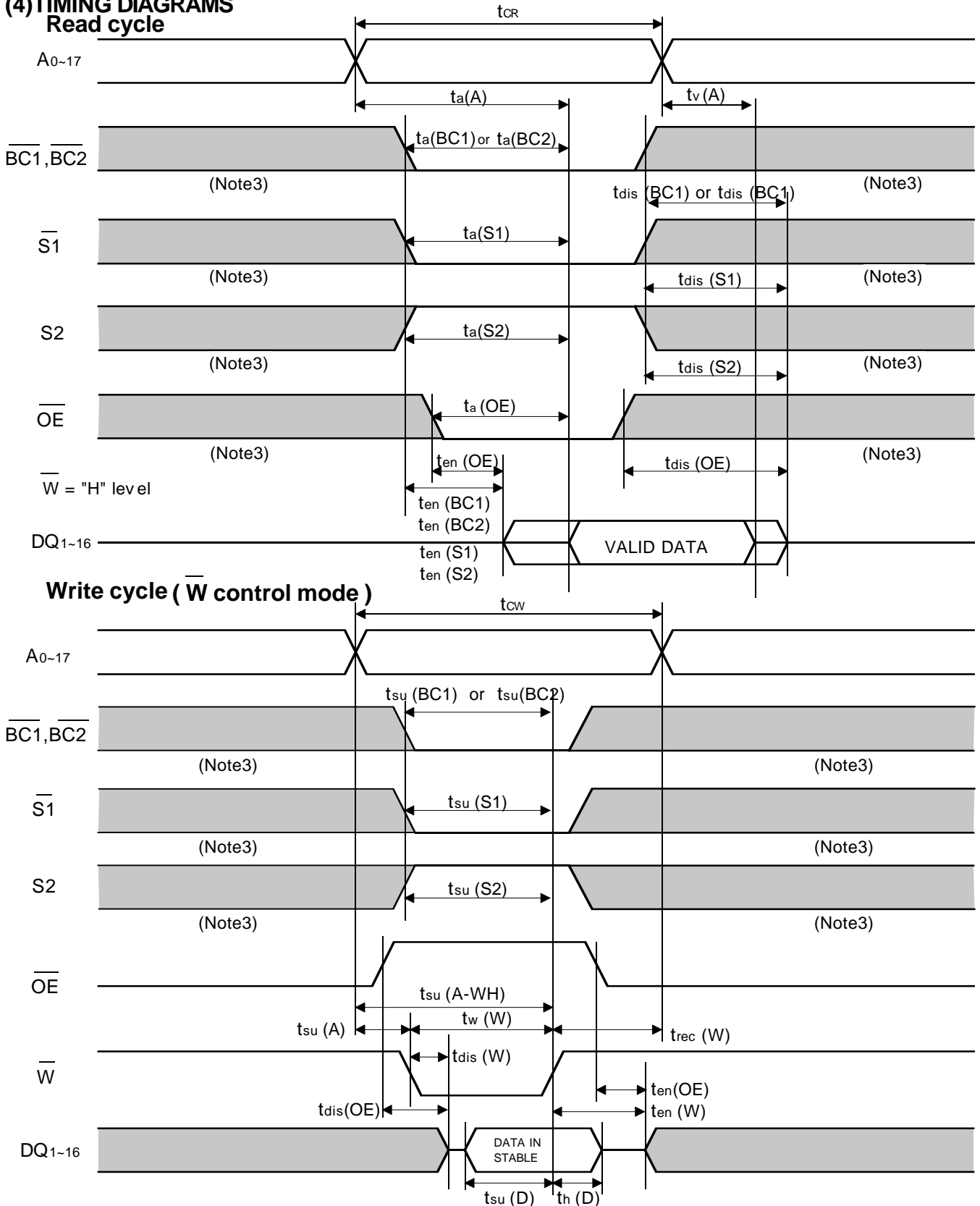
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(4)TIMING DIAGRAMS

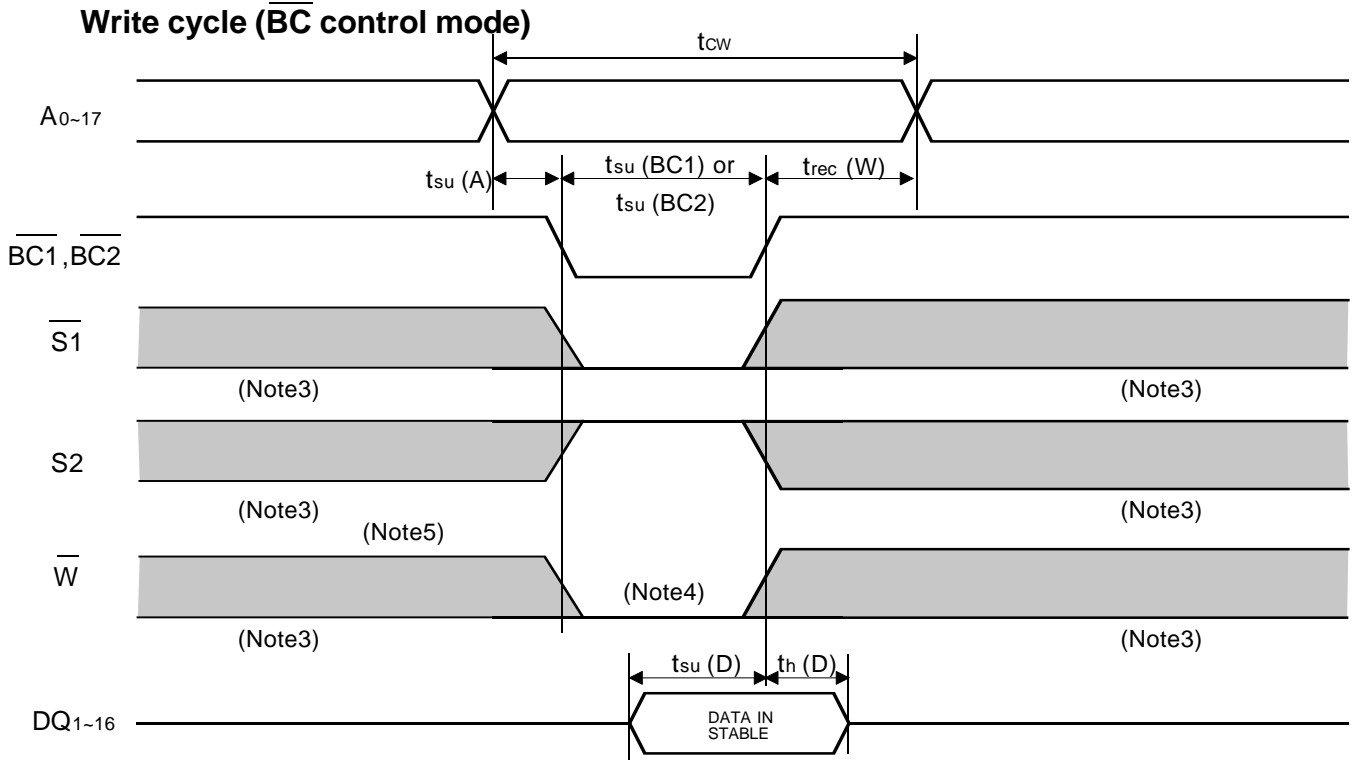


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Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during $\overline{S1}$ low, S2 high overlaps $\overline{BC1}$ and/or $\overline{BC2}$ low and \overline{W} low.

Note 5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{BC1}$ and/or $\overline{BC2}$ or the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.



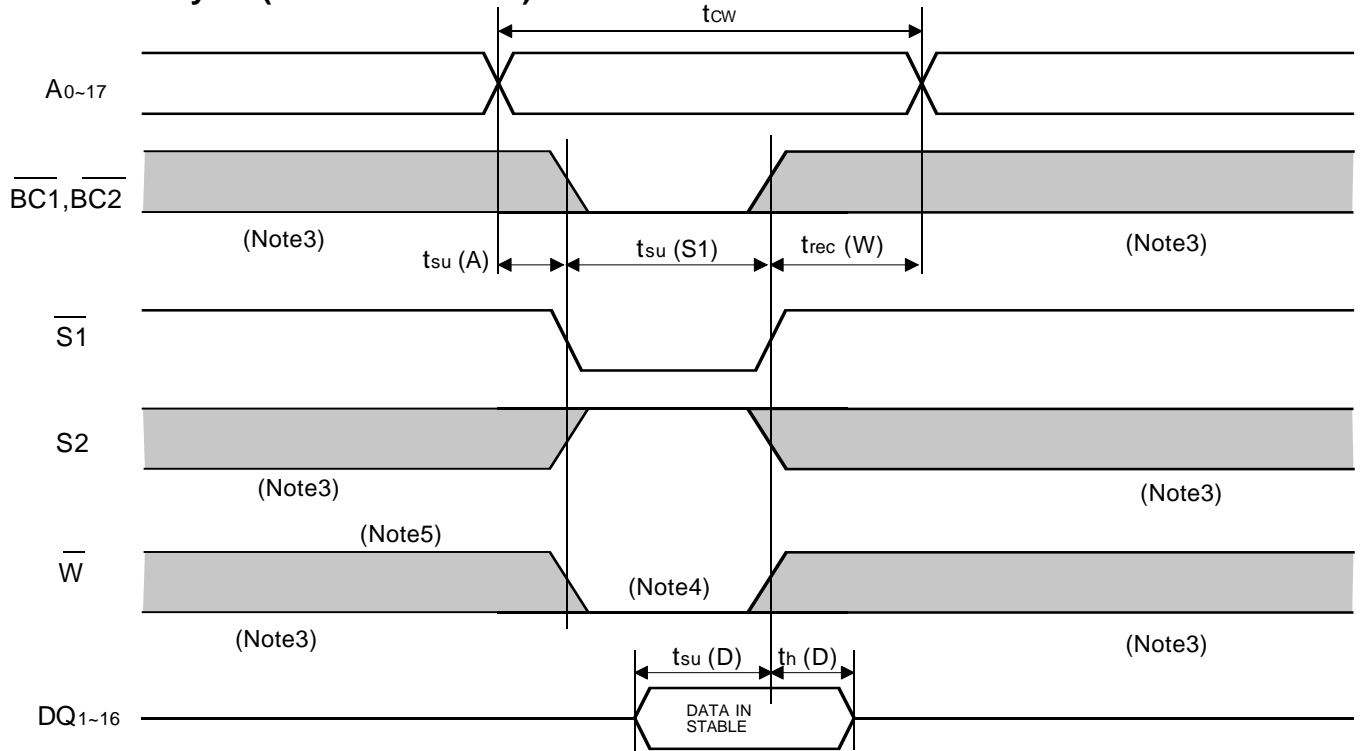
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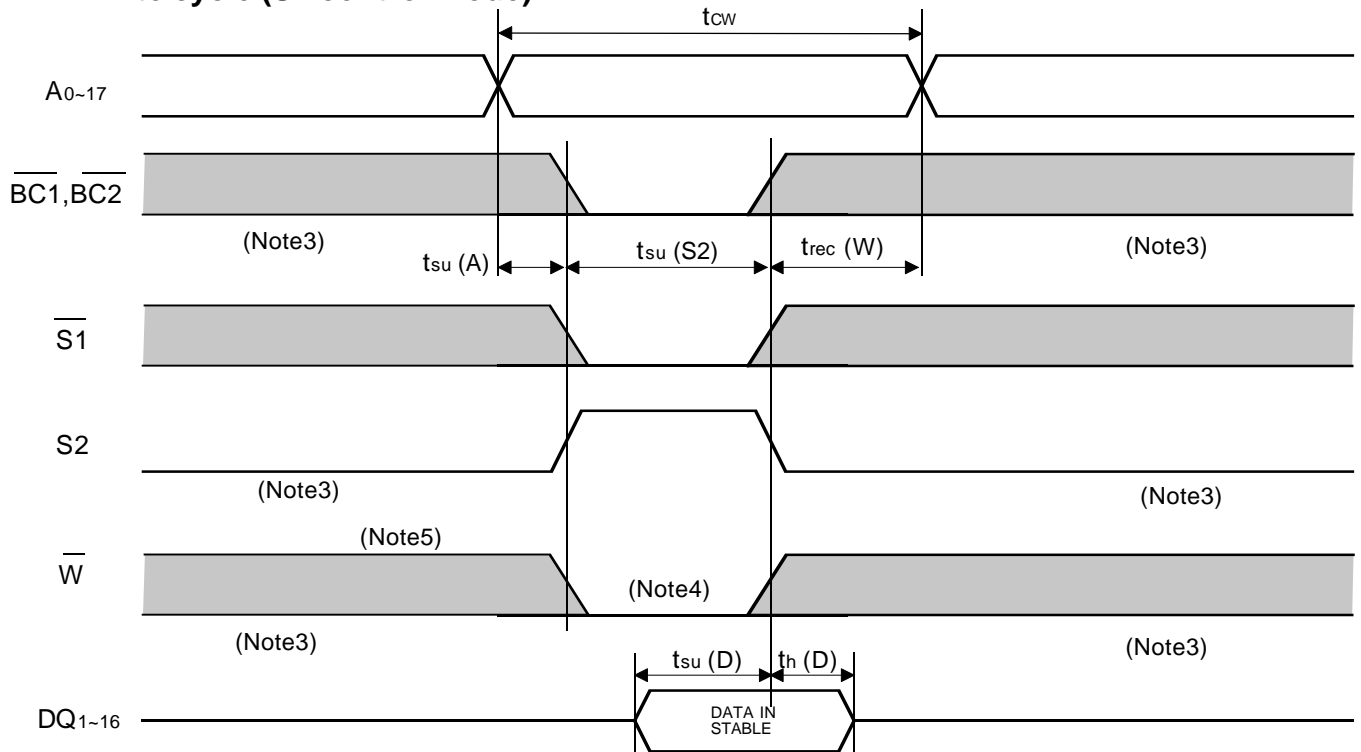
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Write cycle ($\overline{S1}$ control mode)



Write cycle ($S2$ control mode)



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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Units	
			Min	Typ	Max		
V _{CC} (PD)	Power down supply voltage		1.3			V	
V _I (BC)	Byte control input $\overline{BC1}$ & $\overline{BC2}$	$1.65V \leq V_{CC}(PD)$	$0.7 \times V_{CC}$			V	
		$1.3V \leq V_{CC}(PD) \leq 1.65V$		$V_{CC}(PD)$			
V _I (S1)	Chip select input $\overline{S1}$	$1.65V \leq V_{CC}(PD)$	$0.7 \times V_{CC}$			V	
		$1.3V \leq V_{CC}(PD) \leq 1.65V$		$V_{CC}(PD)$			
V _I (S2)	Chip select input S2				0.2	V	
I _{CC} (PD)	Power down supply current	$V_{CC}=1.3V$ (1) $\overline{S1} \geq V_{CC} - 0.2V$, other inputs = 0 - V _{CC} (2) $S2 \leq 0.2V$, other inputs = 0 - V _{CC} (3) $\overline{BC1}$ and $\overline{BC2} \geq V_{CC} - 0.2V$ $\overline{S1} \leq 0.2V$, $S2 \geq V_{CC} - 0.2V$ other inputs = 0 - V _{CC}	~ +25°C	-	0.1	0.7	μA
			~ +40°C	-	0.2	1.5	
			~ +70°C	-	-	5	
			~ +85°C	-	-	10	

Note 2: Typical parameter of I_{CC}(PD) indicates the value for the center of distribution at 1.3V, and not 100% tested.

(2) TIMING REQUIREMENTS

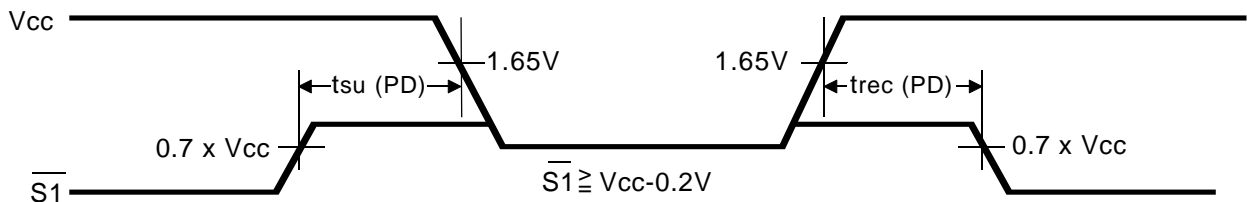
Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t _{SU} (PD)	Power down set up time		0			ns
t _{REC} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

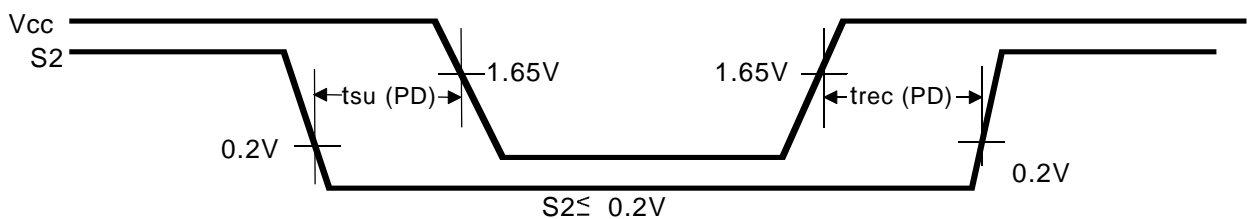
BC control mode



S1 control mode



S2 control mode



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Revision History

Ver. 0.1 / Oct.24.2000	Initial (-85HI)
Ver. 0.2 / Oct.26.2000	min.1.8V ---> 85ns min.1.7V ---> 100ns (-85HI)
Ver. 0.3 / Oct.26.2000	min.1.65V ---> 85ns
Ver. 1.0 / Nov.22.2000	tsu(D)35ns ---> 45ns
Ver. 2.0 / Apr.09.2001	Part#: M5M5W416C --->M5M5Y416C Address#(Timing Diagram) : A18---> A17(Correct) E3 ball: GND ---> NC or GND Add comment for safety
Ver. 3.0 / May.08.2001	t _{dis} (BC1) & t _{dis} (BC2) ---> t _{en} (BC1) & t _{en} (BC2) <Correct> P4 Addition of -70HI spec and notice as "Preliminary" Power down supply voltage : 1.5V to 1.3V

