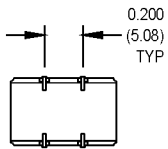
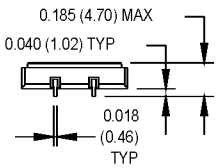
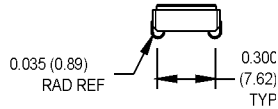
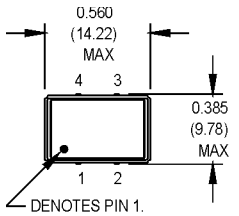


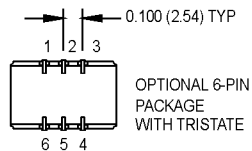
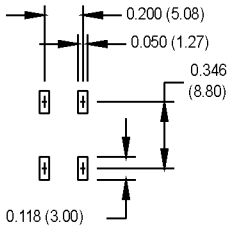
# M5R Series

## 9x14 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillator

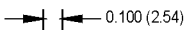


All dimensions in inches (mm).

### SUGGESTED SOLDER PAD LAYOUT



OPTIONAL 6-PIN PACKAGE WITH TRISTATE



### Pin Connections

FUNCTION	4 Pin	6 Pin
N/C or Output $\bar{Q}$	1	1
Enable		2
Ground/Cover	2	3
Output Q	3	4
N/C		5
+Vcc	4	6

### Ordering Information

Product Series	M5R	1	8	Z	Q	J	-R	00.0000	MHz
Temperature Range	1: 0°C to +70°C	2: -40°C to +85°C	6: -20°C to +70°C	7: -0°C to +85°C	8: 0°C to +50°C				
Stability	3: ±100 ppm	4: ±50 ppm	5: ±35 ppm						
Output Type	R: Complementary Enable	T: Single Enable	Z: Complementary w/o Enable	X: Single w/o Enable					
Symmetry/Output Logic Type	L: 45/55% LVDS	P: 45/55% PECL	H: 40/60% LVDS	Q: 40/60% PECL					
Package/Lead Configurations	J: J-lead								
RoHS Compliance	Blank: non-RoHS compliant part	-R: RoHS compliant part							
Frequency (customer specified)									

1. Calibration, deviation over temperature, shock, vibration, and aging.
2. PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.

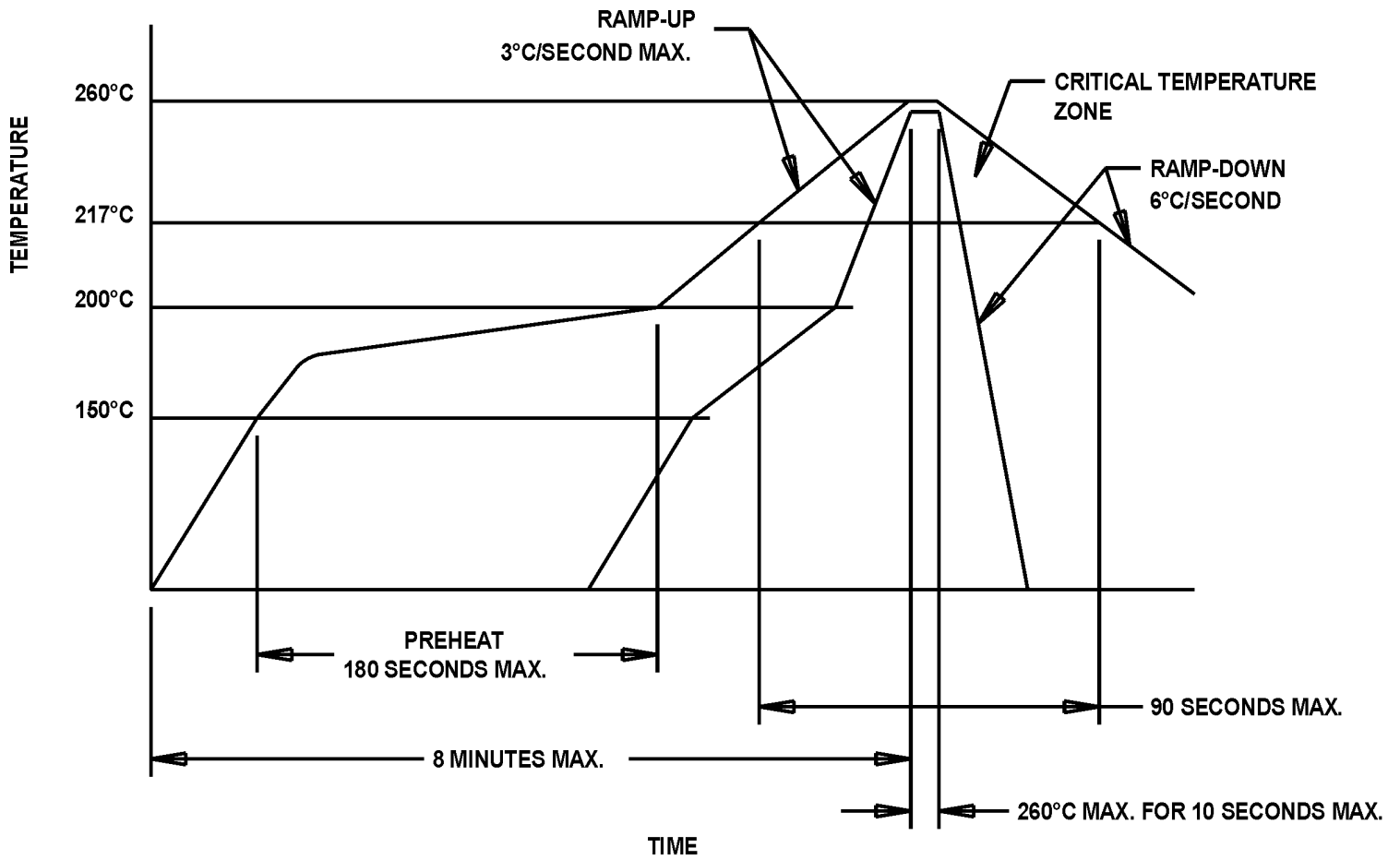
PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	0.75		800	MHz	
Operating Temperature	T <sub>A</sub>	(See Ordering Information)				
Storage Temperature	T <sub>s</sub>	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging						See Note 1
1st Year			±2		ppm	
Thereafter (per year)			±1		ppm	
Input Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V	
PECL Input Current	I <sub>cc</sub>			60	mA	0.75 to 24 MHz
				95	mA	24 to 96 MHz
				105	mA	96 to 800 MHz
LVDS Input Current	I <sub>cc</sub>			30	mA	0.75 to 24 MHz
				60	mA	24 to 800 MHz
Output Type						PECL/LVDS
Load		50 Ohms to V <sub>cc</sub> -2 VDC 100 Ohm differential load				See Note 2 PECL Waveform LVDS Waveform
Symmetry (Duty Cycle)		(See Ordering Information)				
Output Skew				200	ps	PECL
Differential Voltage		250	340	450	mV	LVDS
Logic "1" Level	V <sub>oh</sub>	V <sub>cc</sub> -1.02			V	PECL
Logic "0" Level	V <sub>ol</sub>			V <sub>cc</sub> -1.63	V	PECL
Rise/Fall Time	T <sub>r</sub> /T <sub>f</sub>		0.35	0.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable Function		80% V <sub>cc</sub> min. Or N/C: output active 20% V <sub>cc</sub> max.: output disables to high-Z				"R" & "T" output types
Start up Time			5		ms	
Phase Jitter	φ <sub>J</sub>					Integrated 12 kHz - 20 MHz
≥20 MHz			3	5	ps RMS	

1. Calibration, deviation over temperature, shock, vibration, and aging.
2. PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.

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# MtronPTI Lead Free Solder Profile



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