M61311SP/M61316SP

I²C BUS Controlled Video Pre-amp for High Resolution Color Display

REJ03F0199-0201
Rev.2.01
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Description

M61311SP/M61316SP is semiconductor integrated circuit for CRT display monitor.

It includes OSD blanking, OSD mixing, retrace blanking, video detector, sync separator, wide band amplifier, brightness control.

Main/sub contrast, video response adjust, ret BLK adjust, 4ch D/A OUT and OSD level adjust function can be controlled by I²C BUS.

Features

- Frequency band width: RGB — 200 MHz (M61311SP)
  150 MHz (M61316SP)
  (4 V_{P-P} at −3 dB)
  OSD — 80 MHz
- Input: RGB — 0.7 V_{P-P} (typ.)
  OSD — 3.5 V to 5.0 V (positive)
  OSD BLK — 3.5 V to 5.0 V (positive)
  Retrace BLK — 2.5 V to 5.0 V (positive)
  Clamp pulse — 2.5 V to 5.0 V (positive)
  Output: RGB — 5 V_{P-P} (at Brightness less than 2 V_{DC})
  OSD — 4 V_{P-P} (at Brightness less than 2 V_{DC})
  Sync OUT — 5 V_{P-P}
  Video det OUT — High = 4.2 V_{DC}, Low = 0.7 V_{DC}

Application

CRT display monitor

Recommended Operating Conditions

Supply voltage range:	11.50 V to 12.50 V (V3, V29)
	4.75 V to 5.25 V (V11)
Rated supply voltage:	12.00 V (V3, V29)
	5.00 V (V11)

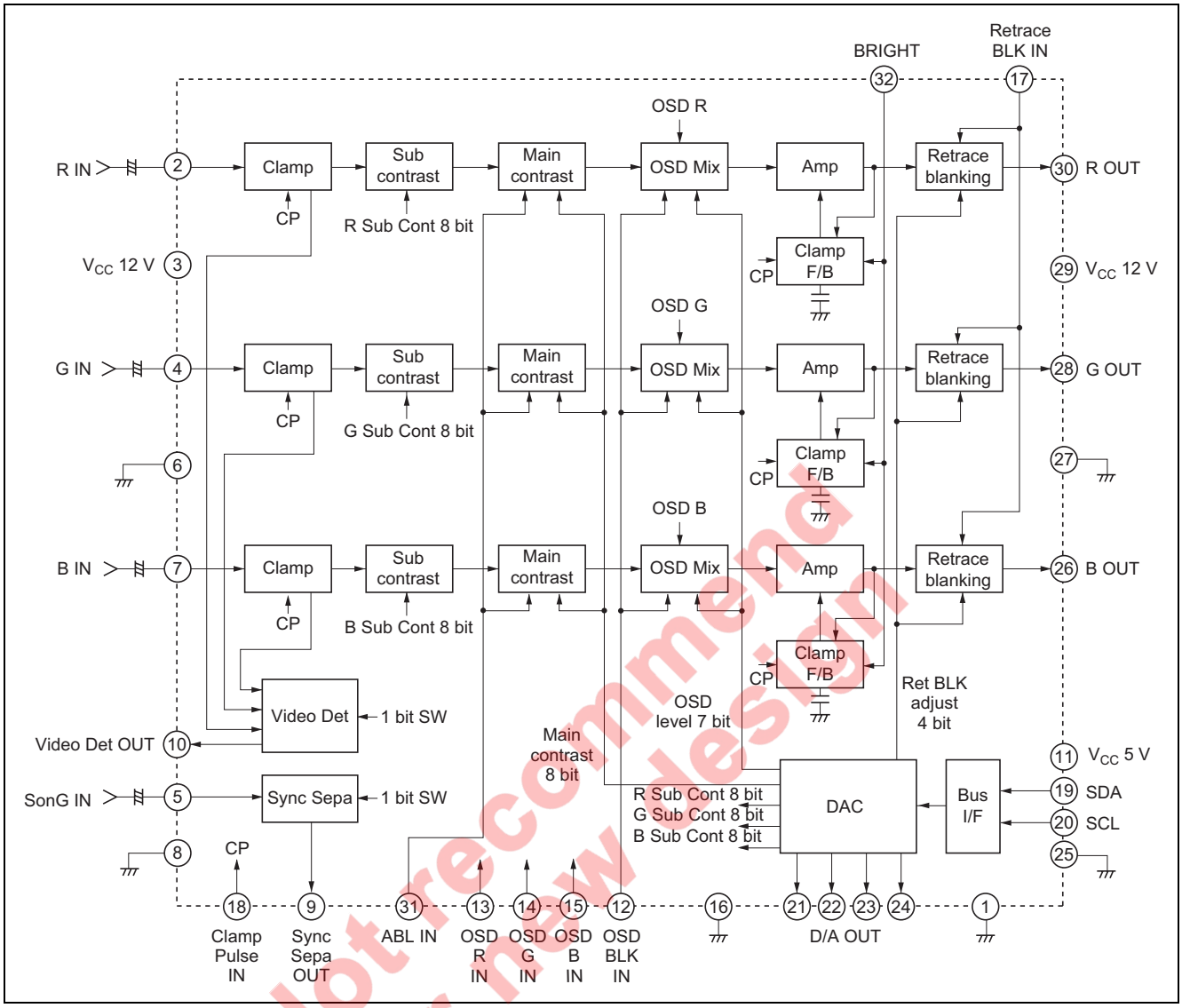
Major Specification

I²C BUS controlled 3ch video pre-amp with OSD mixing function and retrace blanking function.

The difference in the M61311SP/M61316SP is RGB video frequency band width.

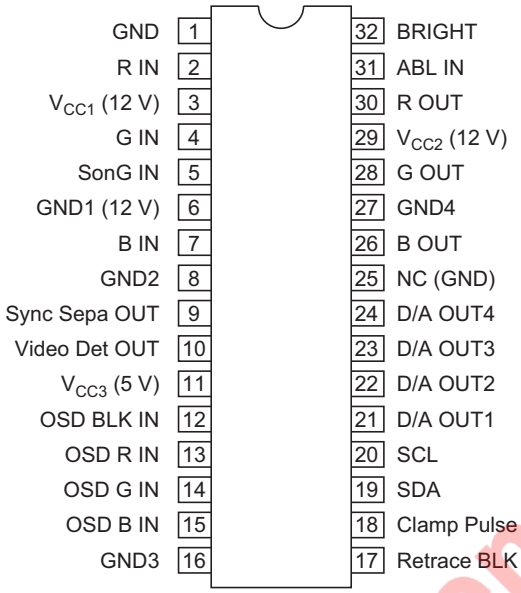
M61311SP is 200 MHz, M61316SP is 150 MHz in conditions RGB output is 4 V_{P-P} at −3 dB.

Block Diagram



Pin Arrangement

M61311SP/M61316SP



(Top view)

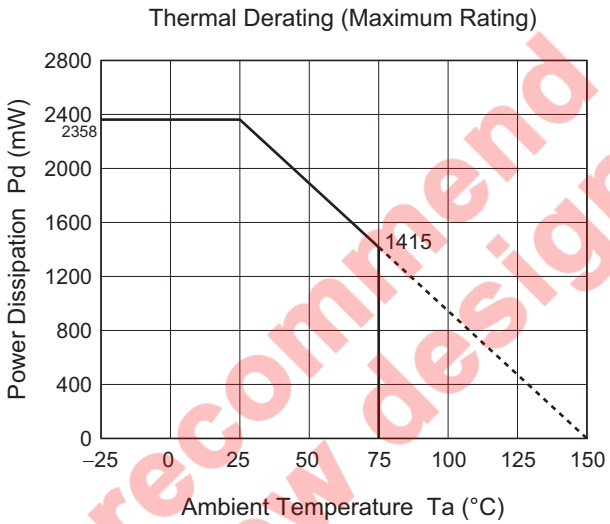
NC: No connection

Outline: PRDP0032BA-A (32P4B)

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply voltage (pin 3, 29)	$V_{CC}12$	13.0	V
Supply voltage (pin 11)	$V_{CC}5$	6.0	V
Power dissipation	Pd	2358	mW
Ambient temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–40 to +150	°C
Recommended supply 12	Vopr12	12.0	V
Recommended supply 5	Vopr5	5.0	V
Voltage range 12	Vopr'12	11.5 to 12.5	V
Voltage range 5	Vopr'5	4.75 to 5.25	V



BUS Control Table

(1) Slave address:

D7	D6	D5	D4	D3	D2	D1	R/W	
1	0	0	0	1	0	0	0	= 88H

(2) Slave receiver format:

Normal mode

	8 bit		8 bit		8 bit		
S	Slave address	A	Sub address	A	Data byte	A	P

Auto increment mode

	8 bit		8 bit		8 bit	
S	Slave address	A	Sub address (0XH) + 10H	A	Data byte (Sub address = 0XH)	A

8 bit		8 bit	
Data (Sub address = 0 (X + 1) H)	A	Data (Sub address = 0 (X + 2) H)	A

Note: S: Start condition, A: Acknowledge, P: Stop condition

(3) Sub address byte and data byte format:

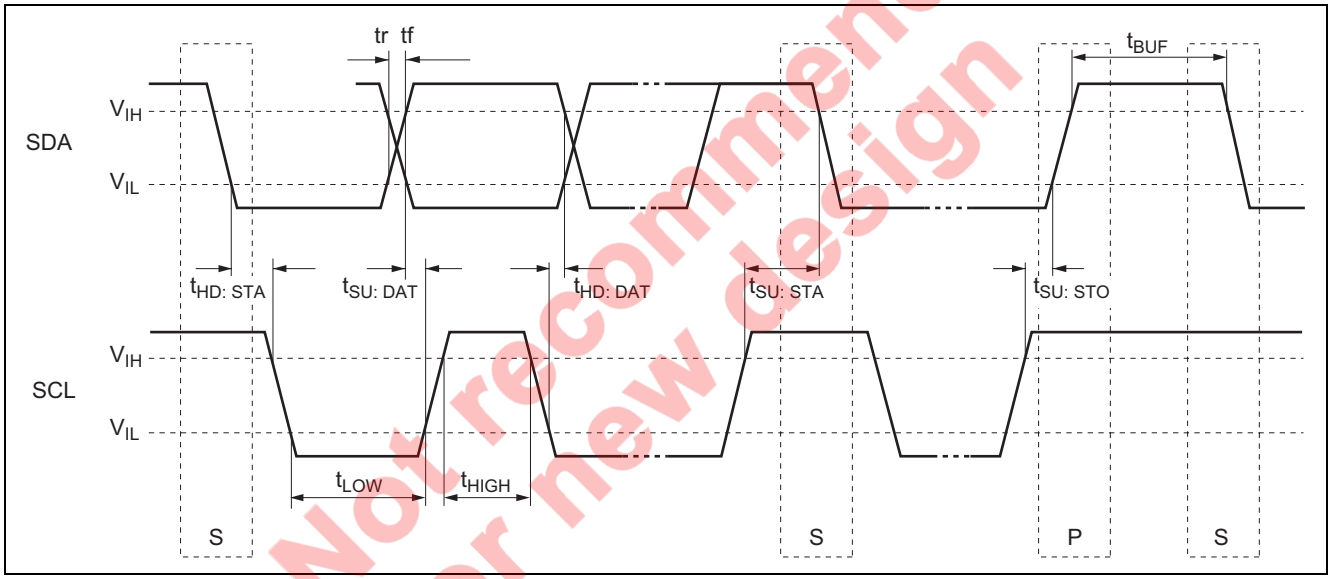
Function	Bit	Sub Add.	Data Byte (Top: Byte Format, Under: Start Condition)							
			D7	D6	D5	D4	D3	D2	D1	D0
Main contrast	8	00H	A07	A06	A05	A04	A03	A02	A01	A00
			0	0	0	0	0	0	0	1*
Sub contrast R	8	01H	A17	A16	A15	A14	A13	A12	A11	A10
			0	0	0	0	0	0	0	1*
Sub contrast G	8	02H	A27	A26	A25	A24	A23	A22	A21	A20
			0	0	0	0	0	0	0	1*
Sub contrast B	8	03H	A37	A36	A35	A34	A33	A32	A31	A30
			0	0	0	0	0	0	0	1*
OSD level	7	04H	—	A46	A45	A44	A43	A42	A41	A40
			—	0	0	0	0	0	0	1*
RE-BLK adjust	4	05H	—	—	—	—	A53	A52	A51	A50
			—	—	—	—	0	0	0	1*
Sharpness control	4	06H	—	—	—	—	A63	A62	A61	A60
			—	—	—	—	0	0	0	1*
Sync Sepa SW	1		—	—	—	A64	—	—	—	—
			—	—	—	0	—	—	—	—*
Video Det SW	1		—	—	A65	—	—	—	—	—
			—	—	0	—	—	—	—	—*
Test mode	2		A67	A66	—	—	—	—	—	—
			0	0	—	—	—	—	—	—*
D/A OUT1	8	07H	A77	A76	A75	A74	A73	A72	A71	A70
			0	0	0	0	0	0	0	1*
D/A OUT2	8	08H	A87	A86	A85	A84	A83	A82	A81	A80
			0	0	0	0	0	0	0	1
D/A OUT3	8	09H	A97	A96	A95	A94	A93	A92	A91	A90
			0	0	0	0	0	0	0	1
D/A OUT4	8	0AH	AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
			0	0	0	0	0	0	0	1

Note: pre-data
Sub add. 06H
Sync Sepa SW A64 0: Sync Sepa ON 1: Sync Sepa OFF
Video Det SW A65 0: Video Det ON 1: Video Det OFF
Always set up as A66 and A67 in 0
For I^2C Data, please transfer in the period of vertical.

I²C BUS Control Section SDA, SCL Characteristics

Item	Symbol	Min.	Max.	Unit
Min. input LOW voltage	V_{IL}	–0.5	1.5	V
Max. input HIGH voltage	V_{IH}	3.0	5.5	V
SCL clock frequency	f_{SCL}	0	400	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	1.3	—	µs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD:STA}$	0.6	—	µs
The LOW period of the clock	t_{LOW}	1.3	—	µs
The HIGH period of the clock	t_{HIGH}	0.6	—	µs
Set up time for start condition (Only relevant for a repeated start condition)	$t_{SU:STA}$	0.6	—	µs
Hold time DATA	$t_{HD:DAT}$	0	0.9	µs
Set-up time DATA	$t_{SU:DAT}$	100	—	ns
Rise time of both SDA and SCL lines	tr	20+0.1Cb	300	ns
Fall time of both SDA and SCL lines	tf	20+0.1Cb	300	ns
Set-up time for stop condition	$t_{SU:STO}$	0.6	—	µs

Timing Chart



Electrical Characteristics

(V_{CC} = 12 V, 5 V; Ta = 25°C, unless otherwise noted)

Item	Symbol	Limits Min.	Typ.	Max.	Unit	Test Point	Input 3 12 V Vcc	2 R IN	4 G IN	5 SonG IN	7 B IN	12 OSD BLK	13 OSD R IN	14 OSD G IN	15 OSD B IN	17 RET BLK	18 CP IN	CTL Vol 31 ABL (V)	32 BRT (V)	BUS CTL (H) 00H Main cont	01H Sub R cont	02H Sub G cont	03H Sub B cont	04H OSD Adj	05H Re-BLK Adj	06H Sharpness	06H SonG SW	06H VDET SW	07H D/A OUT 1	08H D/A OUT 2	09H D/A OUT 3	0AH D/A OUT 4
5 V Circuit current1 power save mode	I_{CC1}	—	6	10	mA	IB	a	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	00 0	00 0	00 0	00 0
12 V Circuit current2 normal mode	I_{CC2}	—	105	130	mA	IA	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	00 0	00 0	00 0	00 0
5 V Circuit current3 normal mode	I_{CC3}	—	4	8	mA	IB	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	00 0	00 0	00 0	00 0
Output dynamic range	Vomax	7.5	9	—	V_{DC}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	0.5	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Maximum input	Vimax	1.4	—	—	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	46 70	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Maximum gain	GV	16	17.5	19	dB	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Relative maximum gain	ΔGV	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Main contrast control characteristics1 (Max.)	VC1	3.3	4	4.7	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	C8 200	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Main contrast control relative characteristics1	ΔVC1	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C8 200	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Main contrast control characteristics2 (Typ.)	VC2	2.3	2.8	3.3	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	80 128	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Main contrast control relative characteristics2	ΔVC2	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	80 128	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Main contrast control characteristics3 (Min.)	VC3	0.25	0.55	0.85	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	10 16	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Main contrast control relative characteristics3	ΔVC3	−0.2	0	0.2	V_{P-P}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	10 16	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Sub contrast control characteristics1 (Max.)	VSC1	3.3	4	4.7	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	C8 200	C8 200	C8 200	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Sub contrast control relative characteristics1	ΔVSC1	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	C8 200	C8 200	C8 200	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Sub contrast control characteristics2 (Typ.)	VSC2	2.3	2.8	3.3	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	80 128	80 128	80 128	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Sub contrast control relative characteristics2	ΔVSC2	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	80 128	80 128	80 128	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Sub contrast control characteristics3 (Min.)	VSC3	0.2	0.5	0.8	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	10 16	10 16	10 16	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Sub contrast control relative characteristics3	ΔVSC3	−0.2	0	0.2	V_{P-P}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	10 16	10 16	10 16	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
ABL control characteristics1	ABL1	3.4	4.2	5.0	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	4	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
ABL control relative characteristics1	ΔABL1	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
ABL control characteristics2	ABL2	1.5	2.0	2.5	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	2	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
ABL control relative characteristics2	ΔABL2	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
ABL control characteristics3	ABL3	−0.3	0	0.3	V_{P-P}	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	0	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
ABL control relative characteristics3	ΔABL3	−0.2	0	0.2	V_{P-P}	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Brightness control characteristics1	VB1	3.4	3.8	4.2	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	a	b	5	4	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Brightness control relative characteristics1	ΔVB1	−0.3	0	0.3	V	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Brightness control characteristics2	VB2	1.6	1.9	2.2	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Brightness control relative characteristics2	ΔVB2	−0.3	0	0.3	V	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Brightness control characteristics3	VB3	0.3	0.5	0.7	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	a	b	5	0.5	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Brightness control relative characteristics3	ΔVB3	−0.3	0	0.3	V	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Pulse characteristics1 (4 V_{P-P})	Tr	—	2.2	3.0	ns*	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	C8 200	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
		—	2.7	3.5																												
Relative pulse characteristics1 (4 V_{P-P})	ΔTr	−0.8	0	0.8	ns	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C8 200	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Pulse characteristics2 (4 V_{P-P})	Tf	—	2.2	3.0	ns*	26, 28, 30	b	b	b	a	b	a	a	a	a	a	b	5	2	C8 200	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
		—	2.7	3.5																												
Relative pulse characteristics2 (4 V_{P-P})	ΔTf	−0.8	0	0.8	ns	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C8 200	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Clamp pulse threshold voltage	VthCP	0.7	1.5	2.3	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255
Clamp pulse minimum width	WCP	0.2	—	—	µs	26, 28, 30	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08 8	0	0	FF 255	FF 255	FF 255	FF 255

Note: Tr and Tf pulse characteristics 1 and 2 (4 Vp-p) top: M61311SP, under: M61316SP

Electrical Characteristics (cont.)

Item	Symbol	Limits			Unit	Test Point	Input												CTL Vol		BUS CTL (H)																					
		Min.	Typ.	Max.			3 12 V Vcc	2 R IN	4 G IN	5 SonG IN	7 B IN	12 OSD BLK	13 OSD R IN	14 OSD G IN	15 OSD B IN	17 RET BLK	18 CP IN	31 ABL (V)	32 BRT (V)	00H Main cont	01H Sub R cont	02H Sub G cont	03H Sub B cont	04H OSD Adj	05H Re-BLK Adj	06H			07H D/A OUT 1	08H D/A OUT 2	09H D/A OUT 3	0AH D/A OUT 4									
																										Sharpness	SonG SW	VDET SW														
OSD pulse characteristics1	OTr	—	2	5	ns	26, 28, 30	b	a	a	a	a	a	b	b	b	a	b	5	2	FF 255	FF 255	FF 255	FF 255	6F 111	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD pulse characteristics2	OTf	—	4	7	ns	26, 28, 30	b	a	a	a	a	a	b	b	b	a	b	5	2	FF 255	FF 255	FF 255	FF 255	6F 111	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD adjust control characteristics1 (Max.)	Oadj1	3.3	4.0	4.9	V_{P-P}	26, 28, 30	b	a	a	a	a	b	b	b	b	a	b	5	2	FF 255	FF 255	FF 255	FF 255	7F 127	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD adjust control relative characteristics1	ΔOadj1	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	7F 127	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD adjust control characteristics2 (Typ.)	Oadj2	1.2	1.8	2.4	V_{P-P}	26, 28, 30	b	a	a	a	a	b	b	b	b	a	b	5	2	FF 255	FF 255	FF 255	FF 255	40 64	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD adjust control relative characteristics2	ΔOadj2	0.8	1.0	1.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	40 64	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD adjust control characteristics3 (Min.)	Oadj3	−0.5	−0.1	0.3	V_{P-P}	26, 28, 30	b	a	a	a	a	b	b	b	b	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD adjust control relative characteristics3	ΔOadj3	−0.2	0	0.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD input threshold voltage	VthOSD	1.7	2.5	3.3	V_{DC}	26, 28, 30	b	a	a	a	a	a	b	b	b	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Black level difference in OSD BLK on/off	OBLK	−0.5	−1.0	0.3	V_{DC}	26, 28, 30	b	a	a	a	a	b	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Relative OBLK	ΔOBLK	−0.2	0	0.2	—	26, 28, 30	b	a	a	a	a	b	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
OSD BLK input threshold voltage	VthBLK	1.7	2.5	3.3	V_{DC}	26, 28, 30	b	b	b	a	b	b	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Retrace BLK characteristics1	HBLK1	1.6	1.9	2.2	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	0F 15	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Retrace BLK characteristics2	HBLK2	1.0	1.3	1.6	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	08 8	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Retrace BLK characteristics3	HBLK3	0.3	0.6	0.9	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Retrace BLK input threshold voltage	Vth-HBLK	0.7	1.5	2.3	V_{DC}	26, 28, 30	b	a	a	a	a	a	a	a	a	b	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
SOG input maximum noise voltage	SS-NV	—	—	0.02	V_{P-P}	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
SOG minimum input voltage	SS-SV	0.2	—	—	V_{P-P}	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Sync output high level	VSH	4.5	4.9	5.0	V_{DC}	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Sync output low level	VSL	0	0.4	0.7	V_{DC}	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Sync output delay time1	TDS-F	10	30	65	ns	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
Sync output delay time2	TDS-R	10	30	65	ns	9	b	a	a	b	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
V-DET input maximum noise voltage	VD-NV	—	—	0.05	V_{P-P}	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
V-DET minimum input voltage	VD-SV	0.2	—	—	V_{P-P}	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
V-DET output high level	VVDH	3.8	4.2	5.0	V_{DC}	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
V-DET output low level	VVDL	0	0.7	1.1	V_{DC}	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
V-DET output delay time1	TDV-F	10	23	50	ns	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
V-DET output delay time2	TDV-R	1	13	40	ns	10	b	b	b	a	b	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
D/A output maximum voltage	VDH	4.7	5.2	5.7	V_{DC}	21, 22, 23, 24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
D/A output minimum voltage	VDL	0	0	0.5	V_{DC}	21, 22, 23, 24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			00 0	00 0	00 0	00 0									
																										8	0	0														
D/A OUT input current1	IA+1	0.18	—	—	mA	21, 22, 23, 24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			00 0	00 0	00 0	00 0									
																										8	0	0														
D/A OUT input current2	IA+2	0.18	—	—	mA	21, 22, 23, 24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			00 0	00 0	00 0	00 0									
																										8	0	0														
D/A OUT output current	IA−	—	—	0.4	mA	21, 22, 23, 24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			FF 255	FF 255	FF 255	FF 255									
																										8	0	0														
D/A nonlinearity	DNL	−1.0	—	1.0	LSB	21, 22, 23, 24	b	a	a	a	a	a	a	a	a	a	b	5	2	FF 255	FF 255	FF 255	FF 255	00 0	00 0	08			variable	variable	variable	variable									
																										8	0	0														

Electrical Characteristics Test Method

I_{CC1} 5 V Circuit Current1 Power Save Mode

Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point IB.

I_{CC2} 12 V Circuit Current2 Normal Mode

Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point IA.

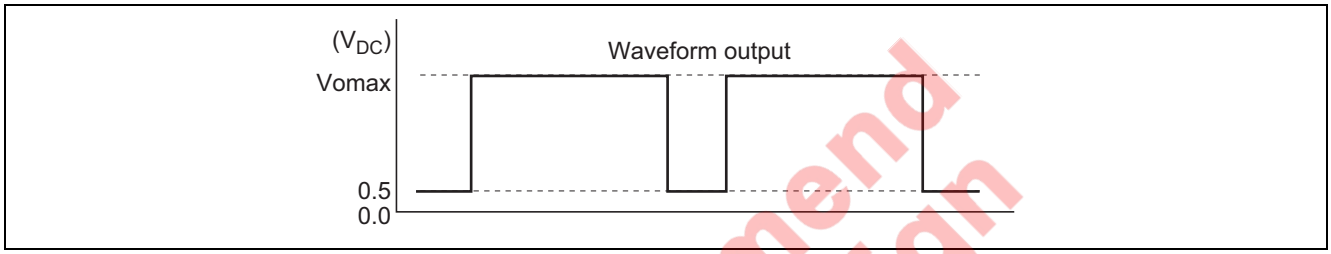
I_{CC3} 5 V Circuit Current3 Normal Mode

Measuring conditions are as listed in supplementary Table. Measured with a current meter at test point IB.

Vomax Output Dynamic Range

It makes the amplitude of SG1 1.4 $_{p\text{-}p}$. Measure the DC voltage of the white level of the waveform output.

The measured value is called Vomax.



Vimax Maximum Input

Increase the input signal (SG1) amplitude gradually, starting from 0.7 $V_{p\text{-}p}$. Measure the amplitude of the input signal when the output signal starts becoming distorted.

GV Maximum Gain

Input SG1, and measure the amplitude output at OUT (26, 28, 30). The amplitude is called VOUT (26, 28, 30).

Maximum gain GV is calculated by the equation below:

$$GV = 20\log (VOUT / 0.7)\ (dB)$$

ΔGV Relative Maximum Gain

Relative maximum gain ΔGV is calculated by the equation below:

$$\Delta GV = VOUT (26) / VOUT (28),$$
$$VOUT (28) / VOUT (30),$$
$$VOUT (30) / VOUT (26)$$

VC1 Main Contrast Control Characteristics1 (Max.)

Input SG1, and measure the amplitude output at OUT (26, 28, 30). The amplitude is called VOUT (26, 28, 30).

The measured value is called VC1.

ΔVC1 Main Contrast Control Relative Characteristics1

Relative characteristics ΔVC1 is calculated by the equation below:

$$\Delta VC1 = VOUT (26) / VOUT (28),$$
$$VOUT (28) / VOUT (30),$$
$$VOUT (30) / VOUT (26)$$

VC2 Main Contrast Control Characteristics2 (Typ.)

Measuring condition and procedure are the same as described in VC1.

ΔVC2 Main Contrast Control Relative Characteristics2

Measuring condition and procedure are the same as described in ΔVC1.

VC3 Main Contrast Control Characteristics3 (Min.)

Measuring condition and procedure are the same as described in VC1.

ΔVC3 Main Contrast Control Relative Characteristics3

Relative characteristics ΔVC3 is calculated by the equation below:

ΔVC3 = VOUT (26) – VOUT (28),
VOUT (28) – VOUT (30),
VOUT (30) – VOUT (26)

VSC1 Sub Contrast Control Characteristics1 (Max.)

Input SG1, and measure the amplitude output at OUT (26, 28, 30). The amplitude is called VOUT (26, 28, 30). The measured value is called VSC1.

ΔVSC1 Sub Contrast Control Relative Characteristics1

Relative characteristics ΔVSC1 is calculated by the equation below:

ΔVSC1 = VOUT (26) / VOUT (28),
VOUT (28) / VOUT (30),
VOUT (30) / VOUT (26)

VSC2 Sub Contrast Control Characteristics2 (Typ.)

Measuring condition and procedure are the same as described in VSC1.

ΔVSC2 Sub Contrast Control Relative Characteristics2

Measuring condition and procedure are the same as described in ΔVSC1.

VSC3 Sub Contrast Control Characteristics3 (Min.)

Measuring condition and procedure are the same as described in VSC1.

ΔVSC3 Sub Contrast Control Relative Characteristics3

Relative characteristics ΔVSC3 is calculated by the equation below:

ΔVSC3 = VOUT (26) – VOUT (28),
VOUT(28) – VOUT (30),
VOUT (30) – VOUT (26)

ABL1 ABL Control Characteristics1

Measure the amplitude output at OUT (26, 28, 30). The amplitude is called VOUT (26, 28, 30).

The measured value is ABL1.

ΔABL1 ABL Control Relative Characteristics1

Relative characteristics ΔABL1 is calculated by the equation below:

ΔABL1 = VOUT (26) / VOUT (28),
VOUT (28) / VOUT (30),
VOUT (30) / VOUT (26)

ABL2 ABL Control Characteristics2

Measuring condition and procedure are the same as described in ABL1.

ΔABL2 ABL Control Relative Characteristics2

Measuring condition and procedure are the same as described in ΔABL1.

ABL3 ABL Control Characteristics3

Measuring condition and procedure are the same as described in ABL1.

ΔABL3 ABL Control Relative Characteristics3

Relative characteristics ΔABL3 is calculated by the equation below:

ΔABL3 = VOUT (26) – VOUT (28),
VOUT (28) – VOUT (30),
VOUT (30) – VOUT (26)

VB1 Brightness Control Characteristics1

Measure the DC voltage at OUT (26, 28, 30). The amplitude is called VOUT (26, 28, 30).

The measured value is called VB1.

ΔVB1 Brightness Control Relative Characteristics1

Relative characteristics ΔVB1 is calculated by the equation below:

ΔVB1 = VOUT (26) – VOUT (28),
VOUT (28) – VOUT (30),
VOUT (30) – VOUT (26)

VB2 Brightness Control Characteristics2

Measuring condition and procedure are the same as described in VB1.

ΔVB2 Brightness Control Relative Characteristics2

Measuring condition and procedure are the same as described in ΔVB1.

VB3 Brightness Control Characteristics3

Measuring condition and procedure are the same as described in VB1.

ΔVB3 Brightness Control Relative Characteristics3

Measuring condition and procedure are the same as described in ΔVB1.

Tr Pulse Characteristics1 (4 V_{P-P})

Measure the time needed for the input pulse to rise from 10% to 90% (Tr1) and for the output pulse to rise from 10% to 90% (Tr2) with an active probe.

Pulse characteristics Tr is calculated by the equations below:

$$Tr = \sqrt{(Tr2)^2 - (Tr1)^2} \quad (ns)$$

ΔTr Relative Pulse Characteristics1 (4 V_{P-P})

Relative characteristics ΔTr is calculated by the equation below:

$$\Delta Tr = Tr\ (26) - Tr\ (28),$$
$$Tr\ (28) - Tr\ (30),$$
$$Tr\ (30) - Tr\ (26)$$

Tf Pulse Characteristics2 (4 V_{P-P})

Measure the time needed for the input pulse to fall from 90% to 10% (Tf1) and for the output pulse to fall from 90% to 10% (Tf2) with an active probe.

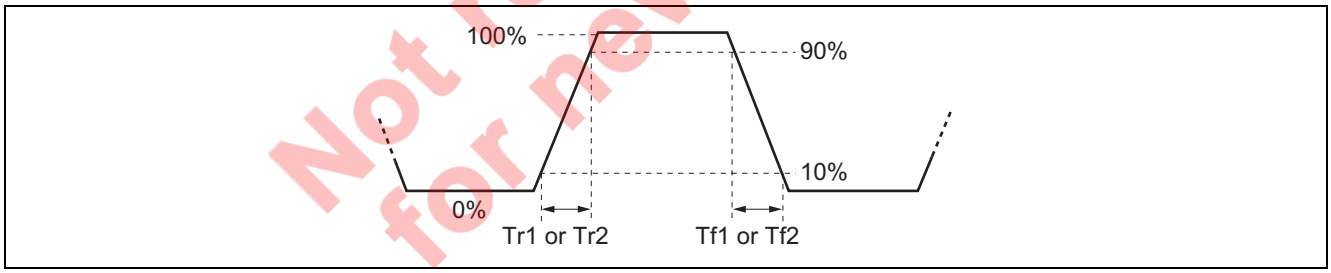
Pulse characteristics Tf is calculated by the equations below:

$$Tf = \sqrt{(Tf2)^2 - (Tf1)^2} \quad (ns)$$

ΔTf Relative Pulse Characteristics2 (4 V_{P-P})

Relative characteristics ΔTf is calculated by the equation below:

$$\Delta Tf = Tf\ (26) - Tf\ (28),$$
$$Tf\ (28) - Tf\ (30),$$
$$Tf\ (30) - Tf\ (26)$$



VthCP Clamp Pulse Threshold Voltage

Decrease the SG5 input level gradually from 5.0 V_{P-P} monitoring the waveform output. Measure the top level of input pulse when the output pedestal voltage turn decrease with unstable. And increase the SG5 input level gradually from 0 V_{P-P}. Measure the top level of input pulse when the output pedestal voltage turn increase with stable (a point of 2.0 V). The measured value is called VthCP.

WCP Clamp Pulse Minimum Width

Decrease the SG5 pulse width gradually from 0.5 µs, monitoring the output. Measure the SG5 pulse width when the output pedestal voltage turn decrease with unstable. And increase the SG5 pulse width gradual from 0 µs. Measure the SG5 pulse width when the output pedestal voltage turn increase with stable (a point of 2.0 V). The measured value is called WCP.

OTr OSD Pulse Characteristics1

Measure the time needed for the output pulse to rise from 10% to 90% (OTr) with an active probe.

OTf OSD Pulse Characteristics2

Measure the time needed for the output pulse to fall from 90% to 10% (OTf) with an active probe.

Oadj1 OSD Adjust Control Characteristics1 (Max.)

Measure the amplitude output at OUT (26, 28, 30). The amplitude is called VOUT (26, 28, 30).
The measured value is called Oadj1.

ΔOadj1 OSD Adjust Control Relative Characteristics1

Relative characteristics ΔOadj1 is calculated by the equation below:

ΔOadj1 = VOUT (26) / VOUT (28),
VOUT (28) / VOUT (30),
VOUT (30) / VOUT (26)

Oadj2 OSD Adjust Control Characteristics2 (Typ.)

Measuring condition and procedure are the same as described in Oadj1.

ΔOadj2 OSD Adjust Control Relative Characteristics2

Measuring condition and procedure are the same as described in ΔOadj1.

Oadj3 OSD Adjust Control Characteristics3 (Min.)

Measuring condition and procedure are the same as described in Oadj1.

ΔOadj3 OSD Adjust Control Relative Characteristics3

Relative characteristics ΔOadj3 is calculated by the equation below:

ΔOadj3 = VOUT (26) – VOUT (28),
VOUT (28) – VOUT (30),
VOUT (30) – VOUT (26)

VthOSD OSD Input Threshold Voltage

Decrease the SG6 input level gradually from 5.0 V_{P-P}, monitoring the output. Measure the top level of SG6 when the output is disappeared. And increase the SG6 input level gradually from 0 V_{P-P}. Measure the top level of SG6 when the output is appeared. The measured value is called VthOSD.

OBLK Black Level Difference in OSD BLK on/off

Calculating the black level voltage minus the output voltage of high section of SG6 it makes VOUT (26, 28, 30). The calculated value is called OBLK.

ΔOBLK Relative OBLK

Relative characteristics ΔOBLK is calculated by the equation below:

ΔOBLK = VOUT (26) – VOUT (28),
VOUT (28) – VOUT (30),
VOUT (30) – VOUT (26)

VthBLK OSD BLK Input Threshold Voltage

Confirm that output signal is being blanked by the SG6 at the time.

Decrease the SG6 input level gradually from 5.0 V_{P-P}, monitoring the output. Measure the top level of SG6 when the blanking period is disappeared. And increase the SG6 input level gradually from 0 V_{P-P}. Measure the top level of SG6 when the blanking period is appeared. The measured value is called VthBLK.

HBLK1 Retrace BLK Characteristics1

Measure the bottom voltage at amplitude of OUT (26, 28, 30). The measured value is called HBLK1.

HBLK2 Retrace BLK Characteristics2

Measuring condition and procedure are the same as described in HBLK1.

HBLK3 Retrace BLK Characteristics3

Measuring condition and procedure are the same as described in HBLK1.

VthHBLK Retrace BLK Input Threshold Voltage

Decrease the SG7 input level gradually from 5.0 V_{P-P}, monitoring the output. Measure the top level of SG7 when the output is disappeared. And increase the SG7 input level gradually from 0 V_{P-P}. Measure the top level of SG7 when the output is appeared. The measured value is called VthHBLK.

SS-NV SOG Input Maximum Noise Voltage

When SG4 is all black (no video), the sync's amplitude of SG4 gradually from 0 V_{P-P} to 0.02 V_{P-P}. No pulse output permitted.

SS-SV SOG Minimum Input Voltage

When SG4 is all white or all black, the sync's amplitude of SG4 gradually from 0.2 V_{P-P} to 0.3 V_{P-P}. Positive pulse has occurred to Sync Sepa OUT.

VSH Sync Output High level

Measure the high voltage at Sync Sepa OUT. The measured value is treated as VSH.

VSL Sync Output Low Level

Measure the low voltage at Sync Sepa OUT. The measured value is treated as VSL.

TDS-F Sync Output Delay Time1

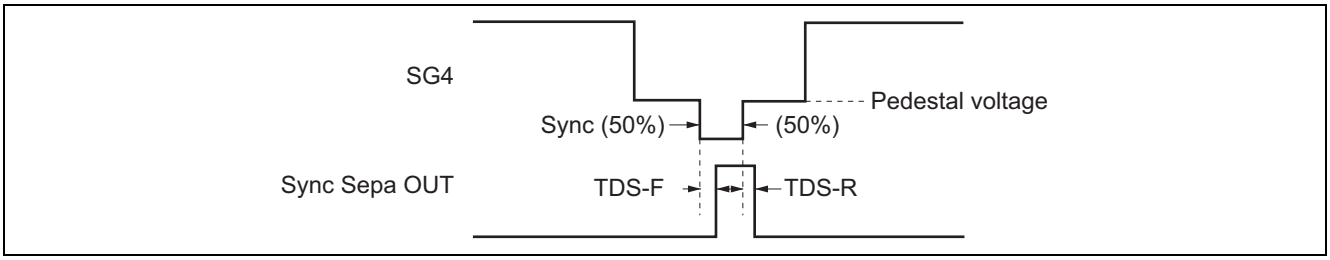
Sync Sepa OUT becomes high with sink part of SG4.

Measure the time needed for the front edge of SG4 Sync to fall from 50% and for SyncOUT to rise from 50% with an active probe. The measured value is called TDS-F.

TDS-R Sync Output Delay Time2

Sync Sepa OUT becomes high with sink part of SG4.

Measure the time needed for the rear edge of SG4 Sync to rise from 50% and for SyncOUT to fall from 50% with an active probe. The measured value is called TDS-R.



VD-NV V-DET Input Maximum Noise Voltage

Increase the SG1 input level gradually from 0 V_{P-P} to 0.05 V_{P-P}. No pulse Video Det OUT permitted.

VD-SV V-DET Minimum Input Voltage

Decrease the SG1 input level gradually from 0.2 V_{P-P} to 0.3 V_{P-P}. Positive pulse has occurred to Video Det OUT.

VVDH V-DET Output High Level

Measure the high voltage at Video Det OUT. The measured value is treated as VVDH.

VVDL V-DET Output Low Level

Measure the low voltage at Video Det OUT. The measured value is treated as VVDL.

TDV-F V-DET Output Delay Time1

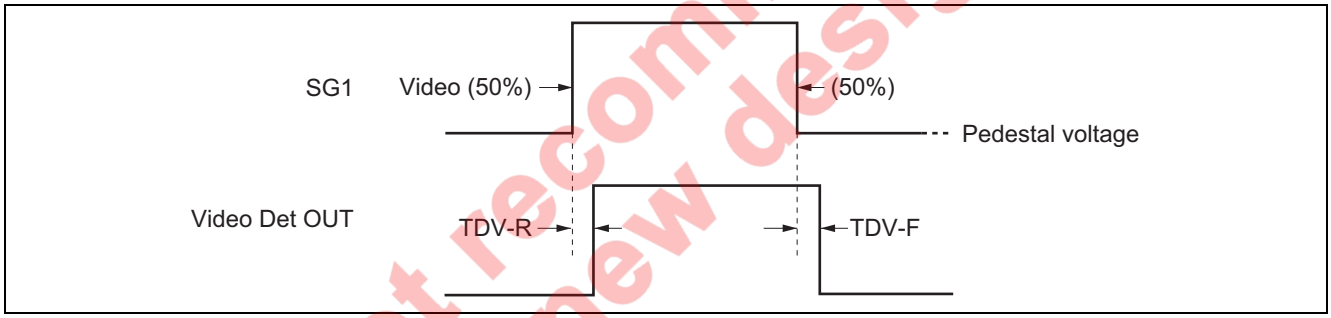
Video Det OUT becomes high with signal part of SG1.

Measure the time needed for the SG1 to fall from 50% and for Video Det OUT to fall from 50% with an active probe. The measured value is called TDV-F.

TDV-R V-DET Output Delay Time2

Video Det OUT becomes high with signal part of SG1.

Measure the time needed for the SG1 to rise from 50% and for Video Det OUT to rise from 50% with an active probe. The measured value is called TDV-R.



VDL D/A Output Minimum Voltage

Measure the DC voltage at D/A OUT. The measured value is called VDL.

IA+1 D/A OUT Input Current1

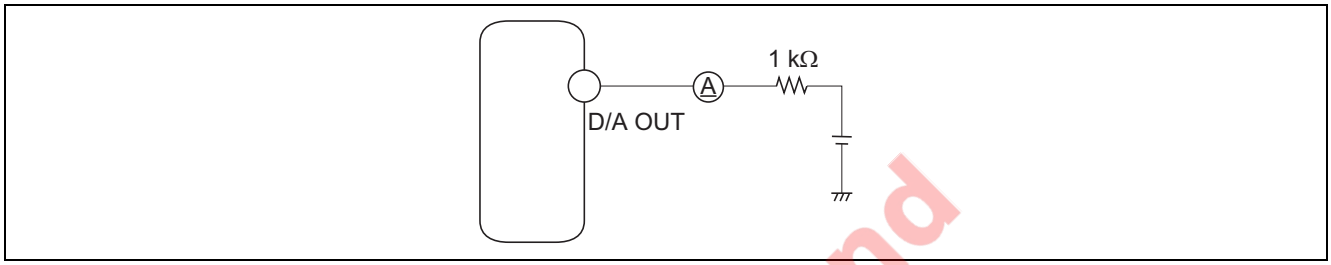
Measure the input current that flows into D/A OUT through 1 kΩ by 2 V_{DC}.

IA+2 D/A OUT Input Current2

Measure the input current that flows into D/A OUT through 1 kΩ by 0.5 V_{DC}.

IA– D/A OUT Output Current

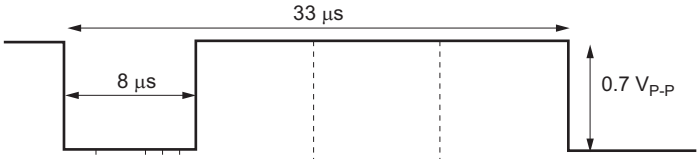
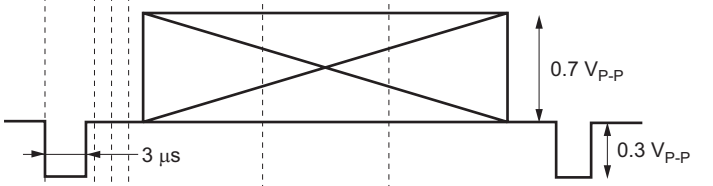
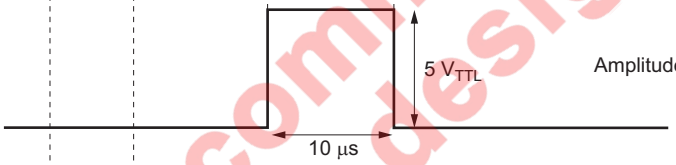
Measure the output current that flows out of D/A OUT through 1 kΩ by 4.2 V_{DC}.



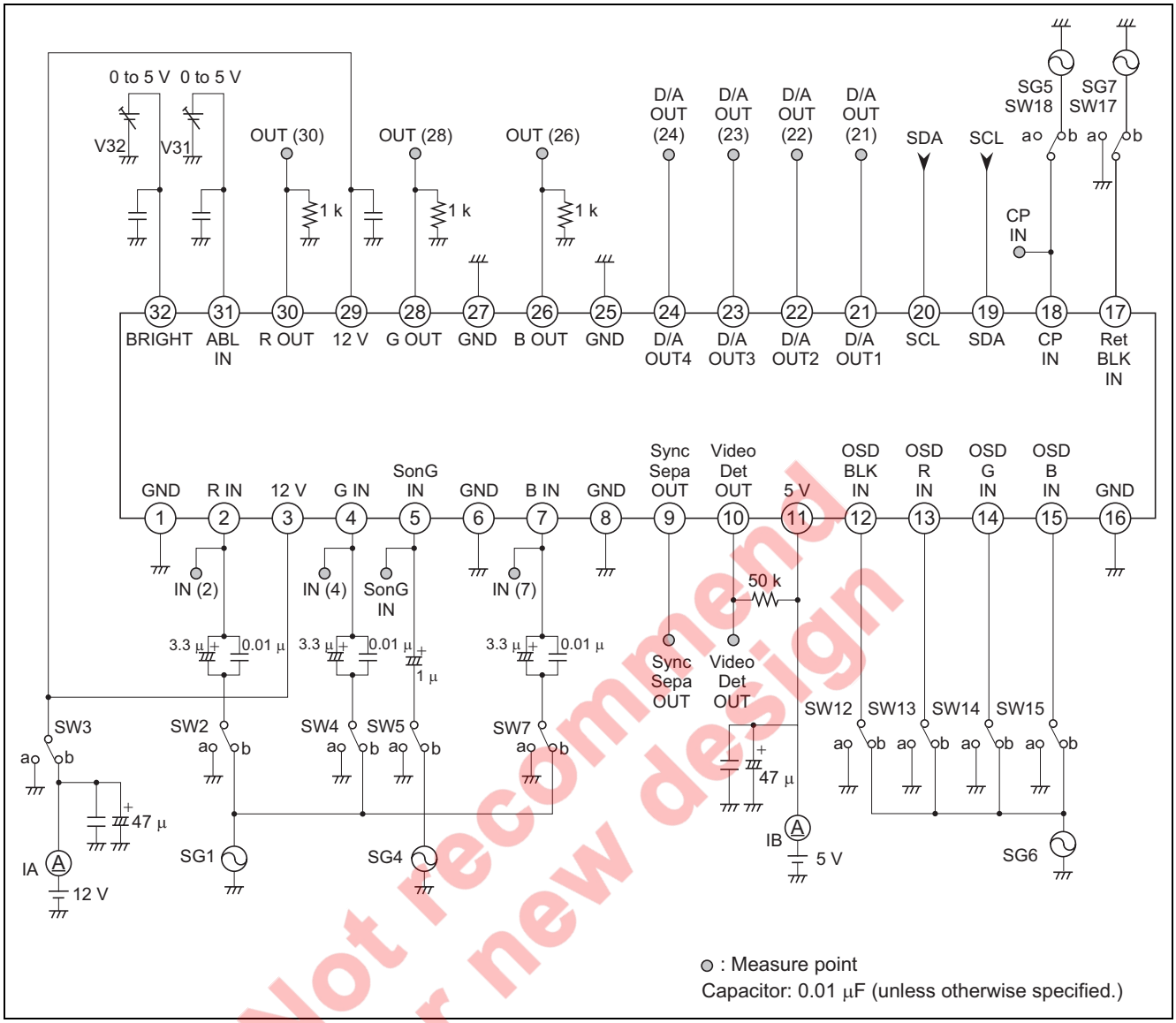
DNL D/A Nonlinearity

The difference of differential non-linearity of D/A OUT must be less than ±1.0 LSB.

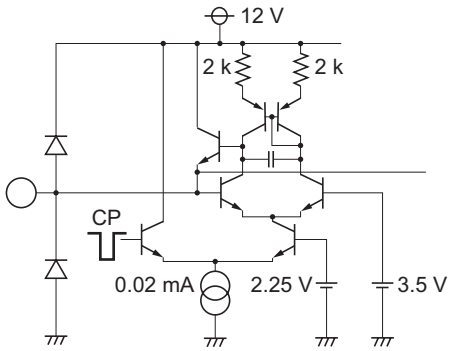
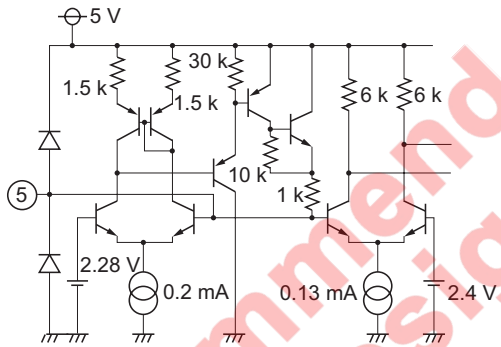
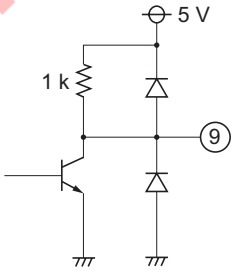
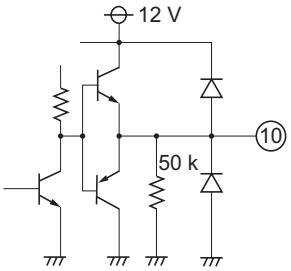
Input Signal

SG No.	Signals
SG1 Video signal (all white)	Pulse with amplitude of 0.7 V_{P-P} (f = 30 kHz). Video width of 25 µs. (75%) (Amplitude is variable.) 
SG4 Video signal (all white, all black)	Video width of 25 µs. (75%)  All white or all black variable. Sync's amplitude is variable.
SG5 Clamp pulse	Pulse width and amplitude are variable. 
SG6 OSD pulse	 Amplitude is variable.
SG7 BLK pulse	Amplitude is variable. 

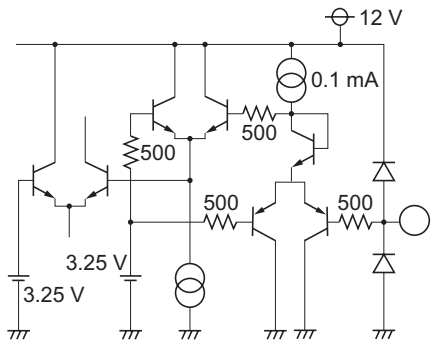
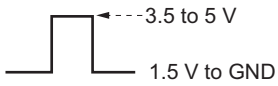
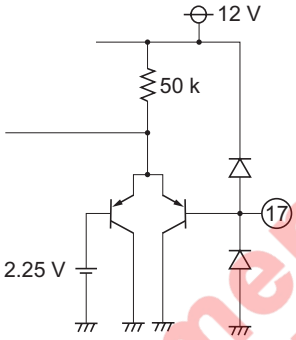
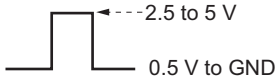
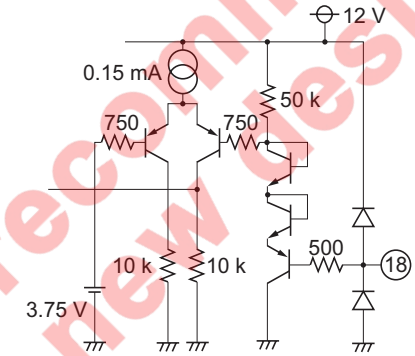
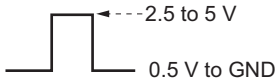
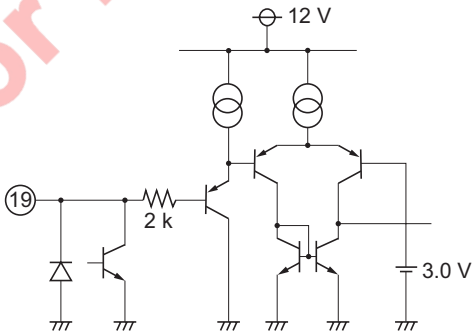
Test Circuit



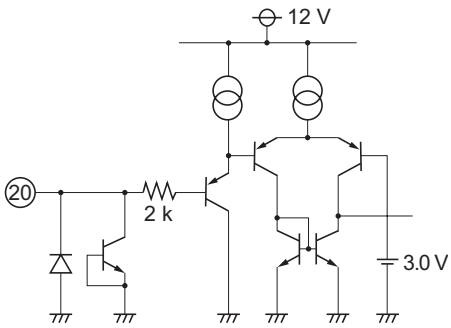
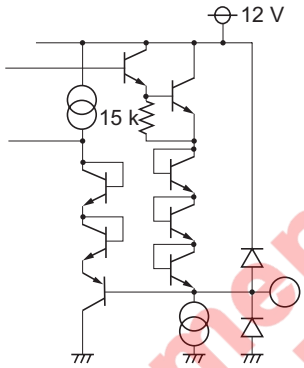
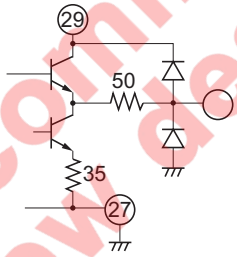
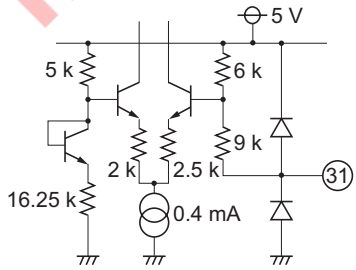
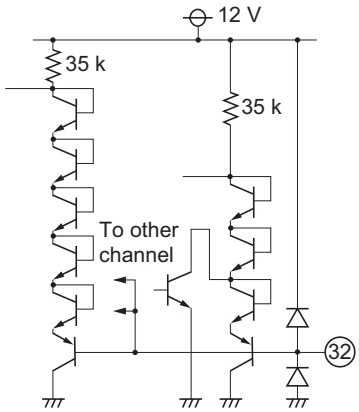
Pin Description

Pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
2 4 7	R IN G IN B IN	3.5		Clamp to about 3.5 V due to clamp pulse from pin 18. Input at low impedance.
3	V_{CC1} (12 V)	12	—	Connect to the power supply that stabilized.
5	SonG IN	When open 2.3		SYNC ON VIDEO input pin. Sync is negative. Input signal at pin 5, compare with the reference voltage of internal circuit in order to separate Sync signal from Sync on Green signal. Input at low impedance. Do not input the signal without the Sync. When it does not use this function, connect to capacitor between GND, turn on Sync Sepa SW by I^2C BUS.
1 6 8 16 27	GND GND 1 GND 2 GND 3 GND 4	GND	—	Connect to GND.
9	Sync Sepa OUT	—		Sync Sepa output pin. When the rise time of the signal is sped up, connect about 2.3 kΩ between 5 V power supply. When it does not use, do openly. So as not to flow into pin 9 8 mA over, resistance value does not make to 2.3 kΩ or under. Output is a positive.
10	Video Det OUT	—		pin 10 needs to connect the 50 kΩ between 5 V power supply. When it does not use this function, turn off Video Det SW by I^2C BUS.
11	V_{CC} (5 V)	5	—	Connect to the power supply that stabilized.

Pin Description (cont.)

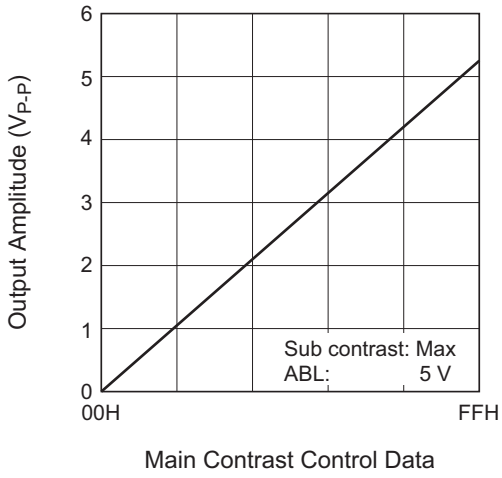
Pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
12 13 14 15	OSD BLK IN OSD R IN OSD G IN OSD B IN	—		Input the positive pulse  When it does not use this function, connect to GND. When input OSD RGB pulse, input OSD BLK pulse without fail.
17	Retrace BLK IN	—		Input the positive pulse  When it does not use this function, connect to GND.
18	Clamp Pulse IN	—		Input the positive pulse which width 200 ns over. Input at low impedance. 
19	SDA	—		SDA of I^2C BUS (Serial data line) Tth = 2.3 V

Pin Description (cont.)

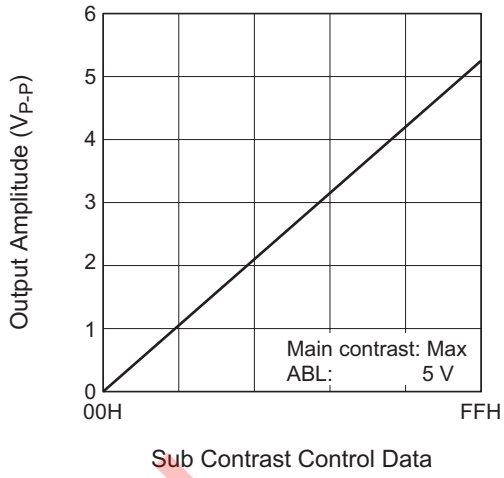
Pin No.	Name	DC Voltage (V)	Peripheral Circuit	Function
20	SCL	—		SCL of I²C BUS (Serial clock line) Tth = 2.3 V
21 22 23 24	D/A OUT 1 D/A OUT 2 D/A OUT 3 D/A OUT 4	—		D/A output pin. Output voltage range is 0 V to 5 V. Input current is below 0.18 mA. Output current is below 0.4 mA.
26 28 30	B OUT G OUT R OUT	Variable		This terminal needs to connect the 1 to 3 kΩ resister between GND. This resistance value may be changed, to improve the video output characteristics.
27	GND 4	—		Connect to GND
29	V_{CC2} (12 V)	12		It is the power supply of emitter follower of RGB output exclusive use.
31	ABL IN	When open 2.5 V		ABL (Automatic beam limiter) input pin. Input voltage in the ranges of 0 V to 5 V. Output amplitude Max with 5 V. Output amplitude Min with 0 V. When it does not use this function, connect to 5 V.
32	BRIGHT	—		It is recommended that the IC is used between pedestal voltage 2 V to 3 V.
25	NC	—	—	Connect to GND.

Typical Characteristics (Reference data)

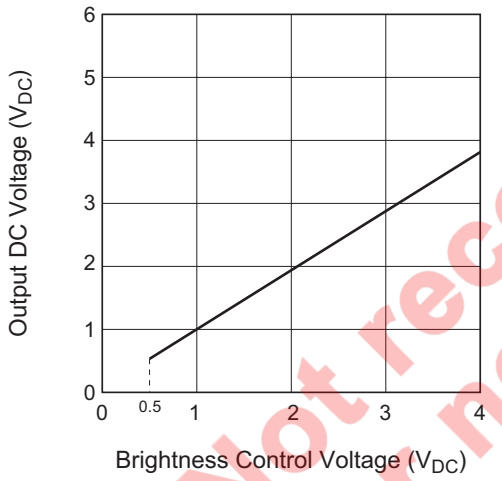
Main Contrast Control Characteristics



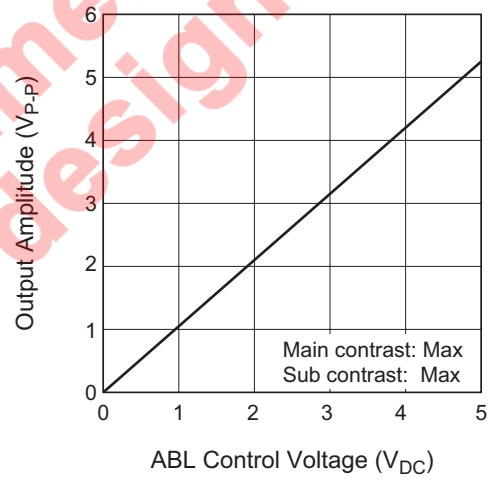
Sub Contrast Control Characteristics



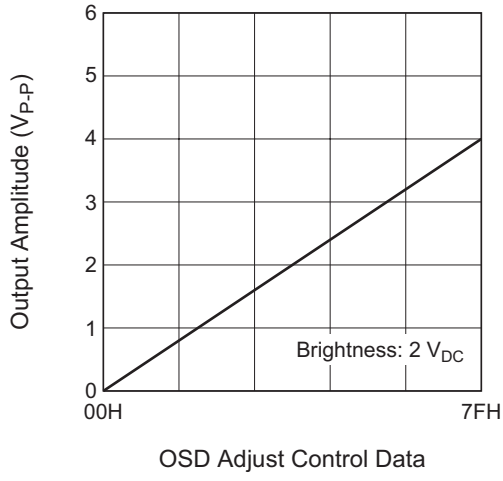
Brightness Control Characteristics



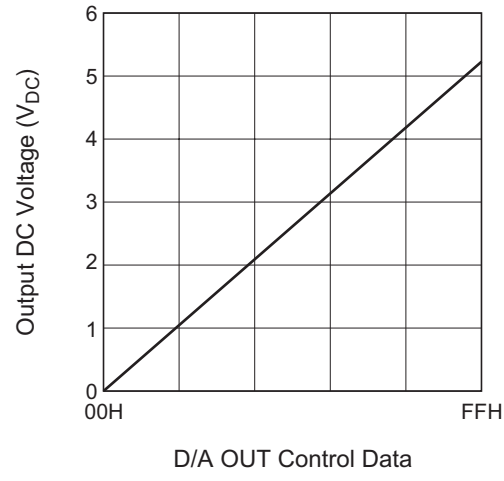
ABL Control Characteristics



OSD Adjust Control Characteristics



D/A OUT Control Characteristics



Application Method for M61311SP/M61316SP

About Clamp Pulse Input

Clamp pulse needs to be always inputted.

Clamp pulse width is recommended:

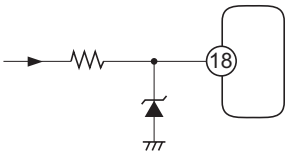
15 kHz at 1.0 µs over

30 kHz at 0.5 µs over

64 kHz at 0.3 µs over

The clamp pulse circuit in ordinary set is a long round about way, and beside high voltage, sometimes connected to external terminal, it is very easy affected by large surge.

Therefore, the figure shown below is recommended.



Notice of Application

Make the nearest distance between output and pull down resister.

Recommend this resister is 1 to 3 kΩ.

Power dissipation in 3 kΩ is smaller than 1 kΩ.

Recommend pedestal voltage of IC output signal is 2 V.

As for the low level of the pulse input of OSD BLK, OSD, Clamp Pulse, Retrace BLK etc., avoid cons the GND level or under.

Pin 31 connect to the voltage that stabilized, and pay attention as surge etc. does not flow into.

V_{CC} (12 V, 5 V) connects to the power supply that stabilized, and bypass-capacitor connects near the term.

When capacitor is connected to pin 29, it sometimes oscillates. Do not connect capacitor to pin 29.

Connect to bypass-capacitance of the DC line near the terminal.

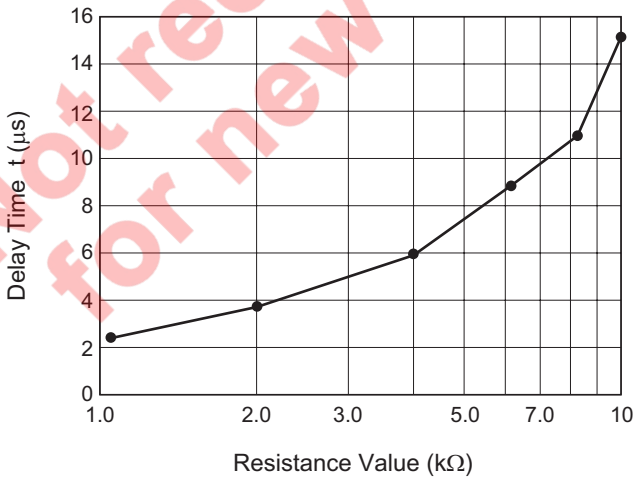
Connect to the NC pin to GND.

The time (t) is from fall of 9 bit of SCL to rise of acknowledge.

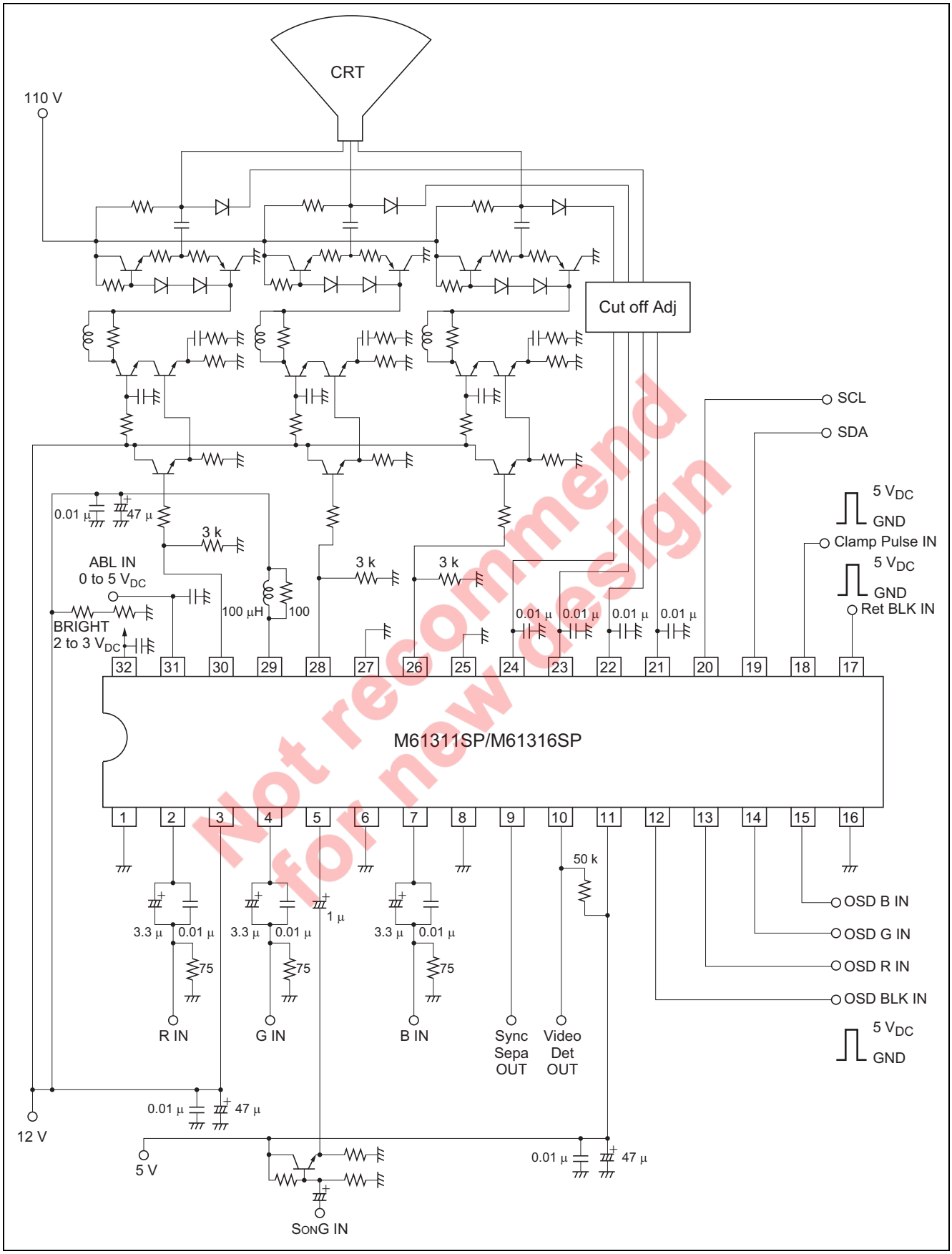
About the forwarding of I^2C BUS, the time (t) changes with the resistance that connected outside.

The next SCL does not overlap into this time (t).

Acknowledge Delay Time Characteristics (Reference data)

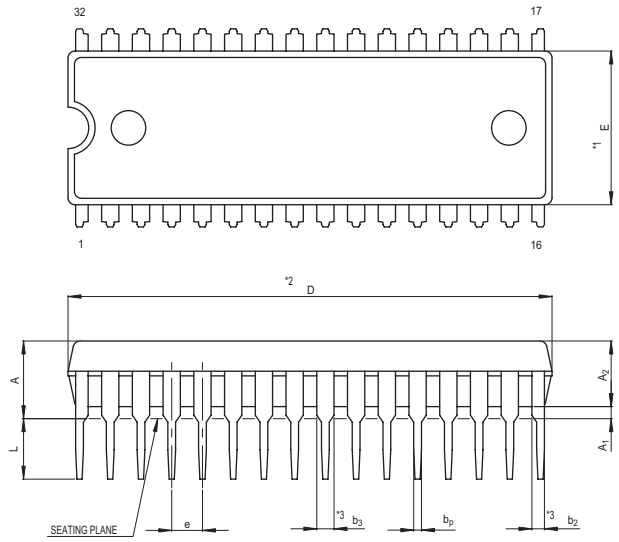


Application Example



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP32-8.9x28-1.78	PRDP0032BA-A	32P4B	2.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	9.86	10.16	10.46
D	27.8	28.0	28.2
E	8.75	8.9	9.05
A	—	—	5.08
A_1	0.51	—	—
A_2	—	3.8	—
b_p	0.35	0.45	0.55
b_2	0.63	0.73	1.03
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

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Colophon .7.2