M62001L/FP to M62008L/FP

Low Power 2 Output System Reset IC Series

REJ03D0781-0100
Rev.1.00
Sep 14, 2005

Description

The M62001 to M62008 are semiconductor integrated circuits whose optimum use is for the detection of the rise and fall in the power supply to a microcomputer system in order to reset or release the microcomputer system.

The M62001 to M62008 carry out voltage detection in two-steps and have two output pins. As Bi-CMOS process and low power dissipating circuits are employed, they output optimum signals through each output pin to a system that requires RAM backup. As output signals, interruption ($\overline{INT}$) and compulsive reset ($\overline{RESET}$) signals are available. The interruption signal ($\overline{INT}$) is used to alter the microcomputer from normal mode to backup mode and vice versa. These output signals are classified into pulse type (M62001 to M62004) and hold type (M62005 to M62008).

Features

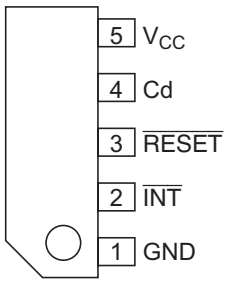
- Bi-CMOS process realizes a configuration of low current dissipating circuits.
  Circuit current
  I_{CC} = 5 µA (Typ, normal mode, V_{CC} = 5.0 V)
  I_{CC} = 1 µA (Typ, backup mode, V_{CC} = 2.5 V)
- Two-step detection of supply voltage
  Detection voltage in normal mode (2 types)
  V_S = 4.45 V/4.25 V (Typ)
  Detection voltage in backup mode
  V_{BATT} = 2.15 V (Typ)
- Two outputs
  Reset output ($\overline{RESET}$): output of compulsive reset signal
  Interruption output ($\overline{INT}$): output of interruption signal
- Two types of output forms: CMOS and open drain
- Two types of interruption output ($\overline{INT}$) signals
  Pulse type (M62001 to M62004)
  Hold type (M62005 to M62008)
- Two types of outline packages
  5-pin plastic SIP (single in-line package)
  8-pin plastic SOP (mini flat package)
- Output based on RAM backup mode (see the timing chart)

Application

- Prevention of errors in microcomputer system in electronic equipment that requires RAM backup, such as office, industrial, and home-use equipment.

Pin Arrangement

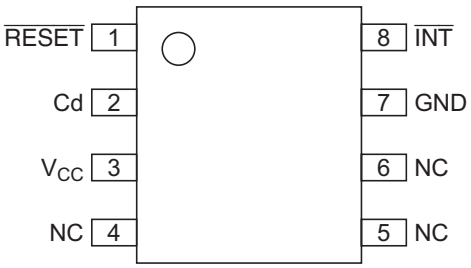
M62001L to M62008L



(Top view)

Package: 5P5T

M62001FP to M62008FP

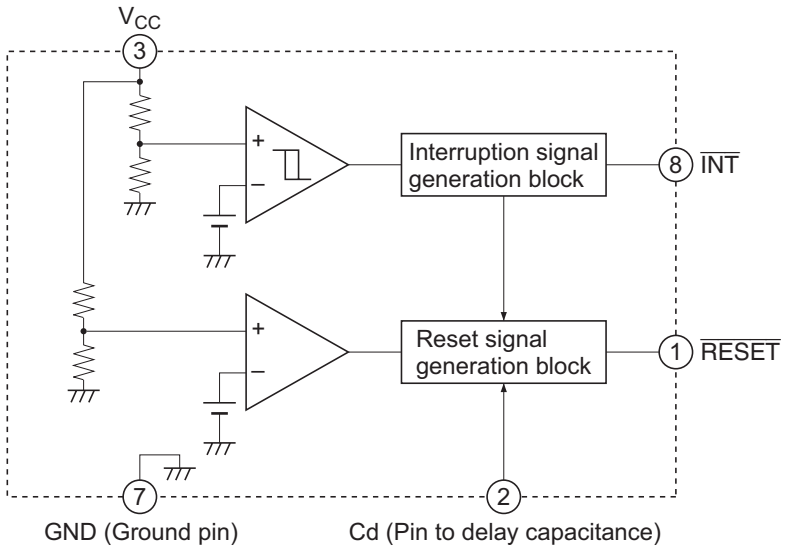


(Top view)

NC: No Connection

Package: PRSP0008DA-A (8P2S-A)

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

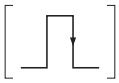
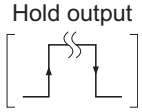
Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	8	V	
Output sink current	Isink	5	mA	
Power dissipation	Pd	440	mW	
Thermal derating	Kθ	4.4	mW/°C	Ta ≥ 25°C
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

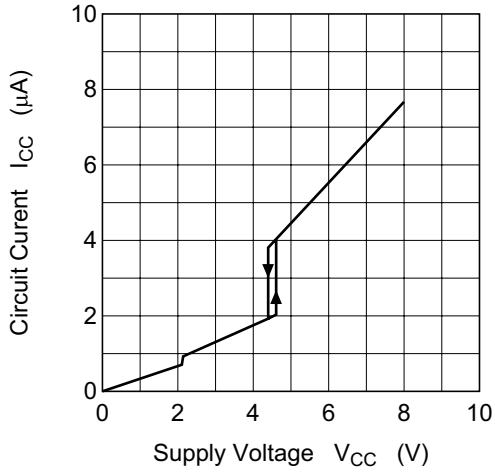
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Supply voltage	V_S	4.30	4.45	4.60	V	Interruption level during V_{CC} drop (Equivalent to V_{SL})	M62001, M62002, M62005, M62006,
		4.05	4.25	4.45			M62003, M62004, M62007, M62008,
Battery voltage	V_{BATT}	2.00	2.15	2.30		Reset level at backup	
Hysteresis voltage	ΔV_S	—	100	—	mV	$\Delta V_S = V_{SH} - V_{SL}$	
Circuit current	I_{CC}	—	5.0	20	μA	V_{CC} = 5.0V: in normal mode	
		—	1.0	4		V_{CC} = 2.5V: in backup mode	
Sink ability	Vsat1	—	0.2	0.4	V	V_{CC} = 4V, I_O = 4mA (Output saturation voltage of N-ch transistor)	
Source ability	Vsat2	—	0.2	0.4		V_{CC} = 4V, I_O = 1mA (Output saturation voltage of P-ch transistor) [CMOS output] M62001, M62003, M62005, M62007	
Delay time	t_d	—	50	—	ms	External capacitance Cd = 0.33μF	
Pulse width	t_{pw}	—	7	10	μs	Output pulse width (M62001, M62002, M62003, M62004)	
Reset output response time	$t_{\overline{RESET}}$	—	30	—	μs	Time between V_{CC} (when falling) = V_{BATT} and output of $\overline{RESET}$ signal	
Interruption output reset time	$t_{\overline{INT}}$	—	100	—	μs	Time between V_{CC} (when falling) = V_S and output of $\overline{INT}$ signal	

Summary of M62001L/FP to M62008L/FP

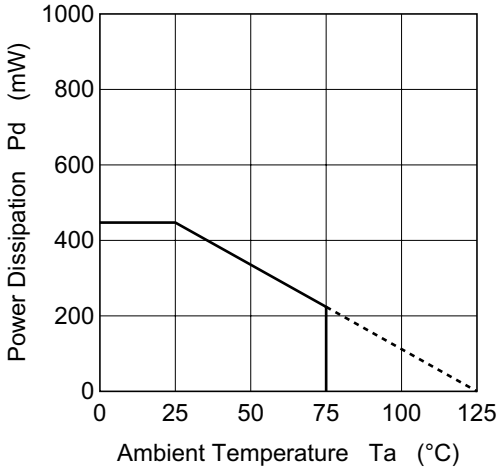
Type No.	Supply Voltage Detection Level V_S (V)	Battery Voltage Detection Level V_{BATT} (V)	Output Form	Interruption Signal Output Mode
M62001L/FP	4.45	2.15	CMOS	Pulse output 
M62002L/FP			Open drain	
M62003L/FP	4.25		CMOS	
M62004L/FP			Open drain	
M62005L/FP	4.45		CMOS	Hold output 
M62006L/FP			Open drain	
M62007L/FP	4.25		CMOS	
M62008L/FP			Open drain	

Typical Characteristics

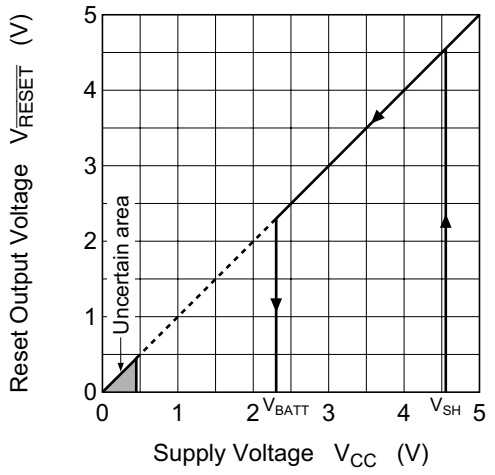
Circuit Curent vs. Supply Voltage



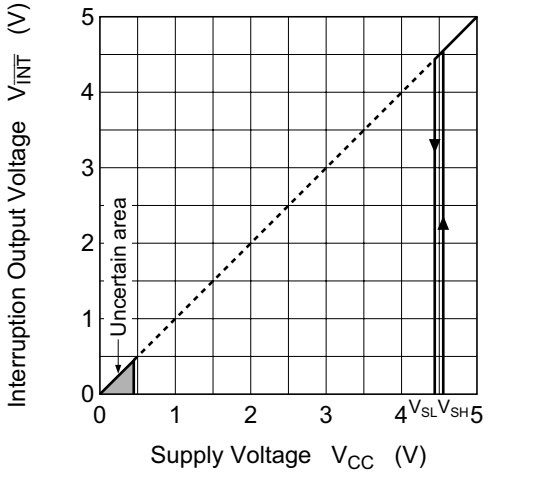
Thermal Derating
(Maximum Rating)



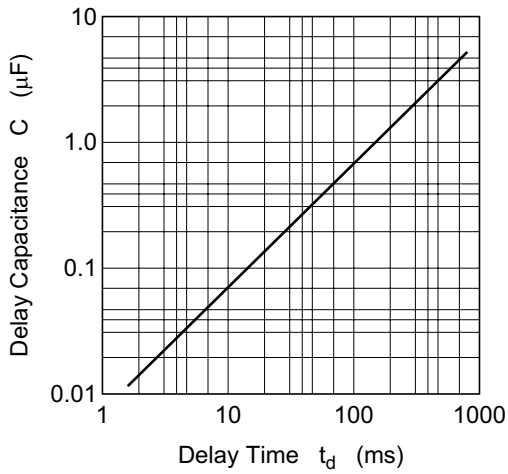
Reset Output Voltage vs. Supply Voltage



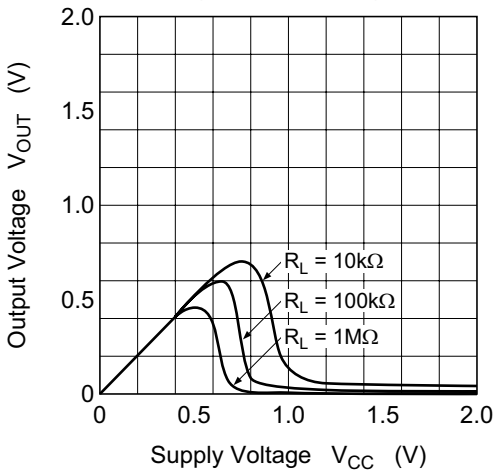
Interruption Output Voltage vs. Supply Voltage



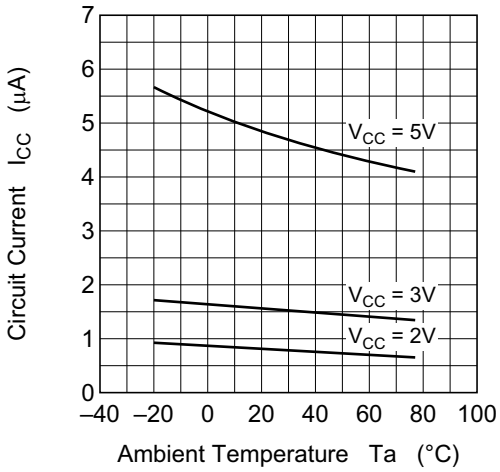
Delay Capacitance vs. Delay Time



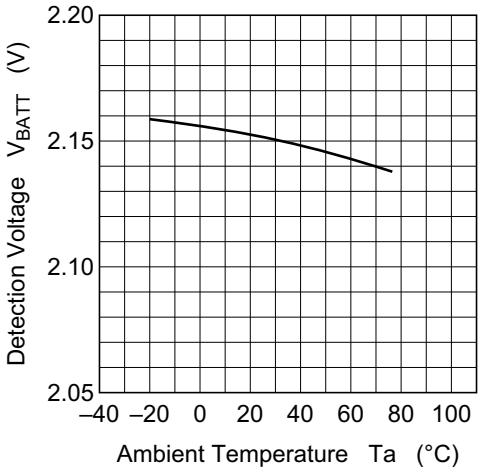
Limit Operating Voltage
(Open drain type)



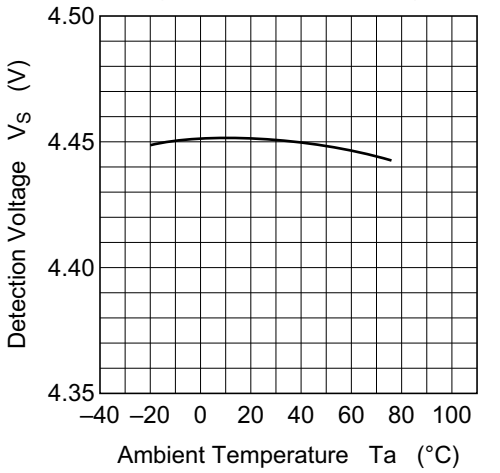
Circuit Current vs. Ambient Temperature



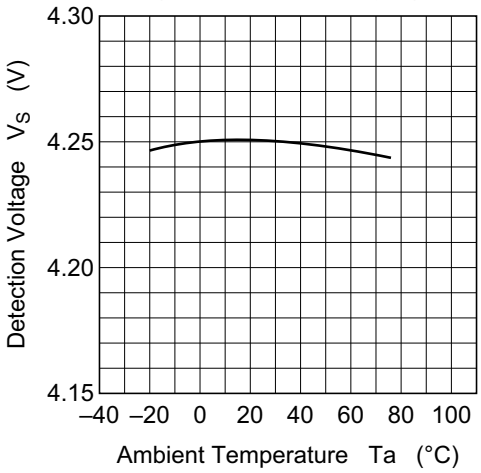
Detection Voltage vs. Ambient Temperature
(Battery voltage)



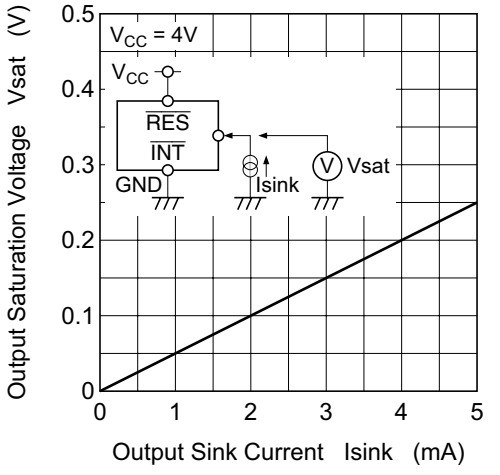
Detection Voltage vs. Ambient Temperature
(Detection at 4.45V type)



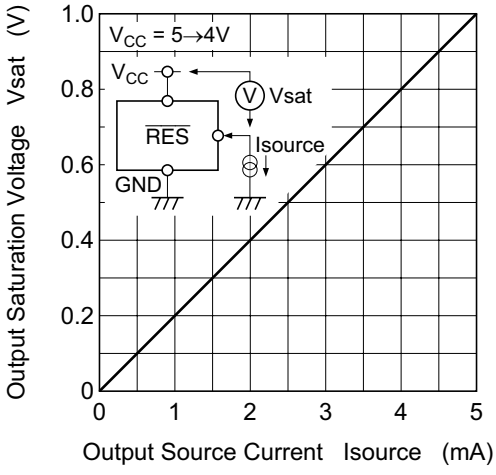
Detection Voltage vs. Ambient Temperature
(Detection at 4.25V type)



Nch Output Saturation Voltage vs. Output Sink Current



Pch Output Saturation Voltage vs. Output Source Current



Operating Principle

Description

In general, the memory backup function of a microcomputer, as shown in figure 1, uses two diodes to switch between main power supply and backup power supply. The M62001 to M62008 are ICs that, in such memory backup operation, monitor in two steps each voltage on the V_{DD} line.

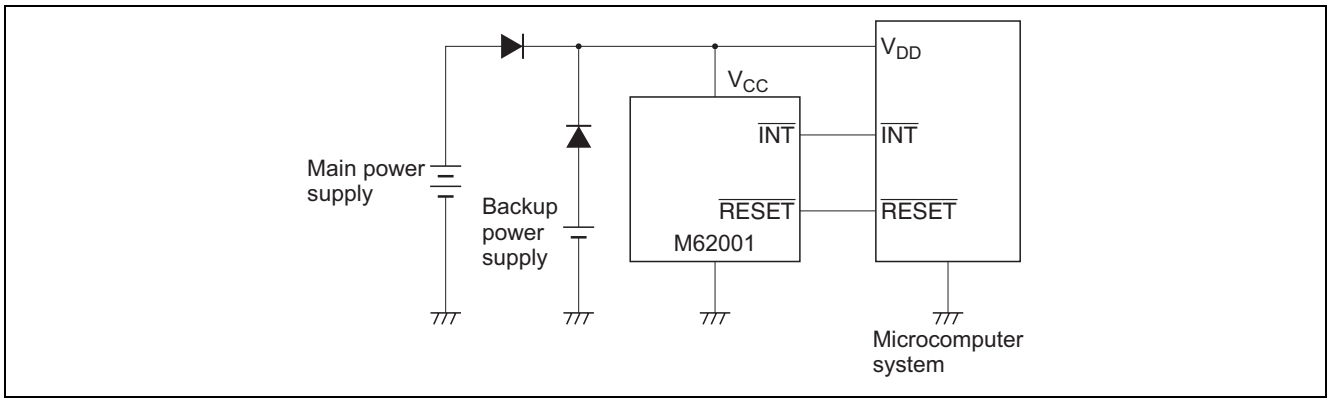


Figure 1

The ICs have an intelligent sequence such as substantial hysteresis action of $\overline{\text{RESET}}$ toward normal state at restoration of supply voltage, as well as two-step detection in low power dissipation mode.

Detailed Description

1. Two-step detection
   The ICs perform two-step detection of supply voltage and have two output pins ($\overline{\text{INT}}$ and $\overline{\text{RESET}}$). Although they have two comparators for two-step detection, they differ significantly from such that are simply provided with independent detectors, because the $\overline{\text{RESET}}$ output signal is dependent at power-up and the like upon the $\overline{\text{INT}}$ output signal.

2. $\overline{\text{INT}}$ output (Detection of 4.45 V and 4.25 V)
   The $\overline{\text{INT}}$ output at the power-up of supply voltage detects V_{SH} (4.45 V/4.25 V) to inform the microcomputer system of the fact that the supply voltage has reached its normal level. When the supply voltage drops from its normal level to V_{SL} (4.45 V/4.25 V) an interruption signal is output to alter the microcomputer system into RAM backup mode. The microcomputer at this point enters sleep state and secures memory by a stop command issued by the interruption signal. These detection voltage, V_{SH} the rise, and V_{SL} the fall, of supply voltage, have a 100 mV hysteresis voltage between themselves.

   $$V_{SH} - V_{SL} \approx 100 \text{ (mV)}$$

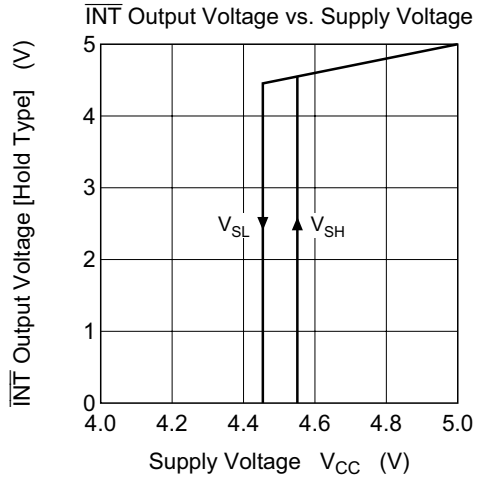


Figure 2 $\overline{\text{INT}}$ Output (Detection of 4.45 V and 4.25 V)

3. $\overline{\text{RESET}}$ output (Detection of 2.15 V)

The $\overline{\text{RESET}}$ outputs a signal to prevent the microcomputer from malfunctioning due to a drop in supply voltage. When powering up, $\overline{\text{RESET}}$ is kept at low level until the supply voltage reaches V_{SH}. If the supply voltage rises to V_{SH}, $\overline{\text{RESET}}$ is set to high level. By inserting a capacitor between the Cd pin and GND, it is possible to produce a desired delay time (t_d). To set a delay time, equation below is used.

$$t_d \approx 1.52 \times 10^5 \times C \text{ (s)}$$

Once the supply voltage has exceeded V_{SH} and the $\overline{\text{RESET}}$ output is set to high level, $\overline{\text{RESET}}$ maintains the high level until the supply voltage drops to V_{BATT}. When the supply voltage drops to V_{BATT}, $\overline{\text{RESET}}$ goes low thereby resetting and initializing the microcomputer.

The $\overline{\text{RESET}}$ output has a large hysteresis voltage of approximately 2 V between the rise in supply voltage at power-up and its fall.

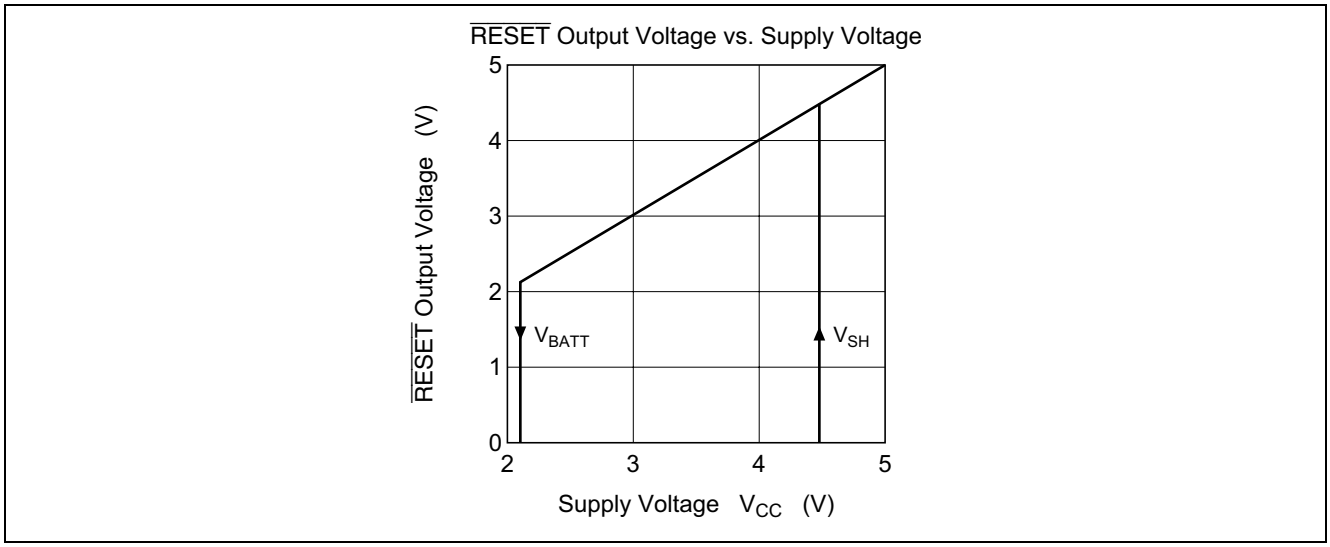
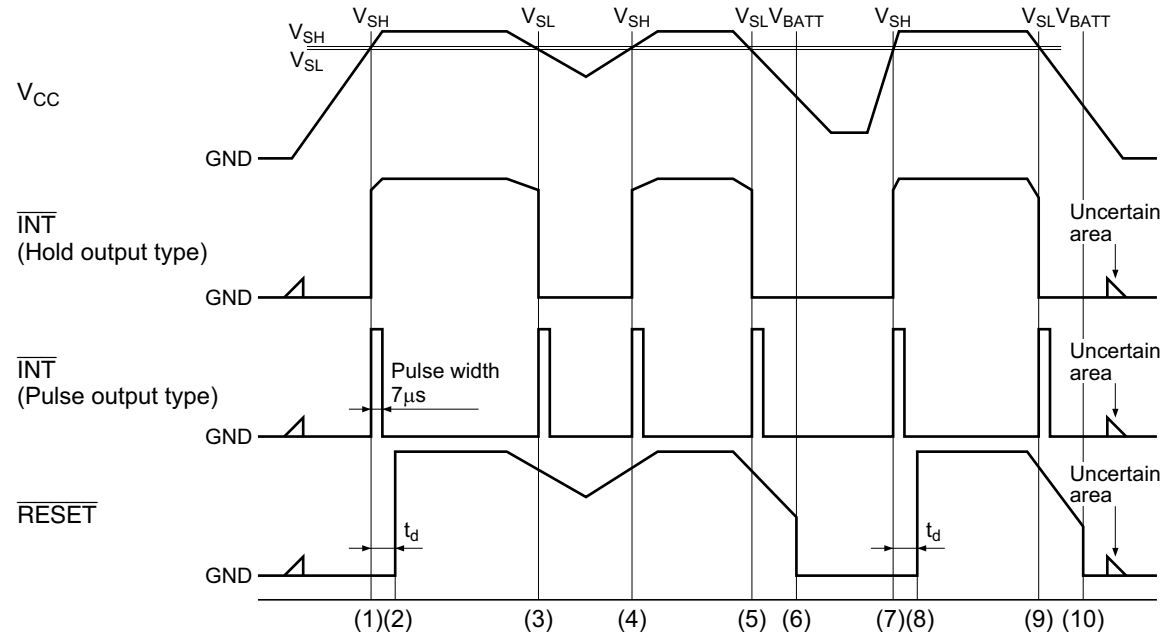


Figure 3 $\overline{\text{RESET}}$ Output (Detection of 2.15 V)

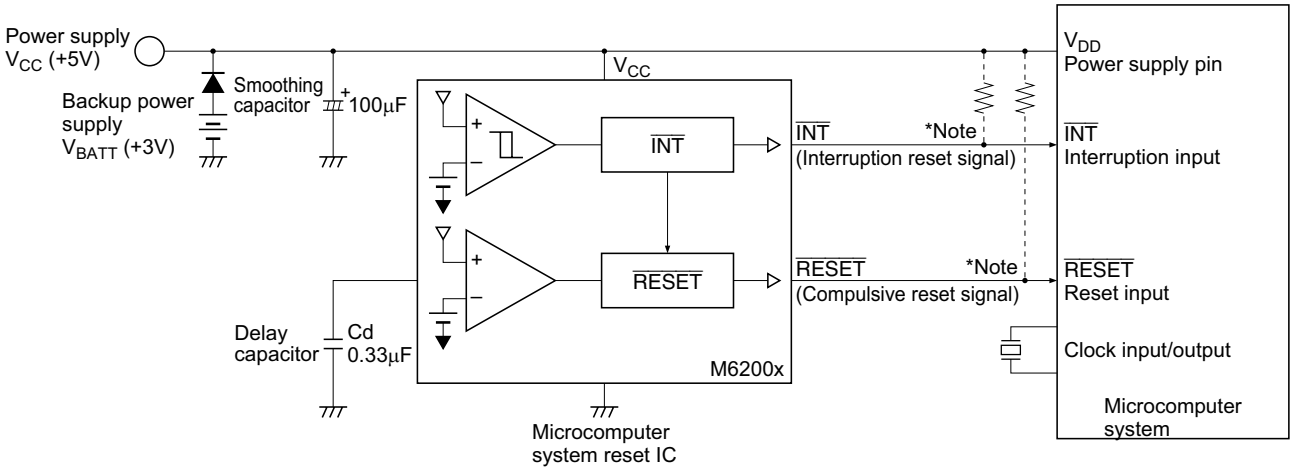
Operating Description



(1): If V_{CC} rises to V_{SH} (4.55V, 4.35V), the $\overline{INT}$ output is set to high level.
*1. A pulse is output if $\overline{INT}$ is of pulse output type.
(2): $\overline{RESET}$ goes high t_d (s) after V_{SH}.
*1. $t_d \approx 1.52 \times 10^5 \times C$ (s)
(3): If V_{CC} drops to V_{SL} (4.45V, 4.25V), $\overline{INT}$ goes low.
*1. A pulse is output if $\overline{INT}$ is of pulse output type.
*2. The $\overline{RESET}$ output continues to be held high.
(4): If V_{CC} returns to V_{SH}, the $\overline{INT}$ output is set to high level.
(5): Same as (3).
(6): If V_{CC} becomes lower than V_{BATT} (2.15V), the $\overline{RESET}$ output is set to low thereby resetting the microcomputer and initializing system.
(7): Same as (1).
(8): Same as (2).
(9): Same as (3) and (5).
(10): Same as (6).

Figure 4 Operating Waveform

Application Example



Note: A pull-up resistor is required only in the case of open-drain output.

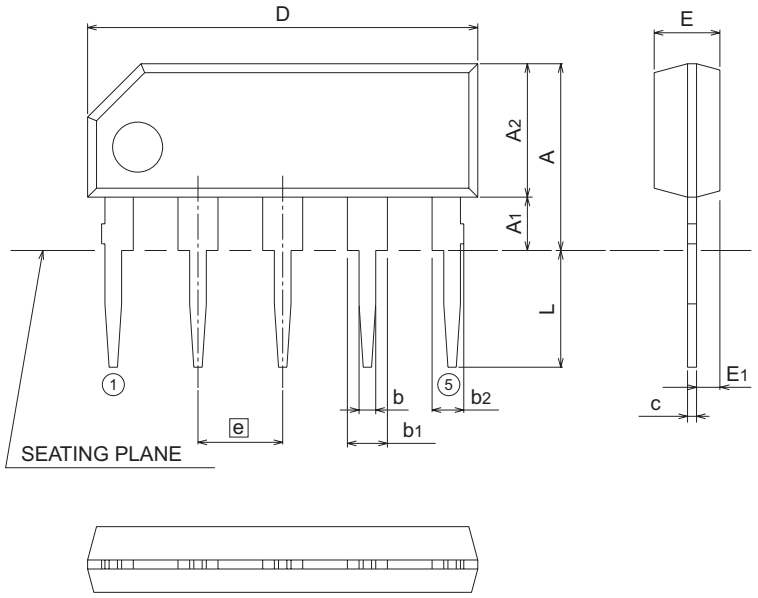
Figure 5 Application Example

Package Dimensions

5P5T

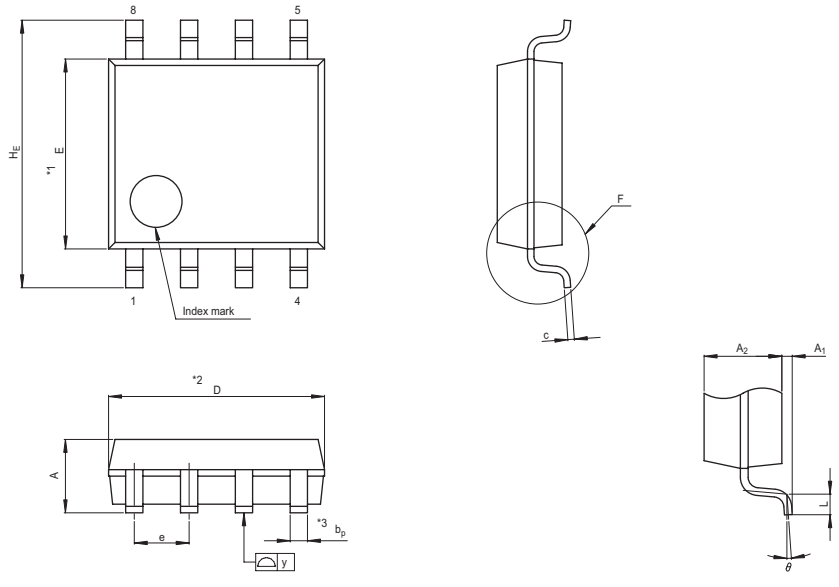
Plastic 5pin 240mil SIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SIP5-P-240-2.54	–	0.22	Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	6.1
A_1	1.4	–	–
A_2	–	4.0	–
b	0.4	0.5	0.6
b_1	1.1	1.2	1.5
b_2	0.75	0.85	1.15
c	0.22	0.27	0.34
D	11.5	11.7	11.9
E	1.77	1.97	2.17
E_1	0.6	0.7	0.8
e	–	2.54	–
L	3.0	–	–

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	——	1.5	——
A_1	0.05	——	——
A	——	——	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	——	10°
H_E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	——	——	0.1
L	0.2	0.4	0.6

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Colophon .3.0