M62021L/P/FP

System Reset IC with Switch for Memory Backup

REJ03D0784-0200
Rev.2.00
Jun 15, 2007

Description

The M62021 is a system IC that controls the memory backup function of microcomputer (internal RAM).

The IC outputs reset signals (RES/$\overline{\text{RES}}$) to a microcomputer at power-down and power failure. It also shifts the power supply to RAM from main to backup, outputs a signal ($\overline{\text{CS}}$) that invokes standby mode, and alters RAM to backup circuit mode.

The M62021 contains, in a single chip, power supply monitor and RAM backup functions needed for a microcomputer system, so that the IC makes it possible to construct a system easily and with fewer components compared with a conventional case that uses individual ICs and discrete components.

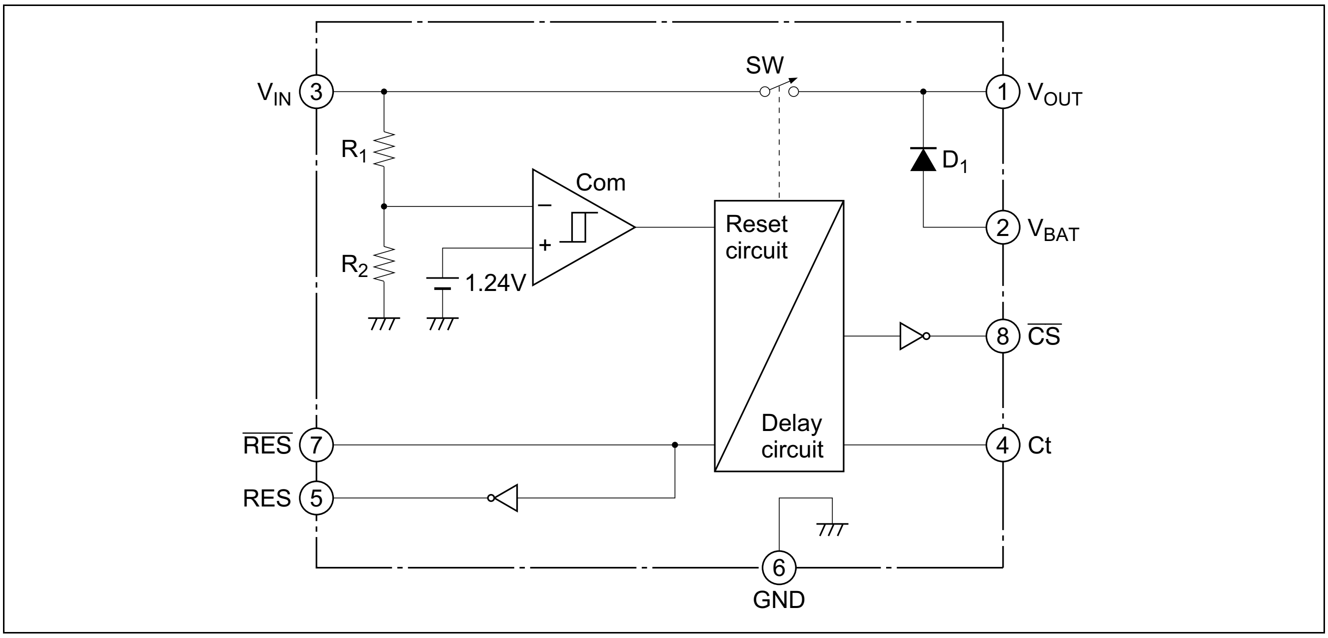
Features

- Built-in switch for selection between main power supply and backup power supply to RAM.
- Small difference between input and output voltage (I_{OUT} = 80 mA, V_{IN} = 5 V) 0.2 V Typ
- Detection voltage (power supply monitor voltage) 4.40 V ± 0.2 V
- Chip select signal output ($\overline{\text{CS}}$)
- Two channels of reset outputs (RES/$\overline{\text{RES}}$)
- Power on reset circuit built-in
- Delay time variable by an external capacitance connected to Ct pin
- Facilitates to form backup function with a few number of components

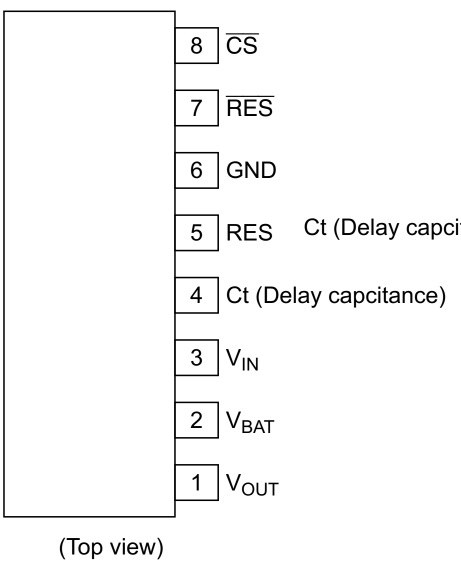
Application

- Power supply control systems for memory backup of microcomputer system and SRAM boards with built-in backup function that require switching between external power supply and battery.

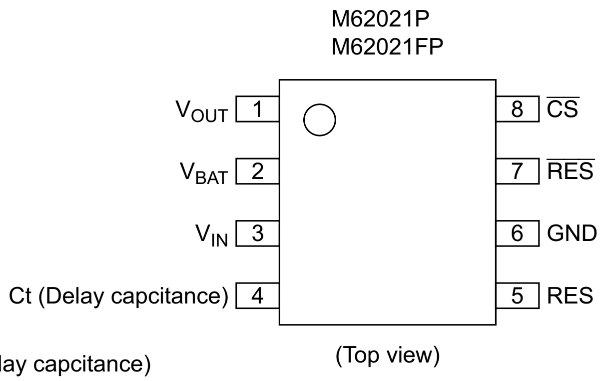
Block Diagram



Pin Arrangement



Outline: PRSS0008AA-A (8P5) [L]



Outline: PRDP0008AA-A (8P4) [P]
PRSP0008DE-C [FP] (recommend)
PRSP0008DA-A (8P2S-A) [FP] (not recommend for new design)

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions	
Input voltage	V_{IN}	7	V		
Output current	I_{OUT}	100	mA		
Power dissipation	Pd	800	mW	8-pin SIP	
		625		8-pin DIP	
		440		8-pin SOP	
Thermal derating	Kθ	8	mW/°C	Ta ≥ 25°C	8-pin SIP
		6.25			8-pin DIP
		4.4			8-pin SOP
Operating temperature	Topr	–20 to +75	°C		
Storage temperature	Tstg	–40 to +125	°C		

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Detection voltage	V_S	4.2	4.4	4.6	V	V_{IN} (at the change from H→L)	
Hysteresis voltage	ΔV_S	50	100	200	mV	$\Delta V_S = V_{SH} - V_{SL}$	
Temperature coefficient of detection voltage	$V_S/\Delta T$	—	0.005	—	%/°C		
Circuit current	I_{CC}	—	2.0	4.0	mA	I_{OUT} = 0mA	V_{IN} = 4V
		—	7.5	12.0			V_{IN} = 5V
Difference between input and output voltage	V_{DROP}	—	0.125	0.25	V	V_{IN} = 5V	I_{OUT} = 50mA
		—	0.2	0.4			I_{OUT} = 80mA
Ct output voltage (high level)	$V_{OH(Ct)}$	4.5	5.0	—	V	V_{IN} = 5V *1	
Ct output voltage (low level)	$V_{OL(Ct)}$	—	0.02	0.1	V	V_{IN} = 4V *1	
RES output voltage (high level)	$V_{OH(RES)}$	3.5	4.0	—	V	V_{IN} = 4V *1	
RES output voltage (low level)	$V_{OL(RES)}$	—	0.02	—	V	V_{IN} = 5V	*1
		—	0.05	0.2			Isink = 1mA
$\overline{RES}$ output voltage (high level)	$V_{OH(\overline{RES})}$	4.5	5.0	—	V	V_{IN} = 5V *1	
$\overline{RES}$ output voltage (low level)	$V_{OL(\overline{RES})}$	—	0.02	—	V	V_{IN} = 4V	*1
		—	0.05	0.2			Isink = 1mA
$\overline{CS}$ output voltage (high level)	$V_{OH(\overline{CS})}$	3.50	3.57	—	V	V_{IN} = 4V *2	
		2.40	2.47	—		V_{IN} = 0V, V_{BAT} = 3V *2	
$\overline{CS}$ output voltage (low level)	$V_{OL(\overline{CS})}$	—	0.08	—	V	V_{IN} = 5V	*1
		—	0.1	0.3			Isink = 1mA
Backup diode leakage current	I_R	—	—	±0.5	µA	V_{BAT} = 3V	V_{IN} = 5V
		—	—	±0.5			V_{IN} = 0V
Backup diode forward direction voltage	V_F	—	0.54	0.6	V	I_F = 10µA	
Delay time	t_{pd}	10	27	55	ms	V_{IN} = 0V→5V, Ct = 4.7µF	
Response time	t_d	—	5.0	25.0	µs	V_{IN} = 5V→4V	
$\overline{RES}$ limit voltage of operation	$V_{OPL(\overline{RES})}$	—	0.65	—	V	*3	

Notes: 1. Regarding conditions to measure V_{OH} and V_{OL}, voltage values are to be generated by internal resistance only and no external resistor is used.

2. These values are produced inserting an external resistor, $R_{\overline{CS}}$ = 1 MΩ, between the $\overline{CS}$ pin and GND.

3. With no external resistor (10 kΩ internal resistance only)

Test Circuit

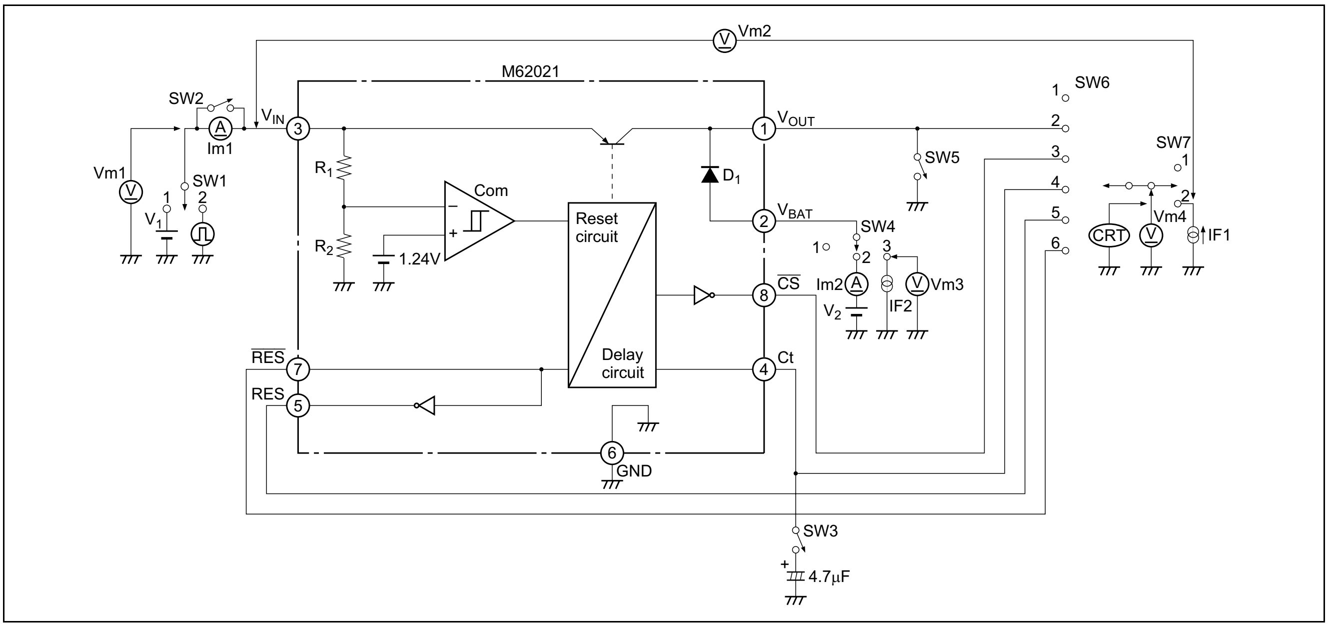


Figure 1 Test Circuit

Switch Matrix

Item		Symbol	V1	V2	IF1	IF2	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	Measuring Instrument
Circuit current		I_{CC}	4V	—	—	—	1	ON	OFF	1	OFF	1	1	Im1
			5V											
Detection voltage (V_{IN} negative-going)	V_{OUT}	V_S (V_{SL})	Decrease from 5V	—	—	—	1	ON	OFF	1	OFF	2	1	*2 Vm4 CRT Vm1
	$\overline{CS}$											3		
	Ct											4		
	RES											5		
	$\overline{RES}$											6		
Difference between input and output voltage		V_{DROP}	5V	—	–50mA	—	1	ON	OFF	1	OFF	2	2	Vm2
					–80mA									
Ct output voltage (high level)		$V_{OH(Ct)}$	5V	—	—	—	1	ON	OFF	1	OFF	4	1	Vm4
Ct output voltage (low level)		$V_{OL(Ct)}$	4V											
RES output voltage (high level)		$V_{OH(RES)}$	4V	—	—	—	1	ON	OFF	1	OFF	5	1	Vm4
RES output voltage (low level)		$V_{OL(RES)}$	5V		1mA								2	
$\overline{RES}$ output voltage (high level)		$V_{OH(\overline{RES})}$	5V	—	—	—	1	ON	OFF	1	OFF	6	1	Vm4
$\overline{RES}$ output voltage (low level)		$V_{OL(\overline{RES})}$	4V		1mA								2	
$\overline{CS}$ output voltage (high level) *1		$V_{OH(\overline{CS})}$	4V	—	—	—	1	ON	OFF	1	OFF	3	1	Vm4
			0V	3V										
$\overline{CS}$ output voltage (low level)		$V_{OL(\overline{CS})}$	5V	—	1mA								2	
Backup diode leakage current		I_R	5V	3V	—	—	1	ON	OFF	2	OFF	1	1	Im2
			0V											
Backup diode forward direction voltage		V_F	0V	—	—	10µA	1	ON	OFF	3	ON	1	1	Vm3
Delay time Response time	V_{OUT}	t_{pd} t_d	—	—	—	—	2 *3	ON	ON *4	1	OFF	2	1	CRT
	$\overline{CS}$											3		
	RES											5		
	$\overline{RES}$											6		

Notes: 1. To measure $V_{OH(\overline{CS})}$, insert a 1 MΩ resistor between the $\overline{CS}$ pin and GND.

2. While monitoring each output by Vm4 or CRT, measure the input voltage Vm1 when the output goes from H to L and L to H. Regarding V_{SH}, raise V_{IN} from 4 V and measure the input voltage Vm1 when the output goes from H to L and L to H. ΔV_S is $V_{SH} - V_{SL}$.

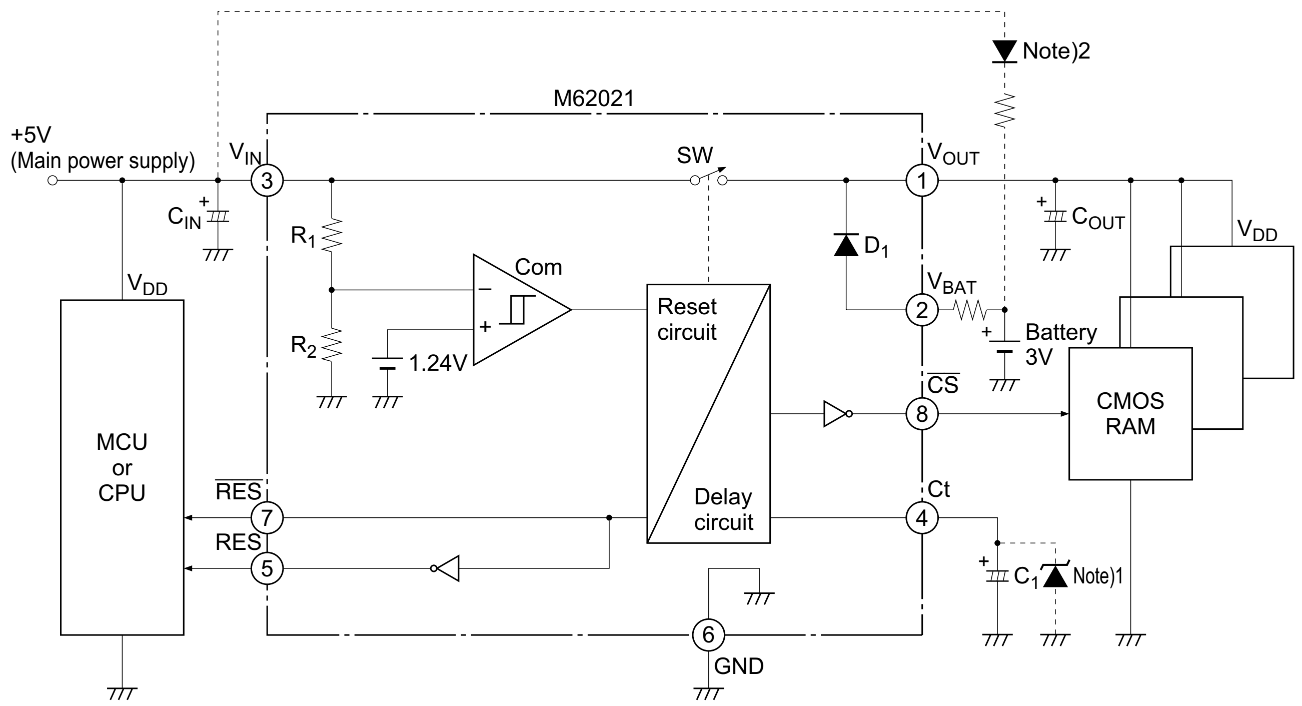
3. To measure delay time, change VIN from 0 V to 5 V and compare, with respect to each pin, the positive-going edge observed on a monitor with that of V_{IN}. To measure response time, change V_{IN} from 5 V to 4 V and compare, with respect to each pin, the negative-going edge observed on a monitor with that of V_{IN}.

4. Set the switch to OFF when measuring response time.

Pin Description

Pin No.	Pin Name	Symbol	Function
1	Power supply output	V_{OUT}	VIN and VBAT are controlled by means of an internal switch and output through VOUT. The pin is capable of outputting up to 100 mA. Use it as VDD of CMOS RAM and the like.
2	Backup power supply input	V_{BAT}	Backup power supply is connected to this pin. If a lithium battery is used, insert a resistor in series for safety purposes.
3	Power supply input	V_{IN}	+5 V input pin. Connect to a logic power supply.
4	Delay capacitor connection pin	Ct	A delay capacitor is connected to this pin. By connecting a capacitor, it is possible to delay each output.
5	Positive reset output	RES	Connect to the positive reset input of a microcomputer. The pin is capable of flowing 1 mA sink current.
6	Ground	GND	Reference for all signals.
7	Negative reset output	$\overline{RES}$	Connect to the negative reset input of a microcomputer. The pin is capable of flowing 1 mA sink current.
8	Chip select output	$\overline{CS}$	Connect to the chip select of RAM. The CS output is at low level in normal state thereby letting RAM be active. Under failure or backup condition, the CS output is set to high level, then RAM enters standby state disabling read/write function. The pin is capable of flowing a 1 mA sink current.

Application Example



Notes: * Capacitance to be connected: C_{IN}: 10µF, C_{OUT}: 4.7µF, Ct: 4.7µF

1. If connecting a zener diode, select one of $V_Z \approx 2V$ to 3V. (I_Z = 0.1mA)
2. When it is necessary to charge the back-up power supply such as using the large-capacity capacitor, connect it to V_{IN} via a diode and a protection resistor.

Figure 2 Application Example

Configuration

Power Supply Detection

The internal reference voltage Vref is compare by means of a comparator with resistor-divided voltage V_R (resistor-divided voltage produced by R_1 and R_2 from V_{IN}).

If the input voltage is 5 V, V_R is set to 1.24 V or higher, so the comparator output is at low level and the Ct output (Q_1 collector output) is set to high level. If the input voltage drops to below 4.4 V in an abnormal condition, V_R becomes below 1.24 V, so the comparator output goes from low to high level and the Ct output, from high to low. The input voltage at this point is called V_{SL}. Next, when the input voltage, restored from abnormal state, has a rise, the comparator output goes from high to low level and the Ct output, from low to high.

The comparator used for detection has 100 mV hysteresis (ΔV_S), so that malfunctioning is prevented in case that the input voltage slowly drops or V_R nearly equals Vref.

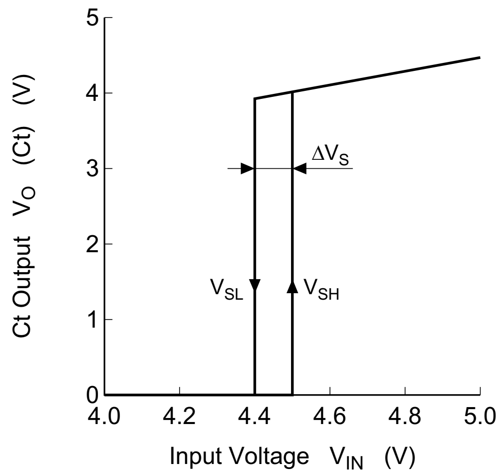


Figure 3

Delay Circuit

Connecting an external capacitor to the Ct pin lets RES, $\overline{\text{RES}}$, $\overline{\text{CS}}$, and V_{OUT} be delayed due to RC transient phenomenon (electric charge).

Delay time is determined as follows.

$$\text{Delay time } (t_{pd}) = C_1 \times (R_3 + R_4) \times 1n \frac{[V_{OH}(Ct) - V_{OL}(Ct)]}{[V_{OH}(Ct) - INV1(V_{TH})]}$$

$$= C_1 \times 22k\Omega \times 0.2614$$

$$\approx 5.75 \times 10^3 \times C_1$$

* C is an external capacitance.

Taking into consideration the time taken by the oscillator of microcomputer to be stable, connect a 4.7 μF capacitor to the Ct pin. (As the response time of detection can be slowed due to internal structure depending in the rising rate of power supply, avoid connecting a too large capacitance.)

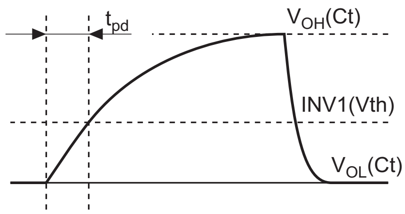


Figure 4 Delayed Output Waveforms of Ct

Schmitt Trigger Circuit

Since waveforms show a gentle rise due to the RC delay circuit, INV1, INV2, R5, and R6 constitute a Schmitt trigger circuit to produce hysteresis so as to prevent each output from chattering.

Internal Circuit

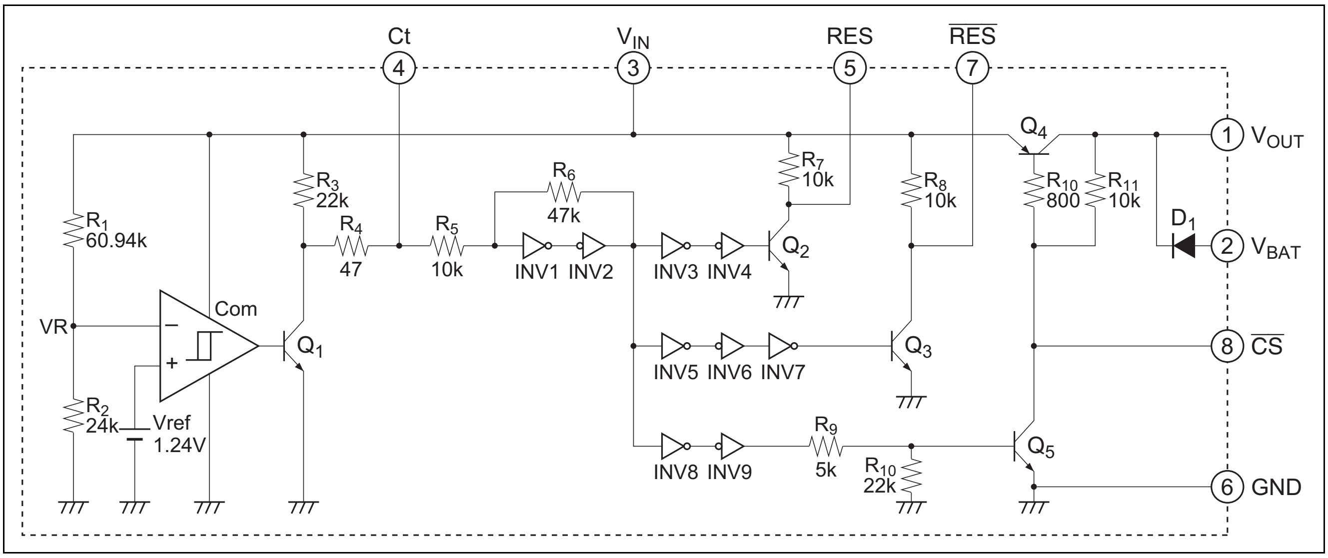


Figure 5 Internal Circuit

Timing Chart

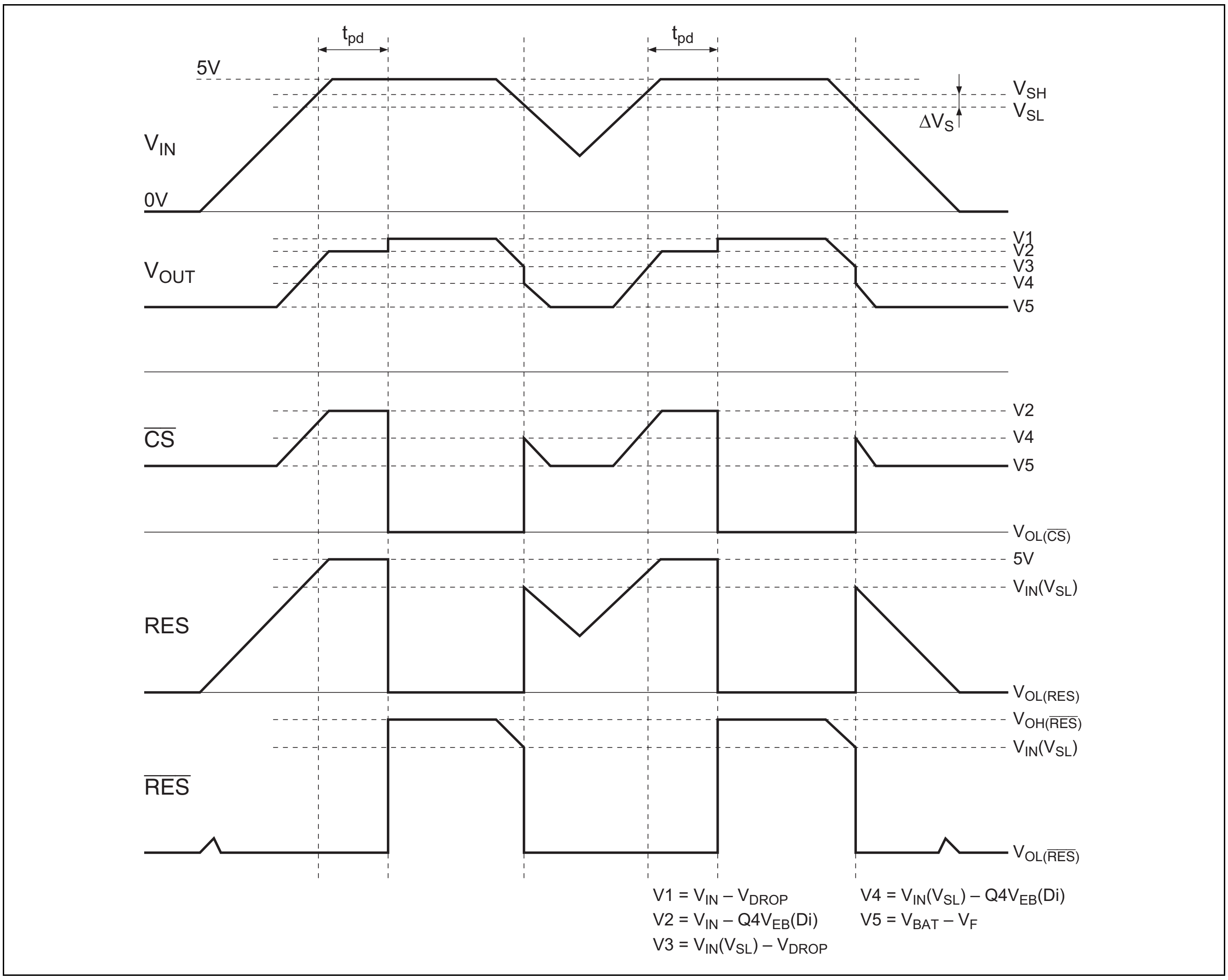
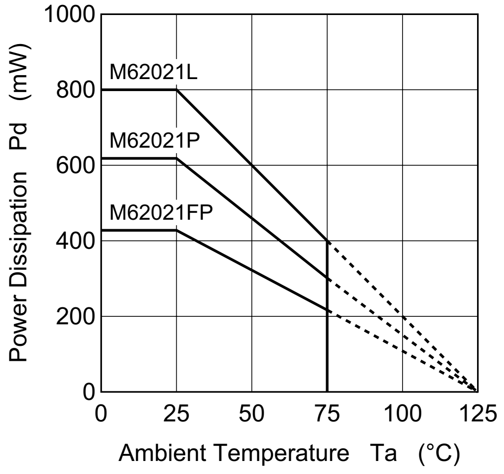


Figure 6 Timing Chart

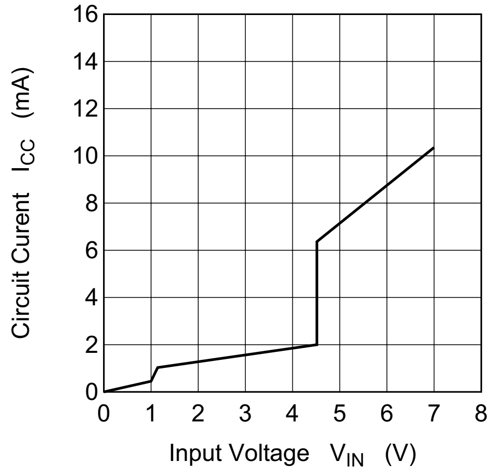
Input Voltage / Output Pin	In Normal Operation	In Failure (Instantaneous Drop)	Restoration from Failure (Instantaneous Drop)	In Backup State
	Input voltage: 5V	Input voltage: 5V→4V Each output varies if the input voltage drops to V_{SL} or under	Input voltage: 4V→5V If the input voltage goes higher than VSL by 100mV, each output varies after delay produced by the delay circuit	Input voltage: 0V Backup voltage: 3V
V_{OUT}	With Q4 set to ON, a voltage (V_{IN} – V_{DROP}) is output	Q4 is turned OFF. A voltage (V_{IN} – Q4V_{EB}(Di)) is output by the diode between E and B of Q4.	Q4 is turned ON after delay and a voltage (V_{IN} – V_{DROP}) is output.	V_{BAT} – V_F
RES	The output level is V_{OL} ($\overline{RES}$) with a logic low	As the state shifts from a logic low to logic high, the output level becomes approximately equal to the input voltage.	A logic high is maintained, and than shifts to a logic high.	—
$\overline{RES}$	The output level is V_{OH} ($\overline{RES}$) with a logic low	As the state shifts from a logic high to logic low, the output level becomes V_{OL} ($\overline{RES}$).	A logic low is held, and than shifts to a logic high.	—
$\overline{CS}$	The output level is V_{OL} ($\overline{CS}$) with a logic low	As the state shifts from a logic low to logic high, the output level becomes the voltage V_{IN} – Q4V_{EB}(Di).	A logic high is maintained, and than shifts to a logic high.	The output is a logic high and the output level is V_{BAT} – V_F

Typical Characteristics

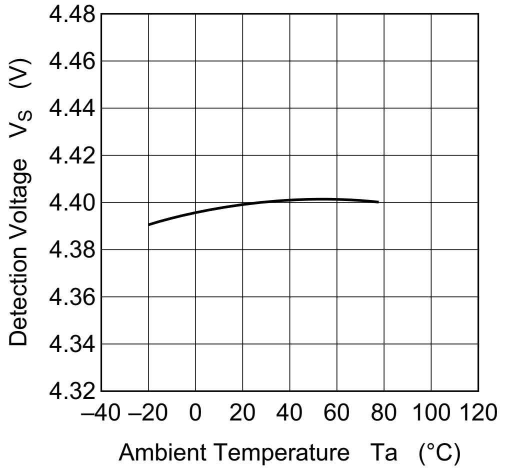
Thermal Derating
(Maximum Rating)



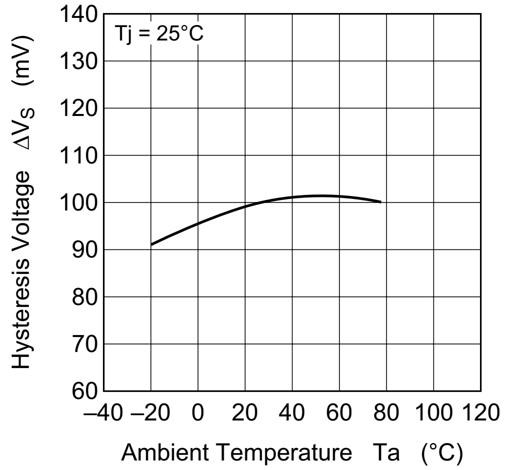
Circuit Curent vs. Input Voltage



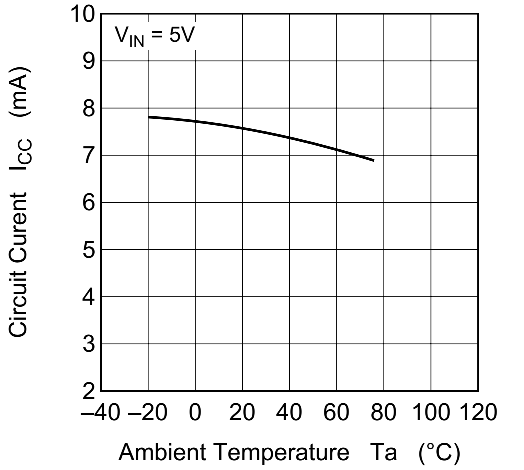
Detection Voltage vs. Ambient Temperature



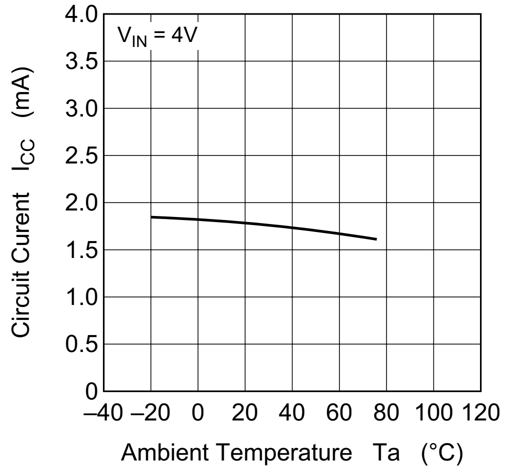
Hysteresis Voltage vs. Ambient Temperature



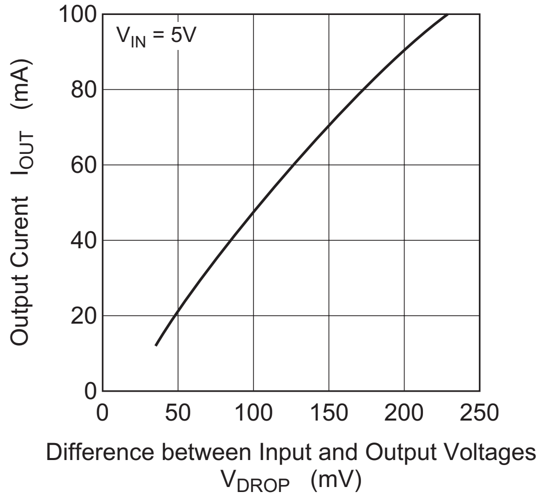
Circuit Curent vs. Ambient Temperature



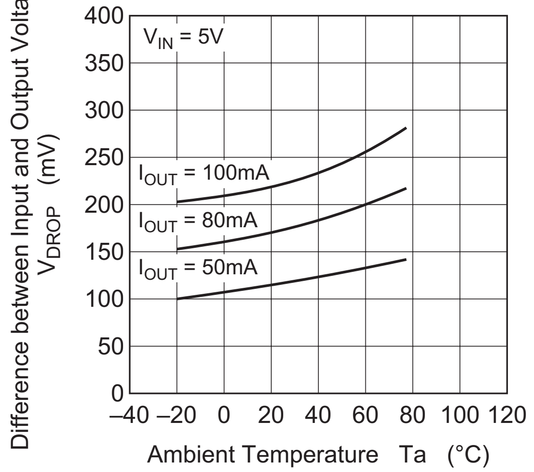
Circuit Curent vs. Ambient Temperature



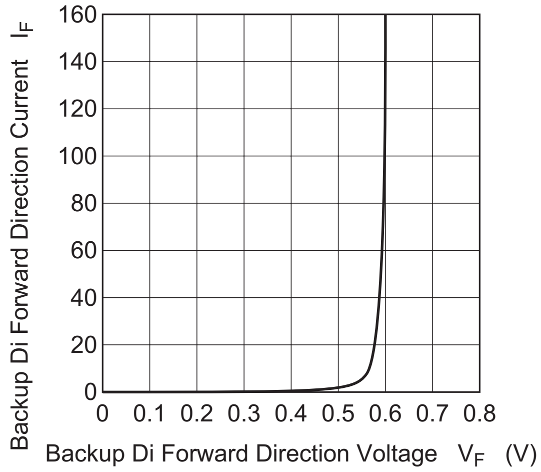
Output Curent vs.
Difference between Input and Output Voltages



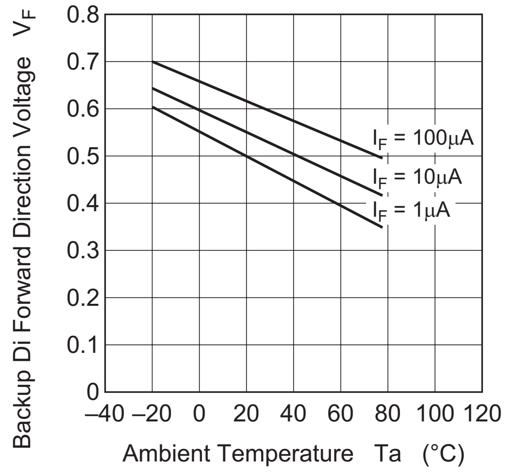
Difference between Input and Output Voltages vs.
Ambient Temperature



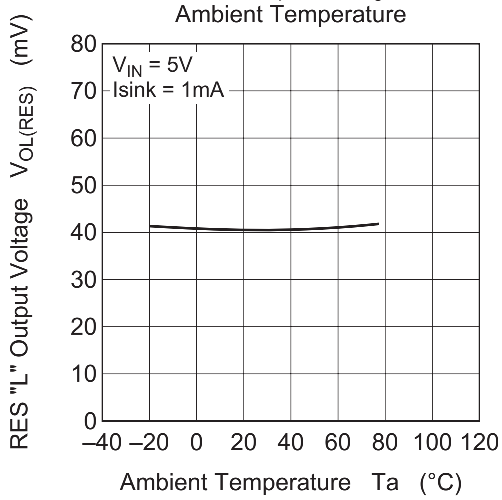
Backup Di Forward Direction Current vs.
Backup Di Forward Direction Voltage



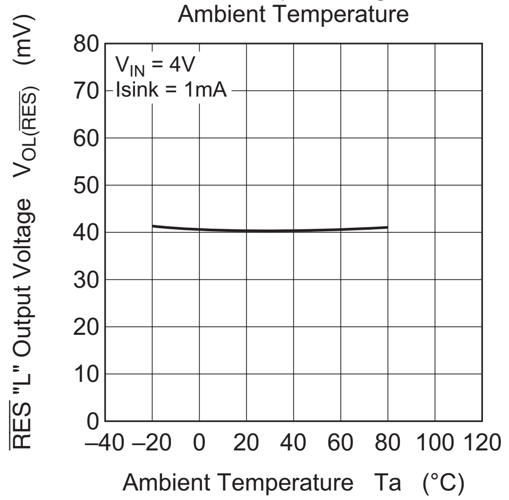
Backup Di Forward Direction Voltage vs.
Ambient Temperature



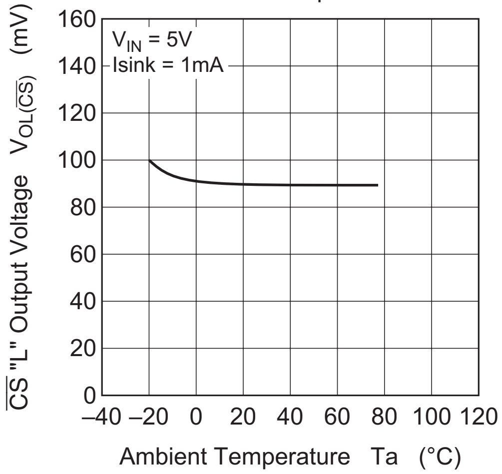
RES "L" Output Voltage vs.
Ambient Temperature



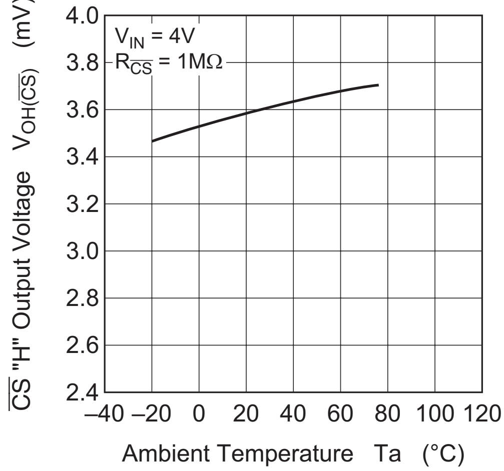
$\overline{RES}$ "L" Output Voltage vs.
Ambient Temperature



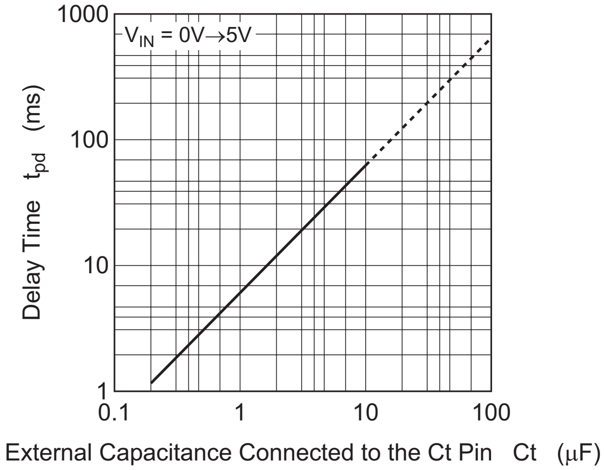
$\overline{CS}$ "L" Output Voltage vs. Ambient Temperature



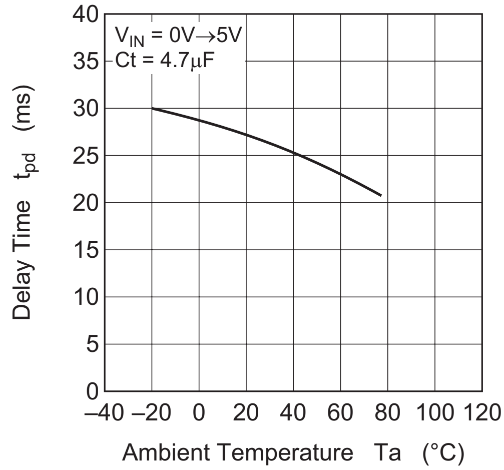
$\overline{CS}$ "H" Output Voltage vs. Ambient Temperature



Delay Time vs. External Capacitance Connected to the Ct Pin

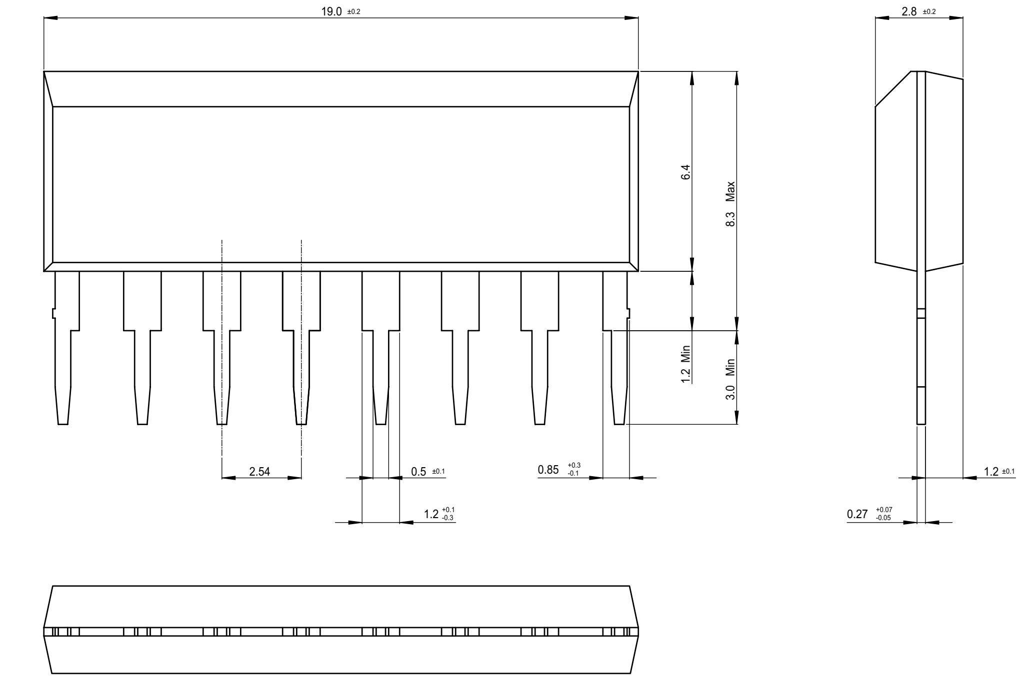


Delay Time vs. Ambient Temperature

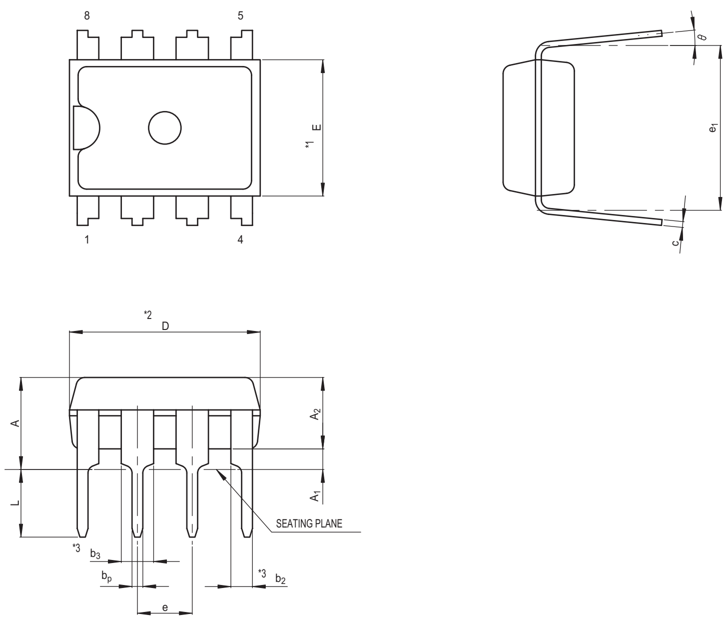


Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SIP8-6.4x19-2.54	PRSS0008AA-A	8P5	0.73g



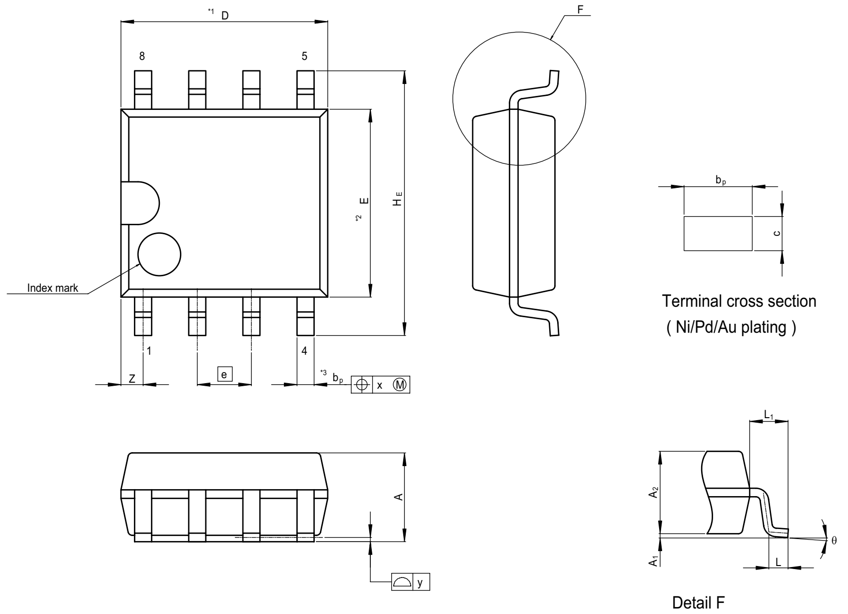
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x8.84-2.54	PRDP0008AA-A	8P4	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	8.7	8.9	9.1
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

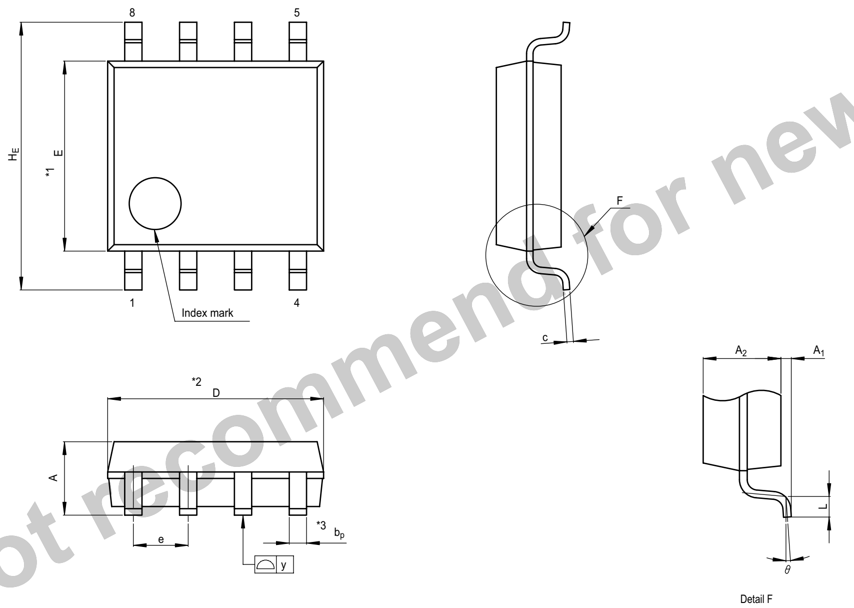
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A_2	—	1.85	—
A_1	0.00	0.1	0.20
A	—	—	2.03
b_p	0.34	0.4	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.7	6.2	6.5
e	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L_1	—	0.90	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	—	1.5	—
A_1	0.05	—	—
A	—	—	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

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