

# M62500P/FP

## SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

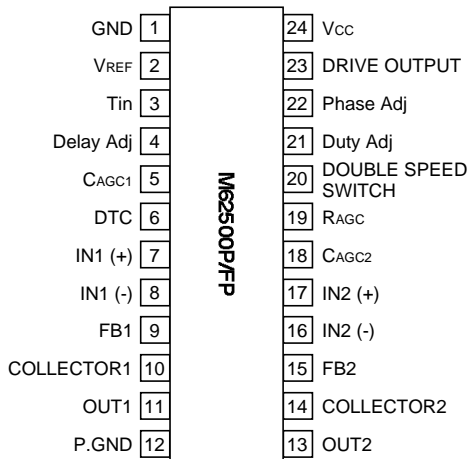
### DESCRIPTION

The M62500 is a semiconductor integrated circuit designed and developed as a deflection control of the CRT display monitor. The built-in trigger mode oscillator allows stable PWM control to be gained against a wide range of change of external signals. The M62500 provides a low supply voltage output malfunction preventive circuit (UVLO) and software start function optimum to horizontal output correction of monitor, high voltage drive and high voltage regulator.

### FEATURES

- PWM output in synchronization with external signals
- Wide range of PWM control frequency  
15kHz to 150kHz
- The PWM output phase is adjustable against external signals
- Soft start
- Built-in low voltage output malfunction prevention circuit  
Start  $V_{CC} > 9V$   
Stop  $V_{CC} < 6V$

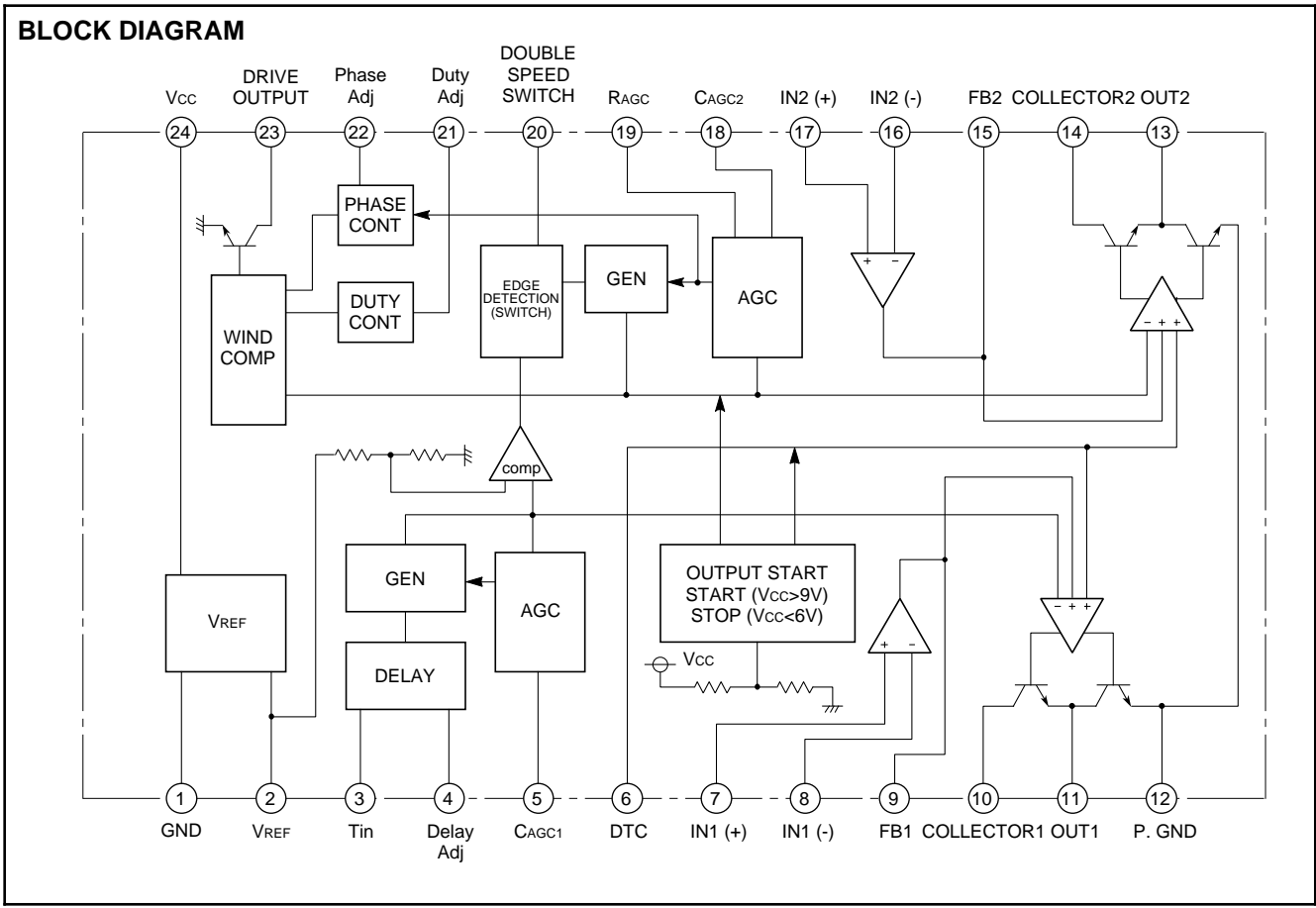
### PIN CONFIGURATION (TOP VIEW)



Outline 24P4D (P)  
24P2V-A (FP)

### APPLICATION

CRT display monitor



**SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC**

**ABSOLUTE MAXIMUM RATINGS** (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Ratings		Unit
V <sub>CC</sub>	Supply voltage	15		V
V <sub>OUT</sub>	Output voltage	15		V
I <sub>OUT</sub>	Output current	±150		mA
V <sub>d</sub>	Drive output voltage	15		V
I <sub>d</sub>	Drive output current	20		mA
V <sub>ICM</sub>	Common mode input voltage range of error amplifier	-0.3 to V <sub>CC</sub>		V
V <sub>ID</sub>	Common mode differential input voltage of error amplifier	V <sub>CC</sub>		V
P <sub>d</sub>	Power dissipation	P	FP	mW
		1400	1000	
K <sub>θ</sub>	Thermal derating	P	FP	mW/°C
		11.2	8	
T <sub>opr</sub>	Operating temperature	-20 to +75		°C
T <sub>stg</sub>	Storage temperature	-40 to +125		°C

Note. For the polarity of current, the direction in which current flows to the IC is specified positive (+), while the direction in which current flows out from the IC is specified to be negative (-).

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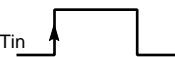
**ELECTRICAL CHARACTERISTICS** ( $V_{CC}=12V$ ,  $f_{IN}=40kHz$ ,  $T_a=25^{\circ}C$ , unless otherwise noted)

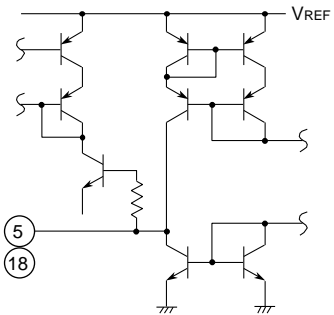
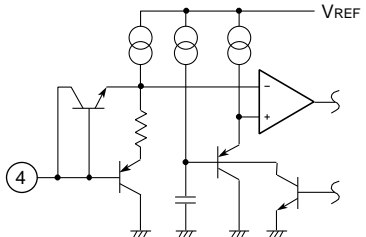
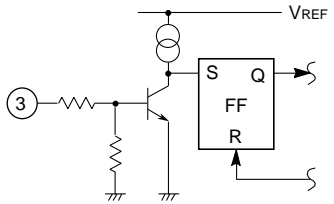
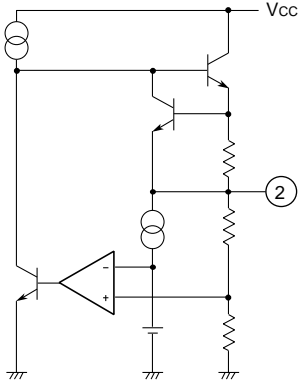
Block	Symbol	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
Supply voltage section	V <sub>CC</sub>	Range of power supply voltage		V <sub>CC off</sub>		14	V
	I <sub>CC</sub>	Dissipation current	Without signal	20	40	70	mA
	V <sub>CC ON</sub>	Activation start voltage		8	9	10	V
	V <sub>CC OFF</sub>	Activation stop voltage		5.4	6.0	6.6	V
Error amp. section	V <sub>IO</sub>	Input offset voltage				7	mV
	I <sub>IB</sub>	Input bias voltage		-100			nA
	I <sub>IO</sub>	Input offset current		-100		100	nA
	V <sub>ICM</sub>	Common mode input range		-0.3		V <sub>CC</sub> -2	V
	A <sub>V</sub>	Open loop gain		70	110		dB
	S <sub>R</sub>	Through rate			4		V/μs
	V <sub>OR</sub>	Output voltage range 1)		0.3		V <sub>REF</sub> -1.5	V
	I <sub>SINK</sub>	Output sink current		10			mA
	I <sub>SOURCE</sub>	Output source current				-10	mA
PWM output section	V <sub>SAT L</sub>	Output saturation voltage L	I <sub>O</sub> =100mA		0.7	1.4	V
	V <sub>SAT H</sub>	Output saturation voltage H	I <sub>O</sub> =-100mA	9.5	10.5		V
Std. voltage section	V <sub>REF</sub>	Reference voltage	I <sub>REF</sub> =-5mA	4.80	5.00	5.20	V
	R <sub>EG-IN</sub>	Input stability	V <sub>CC</sub> =7 to 14V I <sub>REF</sub> =-5mA		1	10	mV
	R <sub>EG-L</sub>	Load voltage	I <sub>REF</sub> =0 to -5mA		2	20	mV
	T <sub>CVREF</sub>	Temperature coefficient of reference voltage	T <sub>a</sub> =-20 to +75°C		0.01		%/°C
	I <sub>REF MAX</sub>	Maximum reference current			-40		mA
	I <sub>S</sub>	Short-circuit current			-70		mA
Delay adj section	I <sub>IN</sub>	Input current	V <sub>IN</sub> =5V	—	140	200	μA
	V <sub>IN L</sub>	"L" input voltage		—	—	0.6	V
	V <sub>IN H</sub>	"H" input voltage		2.0	—	—	V
	I <sub>DELAY</sub>	Input current		-0.6	-0.1	—	μA
	T <sub>D min</sub>	Minimum delay time	V <sub>Delay adj</sub> =0V	—	0.8	1	μs
	T <sub>D max</sub>	Maximum delay time	V <sub>Delay adj</sub> =3.0V	10	15	—	μs
PWM comp section	I <sub>DTC</sub>	Input current		—	0.5	2.0	μA
	V <sub>th U</sub>	Upper limit voltage of saw tooth wave		0.65V <sub>REF</sub>	0.7V <sub>REF</sub>	0.75V <sub>REF</sub>	V
	V <sub>th L</sub>	Lower limit voltage of saw tooth wave		0.28V <sub>REF</sub>	0.3V <sub>REF</sub>	0.32V <sub>REF</sub>	V
	T <sub>Duty</sub>	PWM output duty	V <sub>DTC</sub> =2.5V	45	50	55	%
Duty adj section	I <sub>Duty</sub>	Input current	V <sub>Duty adj</sub> =2.5V	-6.5	-1.3	—	μA
	Duty min	Minimum duty		—	10	20	%
	Duty max	Maximum duty		80	95	—	%
	Duty	Duty	V <sub>Duty adj</sub> =2.5V	45	50	55	%
	Phase adj section	I <sub>Phase</sub>	Input current	V <sub>Phase adj</sub> =2.5V	-3.5	-0.7	—
T <sub>2 min</sub>		Minimum leading time of drive output		—	0.7	1.6	μs
T <sub>2 max</sub>		Minimum leading time of drive output		9	9.4	—	μs
T <sub>2</sub>		Leading time of drive output	V <sub>Phase adj</sub> =1.0V	4.5	5.5	7.0	μs
Drive output section	V <sub>SAT D</sub>	Output saturation voltage	I <sub>d</sub> =10mA			0.4	V
	I <sub>LD</sub>	Output leak current	V <sub>DO</sub> =12V			1	μA
fh switch section	I <sub>fh</sub>	fh pin current	V <sub>fh</sub> =5V	—	330	430	μA
	V <sub>fh</sub>	fh switching voltage		0.4V <sub>REF</sub>	0.5V <sub>REF</sub>	0.6V <sub>REF</sub>	V

Note 1. Output must not be reversed with input of 0.

**SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC**

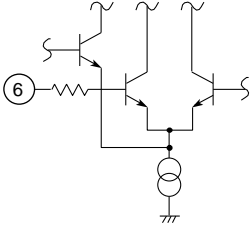
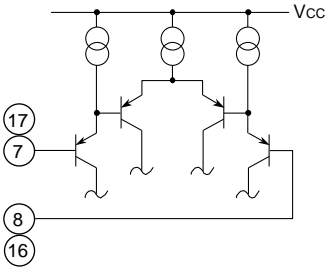
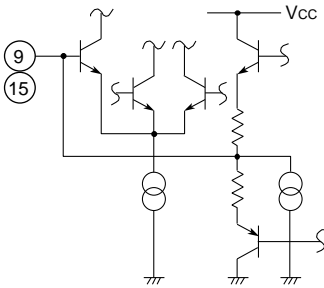
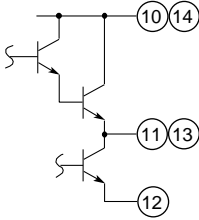
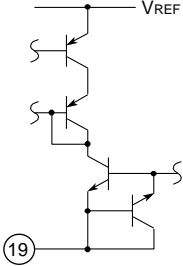
**EXPLANATION OF TERMINALS**

Pin No.	Symbol	Function and peripheral circuit of pins
①	GND	GND
②	VREF	5.0V reference voltage External load of about 5mA can be taken out.
③	Tin	Trigger input Read at the rising edge 
④	Delay Adj	Delay adjustment Delay of read trigger signal V <sub>Delay</sub> : 0 to 3.0V T <sub>Delay</sub> : 1μ to 10μsec
⑤ ⑱	CAGC1 CAGC2	AGC capacitance Connects capacitance between each pin and GND and sets up AGC sensitivity



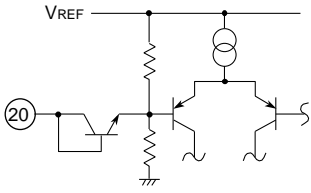
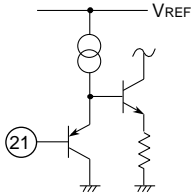
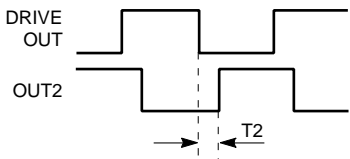
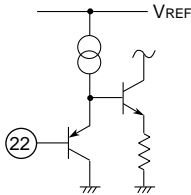
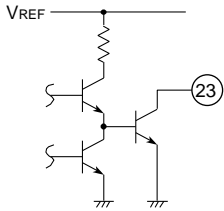
**SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC**

**EXPLANATION OF TERMINALS (Cont.)**

Pin No.	Symbol	Function and peripheral circuit of pins
⑥	DTC	Dead time control (PWM comparator ⊕ pin) 
⑦ ⑧ ⑬ ⑭	IN1 (+) IN1 (-) IN2 (-) IN2 (+)	Air amplifier input pin 
⑨ ⑮	FB1 FB2	Air amplifier output (PWM comparator ⊕ input pin) 
⑩ ⑪ ⑫ ⑬ ⑭	COLLECTOR1 OUT1 P.GND OUT2 COLLECTOR2	PWM output section 
⑲	RAGC	AGC current setup Connects resistance between pin ⑲ and GND and sets up AGC current on the OUT2 side. 

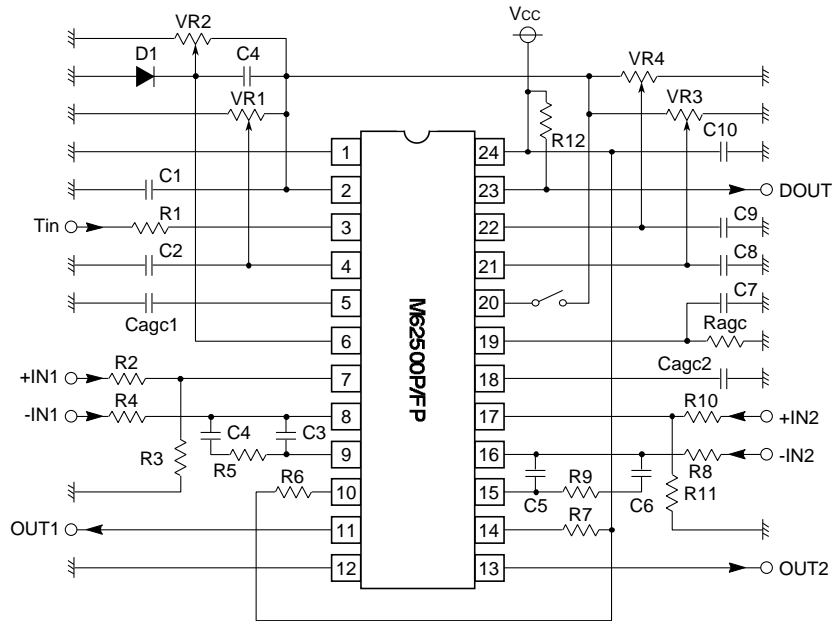
**SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC**

**EXPLANATION OF TERMINALS (Cont.)**

Pin No.	Symbol	Function and peripheral circuit of pins
⑳	fh/2fh	<p>Double speed switch                      Switches frequency of OUT2                      and drive output to the double frequency.                      OPEN, GND → fh                      VREF → 2fh</p> 
㉑	Duty Adj	<p>Duty adjustment of drive output</p> 
㉒	Phase Adj	<p>Phase adjustment of drive output against OUT2 (T2)</p>  
㉓	DRIVE OUTPUT	<p>Open collector output</p> 
㉔	Vcc	<p>Supply terminal</p>

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

APPLICATION EXAMPLE



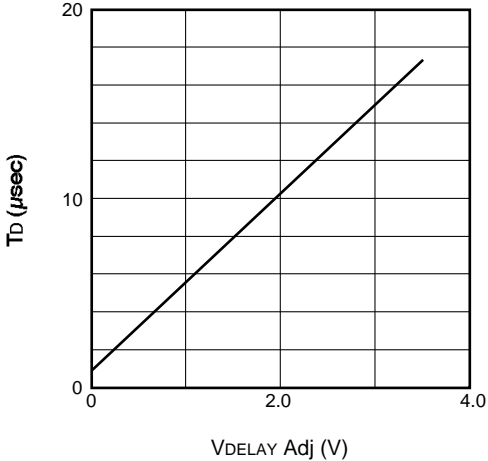
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|--|--|
| <p>C1, C10 : Is required for stabilization of Vcc and VREF. Is normally set to tens of <math>\mu\text{F}</math> to hundreds of <math>\mu\text{F}</math>.</p> <p>VR 1, 2, 3, 4 : Is determined taking into account the load capability of VREF. (External load capability of approx. 5mA) Shall be normally set to approx. 10k .</p> <p>C2, C8, C9 : Is added to high impedance pin of voltage control for improvement in noise margin. Depends on the device installation environment. Shall be normally set to approx. 0.1<math>\mu\text{F}</math>.</p> <p>C4, D1 : Is added for the execution of software start. Set a time constant, taking into account the set value of VR2.</p> <p>R1 : Is added to reduce interference by Tin and outputs. With VIN=approx. 2.5V to 5V, the resistance value of approx. 22k is recommended.</p> <p>Cagc 1, 2 : Capacitance necessary for stabilization of AGC. As the capacitance is larger, the stability is larger, but the characteristic of answering becomes worse. The capacitance value of 1<math>\mu\text{F}</math> is recommended.</p> | <p>R2, R3, R10, R11 : A gain setup constant of error Amp. To assure the stability of feedback, R4 and R8 shall be set to several k to tens of k to set the gain to approx. 20dB to 40dB with f=1 kHz. If the gain is too low, jitter may take place. It is therefore recommended to set C3 and C5 to tens of pF to hundreds of pF, C4 and C6 to thousands of pF to tens of thousands of pF, and R5 and R9 to tens of k to hundreds of k .</p> <p>R4, R5, R8, R9 : Shall be set to several k to tens of k to set the gain to approx. 20dB to 40dB with f=1 kHz. If the gain is too low, jitter may take place. It is therefore recommended to set C3 and C5 to tens of pF to hundreds of pF, C4 and C6 to thousands of pF to tens of thousands of pF, and R5 and R9 to tens of k to hundreds of k .</p> <p>C3, C4, C5, C6 : Shall be set to several k to tens of k to set the gain to approx. 20dB to 40dB with f=1 kHz. If the gain is too low, jitter may take place. It is therefore recommended to set C3 and C5 to tens of pF to hundreds of pF, C4 and C6 to thousands of pF to tens of thousands of pF, and R5 and R9 to tens of k to hundreds of k .</p> <p>Ragc : Resistance for setting AGC on the OUT2 side. Is set with Ragc=27k .</p> <p>C7 : If f to be input into Tin suddenly changes, addition of C7 shortens non-control time of Dout (output of "H"). As a capacitance value, it is recommended to adopt 2.2<math>\mu\text{F}</math>. In the case of adding C7, however, Cagc2 0.68<math>\mu\text{F}</math> is recommended.</p> <p>R6, R7 : Current limit resistance of OUT1/2. Is normally set to several . Insertion of direct limit resistance into OUT1/2 pin is also effective.</p> <p>R12 : Pull-up resistance of DOUT output. DOUT is an open collector output and requires R12. Is normally set to several k .</p> |
|--|--|

\* Note: To reduce interference in the signal system, pins ① GND and ⑫ P.GND shall be grounded at a point in the power supply block.

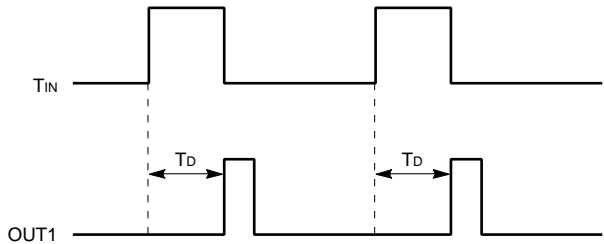
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SETUP OF VOLTAGE CONTROL BLOCK

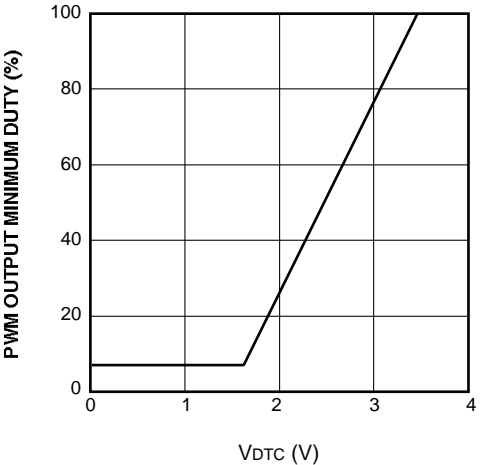
T<sub>D</sub> vs. V<sub>DELAY Adj</sub> CHARACTERISTICS (f=40kHz)



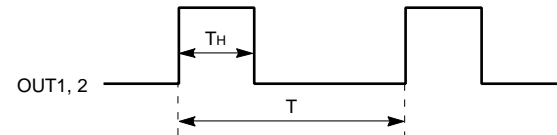
Applying a voltage to the DELAY Adj pin can control the delay time of OUT1 to T<sub>IN</sub>.



PWM OUTPUT MINIMUM DUTY vs. V<sub>DTC</sub> CHARACTERISTICS (f=40kHz)



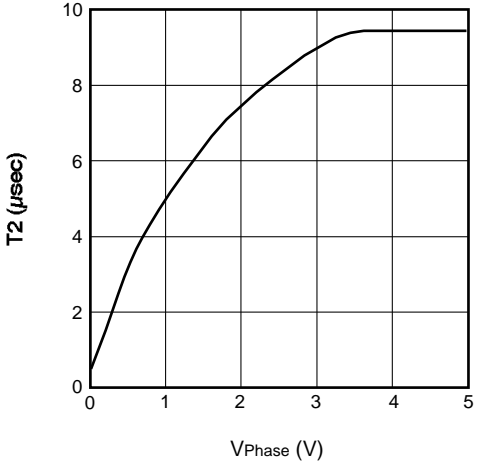
Applying a voltage to the DTC pin can control the dead time of PWM output.



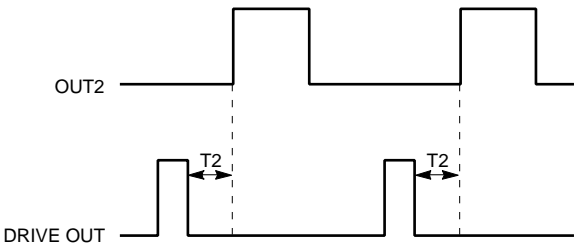
PWM output minimum duty

$$T_{DUTY} = \frac{T_H}{T} \times 100 (\%)$$

T<sub>2</sub> vs. V<sub>Phase</sub> CHARACTERISTICS (f=40kHz)



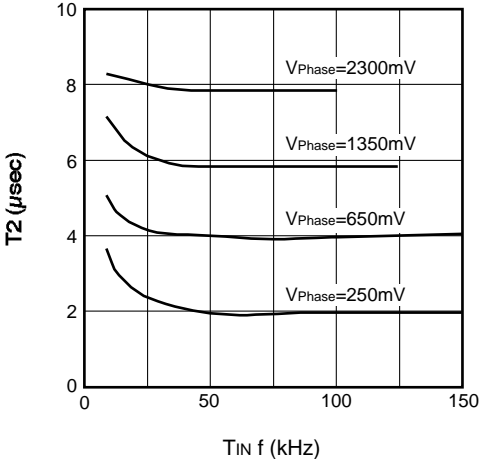
Applying a voltage to the Phase Adj pin can control a leading time of drive output to OUT2.



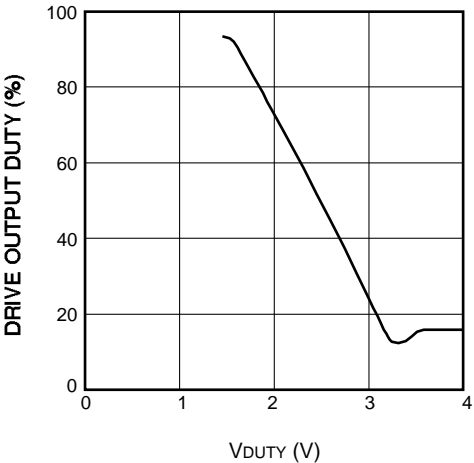


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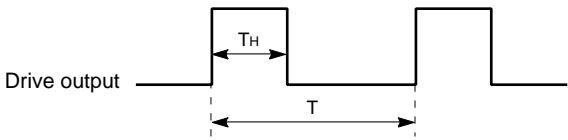
T2 vs. f CHARACTERISTICS



DRIVE OUTPUT DUTY vs. VDUTY CHARACTERISTICS (f=40kHz)



Applying a voltage to the DUTY Adj pin can control drive output duty.

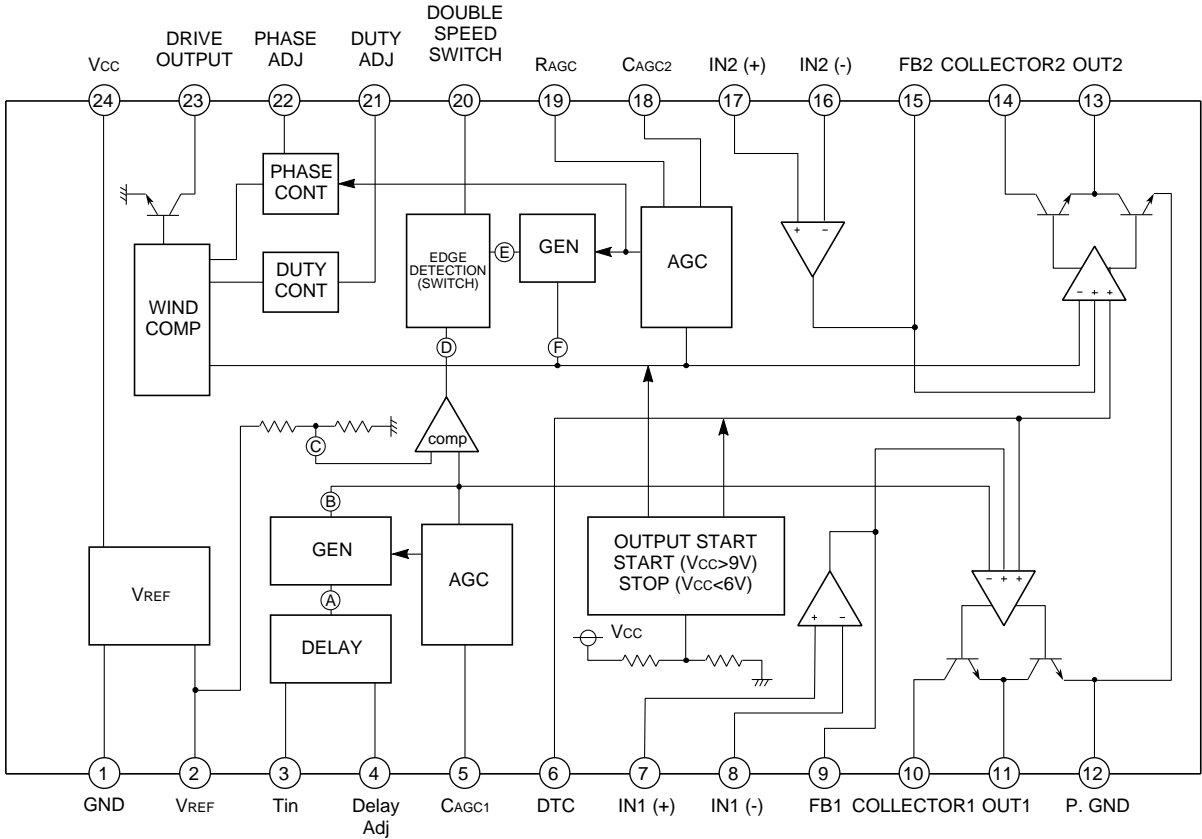


Drive output duty

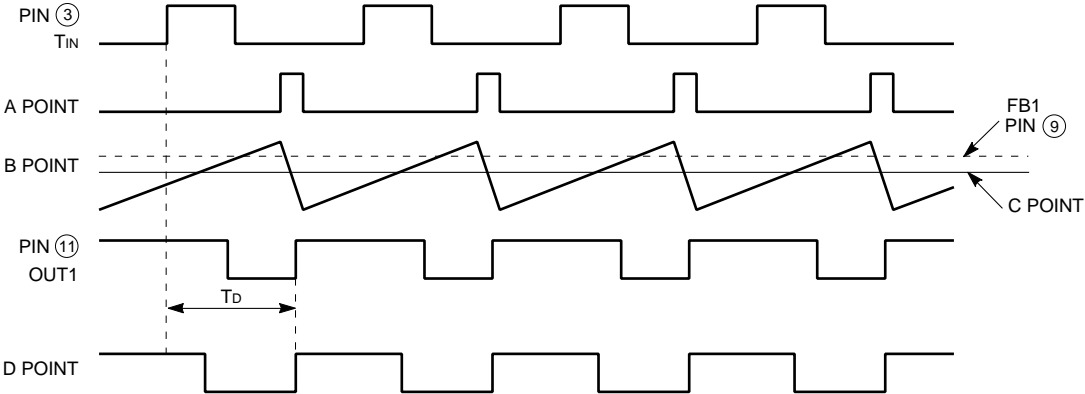
$$T_{DUTY} = \frac{T_H}{T} \times 100 (\%)$$

SYNCHRONIZATION DEFLECTION SYSTEM CONTROL PWM IC

TIME CHART

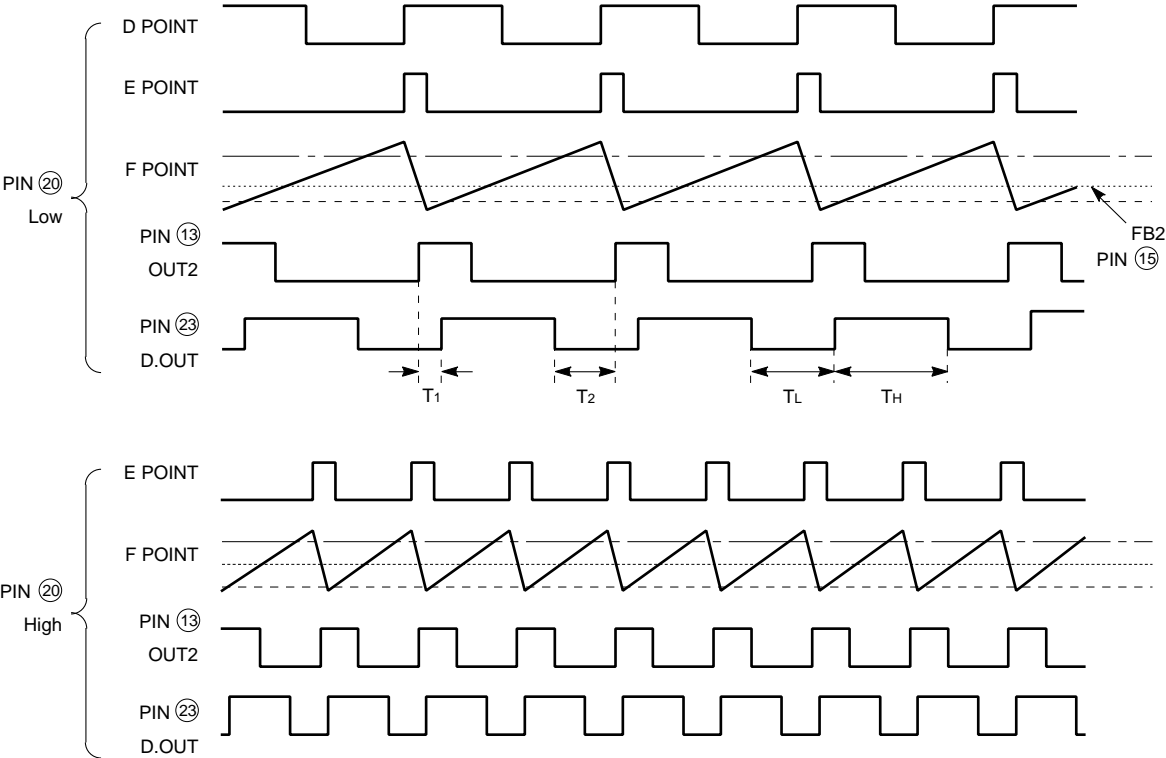


PIN WAVE



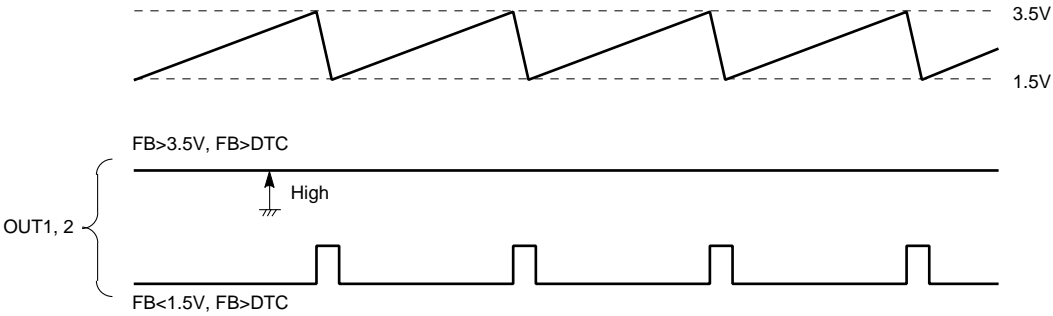
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PIN WAVE (Cont.)



PWM OUT NON-CONTROL STATUS

With trigger input at pin 3



Without trigger at pin 3 (in case of GND)

