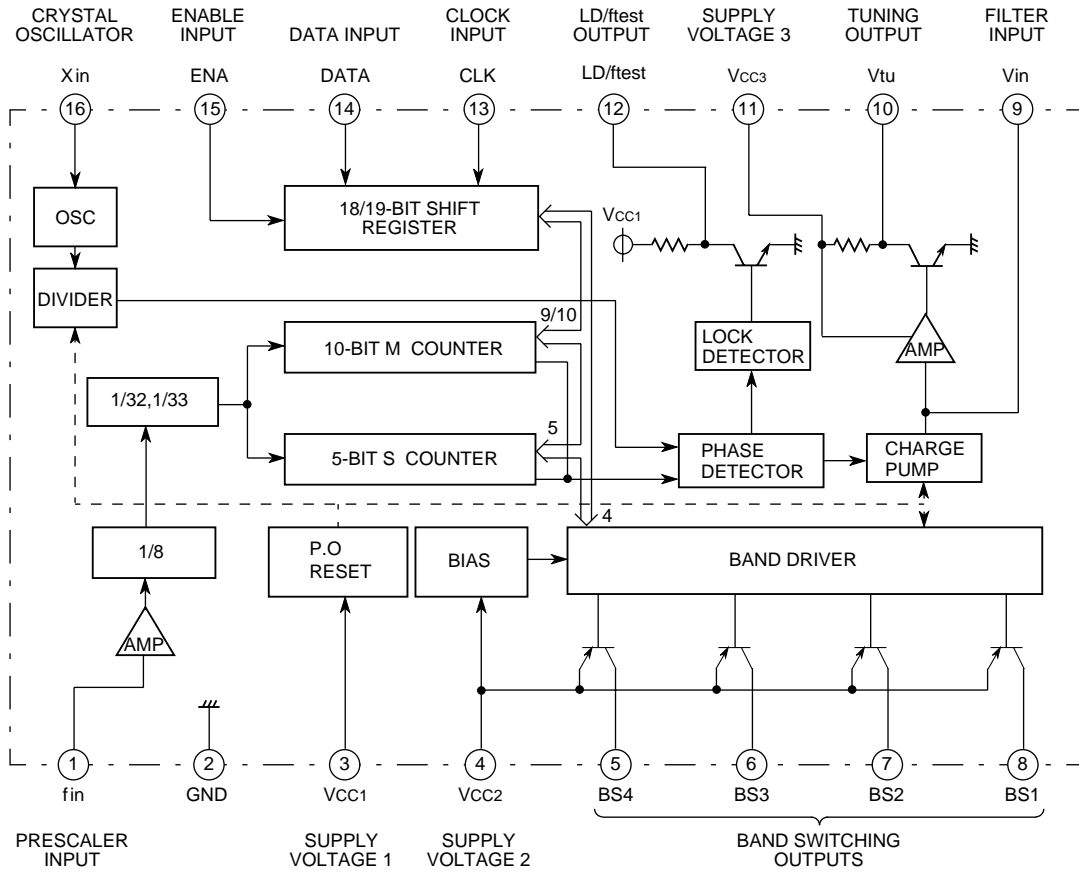




# M64892AFP/GP

## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### BLOCK DIAGRAM



**M64892AFP/GP**

**SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR**

**DESCRIPTION OF PIN**

Pin No.	Symbol	Pin name	Function
1	fin	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0V.
3	Vcc1	Power supply voltage 1	Power supply voltage terminal. 5.0V±0.5V
4	Vcc2	Power supply voltage 2	Power supply for band switching, Vcc1 to 13.2V
5	BS4	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
6	BS3		
7	BS2		
8	BS1		
9	Vin	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f1/N) is ahead compared to the reference frequency (fref), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
10	Vtu	Tuning output	This supplies the tuning voltage.
11	Vcc3	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35V
12	LD/ftest	Lock detect/Test port	When 18/19 bit data is input, lock detector is output. When 27 bit data is input, lock detector is output, the programmable freq. Divider output and reference freq. Output is selected by the test mode.
13	CLK	Clock input	Data is read into the shift register when the clock signal falls.
14	DATA	Data input	Input for band SW and programmable freq. divider set up.
15	ENA	Enable input	This is normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the enable signal after the 18th signal of the clock signal falls or when the 19th pulse of the clock signal falls.
16	Xin	This is connected to the crystal oscillator	4.0MHz crystal oscillator is connected.

**ABSOLUTE MAXIMUM RATINGS** (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
VCC1	Supply voltage 1	Pin3	6.0	V
VCC2	Supply voltage 2	Pin4	14.4	V
VCC3	Supply voltage 3	Pin11	36.0	V
Vi	Input voltage	Not to exceed Vcc1	6.0	V
Vo	Output voltage	LD output	6.0	V
VBSOFF	Voltage applied when the band output is OFF		14.4	V
IBSON	Band output current	Per 1 band output circuit	50.0	mA
tBSON	ON the time when the band output is ON	50mA per 1 band output circuit 3circuits are pn at same time	10	sec
Pd	Power dissipation	Ta=+75°C (SOP/SSOP)	FP: 450 (GP: 470)	mW
Topr	Operating temperature		-20 to +75	°C
Tstg	Storage temperature		-40 to +125	°C

**RECOMMENDED OPERATING CONDITIONS** (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
VCC1	Supply voltage 1		4.5 to 5.5	V
VCC2	Supply voltage 2		Vcc1 to 13.2	V
VCC3	Supply voltage 3		28 to 35	V
fopr1	Operating frequency (1)	Crystal oscillation circuit	4.0	MHz
fopr2	Operating frequency (2)		80 to 1,000	MHz
IBDL	Band output current 5 to 8	Normally 1 circuit is ON. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0 to 40	mA

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**ELECTRICAL CHARACTERISTICS** (Ta=-20°C to +75°C, Vcc1=5.0V, Vcc2=12V, Vcc3=33V, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V <sub>IH</sub>	Input pin	"H" input voltage	13 to 15		3.0	-	V <sub>CC1</sub> +0.3	V
V <sub>IL</sub>		"L" input voltage	13 to 15		-	-	1.5	V
I <sub>IH</sub>		"H" input current	13 to 15	V <sub>CC1</sub> =5.5V, V <sub>i</sub> =4.0V	-	-	10	μA
I <sub>IL</sub>		"L" input current	13, 15	V <sub>CC1</sub> =5.5V, V <sub>i</sub> =0.4V	-	-6	-20	μA
		"L" input current	14	V <sub>CC1</sub> =5.5V, V <sub>i</sub> =0.4V	-	-18	-30	μA
V <sub>OH</sub>	Lock output	"H" output voltage	12	V <sub>CC1</sub> =5.5V	5.0	-	-	V
V <sub>OL</sub>		"L" output voltage	12	V <sub>CC1</sub> =5.5V	-	0.3	0.5	V
V <sub>BS</sub>	Band SW	Output voltage	5 to 8	V <sub>CC2</sub> =12V, I <sub>o</sub> =-40mA	11.6	11.8	-	V
I <sub>OLK1</sub>		Leak current	5 to 8	V <sub>CC2</sub> =12V band SW is OFF	-	-	-10	μA
V <sub>TOH</sub>	Tuning output	Output voltage "H"	10	V <sub>CC3</sub> =33V	32.5	-	-	V
V <sub>TOL</sub>		Output voltage "L"	10	V <sub>CC3</sub> =33V	-	0.2	0.4	V
I <sub>OH</sub>	Charge pump	"H" output current	9	V <sub>CC1</sub> =5.0V, V <sub>o</sub> =2.5V	-	±270	±370	μA
I <sub>OL</sub>		"L" output current	9	V <sub>CC1</sub> =5.0V, V <sub>o</sub> =2.5V	-	±70	±110	μA
I <sub>CPLK</sub>		Leak current	9	V <sub>CC1</sub> =5.0V, V <sub>o</sub> =2.5V	-	-	±50	nA
I <sub>CC1</sub>	Supply current 1		3	V <sub>CC1</sub> =5.5V	-	20	30	mA
I <sub>CC2A</sub>	Supply current 2	4 circuits: OFF	4	V <sub>CC2</sub> =12V	-	-	0.3	mA
I <sub>CC2B</sub>		1 circuits: ON, Output: OPEN	4	V <sub>CC2</sub> =12V	-	6.0	8.0	mA
I <sub>CC2C</sub>		1 circuits: ON, Output current 40mA	4	V <sub>CC2</sub> =12V I <sub>o</sub> =-40mA	-	46.0	48.0	mA
I <sub>CC3</sub>	Supply current 3		11	V <sub>CC3</sub> =33V Output ON	-	3.0	4.0	mA

Note. Typical values are measured at V<sub>CC1</sub>=5.0V, V<sub>CC2</sub>=12V, V<sub>CC3</sub>=33V and Ta=+25°C.

**SWITCHING CHARACTERISTICS** (Ta=-20°C to +75°C, Vcc1=5.0V, Vcc2=12V, Vcc3=33V, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit	
					Min.	Typ.	Max.		
f <sub>opr</sub>	Prescaler operating frequency		1	V <sub>CC1</sub> =4.5 to 5.5V V <sub>in</sub> =V <sub>inmin</sub> to V <sub>inmax</sub>	80	-	1000	MHz	
V <sub>in</sub>	Operating input voltage		1	V <sub>CC1</sub> =4.5 to 5.5V	80 to 100MHz	-24	-	4	dBm
			100 to 200MHz		-27	-	4		
			200 to 800MHz		-30	-	4		
			800 to 1000MHz		-27	-	4		
t <sub>PWC</sub>	Clock pulse width		13	V <sub>CC1</sub> =4.5 to 5.5V	1	-	-	μs	
t <sub>SU (D)</sub>	Data setup time		14	V <sub>CC1</sub> =4.5 to 5.5V	2	-	-	μs	
t <sub>H (D)</sub>	Data hold time		14	V <sub>CC1</sub> =4.5 to 5.5V	1	-	-	μs	
t <sub>SU (E)</sub>	Enable setup time		15	V <sub>CC1</sub> =4.5 to 5.5V	3	-	-	μs	
t <sub>H (E)</sub>	Enable hold time		15	V <sub>CC1</sub> =4.5 to 5.5V	3	-	-	μs	
t <sub>INT</sub>	Enable data interval time		15, 14	V <sub>CC1</sub> =4.5 to 5.5V	1	-	-	μs	
t <sub>r</sub>	Rise time		13, 14, 15	V <sub>CC1</sub> =4.5 to 5.5V	-	-	1	μs	
t <sub>f</sub>	Fall time		13, 14, 15	V <sub>CC1</sub> =4.5 to 5.5V	-	-	1	μs	
t <sub>bt</sub>	Next enable prohibit time		15	V <sub>CC1</sub> =4.5 to 5.5V	5	-	-	μs	
t <sub>bcl</sub>	Next clock prohibit time		13, 15	V <sub>CC1</sub> =4.5 to 5.5V	5	-	-	μs	

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## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### METHOD OF SETTING DATA

The frequency demultiplying ratio uses 15bits. Setting up the band switching output uses 4bits.

The test mode data uses 8bits. The total bits used is 27bits. Data is read in when the enable signal is "H" and the clock signal falls.

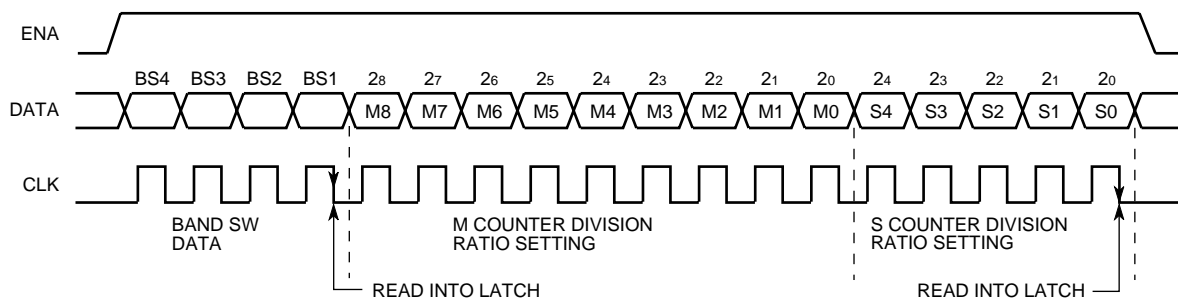
The band switching data is read in at the 4th pulse of the clock signal. The program counter data is read into the latch by the fall of the enable signal after the 18th pulse of the clock signal or the fall of

the 19th pulse of the clock signal. When the enable signal goes to "L" before the 18th pulse of the enable signal, only the band SW data is updated and other data is ignored.

The shift register is equipped with the 18/19 bit automatic decision function. When the 18th bit data is used, the M9 bit of the program counter is reset and the 1/512 division of the reference frequency is set. In case of the 19th bit, 1/1024 division of the reference frequency is set.

#### (1) Transfer of the 18th bit data

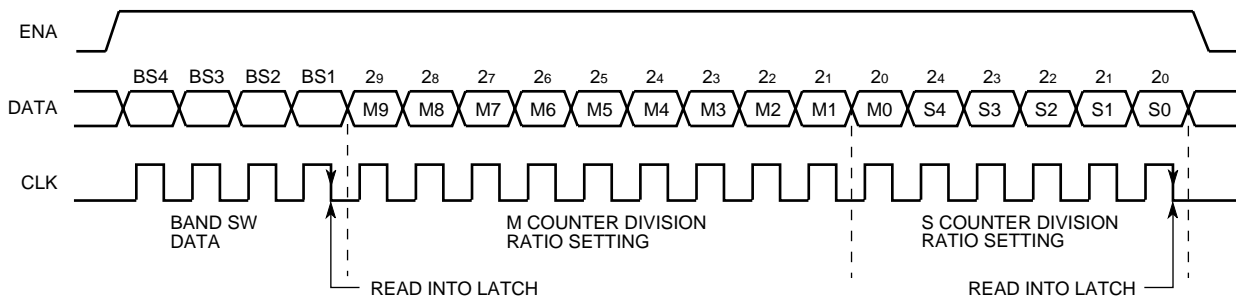
Data is latched by the fall of the enable signal after the 18th clock signal. At this time, the division of the 1/512 of the reference frequency is used.



#### (2) Transfer of the 19th bit data

The data is latched at the 19th pulse of the clock signal. At this time, 1/1024 frequency division ratio is used. Clock signals after the above are invalid.

Notice) To change reference frequency, set up as ENA in "L" after 19th pulse of clock signal by all means



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**METHOD OF SET THE DIVIDING RATIO OF THE PROGRAMMABLE DIVIDER**

(1) Transfer of the 18th bit data

Total division N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N=8 (32M+S) \quad \begin{array}{l} \text{M:9 bit main counter division} \\ \text{S:5 bit swallow counter division} \end{array}$$

The M and S counters are binary the possible ranges of division are as follows.

$$32 \leq M \leq 511$$

$$0 \leq S \leq 31$$

Therefore, the range of division N is 8,192 to 131,064.

The tuning frequency  $f_{VCO}$  is given in the following equations.

$$\begin{aligned} f_{VCO} &= f_{REF} \times N \\ &= 7.8125 \times 8 \times (32M+S) \\ &= 62.5 \times (32M+S) \quad [\text{kHz}] \end{aligned}$$

Therefore, the tuning frequency range is 64MHz to 1023.9375MHz.

(2) Transfer of the 19th bit data

Total division N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N=8 (32M+S) \quad \begin{array}{l} \text{M:10 bit main counter division} \\ \text{S:5 bit swallow counter division} \end{array}$$

The M and S counters are binary the possible ranges of division are as follows.

$$32 \leq M \leq 1023$$

$$0 \leq S \leq 31$$

Therefore, the range of division N is 8,192 to 262,136.

The tuning frequency  $f_{VCO}$  is given in the following equations.

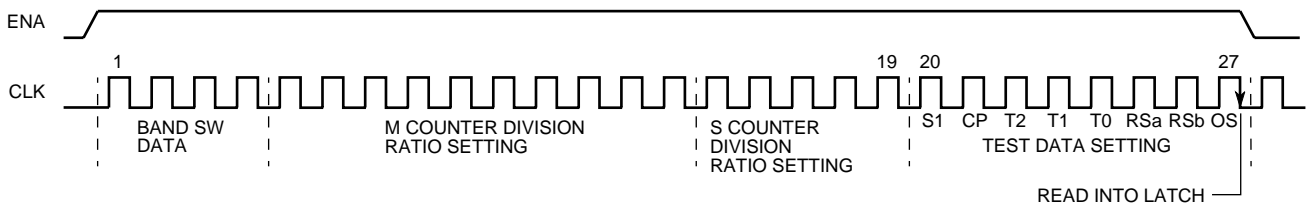
$$\begin{aligned} f_{VCO} &= f_{REF} \times N \\ &= 3.90625 \times 8 \times (32M+S) \\ &= 31.25 \times (32M+S) \quad [\text{kHz}] \end{aligned}$$

Therefore, the tuning frequency range is 32MHz to 1023,9687MHz.

**TEST MODE DATA SET UP METHOD**

The data for the test mode uses 20 to 27bits. Data is latched when the 27th clock signal falls.

(1) When transferring 3-wire 27bit data



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## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

(2) Test mode bit set up

- X : Random, 0 or 1. normal "0"
- CP : Set up the charge pump current value
- T0, T1, and T2 : Set up test modes
- RSa, RSb : Set up for the reference frequency division ratio
- OS : Set up the tuning amplifier
- SI : 1 only (It is prohibit to "0")

**Setting up the charge pump current of the phase comparator**

CP	Charge pump current	Mode
0	70 $\mu$ A	Test
1	270 $\mu$ A	Normal

**Setting up for the test mode**

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	f <sub>REF</sub>	Test mode
1	0	1	High impedance	f <sub>1/N</sub>	Test mode

\* Built-in pull up resistor, and the resistor is unnecessary.

**Set up for the reference frequency division ratio**

RSa	RSb	Frequency ratio
1	1	1/512
0	1	1/1024
X	0	1/640

**Set up the tuning amplifier**

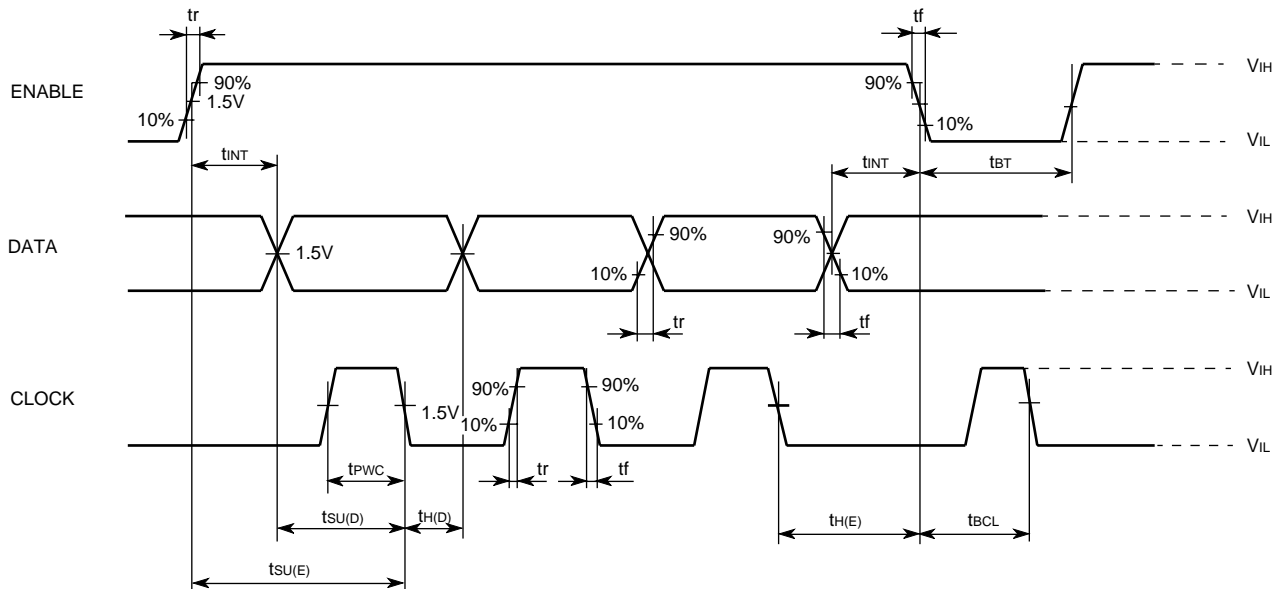
OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

**POWER ON RESET OPERATION**

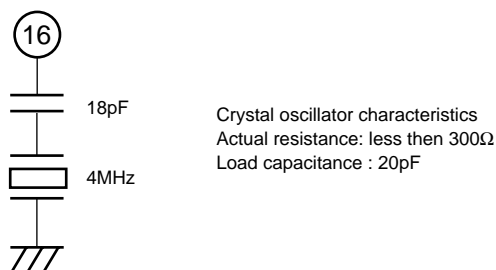
(Initial state the power is turned ON)

- BS4 to BS1 : OFF
- Charge pump : High impedance
- Tuning amplifier : OFF
- Charge pump current : 270 $\mu$ A
- Frequency division ratio : 1/1024
- Lock detect : "H"

**TIMING DIAGRAM**



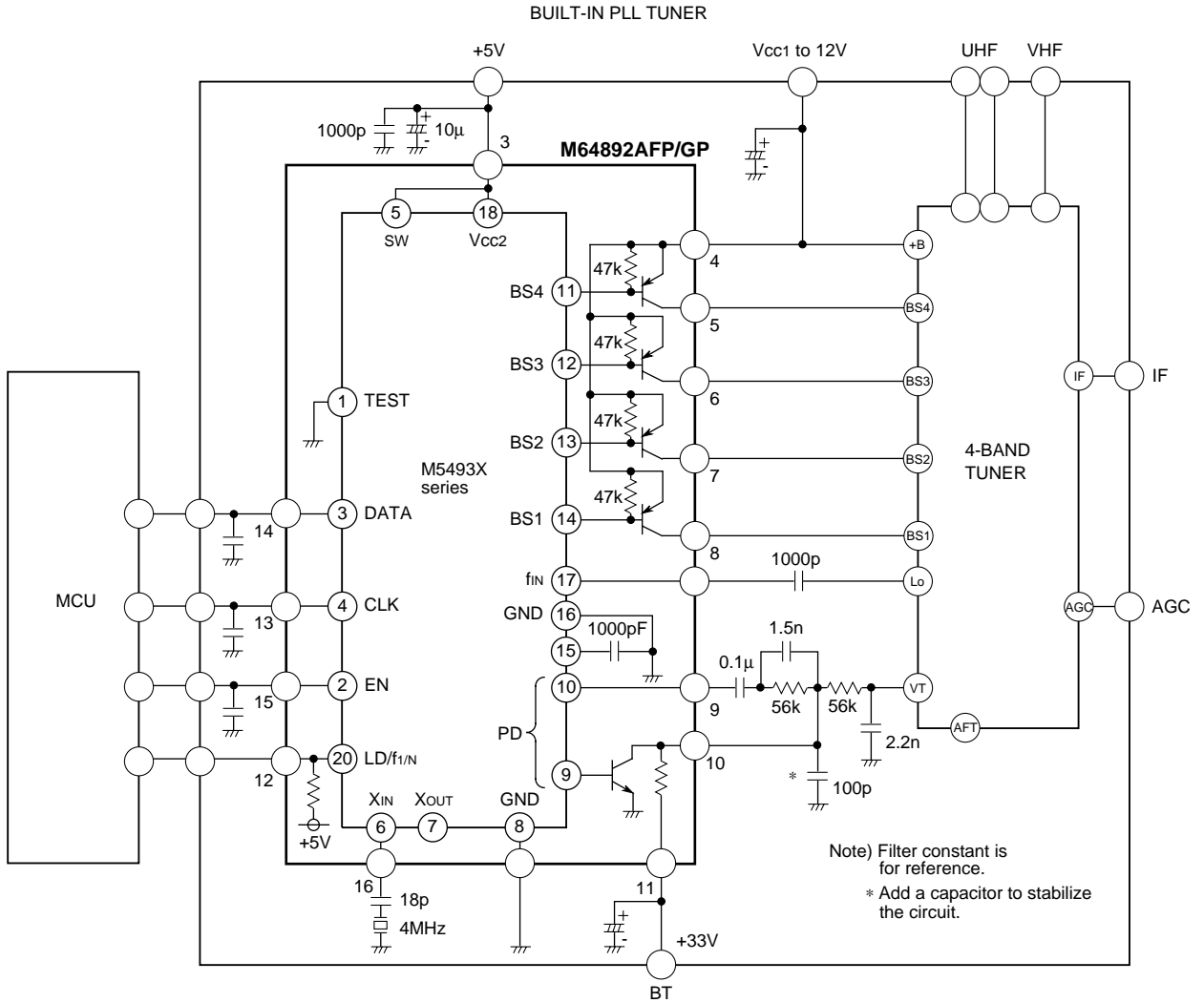
**CRYSTAL OSCILLATOR CONNECTION DIAGRAM**



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## SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

### APPLICATION EXAMPLE



Units Resistance :  $\Omega$   
Capacitance : F