

Features

- Operating Voltage: 3.3V
- Access Time: 40 ns
- Very Low Power Consumption
 - Active: 180 mW (Max)
 - Standby: 70 μ W (Typ)
- Wide Temperature Range: -55°C to +125°C
- 400 Mils Width Package
- TTL Compatible Inputs and Outputs
- Asynchronous
- Designed on 0.35 Micron Process
- Latch-up Immune
- 200 Krads capability
- SEU LET Better Than 3 MeV

Description

The M65609E is a very low power CMOS static RAM organized as 131,072 x 8 bits.

Atmel brings the solution to applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments, or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the M65609E combines an extremely low standby supply current (Typical value = 20 μ A) with a fast access time at 40 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The M65609E is processed according to the methods of the latest revision of the MIL STD 883 (class B or S), ESA SCC 9000 or QML.

It is produced on the same process as the MH1RT sea of gates series.



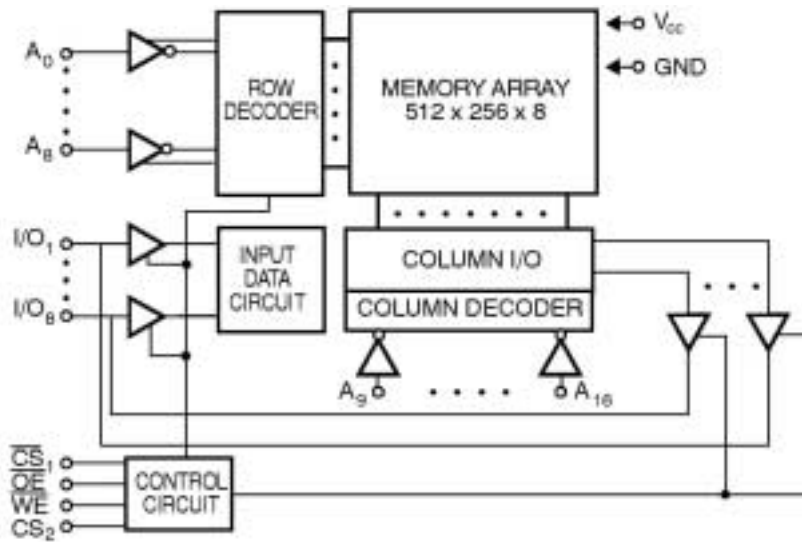
Rad. Hard
128K x 8
3.3-volt
Very Low Power
CMOS SRAM

M65609E

Rev. 4158D-AERO-06/02



Block Diagram



Pin Configuration

32 pins Flatpack 400 MILS



Pin Description

Table 1. Pin Names

Name	Description
A0 - A16	Address Inputs
I/O1 - I/O8	Data Input/Output
\overline{CS}_1	Chip Select 1
CS_2	Chip Select 2
\overline{WE}	Write Enable
OE	Output Enable
V_{CC}	Power
GND	Ground

Table 2. Truth Table

\overline{CS}_1	CS_2	\overline{WE}	\overline{OE}	Inputs/ Outputs	Mode
H	X	X	X	Z	Deselect/ Power-down
X	L	X	X	Z	Deselect/ Power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

Note: L = low, H = high, X = H or L, Z = high impedance.



Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage to GND Potential.....	-0.5V + 5V
DC Input Voltage.....	GND - 0.3V to $V_{CC} + 0.3$
DC Output Voltage High Z State	GND - 0.3V to $V_{CC} + 0.3$
Storage Temperature	-65°C to + 150°C
Output Current Into Outputs (Low)	20 mA
Electro Statics Discharge Voltage.....	> 2001V (MIL STD 883D Method 3015.3)

*NOTE:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Military Operating Range

Operating Voltage	Operating Temperature
3.3V ± 0.3V	-55°C to + 125°C

Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
Gnd	Ground	0.0	0.0	0.0	V
V_{IL}	Input low voltage	GND - 0.3	0.0	0.8	V
V_{IH}	Input high voltage	2.2	–	$V_{CC} + 0.3$	V

Capacitance

Parameter	Description	Min	Typ	Max	Unit
$C_{IN}^{(1)}$	Input low voltage	–	–	8	pF
$C_{OUT}^{(1)}$	Output high voltage	–	–	8	pF

Note: 1. Guaranteed but not tested.

DC Parameters

DC Test Conditions

Parameter	Description	Minimum	Typical	Maximum	Unit
IIX ⁽¹⁾	Input leakage current	-1	–	1	μA
IOZ ⁽¹⁾	Output leakage current	-1	–	1	μA
VOL ⁽²⁾	Output low voltage	-	–	0.4	V
VOH ⁽³⁾	Output high voltage	2.4	–	–	V

1. Gnd < Vin < V_{CC}, Gnd < Vout < V_{CC} Output Disabled.
2. V_{CC} min. IOL = 1 mA.
3. V_{CC} min. IOH = -0.5 mA.

Consumption

Symbol	Description	65609E-40	Unit	Value
ICCSB ⁽¹⁾	Standby supply current	2.5	mA	max
ICCSB ₁ ⁽²⁾	Standby supply current	1.5	mA	max
ICCOP ⁽³⁾	Dynamic operating current	50	mA	max

1. $\overline{CS}_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$ and $\overline{CS}_1 \leq V_{IL}$.
2. $CS_1 \geq V_{CC} - 0.3V$ or, $CS_2 < Gnd + 0.3V$ and $\overline{CS}_1 \leq 0.2V$
3. $F = 1/T_{AVAV}$, I_{OUT} = 0 mA, $\overline{W} = \overline{OE} = V_{IH}$, Vin = Gnd or V_{CC}, V_{CC} max.

Write Cycle

Symbol	Parameter	65609E-40	Unit	Value
t_{AVAW}	Write cycle time	35	ns	min
t_{AVWL}	Address set-up time	0	ns	min
t_{AVWH}	Address valid to end of write	28	ns	min
t_{DVWH}	Data set-up time	28	ns	min
t_{E1LWH}	\overline{CS}_1 low to write end	28	ns	min
t_{E2HWH}	CS_2 high to write end	28	ns	min
t_{WLQZ}	Write low to high Z ⁽¹⁾	15	ns	max
t_{WLWH}	Write pulse width	28	ns	min
t_{WHAX}	Address hold from to end of write	+3	ns	min
t_{WHDX}	Data hold time	0	ns	min
t_{WHQX}	Write high to low Z ⁽¹⁾	0	ns	min

Note: 1. Parameters guaranteed, not tested, with 5 pF output loading (see Section “AC Test Conditions” Figure 2).

Read Cycle

Symbol	Parameter	65609E-40	Unit	Value
t_{AVAV}	Read cycle time	40	ns	min
t_{AVQV}	Address access time	40	ns	max
t_{AVQX}	Address valid to low Z	3	ns	min
t_{E1LQV}	Chip-select ₁ access time	40	ns	max
t_{E1LQX}	\overline{CS}_1 low to low Z ⁽¹⁾	3	ns	min
t_{E1HQZ}	\overline{CS}_1 high to high Z ⁽¹⁾	15	ns	max
t_{E2HQV}	Chip-select ₂ access time	40	ns	max
t_{E2HQX}	CS_2 high to low Z ⁽¹⁾	3	ns	min
t_{E2LQZ}	CS_2 low to high Z ⁽¹⁾	15	ns	max
t_{GLQV}	Output Enable access time	12	ns	max
t_{GLQX}	\overline{OE} low to low Z ⁽¹⁾	0	ns	min
t_{GHQZ}	\overline{OE} high to high Z ⁽¹⁾	10	ns	max

Note: 1. Parameters guaranteed, not tested, with 5 pF output loading (see Section “AC Test Conditions” Figure 2).

AC Parameters

AC Test Conditions

Input Pulse Levels: GND to 3.0V
 Input Rise/Fall Times: 5 ns
 Input Timing Reference Levels: 1.5V
 Output loading IOL/IOH (see figure 1 and 2)..... +30 pF

AC Test Loads Waveforms

Figure 1

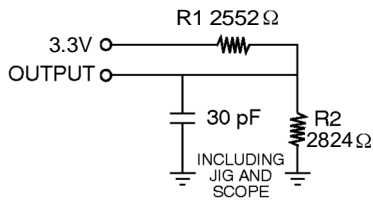


Figure 2

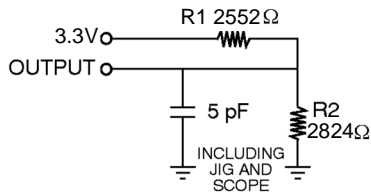
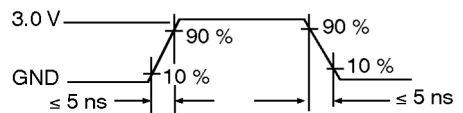
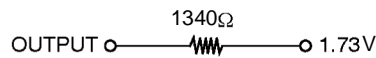


Figure 3



Equivalent to : THEVENIN EQUIVALENT

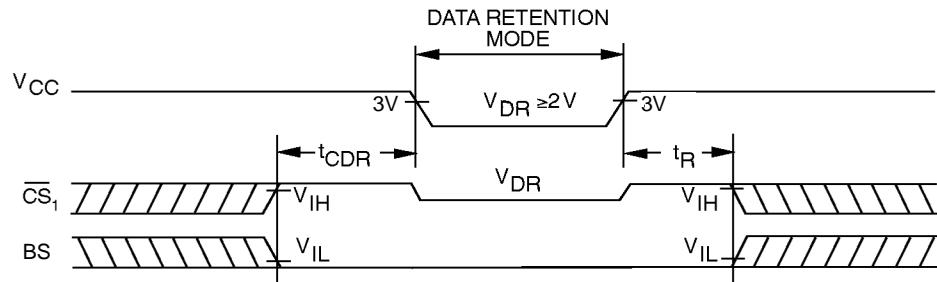


Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention \overline{CS} must be held high within V_{CC} to $V_{CC} - 0.2V$ or chip select BS must be held down within GND to GND +0.2V.
2. Output Enable (\overline{OE}) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions \overline{CS} and \overline{OE} must be kept between $V_{CC} + 0.3V$ and 70% of V_{CC} , or with BS between GND and GND -0.3V.
4. The RAM can begin operation $> t_R$ ns after V_{CC} reaches the minimum operation voltages (3V).

Figure 1. Data Retention Timing

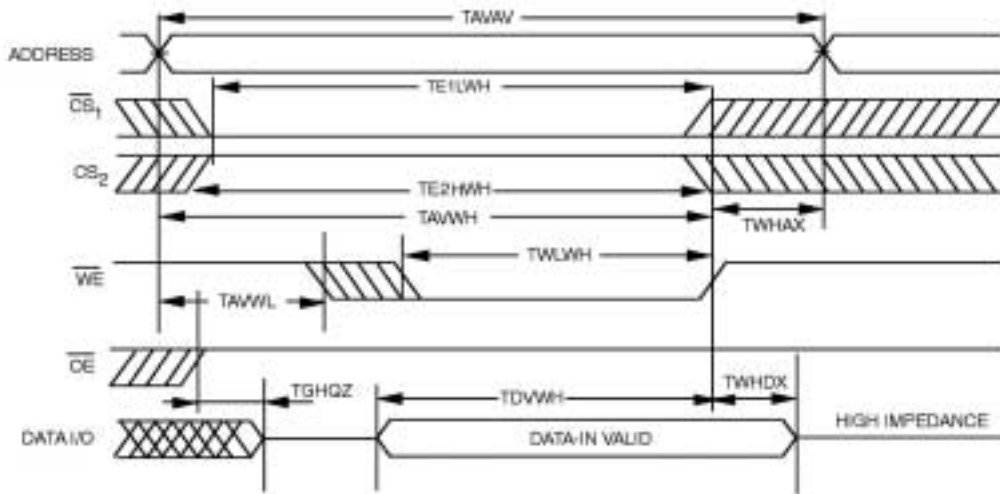


Data Retention Characteristics

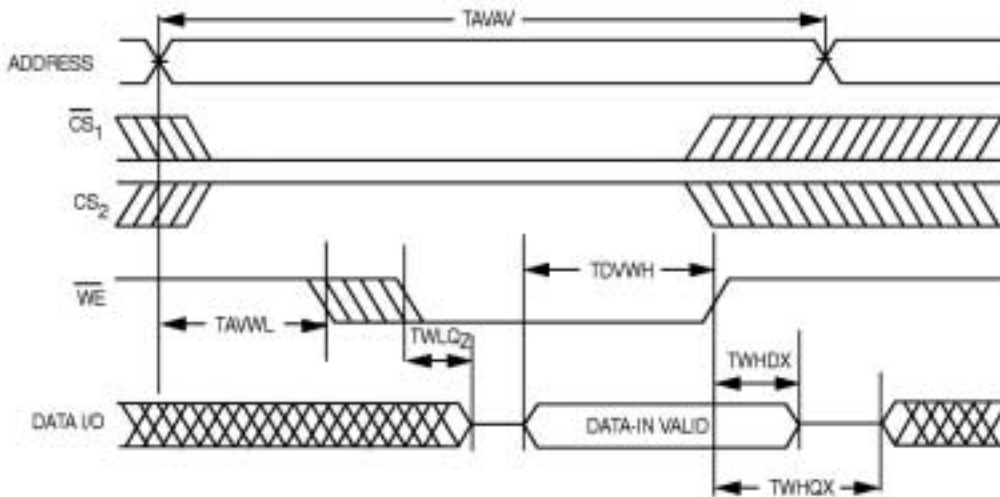
Parameter	Description	Min	Typical $T_A = 25^\circ C$	Max	Unit
V_{CCDR}	V_{CC} for data retention	2.0	–	–	V
T_{CDR}	Chip deselect to data retention time	0.0	–	–	ns
t_R	Operation recovery time	$t_{AVAV}^{(1)}$	–	–	ns
$I_{CCDR1}^{(2)}$	Data retention current at 2.0V	–	0.010	1.0	mA

- Notes: 1. T_{AVAV} = Read Cycle Time
 2. $\overline{CS1} = V_{CC}$ or $\overline{CS2} = \overline{CS1} = GND$, $V_{IN} = GND/V_{CC}$.

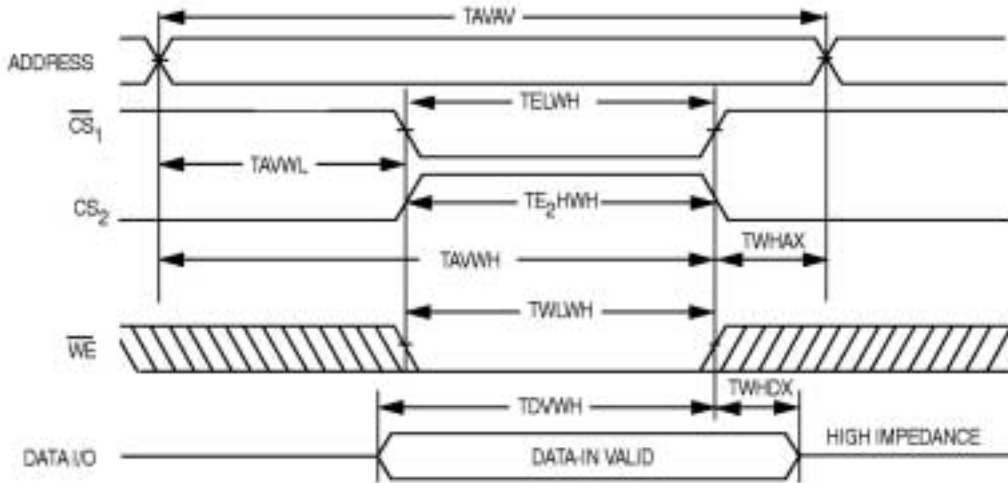
**Write Cycle 1. \overline{WE} Controlled.
OE High During Write**



**Write Cycle 2. \overline{WE} Controlled.
OE Low**

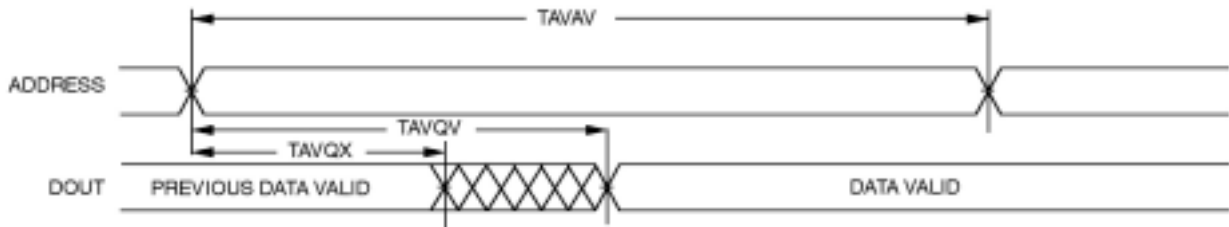


Write Cycle 3. $\overline{CS1}$ or $CS2$ Controlled⁽¹⁾

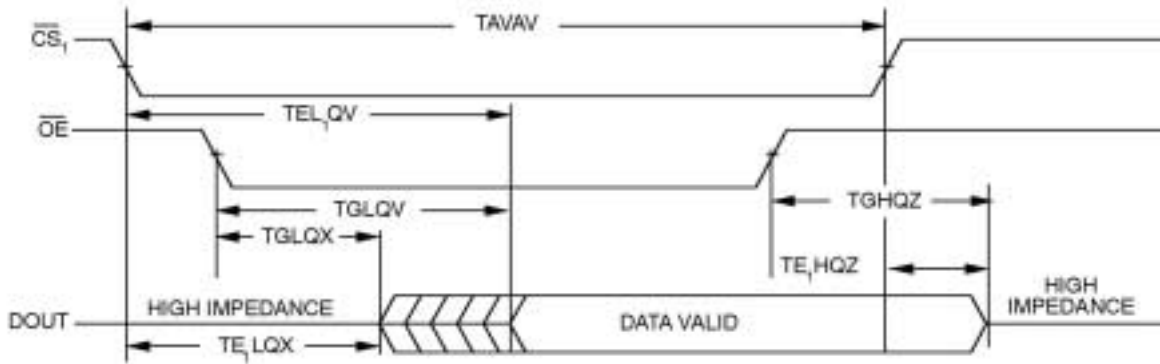


Note: 1. The internal write time of the memory is defined by the overlap of $\overline{CS1}$ LOW and $CS2$ HIGH and \overline{W} LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in activated. The data input setup and hold timing should be referenced to the activated edge of the signal that terminates the write. Data out is high impedance if $OE = V_{IH}$.

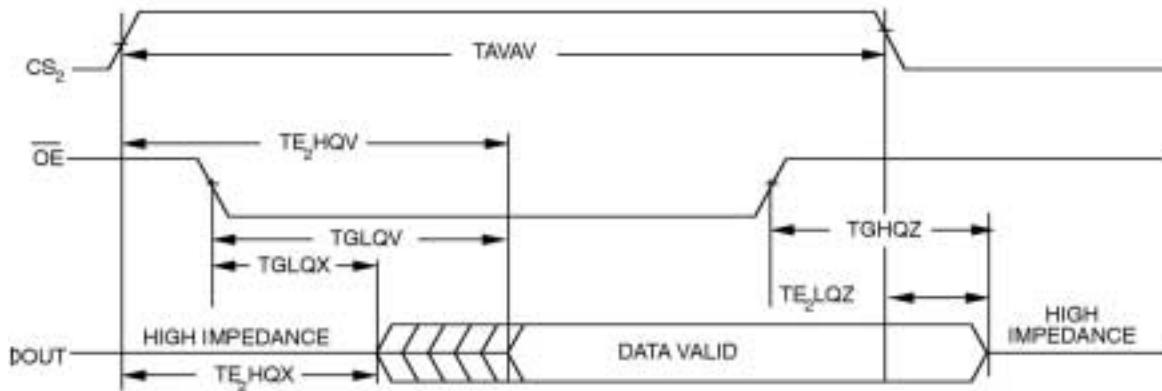
Read Cycle nb 1



Read Cycle nb 2



Read Cycle nb 3





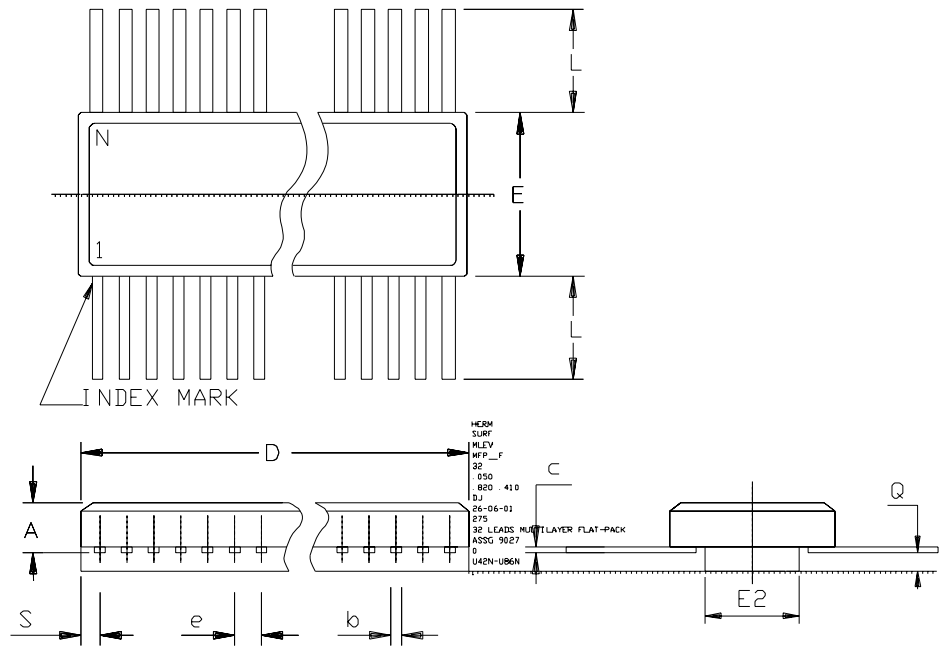
Ordering Information

Part Number	Temperature Range	Speed	Package	Flow
MMDJ-65609EV-40	-55 to +125°C	40 ns	FP32.4	Standard Mil
MMDJ-65609EV-40MQ	-55 to +125°C	40 ns	FP32.4	QML Q
MMDJ-65609EV-40-E	25°C	40 ns	FP32.4	Engineering Samples
MMDJ-65609EV-40/883 ⁽¹⁾	-55 to +125°C	40 ns	FP32.4	MIL 883 B
SMDJ-65609EV-40/883 ⁽¹⁾	-55 to +125°C	40 ns	FP32.4	MIL 883 S
MM0-65609EV-40-E	25°C	40 ns	Die	Engineering Samples
MM0-65609EV-40MQ	-55 to +125°C	40 ns	Die	QML Q

Note: 1. Contact Atmel for availability.

Package Drawing

32-pin Flat Pack (400 Mils)



	MM		INCH	
	Min	Max	Min	Max
A	1.78	2.72	.070	.107
b	0.38	0.48	.015	.019
c	0.076	0.15	.003	.007
D	20.62	21.03	.812	.828
E	10.26	10.57	.404	.416
E2	6.96	7.26	.274	.286
e	1.27	BSC	.050	BSC
L	7.37	7.87	.290	.310
Q	0.51	0.76	.020	.030
S	---	1.14	---	.045
N	32		32	



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Data- com

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

© Atmel Corporation 2002.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

ATMEL® is a registered trademark of Atmel.

Other terms and product names may be the trademarks of others.



Printed on recycled paper.