M65790FP

FBTC IMAGE DATA COMPRESSION and DECOMPRESSION LSI

DESCRIPTION

M65790FP is applied Mitsubishi original image data compression and decompression technology - FBTC (Fixed length Block Truncation Coding) technology that is good for natural image data, computer graphic data and high resolution image data.
M65790FP realizes system cost down, low power and first encoding and decoding of image data.
And also, FBTC type image compression and decompression technology has very low image data loss. It is possible to edit the compressed image deta in the cause of fixed length block encoding method.

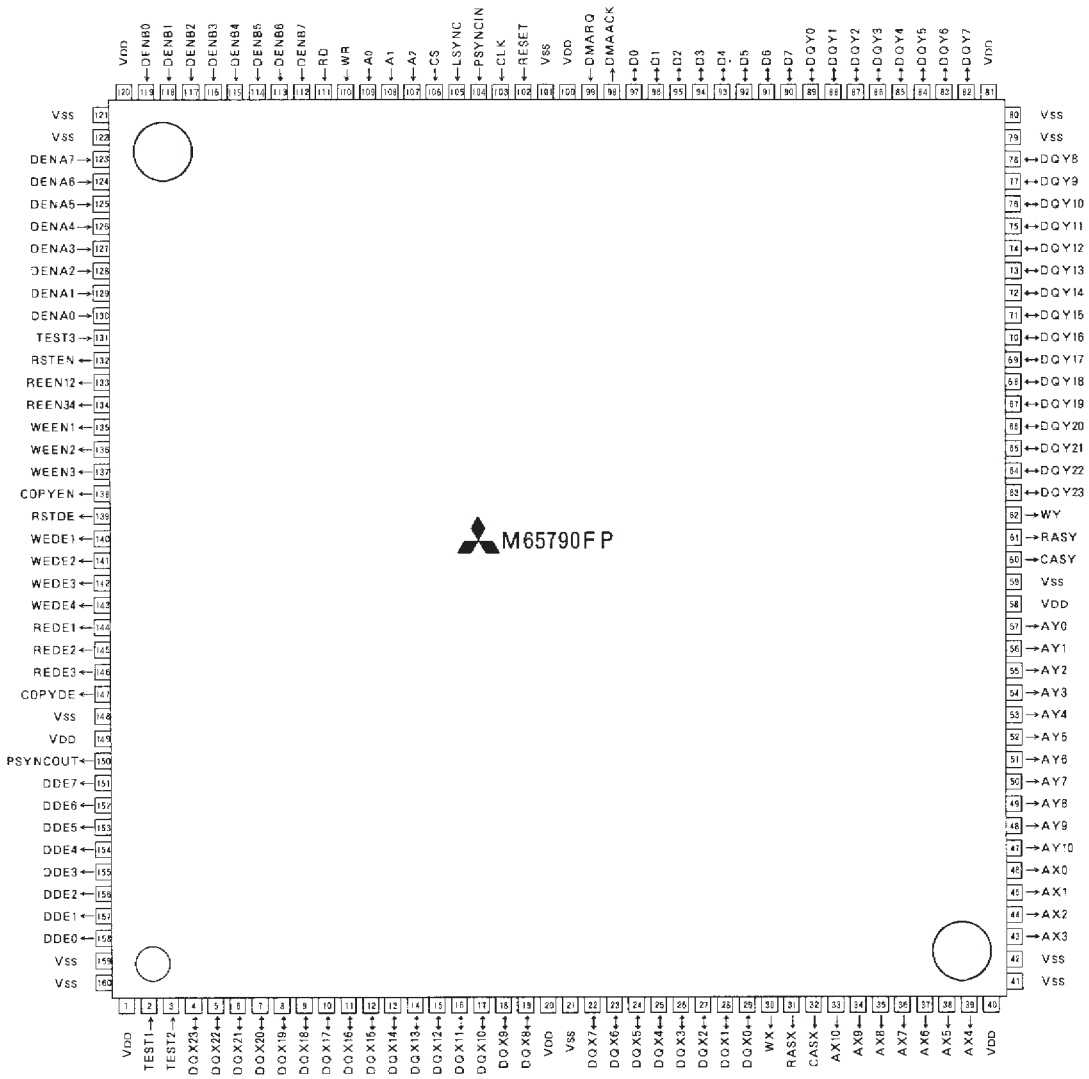
FEATURES

- Low image data distortion by FBTC type image compression and decompression.
- Easy decision for image data memory capacity by constant compression ratio 8/3.
- Enconding, decoding and image data editing with high speed data processing rate-20MBps.
- Capable of image data editing (90°, 180°, 270° rotation etc.) under compressed condition.
- Built in 16 Mbits DRAM controller and original 32 bytes image data is stored in six 16 Mbits DRAM (12Mbytes).
- Easy control for start and image data editing with setting to command register.

APPLICATIONS

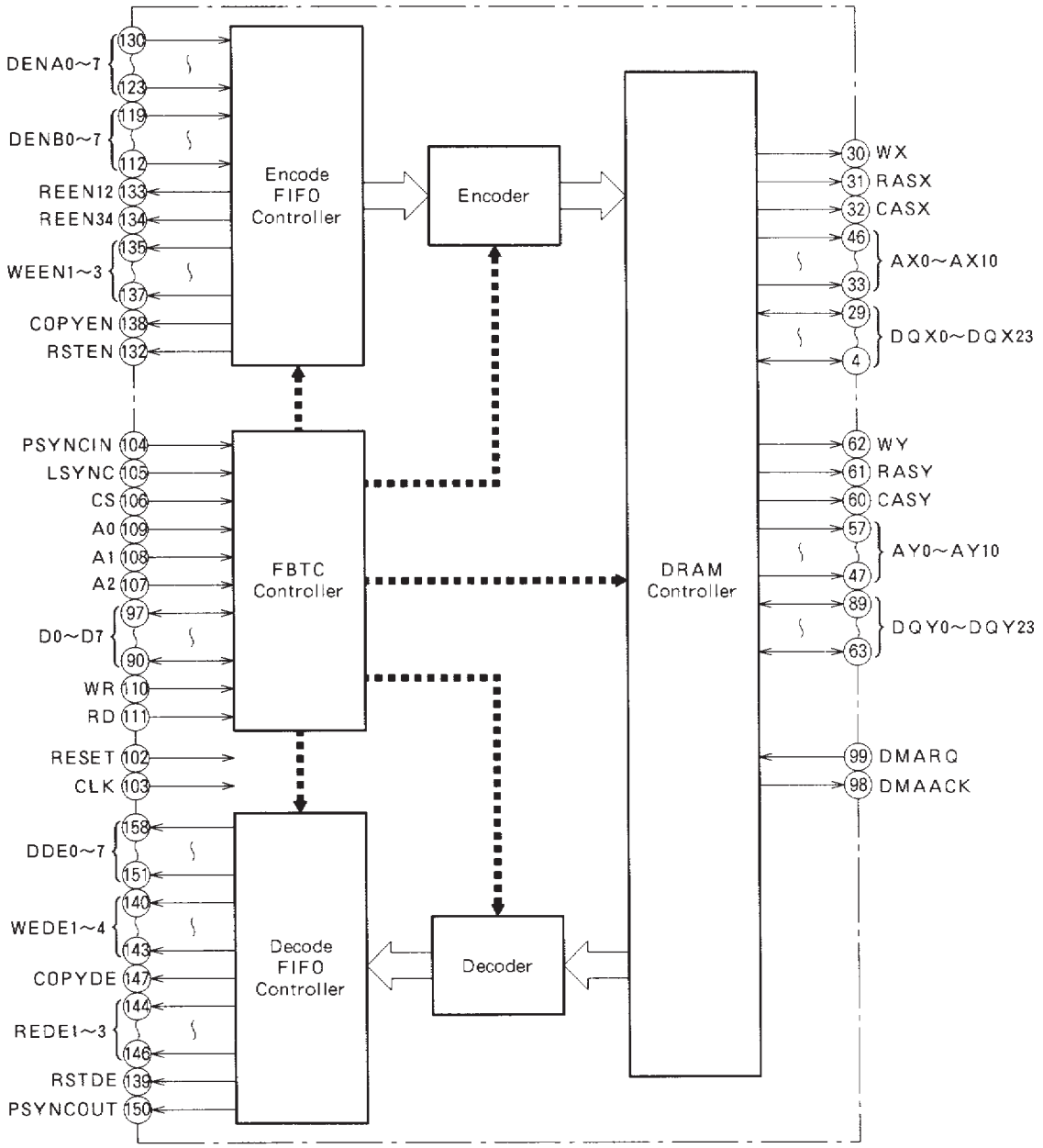
Applications involving the handling of high-resolution image data (digital copiers, color copiers, color printers, color facsimiles, high-definition TV, high-resolution displays etc.)

PIN CONFIGURATION (TOP VIEW)



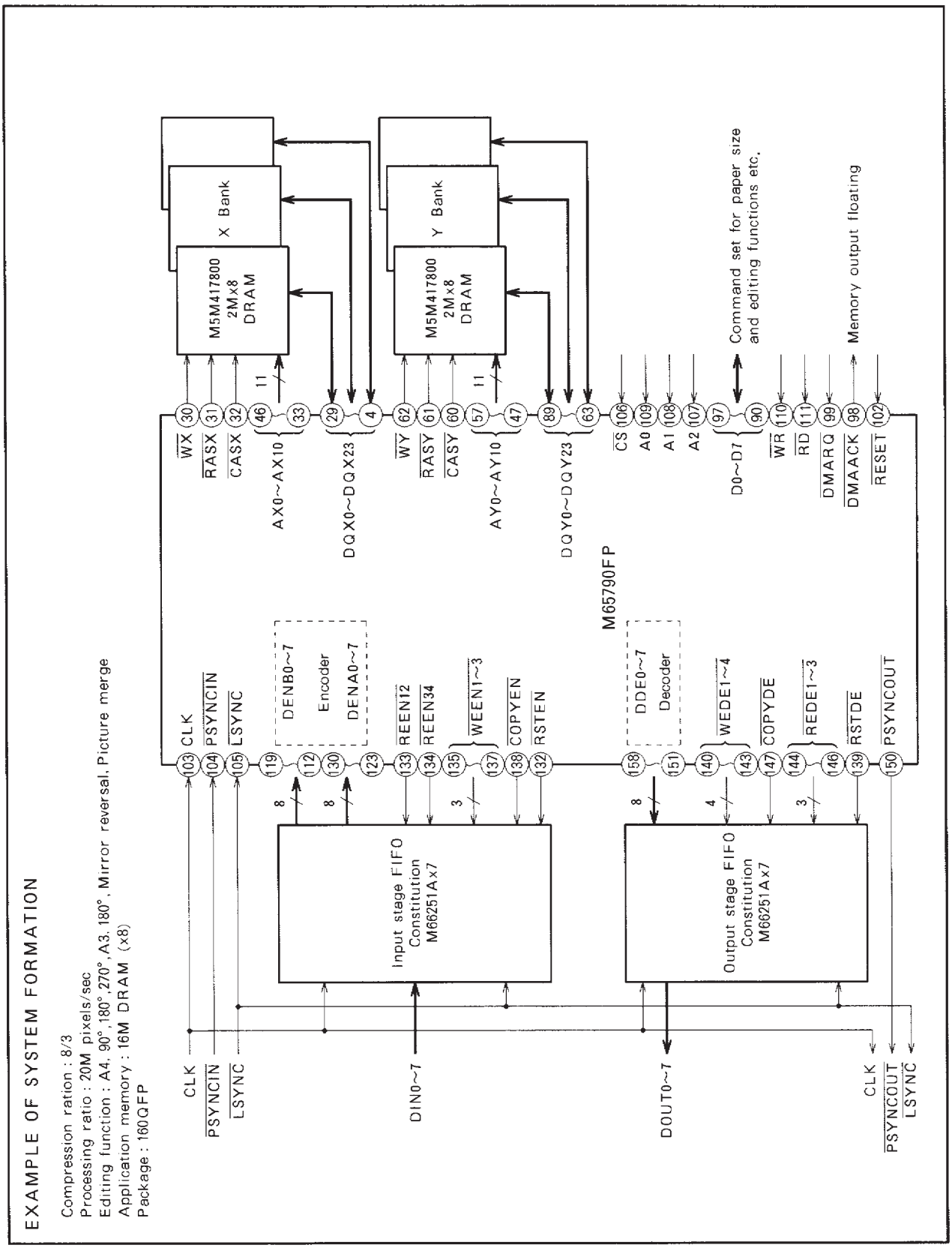
Outline 160P6-C (Plastic molded QFP)

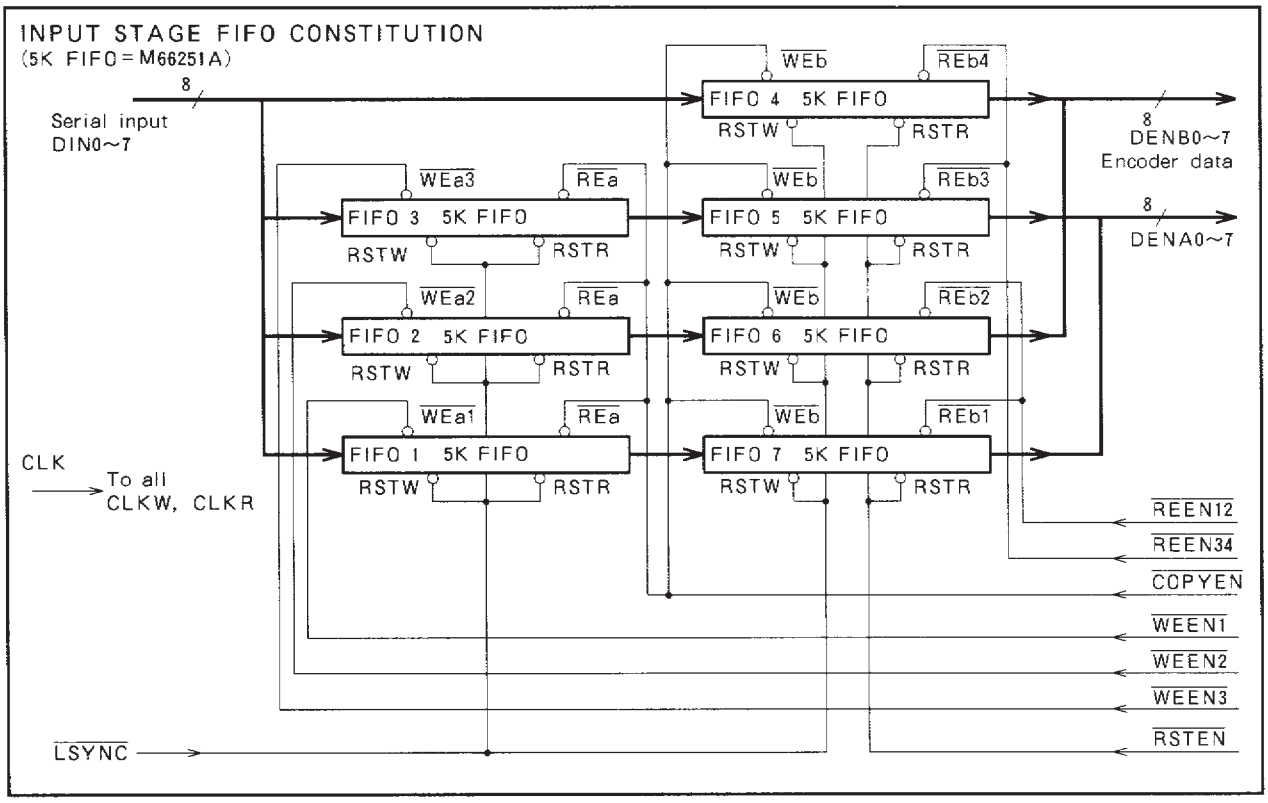
BLOCK DIAGRAM

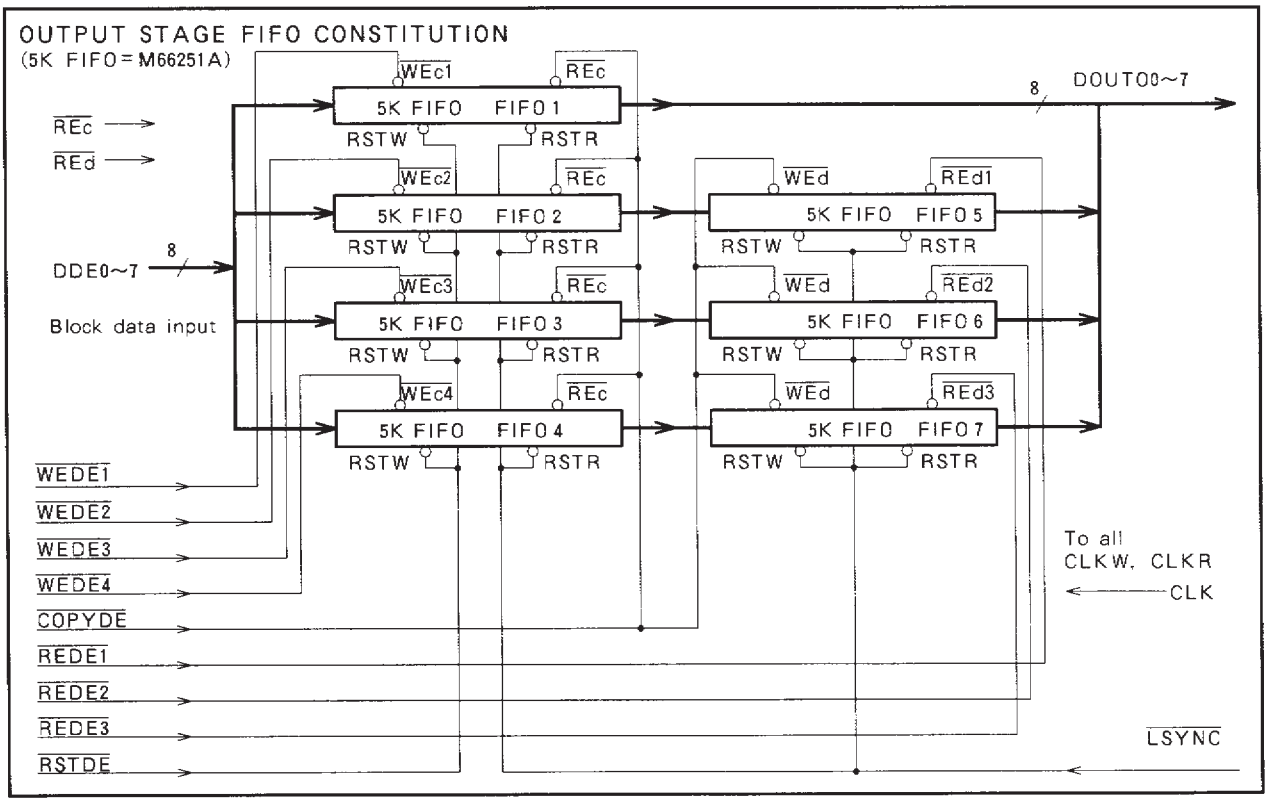


EXAMPLE OF SYSTEM FORMATION

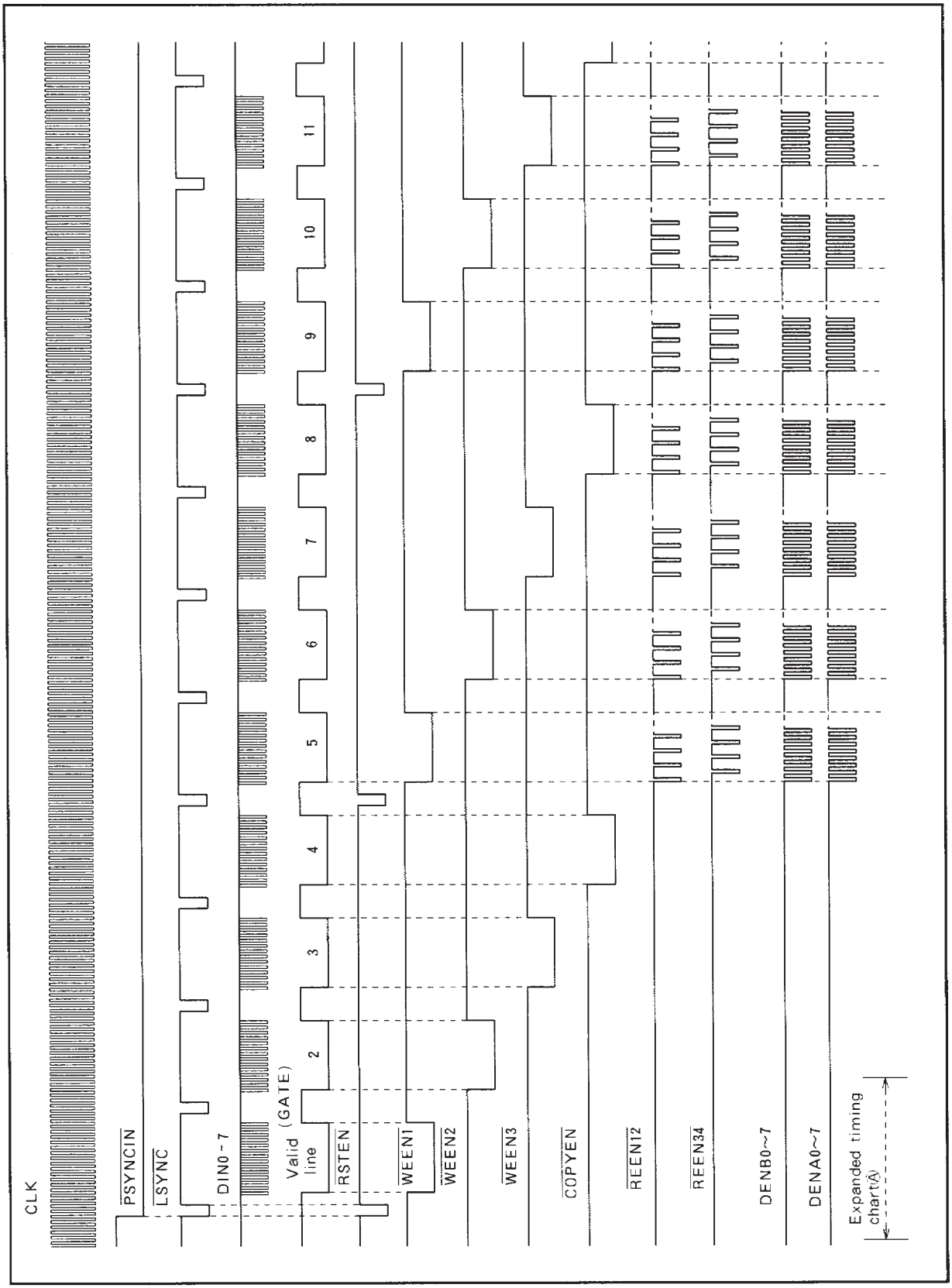
Compression ration : 8/3
Processing ratio : 20M pixels/sec
Editing function : A4, 90°, 180°, 270°, A3, 180°, Mirror reversal, Picture merge
Application memory : 16M DRAM (x8)
Package : 160QFP



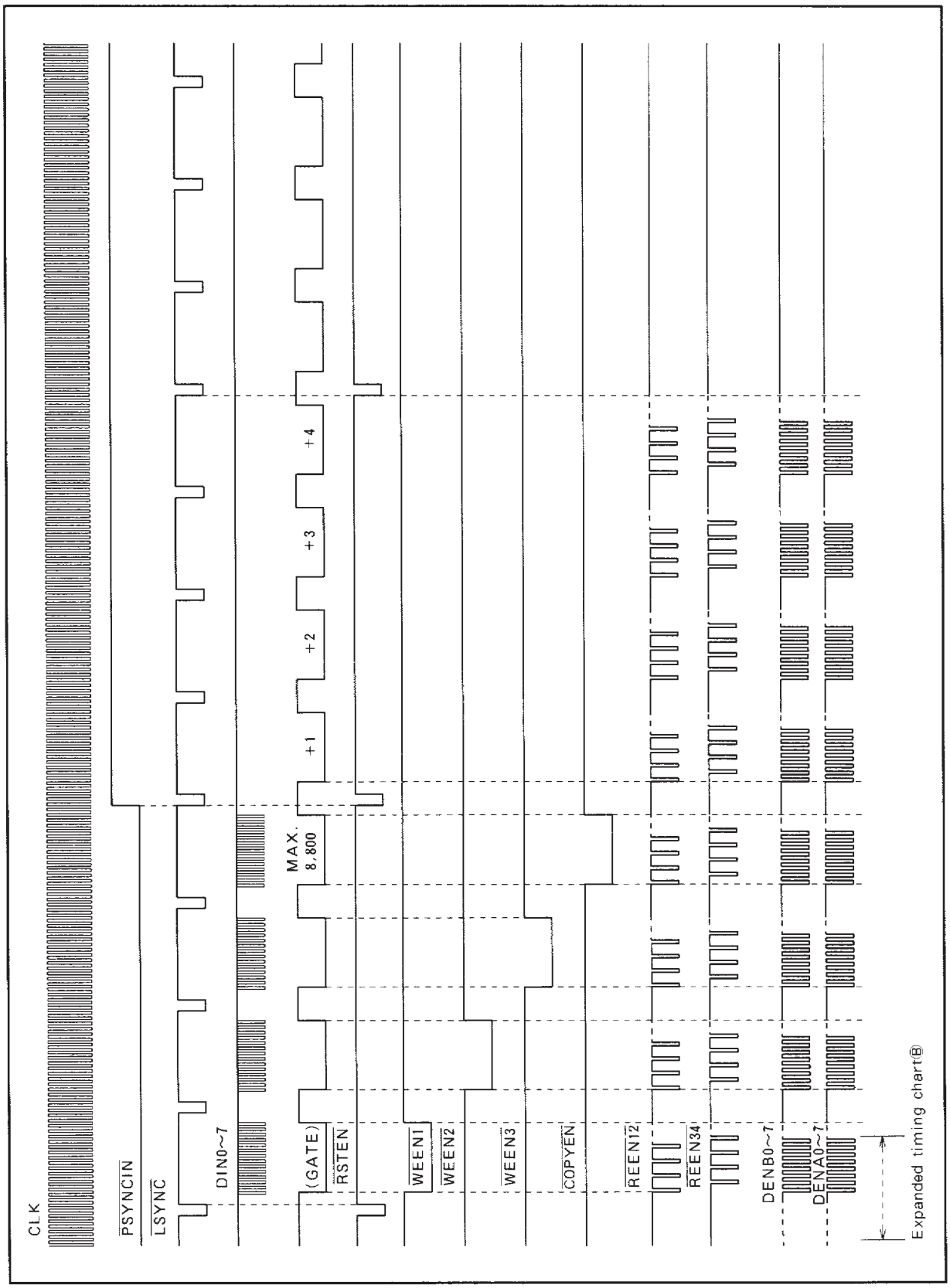

INPUT STAGE FIFO CONSTITUTION
(5K FIFO=M66251A)
8
Serial input
DIN0~7
WEb
REb4
FIFO 4 5K FIFO
RSTW
RSTR
8
DENB0~7
Encoder data
WEa3
REa
WEb
REb3
FIFO 3 5K FIFO
FIFO 5 5K FIFO
8
DENA0~7
WEa2
REa
WEb
REb2
FIFO 2 5K FIFO
FIFO 6 5K FIFO
WEa1
REa
WEb
REb1
FIFO 1 5K FIFO
FIFO 7 5K FIFO
CLK
To all
CLKW, CLKR
REEN12
REEN34
COPYEN
WEEN1
WEEN2
WEEN3
RSTEN
LSYNC


OUTPUT STAGE FIFO CONSTITUTION
(5K FIFO=M66251A)
WEc1
REc
5K FIFO FIFO 1
8
DOUT00~7
REc
REd
WEc2
REc
WEd
REd1
5K FIFO FIFO 2
5K FIFO FIFO 5
8
DDE0~7
WEc3
REc
WEd
REd2
Block data input
5K FIFO FIFO 3
5K FIFO FIFO 6
WEc4
REc
WEd
REd3
5K FIFO FIFO 4
5K FIFO FIFO 7
RSTW
RSTR
WEDE1
WEDE2
WEDE3
WEDE4
COPYDE
REDE1
REDE2
REDE3
RSTDE
To all
CLKW, CLKR
CLK
LSYNC

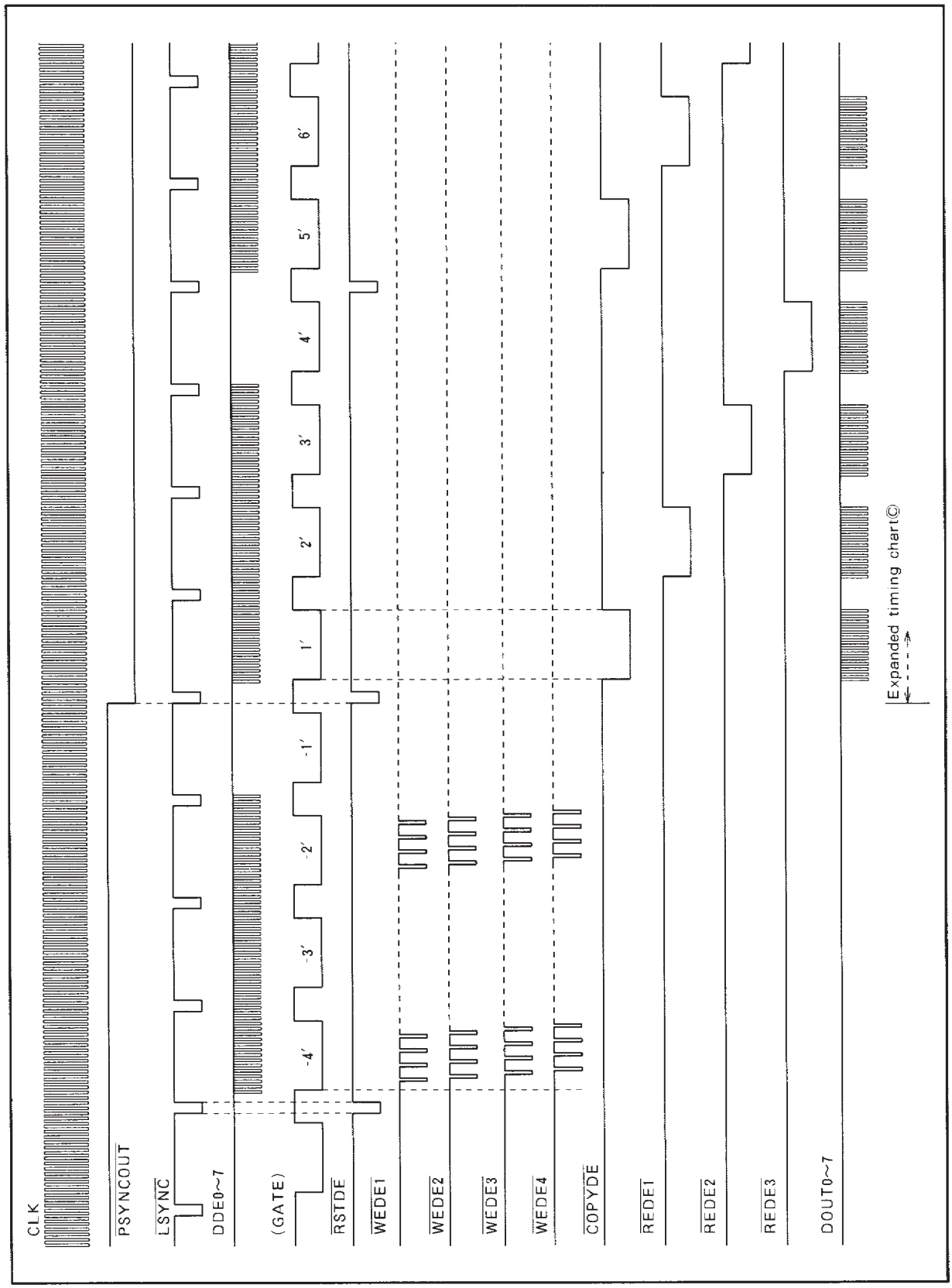
INPUT STAGE FIFO CONSTITUTION TIMING CHART(OVERAII CHART1/2)



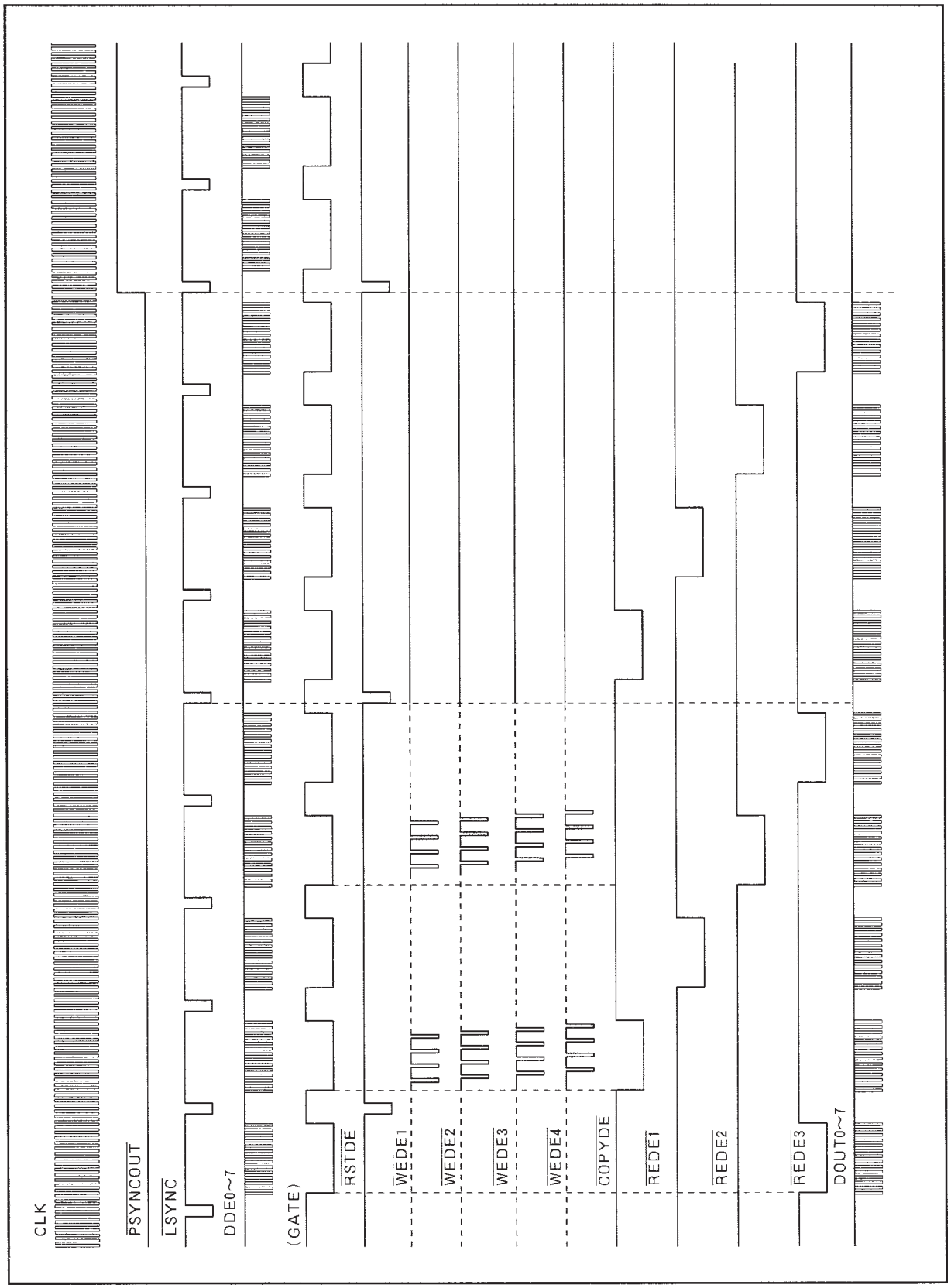
INPUT STAGE FIFO CONSTITUTION TIMING CHART(OVERAII CHART2/2)



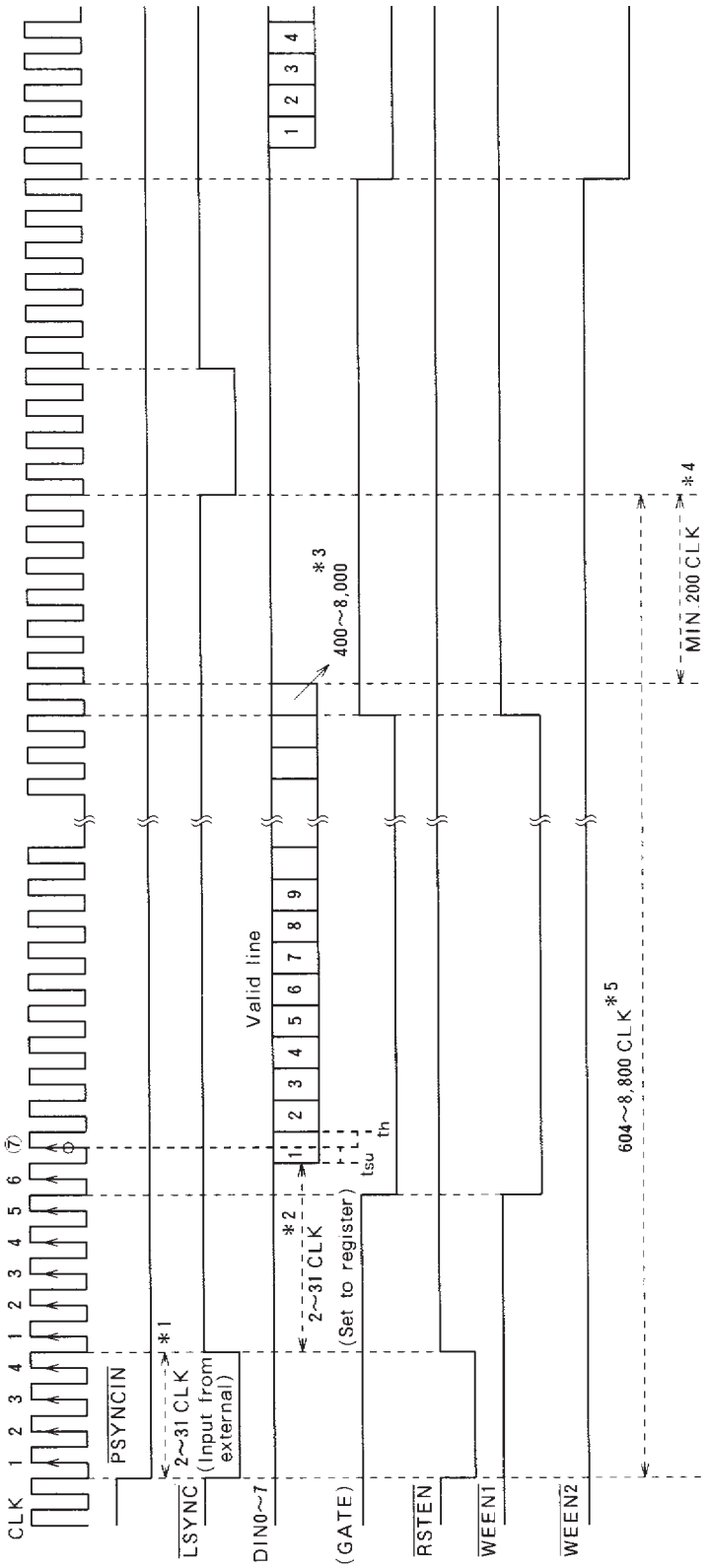
OUTPUT STAGE FIFO CONSTITUTION TIMING CHART(OVERAII CHART1/2)



OUTPUT STAGE FIFO CONSTITUTION TIMING CHART(OVERAII CHART2/2)

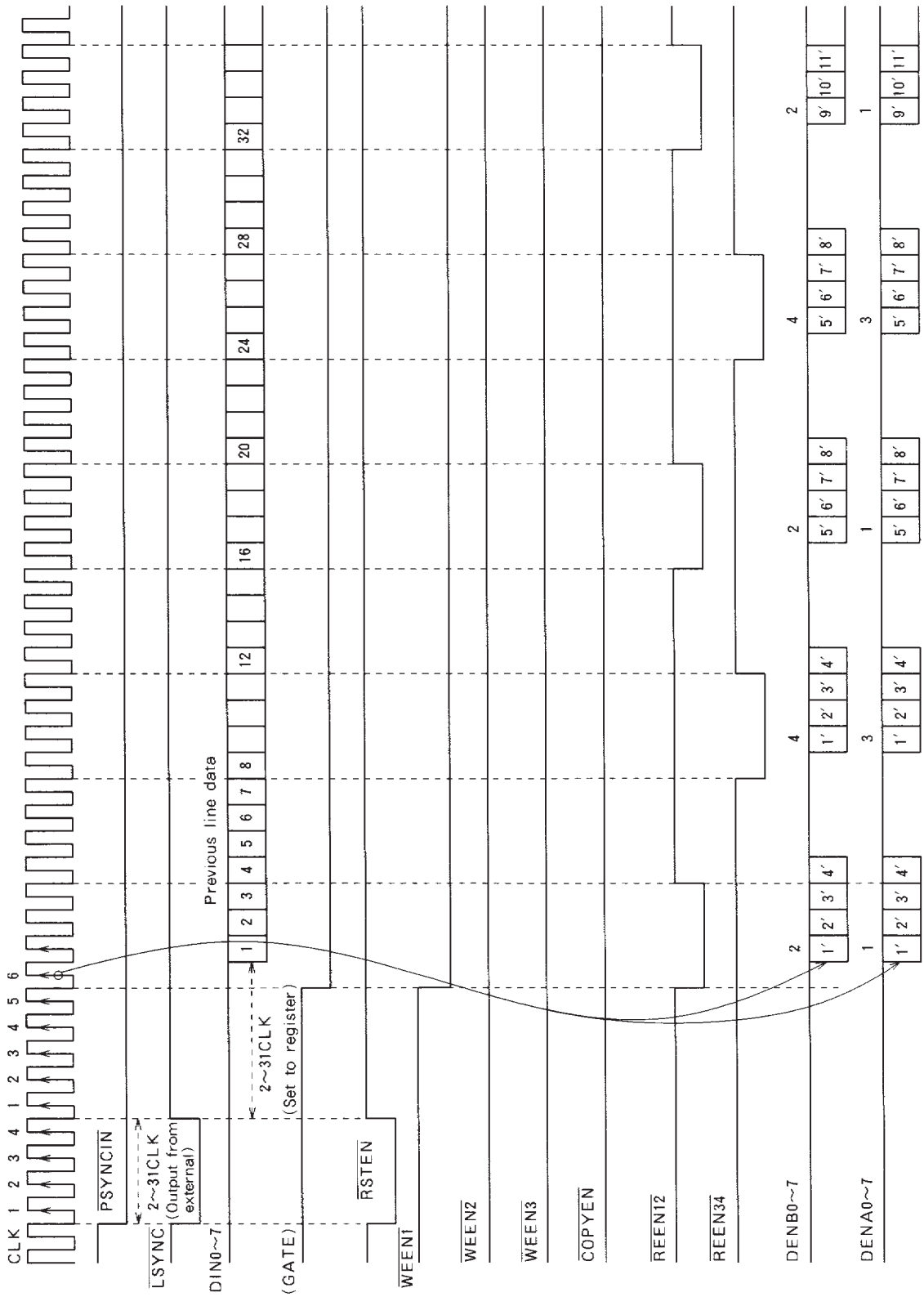


EXPANDED TIMING CHART Ⓐ

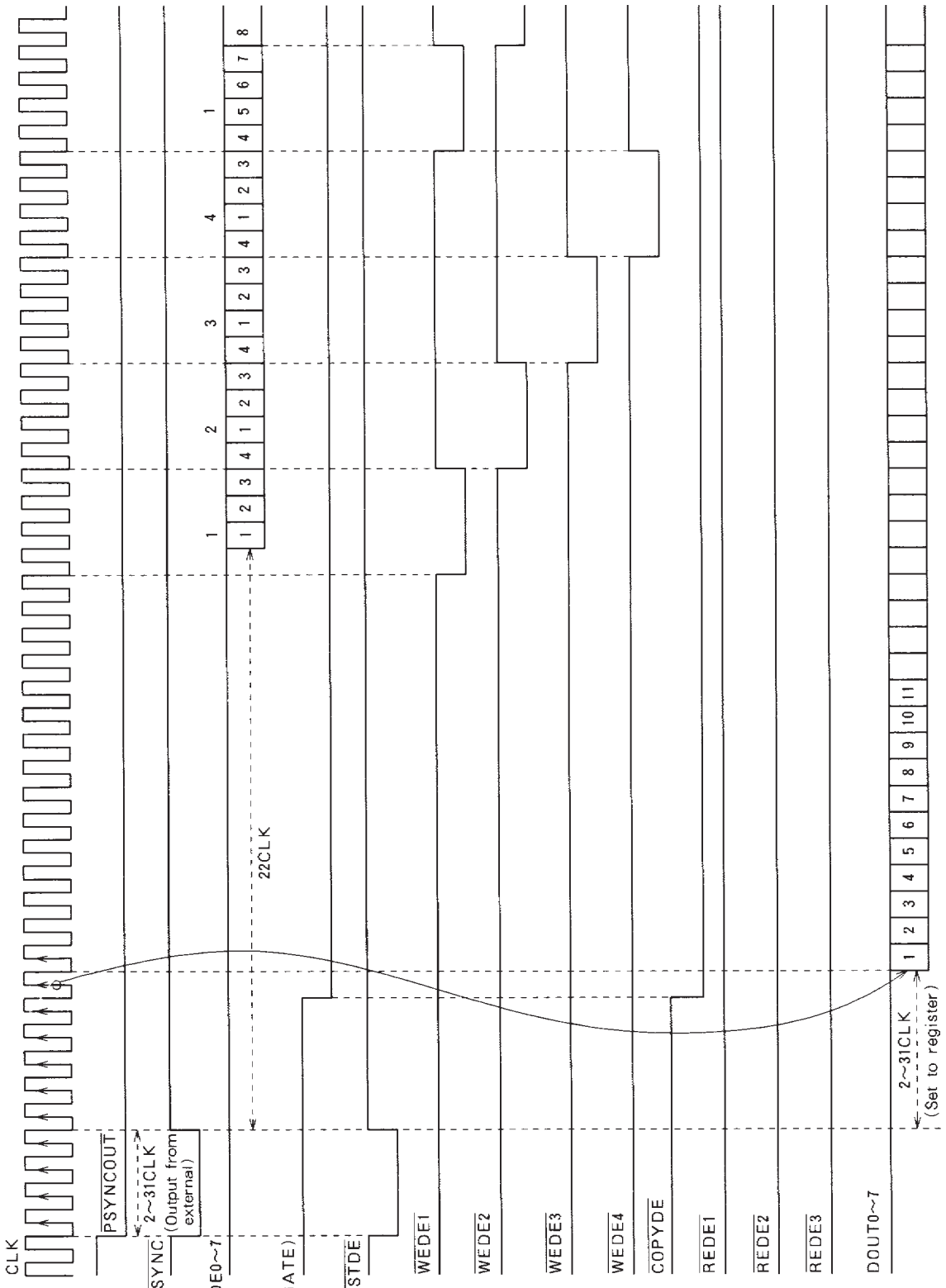


Notes
- *1 : "L" period of LSYNC is two clocks to 31 clocks.
- *2 : The next clock after idling period(2 to 31 clocks from the rising edge of $\overline{\text{LSYNC}}$)is the first valid data. Idling period can be set in the register. This picture shows idling period is set to six clocks.
- *3 : Valid one line data consist of 8000 pixels at the most. Consider memory capacity. Maximum one bank capacity is 16 Mdytes and two banks capacity is 32 Mbytes.
- *4 : Wait for 200 clocks from the end of valid data to the next falling edge of $\overline{\text{LSYNC}}$.
- *5 : The cycle for $\overline{\text{LSYNC}}$ is 8800 clocks at the most.

EXPANDED TIMING CHART Ⓑ



EXPANDED TIMING CHART©



PIN FUNCTION

Pin No.	Pin name	I/O	Function	Pin No.	Pin name	I/O	function
1	VDD	–		41	Vss	–	
2	TEST1	I	Test signal(Fix to "L")	42	Vss	–	
3	TEST2	I	Test signal(Fix to "L")	43	AX3	O	X bank address
4	DQX23	B	DRAM X bank data(MSB)	44	AX2	O	X bank address
5	DQX22	B	DRAM X bank data	45	AX1	O	X bank address
6	DQX21	B	DRAM X bank data	46	AX0	O	X bank address(LSB)
7	DQX20	B	DRAM X bank data	47	AY10	O	Y bank sddress(MSB)
8	DQX19	B	DRAM X bank data	48	AY9	O	Y bank address
9	DQX18	B	DRAM X bank data	49	AY8	O	Y bank address
10	DQX17	B	DRAM X bank data	50	AY7	O	Y bank address
11	DQX16	B	DRAM X bank data	51	AY6	O	Y bank address
12	DQX15	B	DRAM X bank data	52	AY5	O	Y bank address
13	DQX14	B	DRAM X bank data	53	AY4	O	Y bank address
14	DQX13	B	DRAM X bank data	54	AY3	O	Y bank address
15	DQX12	B	DRAM X bank data	55	AY2	O	Y bank address
16	DQX11	B	DRAM X bank data	56	AY1	O	Y bank address
17	DQX10	B	DRAM X bank data	57	AY0	O	Y bank address(LSB)
18	DQX9	B	DRAM X bank data	58	VDD	–	
19	DQX8	B	DRAM X bank data	59	Vss	–	
20	VDD	–		60	CASY	O	Y bank CAS(Low enable)
21	Vss	–		61	RASY	O	Y bank RAS(Low enable)
22	DQX7	B	DRAM X bank data	62	WY	O	Y bank write(Low enable)
23	DQX6	B	DRAM X bank data	63	DQY23	B	DRAM Y bank data(MSB)
24	DQX5	B	DRAM X bank data	64	DQY22	B	DRAM Y bank data
25	DQX4	B	DRAM X bank data	65	DQY21	B	DRAM Y bank data
26	DQX3	B	DRAM X bank data	66	DQY20	B	DRAM Y bank data
27	DQX2	B	DRAM X bank data	67	DQY19	B	DRAM Y bank data
28	DQX1	B	DRAM X bank data	68	DQY18	B	DRAM Y bank data
29	DQX0	B	DRAM X bank data(LSB)	69	DQY17	B	DRAM Y bank data
30	WX	O	X bank write(Low enable)	70	DQY16	B	DRAM Y bank data
31	RASX	O	X bank RAS(Low enable)	71	DQY15	B	DRAM Y bank data
32	CASX	O	X bank CAS(Low enable)	72	DQY14	B	DRAM Y bank data
33	AX10	O	X bank address(MSB)	73	DQY13	B	DRAM Y bank data
34	AX9	O	X bank address	74	DQY12	B	DRAM Y bank data
35	AX8	O	X bank address	75	DQY11	B	DRAM Y bank data
36	AX7	O	X bank address	76	DQY10	B	DRAM Y bank data
37	AX6	O	X bank address	77	DQY9	B	DRAM Y bank data
38	AX5	O	X bank address	78	DQY8	B	DRAM Y bank data
39	AX4	O	X bank address	79	Vss	–	
40	VDD	–		80	Vss	–	

I : Input
O : Output
B : Bi-directional

PIN FUNCTION (Continued)

Pin No.	Pin name	I/O	Function	Pin No.	Pin name	I/O	Function
81	VDD	–		121	VSS	–	
82	DQY7	B	DRAM Y bank data	122	VSS	–	
83	DQY6	B	DRAM Y bank data	123	DENA7	I	Encode A line data(MSB)
84	DQY5	B	DRAM Y bank data	124	DENA6	I	Encode A line data
85	DQY4	B	DRAM Y bank data	125	DENA5	I	Encode A line data
86	DQY3	B	DRAM Y bank data	126	DENA4	I	Encode A line data
87	DQY2	B	DRAM Y bank data	127	DENA3	I	Encode A line data
88	DQY1	B	DRAM Y bank data	128	DENA2	I	Encode A line data
89	DQY0	B	DRAM Y bank data(LSB)	129	DENA1	I	Encode A line data
90	D7	B	Command register data(MSB)	130	DENA0	I	Encode A line data(LSB)
91	D6	B	Command register data	131	TEST3	I	Test signal(Fix to "L")
92	D5	B	Command register data	132	RSTEN	O	Encode FIFO reset(Low enable)
93	D4	B	Command register data	133	REEN12	O	Encode FIFO 6&7 read(L)
94	D3	B	Command register data	134	REEN34	O	Encode FIFO 4&5 read(L)
95	D2	B	Command register data	135	WEEN1	O	Encode FIFO 1 write(L)
96	D1	B	Command register data	136	WEEN2	O	Encode FIFO 2 write(L)
97	D0	B	Command register data(LSB)	137	WEEN3	O	Encode FIFO 3 write(L)
98	DMAACK	O	DMA ACK	138	COPYEN	O	Encode FIFO copy(L)
99	DMARQ	I	DMA request signal(Low enable)	139	RSTDE	O	Decode FIFO reset(Low enable)
100	VDD	–		140	WEDE1	O	Decode FIFO 1 write(L)
101	VSS	–		141	WEDE2	O	Decode FIFO 2 write(L)
102	RESET	I	System reset(Low enable)	142	WEDE3	O	Decode FIFO 3 write(L)
103	CLK	I	System clock	143	WEDE4	O	Decode FIFO 4 write(L)
104	PSYNC	I	Page sync.(Low enable)	144	REDE1	O	Decode FIFO 5 write(L)
105	LSYNC	I	Line sync.(Low enable)	145	REDE2	O	Decode FIFO 6 write(L)
106	CS	I	Chip select(Low enable)	146	REDE3	O	Decode FIFO 7 write(L)
107	A2	I	Command register address(MSB)	147	COPYDE	O	Decode FIFO copy(L)
108	A1	I	Command register address	148	VSS	–	
109	A0	I	Command register address(LSB)	149	VDD	–	
110	WR	I	Command register write(Low enable)	150	PSYNCOUT	O	Decode page sync(Low enable)
111	RD	I	Command register read(Low enable)	151	DDE7	O	Decode data(MSB)
112	DENB7	I	Encode B line data(MSB)	152	DDE6	O	Decode data
113	DENB6	I	Encode B line data	153	DDE5	O	Decode data
114	DENB5	I	Encode B line data	154	DDE4	O	Decode data
115	DENB4	I	Encode B line data	155	DDE3	O	Decode data
116	DENB3	I	Encode B line data	156	DDE2	O	Decode data
117	DENB2	I	Encode B line data	157	DDE1	O	Decode data
118	DENB1	I	Encode B line data	158	DDE0	O	Decode data(LSB)
119	DENB0	I	Encode B line data(LSB)	159	VSS	–	
120	VDD	–		160	VSS	–	

I : Input
O : Output
B : Bi-directional

PIN INFORMATION

Pin No.	Pin name	I/O	Buffer Type	Pin No.	Pin Name	I/O	Buffer Type
1	VDD	–		41	VSS	–	
2	TEST1	I	CMOS SMT input(50kΩP.D)	42	VSS	–	
3	TEST2	I	CMOS SMT input(50kΩP.D)	43	AX3	O	3-STATE Output(I_{OL}=4mA)
4	DQX23	B	Output(I_{OL}=2mA)/CMOS input	44	AX2	O	3-STATE Output(I_{OL}=4mA)
5	DQX22	B	Output(I_{OL}=2mA)/CMOS input	45	AX1	O	3-STATE Output(I_{OL}=4mA)
6	DQX21	B	Output(I_{OL}=2mA)/CMOS input	46	AX0	O	3-STATE Output(I_{OL}=4mA)
7	DQX20	B	Output(I_{OL}=2mA)/CMOS input	47	AY10	O	3-STATE Output(I_{OL}=4mA)
8	DQX19	B	Output(I_{OL}=2mA)/CMOS input	48	AY9	O	3-STATE Output(I_{OL}=4mA)
9	DQX18	B	Output(I_{OL}=2mA)/CMOS input	49	AY8	O	3-STATE Output(I_{OL}=4mA)
10	DQX17	B	Output(I_{OL}=2mA)/CMOS input	50	AY7	O	3-STATE Output(I_{OL}=4mA)
11	DQX16	B	Output(I_{OL}=2mA)/CMOS input	51	AY6	O	3-STATE Output(I_{OL}=4mA)
12	DQX15	B	Output(I_{OL}=2mA)/CMOS input	52	AY5	O	3-STATE Output(I_{OL}=4mA)
13	DQX14	B	Output(I_{OL}=2mA)/CMOS input	53	AY4	O	3-STATE Output(I_{OL}=4mA)
14	DQX13	B	Output(I_{OL}=2mA)/CMOS input	54	AY3	O	3-STATE Output(I_{OL}=4mA)
15	DQX12	B	Output(I_{OL}=2mA)/CMOS input	55	AY2	O	3-STATE Output(I_{OL}=4mA)
16	DQX11	B	Output(I_{OL}=2mA)/CMOS input	56	AY1	O	3-STATE Output(I_{OL}=4mA)
17	DQX10	B	Output(I_{OL}=2mA)/CMOS input	57	AY0	O	3-STATE Output(I_{OL}=4mA)
18	DQX9	B	Output(I_{OL}=2mA)/CMOS input	58	VDD	–	
19	DQX8	B	Output(I_{OL}=2mA)/CMOS input	59	VSS	–	
20	VDD	–		60	CASY	O	3-STATE Output(I_{OL}=4mA)
21	VSS	–		61	RASY	O	3-STATE Output(I_{OL}=4mA)
22	DQX7	B	Output(I_{OL}=2mA)/CMOS input	62	WY	O	3-STATE Output(I_{OL}=4mA)
23	DQX6	B	Output(I_{OL}=2mA)/CMOS input	63	DQY23	B	Output(I_{OL}=2mA)/CMOS input
24	DQX5	B	Output(I_{OL}=2mA)/CMOS input	64	DQY22	B	Output(I_{OL}=2mA)/CMOS input
25	DQX4	B	Output(I_{OL}=2mA)/CMOS input	65	DQY21	B	Output(I_{OL}=2mA)/CMOS input
26	DQX3	B	Output(I_{OL}=2mA)/CMOS input	66	DQY20	B	Output(I_{OL}=2mA)/CMOS input
27	DQX2	B	Output(I_{OL}=2mA)/CMOS input	67	DQY19	B	Output(I_{OL}=2mA)/CMOS input
28	DQX1	B	Output(I_{OL}=2mA)/CMOS input	68	DQY18	B	Output(I_{OL}=2mA)/CMOS input
29	DQX0	B	Output(I_{OL}=2mA)/CMOS input	69	DQY17	B	Output(I_{OL}=2mA)/CMOS input
30	WX	O	3-STATE Output(I_{OL}=4mA)	70	DQY16	B	Output(I_{OL}=2mA)/CMOS input
31	RASX	O	3-STATE Output(I_{OL}=4mA)	71	DQY15	B	Output(I_{OL}=2mA)/CMOS input
32	CASX	O	3-STATE Output(I_{OL}=4mA)	72	DQY14	B	Output(I_{OL}=2mA)/CMOS input
33	AX10	O	3-STATE Output(I_{OL}=4mA)	73	DQY13	B	Output(I_{OL}=2mA)/CMOS input
34	AX9	O	3-STATE Output(I_{OL}=4mA)	74	DQY12	B	Output(I_{OL}=2mA)/CMOS input
35	AX8	O	3-STATE Output(I_{OL}=4mA)	75	DQY11	B	Output(I_{OL}=2mA)/CMOS input
36	AX7	O	3-STATE Output(I_{OL}=4mA)	76	DQY10	B	Output(I_{OL}=2mA)/CMOS input
37	AX6	O	3-STATE Output(I_{OL}=4mA)	77	DQY9	B	Output(I_{OL}=2mA)/CMOS input
38	AX5	O	3-STATE Output(I_{OL}=4mA)	78	DQY8	B	Output(I_{OL}=2mA)/CMOS input
39	AX4	O	3-STATE Output(I_{OL}=4mA)	79	VSS	–	
40	VDD	–		80	VSS	–	

I : Input
O : Output
B : Bi-directional

SMT : Schmitt
P.D : Pull down

PIN INFORMATION (Continued)

Pin No.	Pin Name	I/O	Buffer Type	Pin No.	Pin Name	I/O	Buffer Yype
81	VDD	–		121	Vss	–	
82	DQY7	B	Output(IOL=2mA)/CMOS input	122	Vss	–	
83	DQY6	B	Output(IOL=2mA)/CMOS input	123	DENA7	I	CMOS input(50kΩ P.U)
84	DQY5	B	Output(IOL=2mA)/CMOS input	124	DENA6	I	CMOS input(50kΩ P.U)
85	DQY4	B	Output(IOL=2mA)/CMOS input	125	DENA5	I	CMOS input(50kΩ P.U)
86	DQY3	B	Output(IOL=2mA)/CMOS input	126	DENA4	I	CMOS input(50kΩ P.U)
87	DQY2	B	Output(IOL=2mA)/CMOS input	127	DENA3	I	CMOS input(50kΩ P.U)
88	DQY1	B	Output(IOL=2mA)/CMOS input	128	DENA2	I	CMOS input(50kΩ P.U)
89	DQY0	B	Output(IOL=2mA)/CMOS input	129	DENA1	I	CMOS input(50kΩ P.U)
90	D7	B	Output(IOL=4mA)/CMOS input	130	DANA0	I	CMOS input(50kΩ P.U)
91	D6	B	Output(IOL=4mA)/CMOS input	131	TEST3	I	CMOS SMT input(50kΩ P.U)
92	D5	B	Output(IOL=4mA)/CMOS input	132	RSTEN	O	Output(IOL=4mA)
93	D4	B	Output(IOL=4mA)/CMOS input	133	REEN12	O	Output(IOL=4mA)
94	D3	B	Output(IOL=4mA)/CMOS input	134	REEN34	O	Output(IOL=4mA)
95	D2	B	Output(IOL=4mA)/CMOS input	135	WEEN1	O	Output(IOL=4mA)
96	D1	B	Output(IOL=4mA)/CMOS input	136	WEEN2	O	Output(IOL=4mA)
97	D0	B	Output(IOL=4mA)/CMOS input	137	WEEN3	O	Output(IOL=4mA)
98	DMAACK	O	Output(IOL=4mA)	138	COPYEN	O	Output(IOL=8mA)
99	DMARQ	I	CMOS SMT input	139	RSTDE	O	Output(IOL=4mA)
100	VDD	–		140	WEDE1	O	Output(IOL=4mA)
101	Vss	–		141	WEDE2	O	Output(IOL=4mA)
102	RESET	I	CMOS SMT input	142	WEDE3	O	Output(IOL=4mA)
103	CLK	I	CMOS SMT input	143	WEDE4	O	Output(IOL=4mA)
104	PSYNC	I	CMOS SMT input	144	REDE1	O	Output(IOL=4mA)
105	LSYNC	I	CMOS SMT input	145	REDE2	O	Output(IOL=4mA)
106	CS	I	CMOS input	146	REDE3	O	Output(IOL=4mA)
107	A2	I	CMOS input	147	COPYDE	O	Output(IOL=8mA)
108	A1	I	CMOS input	148	Vss	–	
109	A0	I	CMOS input	149	VDD	–	
110	WR	I	CMOS input	150	PSYNCOUT	O	Output(IOL=4mA)
111	RD	I	CMOS input	151	DDE7	O	Output(IOL=8mA)
112	DENB7	I	CMOS input(50kΩ P.U)	152	DDE6	O	Output(IOL=8mA)
113	DENB6	I	CMOS input(50kΩ P.U)	153	DDE5	O	Output(IOL=8mA)
114	DENB5	I	CMOS input(50kΩ P.U)	154	DDE4	O	Output(IOL=8mA)
115	DENB4	I	CMOS input(50kΩ P.U)	155	DDE3	O	Output(IOL=8mA)
116	DENB3	I	CMOS input(50kΩ P.U)	156	DDE2	O	Output(IOL=8mA)
117	DENB2	I	CMOS input(50kΩ P.U)	157	DDE1	O	Output(IOL=8mA)
118	DENB1	I	CMOS input(50kΩ P.U)	158	DDE0	O	Output(IOL=8mA)
119	DENB0	I	CMOS input(50kΩ P.U)	159	Vss	–	
120	VDD	–		160	Vss	–	

I : Input
O : Output
B : Bi-directional

P.U : Pull up

ABSOLUTE MAXIMUM RATINGS (Vss=0V, unless otherwise noted)

Symbol	Paramater	Ratings		Unit
		Min.	Max.	
V_{DD}	Supply voltage	Vss−0.3	Vss+6.5	V
V_I	Input voltage	Vss−0.3	VDD+0.3	V
V_O	Output voltage	Vss−0.3	VDD+0.3	V
I_{IK}	Input protection diode current (Note 1)	−16	+16	mA
I_{OK}	output parasitic diode current (Note 2)	−16	+16	mA
I_O	Output current (Note 2)	−16	+16	mA
I_{DD}	VDD Supply current (Note 3)		80	mA
I_{SS}	Vss Supply current (Note 4)	−80		mA
T_{stg}	Storage temperature	−55	150	℃
P_{dout}	Output load (Note 5)		1600 (Note 6)	MHz·pF
			1200 (Note 7)	
			600 (Note 8)	
P_d	Power dissipation		500	mW

Note 1. Rating for one input buffer
2. Rating for one output buffer
3. Rating for one VDD pin
4. Rating for one Vss pin
5. P_{dout} = (Output frequency MHz) × [(Output load capacity pF) + 8 pF]
6. Rating for buffer for which I_{OL} = 8 mA
7. Rating for buffer for which I_{OL} = 4 mA
8. Rating for buffer for which I_{OL} = 2 mA

RECOMMENDED OPERATING CONDITIONS (Vss= 0 V, unless otherwise noted)

Symbol	Paramater		Ratings		Unit
			Min.	Max.	
V_{DD}	Supply voltage	CMOS input	4.5	5.5	V
V_I	Input voltage		0	VDD	V
V_O	Output voltage		0	VDD	V
I_O	Output current for one terminal			2/4/8(Note 1)	mA
T_{opr}	Operating temperature	CMOS input	−20	75	℃
C_L	Output load capacity			50 (Note 2)	pF
tr, tf	Input rise and fall time	Normal input		500	ns
		Schmitt input		5	sec

Note 1. Rating per I_{OL} for each output buffer
2. IC pin capacity (8pF) excluded

ELECTRICAL CHARACTERIS (T_a=−20~75℃, V_{SS}=0 V, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings			Unit
				Min.	Typ.	Max.	
V_{IH}	Input voltage (CMOS interface)	H level	V_{DD}=5.5V	3.85		5.5	V
V_{IL}		L level	V_{DD}=4.5V	0		1.35	
V_{T+}	Schmitt input voltage (CMOS interface)	Normal direction	V_{DD}=5.0V	2.30		3.70	V
V_{T-}		Reverse direction		0.85		2.50	
V_H		Hysteresis		0.50		1.60	
V_{OH}	Output voltage	H level	V_{DD}=5.0V $\lvert I_O\rvert$<1 μA	4.95			V
V_{OL}		L level				0.05	
I_{OH}	Output current	H level	V_{DD}=4.5V V_{OH}=4.1V			−6(Note 1)	mA
						−3(Note 2)	
						−2(Note 3)	
I_{OL}		L level	V_{DD}=4.5V V_{OH}=0.4V	8(Note 1)			
				4(Note 2)			
				2(Note 3)			
I_{IH}	Input current	H level	V_{DD}=5.0V, V_I=5.5V	−1		1	μA
I_{IL}		L level	V_{DD}=5.0V, V_I=0V	−1		1	
I_{OZH}	Output leak current (note 4)	H level	V_{DD}=5.0V, V_O=5.5V	−1		1	μA
I_{OZL}		L level	V_{DD}=5.0V, V_O=0V	−1		1	
R_U	Pull up resistance		V_{DD}=5.0V, V_I=0V	10		120	kΩ
R_D	Pull down resistance		V_{DD}=5.0V, V_I=5.5V	10		120	kΩ
C_I	Terminal capacitance (note 5)	Input	f=1MHz V_{DD}=0V		8	12	pF
C_O		Output			8	12	
C_{IO}		I/O			8	12	
I_{DD}	Supply Current		V_I=V_{SS}, V_{DD} I_O=0 μA (Note 6)			1	mA

Note 1. Rating for buffer for which I_{OL}=8mA
2. Rating for buffer for which I_{OL}=4mA
3. Rating for buffer for which I_{OL}=2mA
4. Only for tristate or open drain output terminal
5. Rating for one buffer
6. Current resulting from pull up or pull down resistance excluded

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

Timing requirements are shown in Table 1, switching characteristics in Table 2, and timing charts in Fig.1-1~1-4.

Table 1. TIMING REQUIREMENTS (T_a=−20~75℃, V_{DD}=5V±10%, unless other wise noted)

Symbol	Parameter	Limits		Unit	Timing
		Min.	Typ.		
twck	CLK cycle time	50	500	ns	Fig.1-1
tw(CLKH)	CLK"H" pulse width	20		ns	
tw(CLKL)	CLK"L" pulse width	20		ns	
tsu(LSYNCL-CLK)	LSYNCL"L" - CLK setup time	15		ns	
th(CLK-LSYNCL)	CLK - LSYNCL"L" hold time	10		ns	
tsu(DEN-CLK)	DEN - CLK setup time	10		ns	
th(CLK-DEN)	CLK - DEN hold time	5		ns	
tw(WRL)	WR"L" pulse width	15		ns	Fig.1-2
tsu(AD-WRL)	AD - WR"L" setup time	10		ns	
th(WRH-AD)	WR"H" - AD hold time	5		ns	
tsu(CS-WRL)	CS - WR"L" setup time	10		ns	
th(WRH-CS)	WR"H" - CS hold time	5		ns	
tsu(DI-WR)	DI - WR setup time	10		ns	
th(WR-DI)	WR - DI hold time	5		ns	
tw(RDL)	RD"L" pulse width	15		ns	
tsu(AD-RDL)	AD - RD"L" setup time	10		ns	
th(RDH-AD)	RD"H" - AD hold time	5		ns	
tsu(CS-RDL)	CS - RD"L" setup time	10		ns	
th(RDH-CS)	RD"H" - CS hold time	5		ns	
tc	WR/RD cycle time	90		ns	
tsu(DQ-CASH)	DQX(Y) - CAS"H" setup time	35		ns	Fig.1-3-b
th(CASH-DQ)	CAS"H" - DQX(Y) hold time	0		ns	

Table 2. SWITCHING CHARACTERISTICS (T_a = −20~75℃, V_{DD} = 5V ± 10%, C_L = 50pF, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit	Timing
			Min.	Typ.		
td(CLK-FIFOL)	CLK - FIFOENABL fall output propagation time	C_L = 10~70pF (Note)	5	25	ns	Fig.1-1
td(CLK-FIFOH)	CLK - FIFOENABL rise output propagation time	C_L = 10~70pF (Note)	5	25	ns	
td(CLK-RSTL)	CLK - RSTEN/RSTDE fall output propagation time		5	25	ns	
td(CLK-RSTH)	CLK - RSTEN/RSTDE rise output propagation time		5	25	ns	
td(LSYNCL-POUTL)	LSYNC"L" - PSYNCOUT fall output propagation time	C_L = 30pF	3	20	ns	
td(CLK-DDE)	CLK - DDE output propagation time	C_L = 40pF	5	25	ns	
td(RDL-DO)	RD"L" - data output enable time		3	25	ns	Fig.1-2
td(RDH-DO)	RD"H" - data output disenable time		3	25	ns	
td(CLK-WL)	CLK - W fall output propagation time		5	25	ns	Fig.1-3 -a, -b
td(CLK-WH)	CLK - W rise output propagation time		5	30	ns	
td(CLK-RASL)	CLK - RAS fall output propagation time		5	35	ns	
td(CLK-RASH)	CLK - RAS rise output propagation time		5	40	ns	
td(CLK-CASL)	CLK - CAS fall output propagation time		5	35	ns	
td(CLK-CASH)	CLK - CAS rise output propagation time		5	40	ns	
td(CLK-AD0)	CLK - AD0 output enable time		5	35	ns	
td(CLK-AD1)	CLK - AD1 output enable time		5	35	ns	
td(CASH-AD2)	CLK - AD2 output enable time		5	35	ns	
td(CASH-AD3)	CLK - AD3 output enable time		5	35	ns	
td(CASH-DQ)	CAS"H" - DQ(X) output enable time	C_L = 20pF	0	10	ns	
td(CLK-ACKL)	CLK - DMAACK fall output propagation time		3	30	ns	
td(CLK-DRAMZ)	CLK - DRAMOUT output disenable time		5	25	ns	
td(RQH-ACKH)	DMARQ"H" - DMAACK rise output propagation time		3	20	ns	
td(CLK-DRAMX)	CLK - DRAMOUT output enable time		5	25	ns	
td(CLK-RCASL)	CLK - Refresh CAS fall output propagation time		5	25	ns	Fig.1-4
td(CLK-RCASH)	CLK - Refresh CAS rise output propagation time		5	25	ns	
td(CLK-RRASL)	CLK - Refresh RAS fall output propagation time		5	25	ns	
td(CLK-RRASH)	CLK - Refresh RAS rise output propagation time		5	25	ns	

Note. Measurement for FIFO enable signals are conducted with different external load capacities.

RSTEN	40pF
RSTDE	40pF
WEEN1, 2, 3	10pF
COPYEN	70pF
REEN12	20pF
REEN34	20pF
WEDE1, 2, 3, 4	10pF
COPYDE	70pF
REDE1, 2, 3	10pF

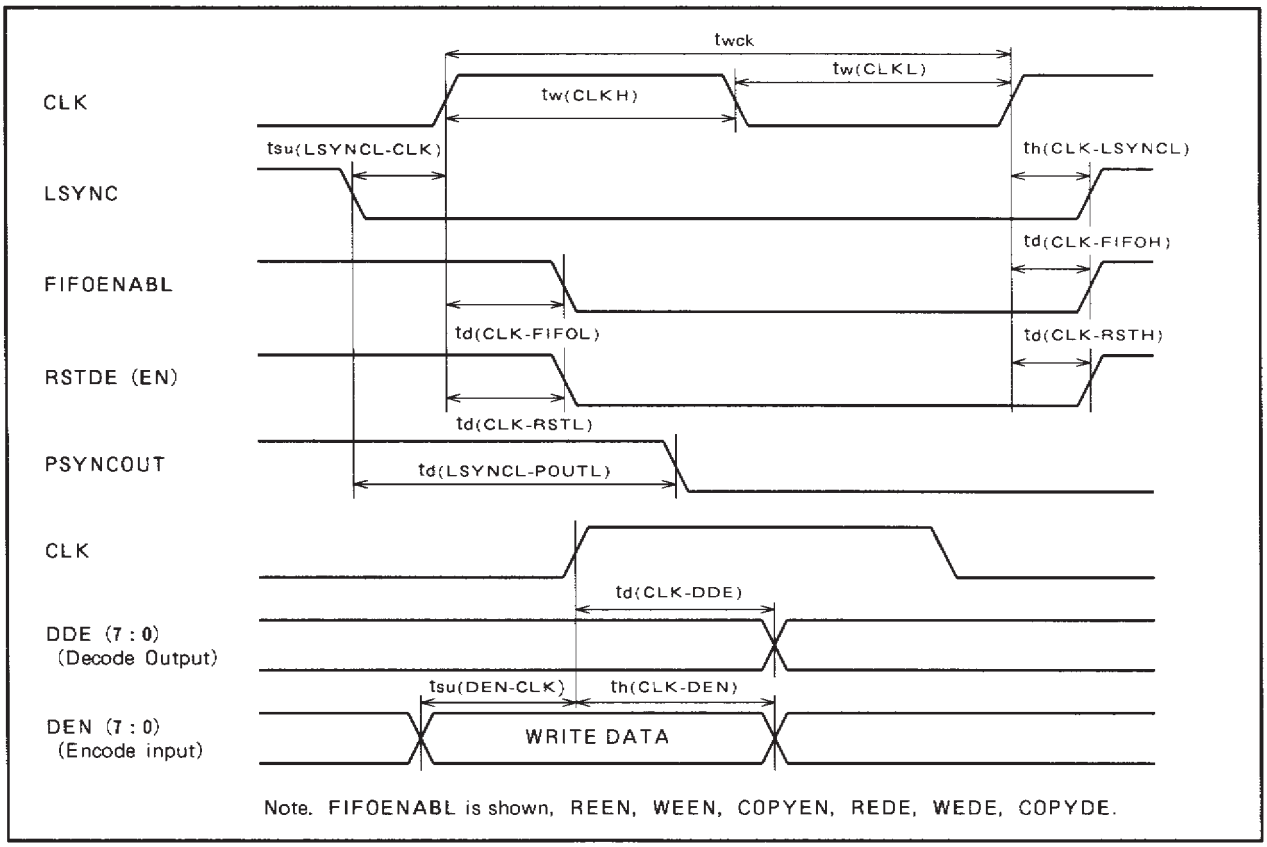


Fig.1-1 System - related Timing

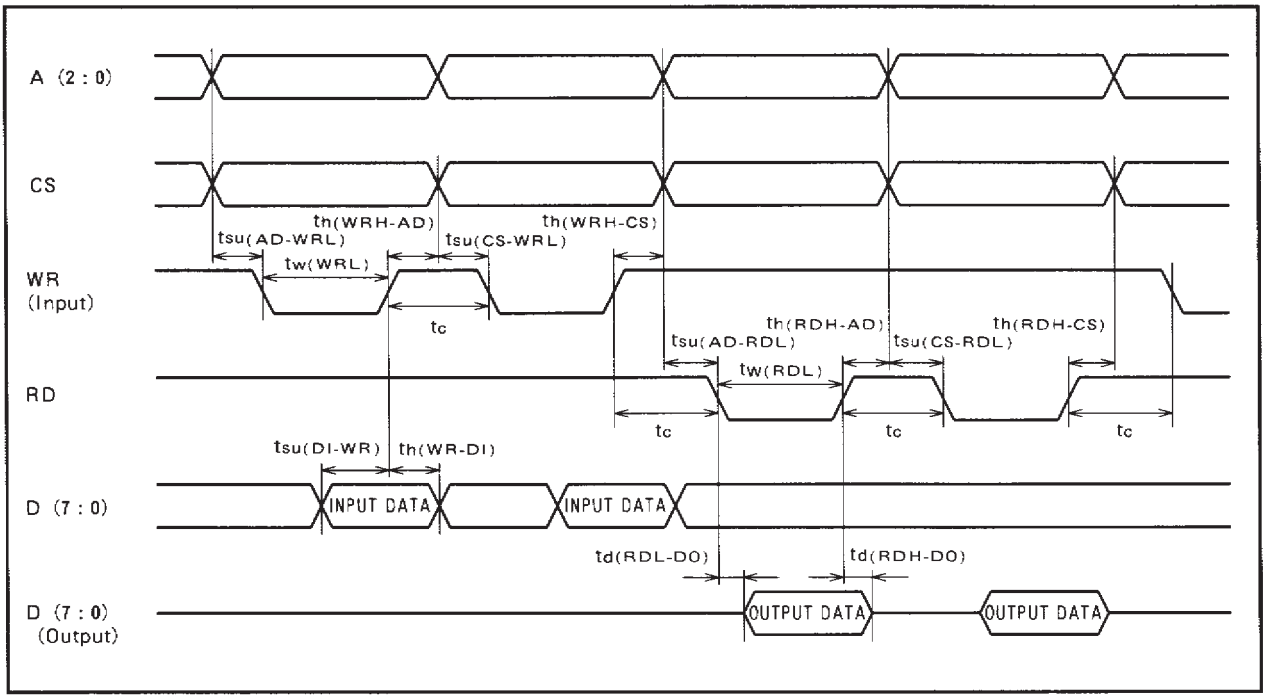


Fig.2-2 CPU Write and Read Timing

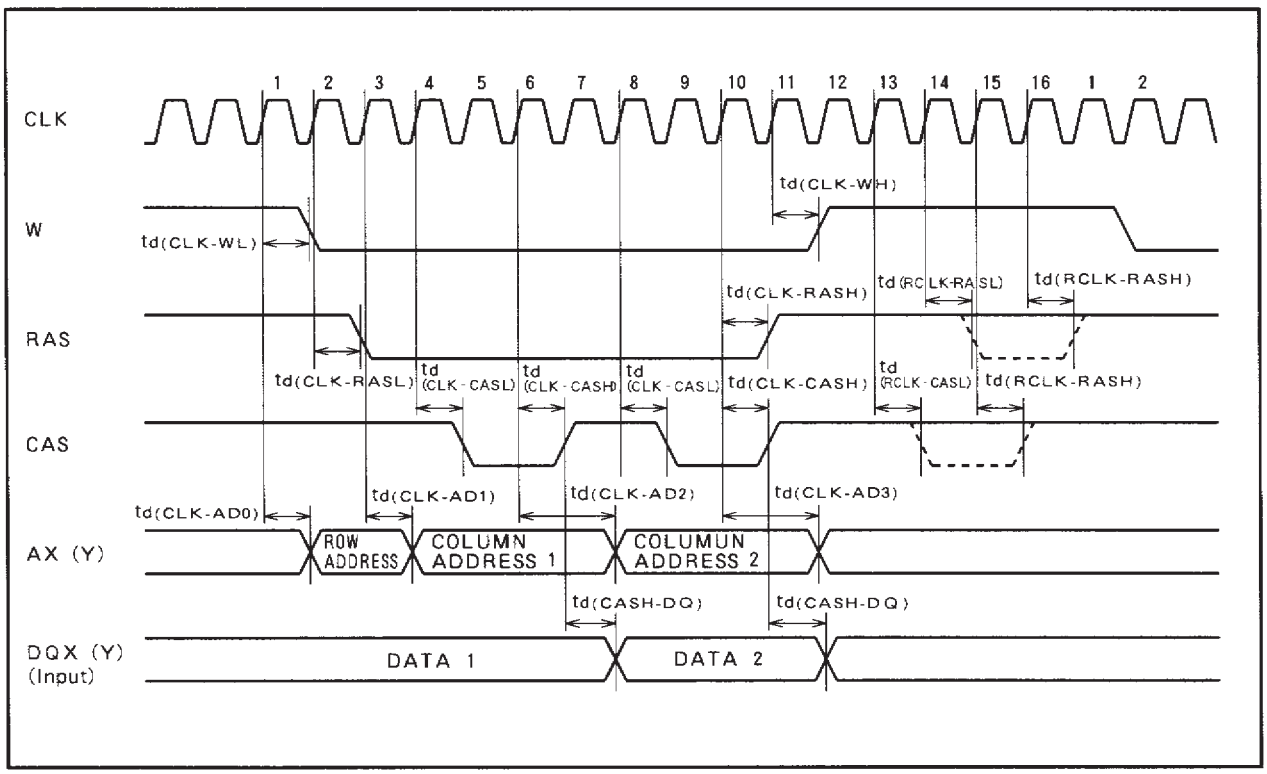


Fig.1-3-a DRAM Writing Timing

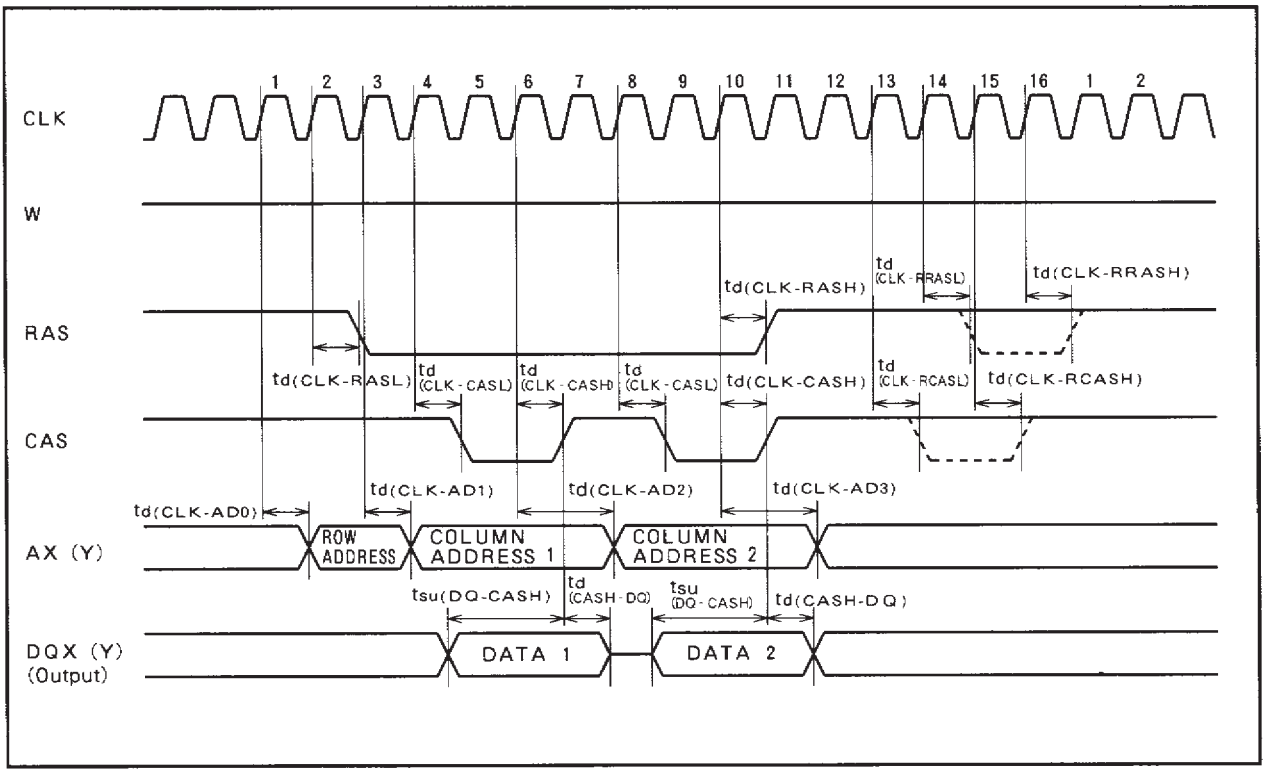


Fig.1-3-b DRAM Read Timing

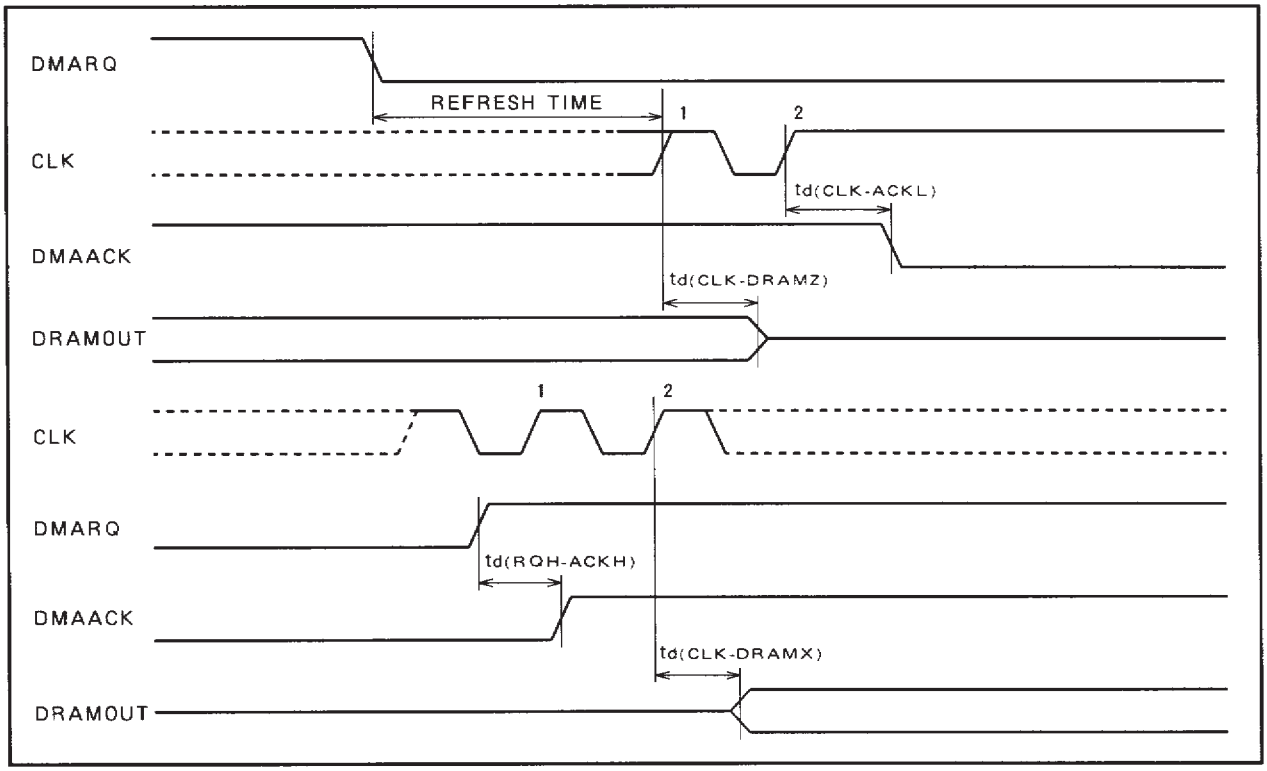


Fig.1-4 DRAMRQ, DRAMACK and DRAM Output Timing

INTERNAL REGISTER CONSTITUTION

Register Name	A2	A1	A0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	FUNCTION
LRR	L	L	L	L	L	H	Data read from internal counter
	L	L	L	L	H	↑	Data write to internal counter
EDR	L	L	H	L	L	H	Data read from edit mode
	L	L	H	L	H	↑	Data write to edit mode
MSLR	L	H	L	L	L	H	Data read from main sweep size register (Low grade)
	L	H	L	L	H	↑	Data write to main sweep size register (Low grade)
MSHR	L	H	H	L	L	H	Data read from main sweep size register (High grade)
	L	H	H	L	H	↑	Data write to main sweep size register (High grade)
SSLR	H	L	L	L	L	H	Data read from sub sweep size register (Low grade)
	H	L	L	L	H	↑	Data write to sub sweep size register (Low grade)
SSHR	H	L	H	L	L	H	Data read from sub sweep size register (High grade)
	H	L	H	L	H	↑	Data write to sub sweep size register (High grade)
CSR	H	H	L	L	L	H	Command status read
	H	H	L	L	H	↑	Command data write
reserve	H	H	H	–	–	–	Non-use
	H	H	H	–	–	–	Non-use

Note. Some bits are fixed access mode in the register.
※Don't access to reserve register.

COUNTER SET REGISTER (LRR)

LRR is the register that controls the valid data idling time from the signal-LSYNC and the refresh time for DRAM.

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
–	REF		LGATE				
R	R/W		R/W				
0	1	1	0	0	0	1	0

• LGATE

This LGATE controls the image data idling time from the rising edge of signal - LSYNC.

Set value is 2 to 31 clocks. The data under 2 is set to 2 .

The first image data is stored to FIFO with the rising edge of LGATE + 1 clock.

※Hardware timing adjustment should be done by this value.

• REF REFRESH

This REF controls the DRAM refresh timer.

00 ×16
01 ×64
10 ×128
11 ×256

Condition : 2048 times/32 msec.

※LRR register should be set after the hardware reset. If you change this value under operation, the operation is not assure.

※HOW TO READ THE REGISTER TABLE

MSB LSB

D7	D6	D5	D5	D3	D2	D1	D0	
								← Bit number
								← Field
								← Access Condition of MPU
								← Initial value

- "-" bit in the field shows non-use.
- "R" shows read and "R/W" shows read and write in the access condition.
- Initial value shows the value after the hardware reset. Non-use bit value is "0".

EDITING REGISTER (EDR)

This EDR controls the edit mode and the area in N in 1 mode.

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
NIN1		EDMODE					
R/W							
0	0	0	0	0	0	0	0

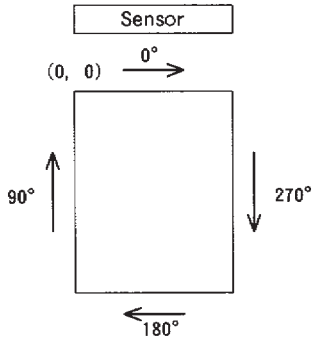
• EDMODE (Edit mode)

This register controls edit mode. The import for each bit is as follows.

D5 D4 D3 D2 D1 D0

- Rotation mode designation
  - 00 No rotation
  - 01 90° rotation
  - 10 180° rotation
  - 11 270° rotation
- Mirror designation (0 : No, 1 : Yes)
- Paper size designation (0 : A4, 1 : A3)
- N in 1 mode designation
  - 00 Normal
  - 01 2 in 1
  - 10 4 in 1

〈Definition of rotation〉



※The assured operation combinations and error combinati on are as follows.
Combinations except for the following table are not error but operation is not assure.

〈ASSURED OPERATION〉						〈ERROR〉	
D5	D4	D3	D2	D1	D0	D5	D4
0	0	0	0	0	0	1	1
0	0	0	0	0	1		
0	0	0	0	1	0		
0	0	0	0	1	1		
0	0	0	1	×	×		
0	0	1	0	×	0		
0	0	1	1	×	0		
0	1	0	×	×	×		
0	1	1	×	×	1		
1	0	0	×	×	×		
1	0	1	×	×	0		

×:Don't care

※The change of edit mode is not accepted under encoding or decoding.

• NIN1 (N in 1 area designation)

This N in 1 designates the encode data writing area under N in 1 mode.

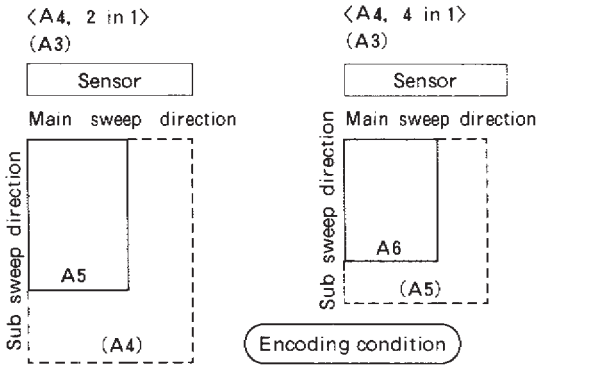
The import for each bit is as follows .

※Following table shows error combinations.

D7	D6	
0	0	Area①
0	1	Area②
1	0	Area③
1	1	Area④

D7	D6	D5	D4
1	0	0	1
1	1	0	1
0	1	0	0
1	0	0	0
1	1	0	0

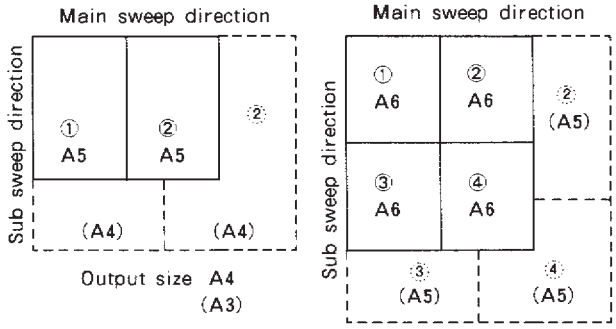
※Encoding condition (paper set direction) and the positional relation for the paper in each area are as follows.



Encoding condition

(Paper set direction)

※Size for main and sub sweep under N in 1 mode should be set the size after reduction.



Decoding condition

(In the case of no rotation)

※Size for main and sub sweep of decoding under N in 1 mode is the same as encoding.

※If you don't designate N in 1 mode, writing operation to N in 1 bit is invalid.

MAIN SWEEP SIZE REGISTER - LOW GRADE (MSLR)

This register designates the main sweep size (Lower 8 bits).

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
MSIZEL							
R/W							
1	1	0	0	0	0	0	0

- MSIZEL (Main sweep size - lower 8 bits)

※The access mode for lower 2 bits (D1, D0) are "R/W", but value is always "0".

MAIN SWEEP SIZE REGISTER - HIGH GRADE (MSHR)

This register designates the main sweep size (higher 5 bits) and monitor the N in 1 mode and the memory bank using status.

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
RAMY	RAMX	NBSY	MSIZEH				
R			R/W				
0	0	0	1	0	0	1	0

- MSIZEH (Main sweep size - higher 5 bits)
- NBSY (N in 1 BUSY)

This bit shows N in 1 operation.

0 The N-th paper encode finish or normal mode.

1 The first page encode finish and the N-th page encoding.

※NBSY is cleared by the change of EDMODE in EDR.

- RAMX (RAM bank X use)

0 Decode finish or encoding

1 Encode finish

- RAMY (RAM bank Y use)

0 Decode finish or encoding

1 Encode finish

SUB SWEEP SIZE REGISTER - LOW GRADE (SSLR)

This register designates the sub sweep size (Lower 8 bits).

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
SSIZEL							
R/W							
0	1	0	0	1	0	0	0

- SSIZEL (Sub sweep size - lower 8 bits)

※The access mode for lower 2 bits (D1, D0) are "R/W", but value is always "0".

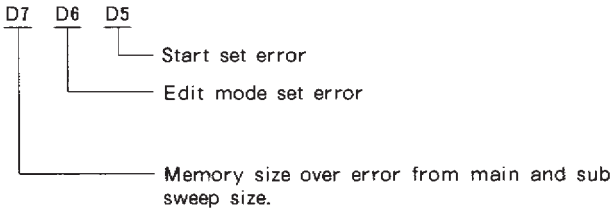
SUB SWEEP SIZE REGISTER - HIGH GRADE (SSHR)

This register designates the sub sweep size (high 5 bits).

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
SERR			SSIZEH				
R			R/W				
0	0	0	0	1	1	0	1

- SSIZEH (Sub sweep size - higher 5 bits)
- SERR (Error information bits for setting)



COMMAND STATUS RESISTER (CSR)

This resister designates the operation command and reads the status.

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
READY	ERR			DECSY	DECSX	ENCSY	ENCSX
R				R/W			
0	0	0	0	0	0	0	0

- ENCSX (X bank encode start)

This bit controls the encode start to RAM bank X.

- ENCSY (Y bank encode start)

This bit controls the encode start to RAM bank Y.

- DECSX (X bank decode start)

This bit controls the decode start to RAM bank X.

- DECSY (Y bank decode start)

This bit controls the decode start to RAM bank Y.

※Above 4 bits (D3, D2, D1, D0) should be set to "1" when the hardware starts. And they becomes "1" under operation.

Writing "0" to them doesn't influence the operation. The combinations for above 4 bits are as follows. Combinations except for following table are error.

A3mode

D3	D2	D1	D0
0	0	1	1
1	1	0	0

Under line portion should be set at the same time.

A4mode

D3	D2	D1	D0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	①	①	0
①	0	0	①

- READY (Start ready for encode)

This bit shows enable status for encode start. It is cleared by "L" of PSYNCIN.

※The signal - PSYNCIN should be active after the ready bit becomes"1". Detail is described in the operation sequence.

- ERR (Error information)

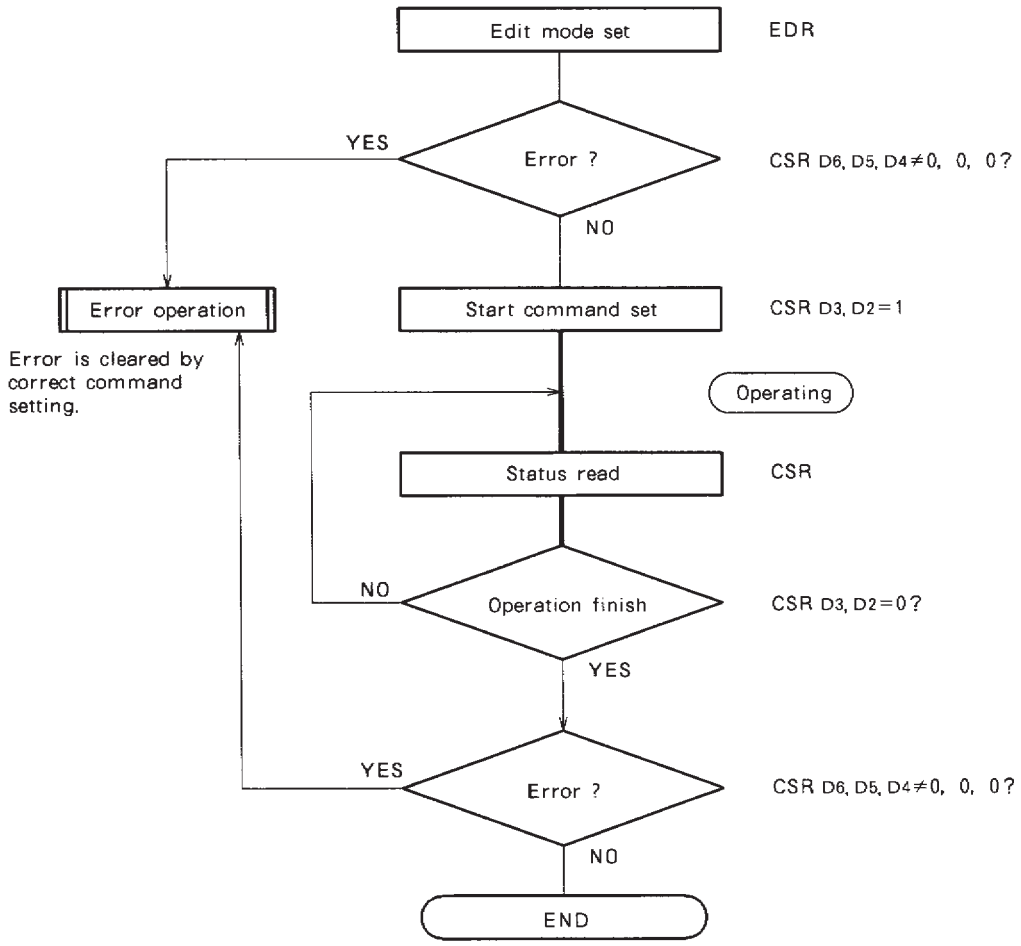
This ERR shows error information when the command is set or the hardware is operating.

D6 D5 D4

- D4 — Error in encoding
- D5 — Error in decoding
- D6 — Setting error (Detail informations are showed in SSHR-D5, D6, D7).

DECODE OPERATION SEQUENCE

Compressed data is stored in the memory.



ENCODE OPERATION SEQUENCE