M66007P/FP

12-BIT INPUT EXPANDER

DESCRIPTION

The M66007 is a semiconductor integrated circuit providing the 12-bit parallel input-serial output shift register function.
This product is completely designed with CMOS to sharply reduce power consumption compared with bipolar or Bi-CMOS product.
The M66007, developed as an input only expander IC necessary for microcomputer periphery, is widely applicable as a data parallel/serial conversion IC.

FEATURES

- Control signals of only two pins including LE/D and $\overline{CLK}$
- Low power consumption of 50 µW/package maximum (Vcc=5V, Ta=25°C at time of standstill)
- Schmitt triggered input (LE/D, $\overline{CLK}$, D0 to D11)
- Wide operating supply voltage range (Vcc=2~6V)
- Wide operating temperature range (Ta=–20~75°C)

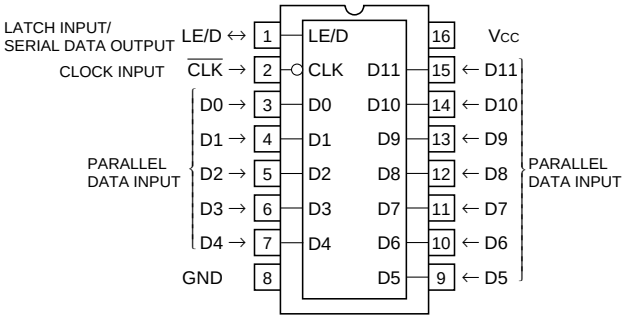
APPLICATION

Parallel/serial data conversion for microcomputer periphery

FUNCTION

The M66007 uses a silicon gate CMOS process to achieve low power consumption and high noise margin.
For control signals, this IC adopts only the two pins of latch input/serial data output LE/D and clock input $\overline{CLK}$. Each bit of shift register of 12-bit parallel input-serial output consists of flip-flop for shift.
When LE/D is placed in input mode, $\overline{CLK}$ is set to "H" and LE/D changes from "H" to "L", the status of parallel data inputs D0 to D11 at that time is latched with the flip-flop for shift and LE/D is switched to output mode to output "L".

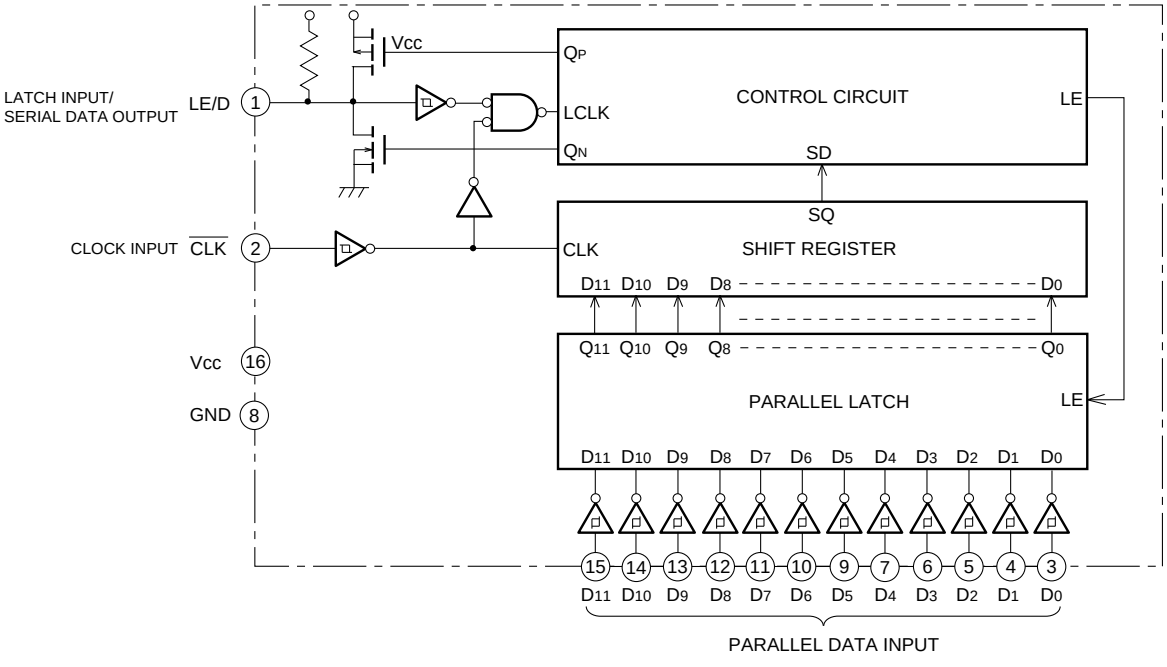
PIN CONFIGURATION (TOP VIEW)



Outline 16P4
16P2N-A

After this, change of $\overline{CLK}$ from "H" to "L" makes the shift register perform shift operation and LE/D outputs the contents of the shift register from D0 in order.
In addition, the shift operation for up to the 12th bit is carried out and then LE/D is switched to the input mode at the falling edge of $\overline{CLK}$ of the 13th bit.
When power is turned on, the input/output mode of LE/D is indeterminate. However, detection of 13 or more falling edges of $\overline{CLK}$ sets LE/D in the input mode.

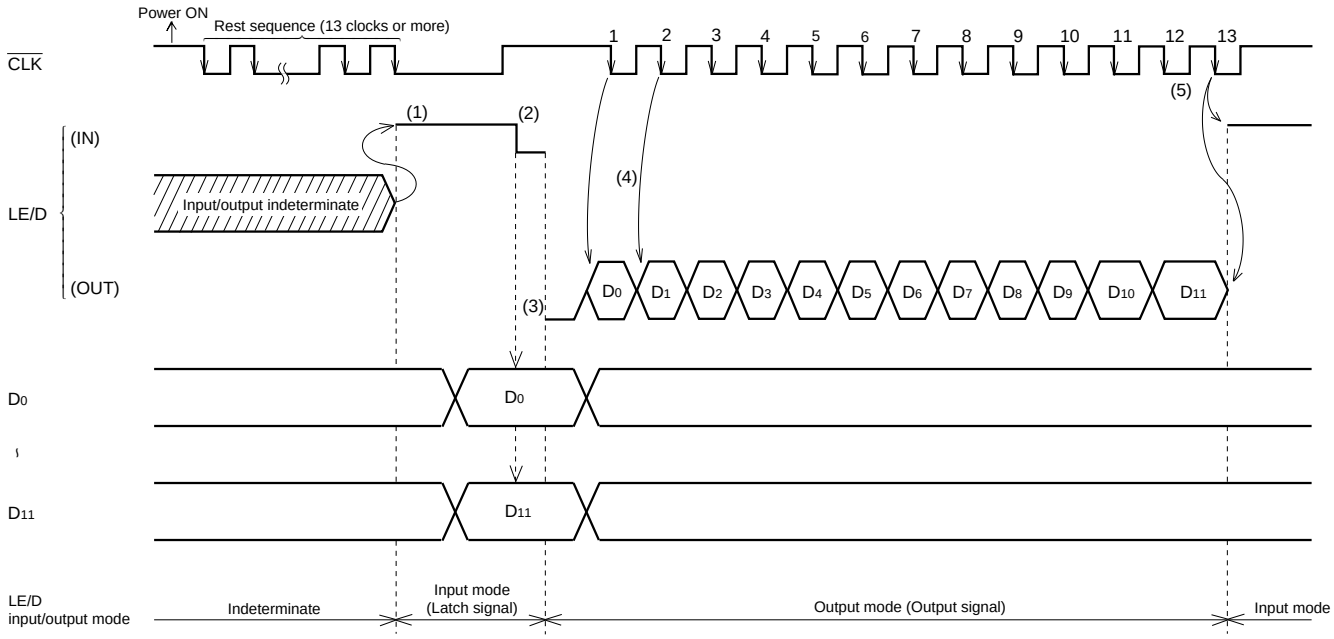
BLOCK DIAGRAM



DESCRIPTION OF OPERATION

(1) When power is turned on, LE/D is placed in input/output indeterminate mode. However, detection of 13 or more of falling edges of $\overline{CLK}$ sets LE/D in input mode.
(2) When LE/D is placed in input mode, and $\overline{CLK}$ is set to "H", access starts at a falling edge of LE/D and the status of D_0 to D_{11} is latched.
(3) In addition, LE/D switches from input mode to output mode and then outputs "L".
(4) At a falling edge of $\overline{CLK}$ from "H" to "L", data latched in step (2) is shifted sequentially and is then output from LE/D in order of D_0 to D_{11}.
(5) After the output of 12-bit data of D_0 to D_{11}, LE/D is switched to input mode at the 13th falling edge of $\overline{CLK}$ to wait for next access. Keep the LE/D pin set to "H" until the next access starts.

OPERATION TIMING CHART



ABSOLUTE MAXIMUM RATINGS (Ta = 20 ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
I_{IK}	Input protection diode current	V_I<0V	–20	mA
		V_I>V_{CC}	20	
I_{OK}	Output incidental diode current	V_O<0V	–20	mA
		V_O>V_{CC}	20	
I_{CC}	Power/GND	V_{CC}, GND	±20	mA
T_{stg}	Storage temperature		–60 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	–20		75	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 2 ~ 6V unless otherwise noted)

Symbol	Parameter	Conditions		Limits					Unit
				T_a=25°C			T_a= –20~75°C		
				Min.	Typ.	Max.	Min.	Max.	
V_{T+}	Threshold voltage in positive direction	V_O=0.1V, V_{CC}–0.1V, I_O=20µA		0.35 × V_{CC}		0.8 × V_{CC}	0.35 × V_{CC}	0.8 × V_{CC}	V
$V_{T–}$	Threshold voltage in negative direction	V_O=0.1V, V_{CC}–0.1V, I_O=20µA		0.2 × V_{CC}		0.65 × V_{CC}	0.2 × V_{CC}	0.65 × V_{CC}	V
V_{OL}	Low-level output voltage	V_I=V_{T+}, $V_{T–}$ V_{CC}=4.5V	I_{OL}=20µA			0.1		0.1	V
			I_{OL}=1mA			0.4		0.5	
V_{OH}	High-level output voltage	V_I=V_{T+}, $V_{T–}$ V_{CC}=4.5V	I_{OH}=–20µA	4.4			4.4		V
			I_{OH}=–1mA	4.1			4.0		
I_O	Maximum output leak current	V_I=V_{T+}, $V_{T–}$ V_{CC}=6V	V_O=V_{CC}			1.0		10.0	µA
			V_O=GND			–0.8		–1.2	mA
I_{CC}	Static consumption current	V_I=V_{CC}, GND, V_{CC}=6V, LE/D="H"				10.0		100.0	µA
		V_I=V_{CC}, GND, V_{CC}=6V, LE/D="L"				0.8		1.2	mA

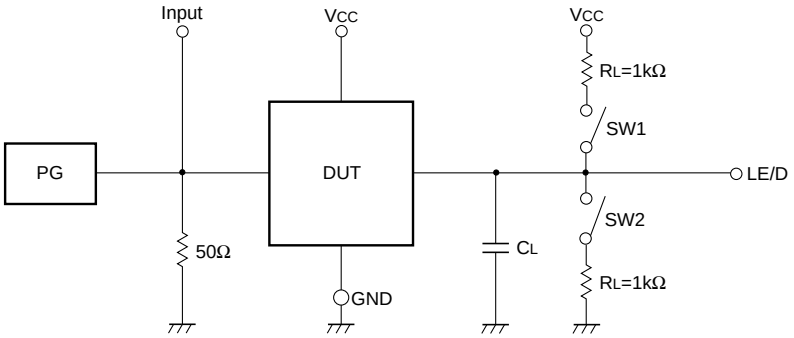
SWITCHING CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Conditions	Limits			Unit
			T_a = –20 ~ 75°C			
			Min.	Typ.	Max.	
f_{max}	Maximum repetition frequency	C_L=50pF (Note 1)	2			MHz
t_{PLH}	Output "L-H", "H-L" propagation time CLK-LE/D				400	ns
t_{PHL}					400	ns
t_{PLZ}	Output "L-Z", "H-Z" propagation time CLK-LE/D				400	ns
t_{PHZ}					400	ns

TIMING REQUIREMENTS (V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits			Unit
			T_a = –20 ~ 75˚C			
			Min.	Typ.	Max.	
t_w	CLK pulse width		250			ns
	LE/D pulse width (Input mode)		250			
t_{su}	CLK set up time for LE/D		100			ns
	D_0~D_{11} set up time for LE/D		100			
t_h	CLK hold time for LE/D		200			ns
	D_0~D_{11} hold time for LE/D		200			

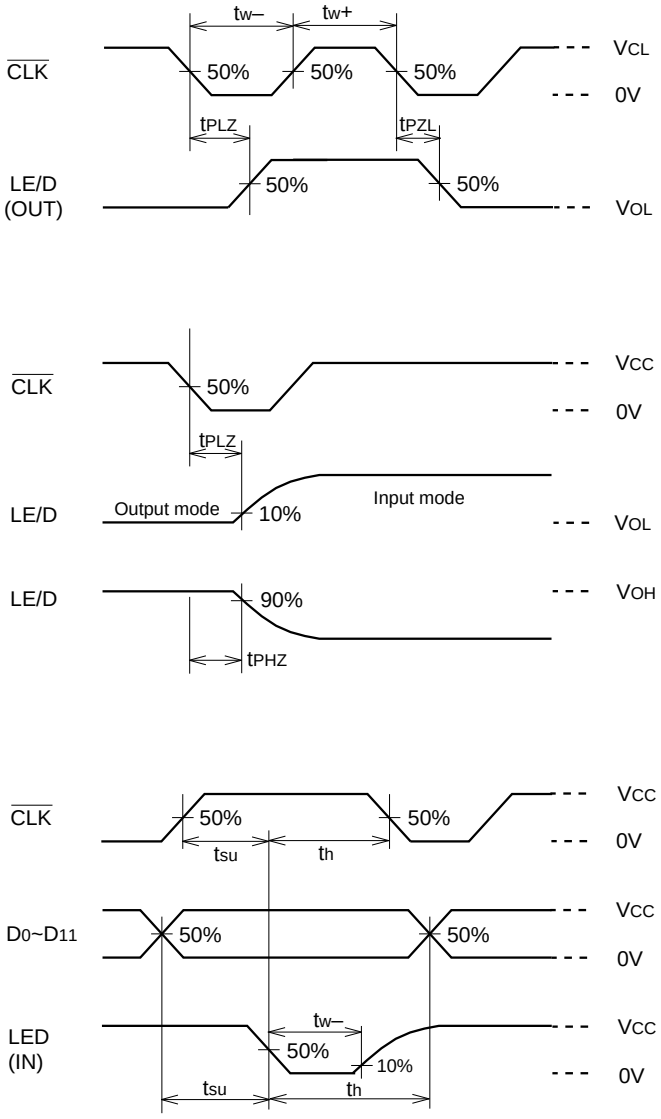
Note 1. Test Circuit



(1) Characteristics (10%~90%) of pulse generator (PG)
t_r = 6ns, t_f = 6ns
(2) Electrostatic capacitance C_L includes the floating capacitance of connection and probe input capacitance.

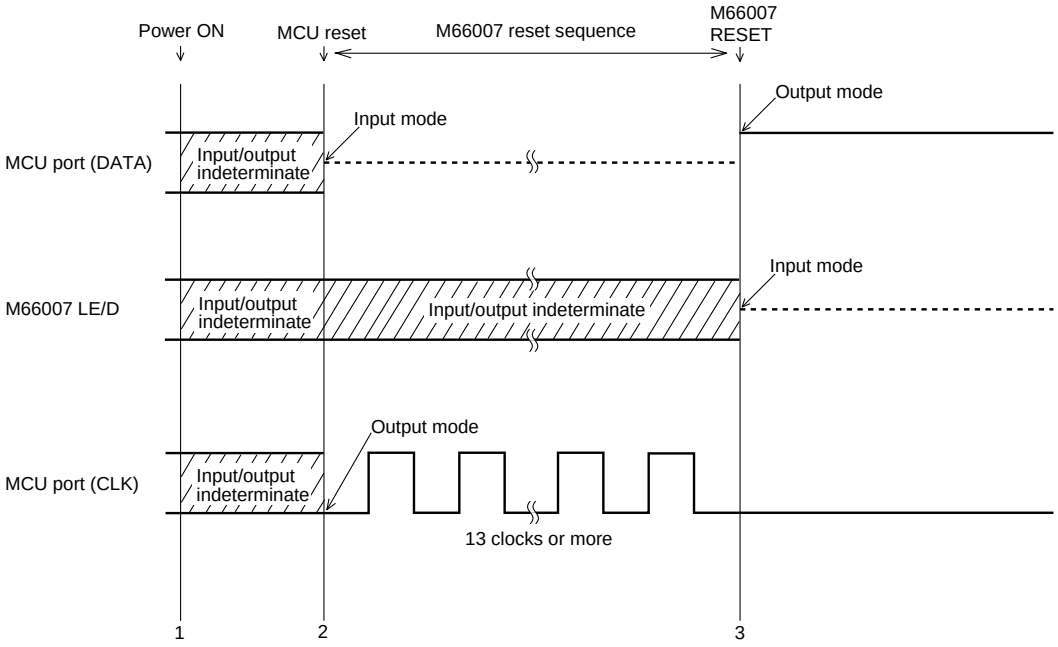
Item	SW1	SW2
t_{PLH}	Open	Open
t_{PHL}	Open	Open
t_{PLZ}	Close	Open
t_{PHZ}	Open	Close

TIMING DIAGRAM

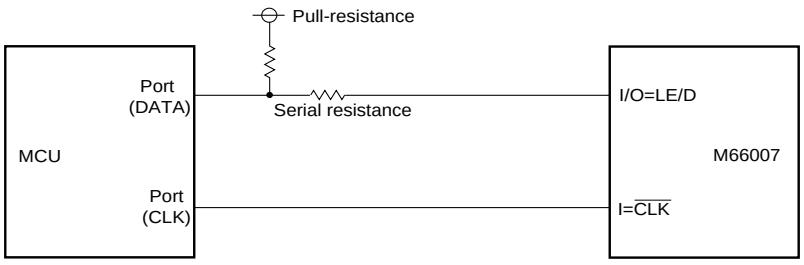


PRECAUTIONS FOR APPLICATION

1. The following timing diagram shows the status of MCU port and LE/D pin of the M66007 when power is turned on. When MCU has been reset to make the collision period of MCU and LE/D line of the M66007 as short as possible, place the port (LE/D) in input mode and execute the reset sequence through the port ($\overline{CLK}$) promptly to reset the M66007.
   As shown in the diagram, to prevent the IC from being broken due to collision of the LE/D line in the 1-2 section, set in the LE/D line in series a resistance of a degree to which the transmission speed cannot be affected.
2. When the LE/D pin on each of the MPU and M66007 sides switches from input mode to output mode or from output mode to input mode, the LE/D pin may be placed in high impedance status, resulting in oscillation.
   To prevent malfunction due to this oscillation, pull up the LE/D line with a high resistance of a degree to which V_{OH} and V_{OL} levels cannot be affected. (with approx. 20kΩ pull-up resistance built-in)



Status of MCU and M66007 with Power Turned on



Connection Example of MCU and M66007