

**DESCRIPTION**

The M66008 is a semiconductor integrated circuit providing the 16-bit serial input-parallel output and parallel input-serial output shift register function.

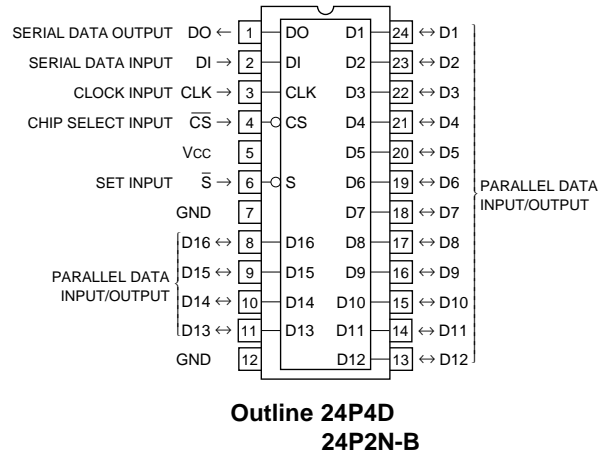
Independent built-in registers for serial input-parallel output and parallel input-serial output enable serial input data to be read into a shift register during output of serial data converted from parallel data. In addition, parallel data input/output pin can be placed in input or output mode in bits.

The M66008 is widely applicable to I/O port extension for MCU, data communication of serial bus system, etc.

**FEATURES**

- Two-way serial data communication with MCU
- Reading of serial data during parallel-serial data conversion
- Division of I/O bit in parallel data input/output
- Low power consumption of 50  $\mu$ W/package maximum  
 ( $V_{cc}=5V, T_a=25^\circ C$  at time of standstill)
- Schmitt triggered input (DI, CLK,  $\bar{S}$ ,  $\bar{CS}$ )
- Open drain output (DO, D1~D16)
- With parallel data input/output (D1~D16)
- Wide operating supply voltage range ( $V_{cc}=2\sim 6V$ )
- Wide operating temperature range ( $T_a=-20\sim 75^\circ C$ )

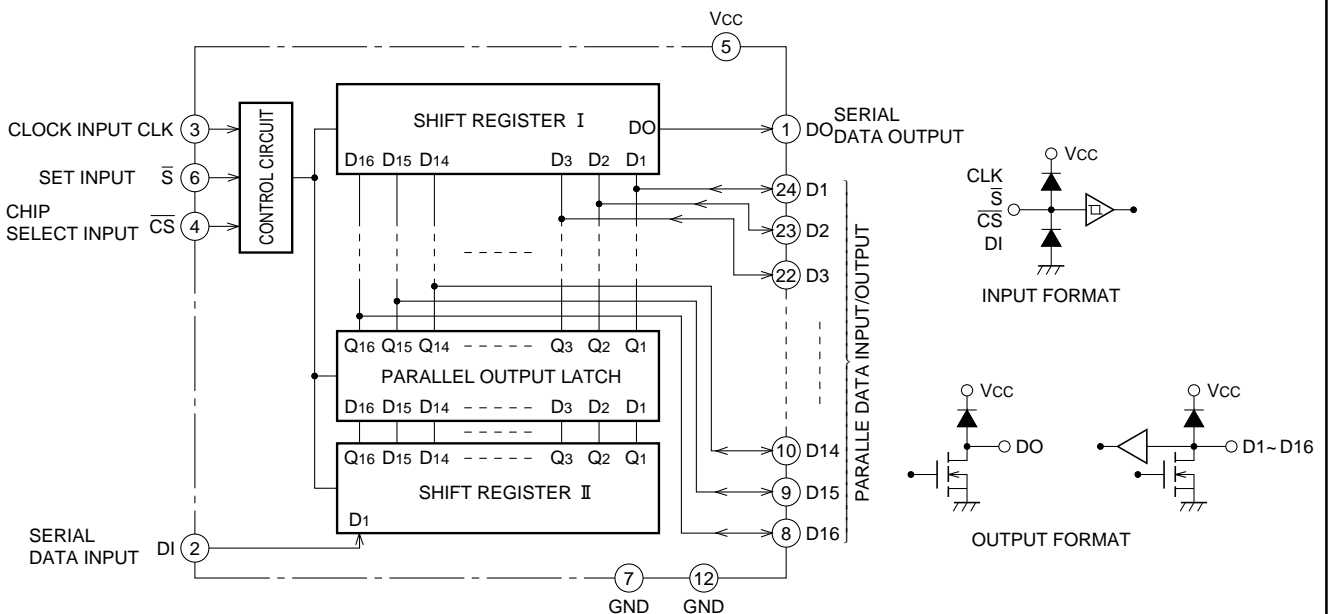
**PIN CONFIGURATION (TOP VIEW)**



**APPLICATION**

Parallel/serial data conversion for MCU periphery, serial bus control by parallel/serial data conversion MCU, etc.

**BLOCK DIAGRAM**



**FUNCTION**

The M66008 uses a silicon gate CMOS process to achieve low power consumption and high noise margin.

The M66008 independently forms a 16-bit serial input-parallel output shift register and a parallel input-serial output shift register to read serial input data during output of serial data converted from parallel data.

The operation for serial output of 16-bit parallel data and operation for reading serial data from MCU by changing  $\overline{CS}$  from "H" to "L". That is, at a falling edge of  $\overline{CS}$ , 16-bit parallel data is latched and serial data is output from the DO pin in synchronization with 16-bit parallel data at a falling edge of shift clock. In addition, serial data from MCU is read into an internal shift register via the DI pin at a rising edge of shift clock. The 17th bit shift clock and later clocks are ignored.

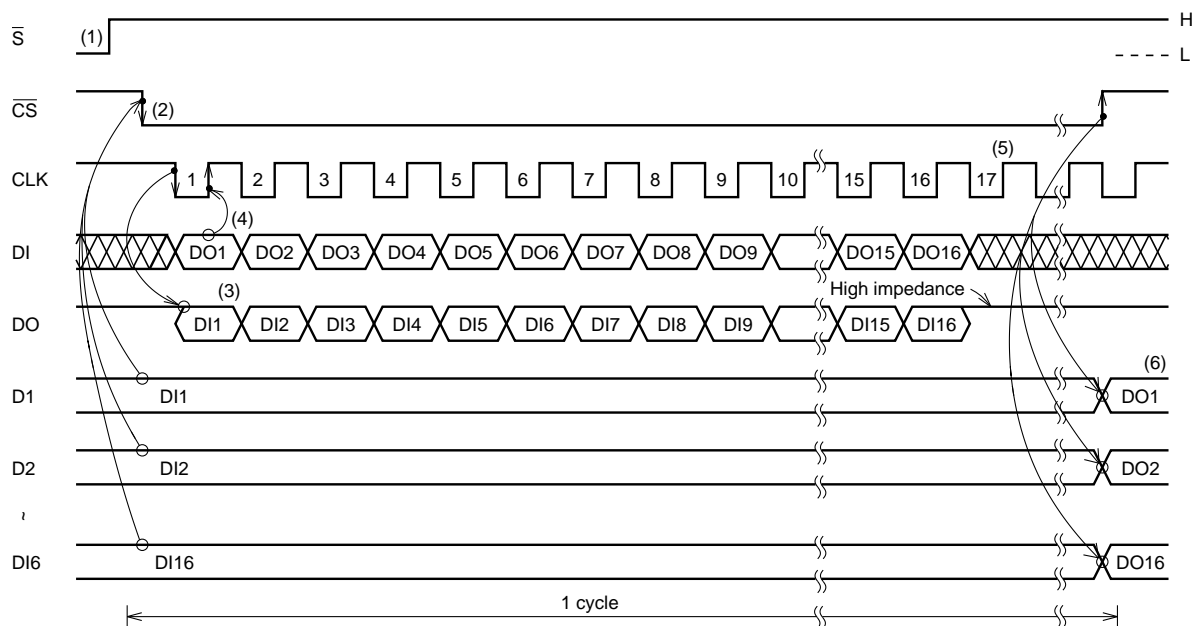
When the reading operation is masked, the DO pin is placed in high impedance status. When  $\overline{CS}$  changes from "L" to "H", 16-bit serial data read from the DI pin is output to pins D1 to D16 in parallel.

Since the output format of the parallel output pin is set to N-channel open drain output, write "H" data into a terminal placed in input mode.

**OPERATION DESCRIPTION**

- (1) When power is turned on, DO and D1–D16 are indeterminate. However, they are placed in high impedance status by setting  $\overline{S}$  to "L".
- (2) The status of D1 to D16 is loaded to shift register I at a falling edge of  $\overline{CS}$ .
- (3) At a falling edge of CLK, 16-bit serial output of the data loaded in step (2) is sequentially performed from DO.
- (4) At a rising edge of CLK, 16-bit serial data is written into shift register II from DI.
- (5) CLK of 17th bit and later is ignored and serial data cannot be written. DO is placed in high impedance status.
- (6) At a rising edge of  $\overline{CS}$ , data written in step (4) is output to D1 to D16.
- (7) Shift register I loads data to be applied externally and AND data having the latched content to parallel output latch.
- (8) When  $\overline{CS}$  is activated before arrival of CLK at the 16th bit, parallel output latch outputs to D1 to D16 by latching the data that has been written into shift register II. Shift registers I and II continues the shift operation until it arrives at the 16th bit of CLK and DO output serial data.
- (9) Serial data is used to control the operation for switching input/output mode of D1 to D16. The pin set to "H" operates as an input pin.

**OPERATION TIMING DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS** ( $T_a = -20 \sim 75^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.5 ~ +7	V
V <sub>I</sub>	Input voltage		-0.5 ~ V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage		-0.5 ~ V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input protection diode current	V <sub>I</sub> < 0V	-20	mA
		V <sub>I</sub> > V <sub>CC</sub>	20	
I <sub>OK</sub>	Output incidental diode current	V <sub>O</sub> < 0V	-20	mA
		V <sub>O</sub> > V <sub>CC</sub>	20	
I <sub>GND</sub>	Current/GND	GND	-64	mA
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>CC</sub>	Supply voltage	2		6	V
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	V
T <sub>opr</sub>	Operating temperature	-20		75	°C

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2 \sim 6\text{V}$  unless otherwise noted)

Symbol	Parameter	Conditions	Limits					Unit	
			T <sub>a</sub> =25°C			T <sub>a</sub> =-20~75°C			
			Min.	Typ.	Max.	Min.	Max.		
V <sub>T+</sub>	Threshold voltage in positive direction	V <sub>O</sub> =0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>  =20μA	CLK, $\overline{\text{CS}}$ S, DI	0.35 × V <sub>CC</sub>		0.8 × V <sub>CC</sub>	0.35 × V <sub>CC</sub>	0.8 × V <sub>CC</sub>	V
V <sub>T-</sub>	Threshold voltage in negative direction	V <sub>O</sub> =0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>  =20μA		0.2 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>	0.2 × V <sub>CC</sub>	0.65 × V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	V <sub>O</sub> =0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>  =20μA	D1~D16	0.75 × V <sub>CC</sub>			0.75 × V <sub>CC</sub>		V
V <sub>IL</sub>	Low-level input voltage	V <sub>O</sub> =0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>  =20μA				0.25 × V <sub>CC</sub>		0.25 × V <sub>CC</sub>	V
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> =V <sub>T+</sub> , V <sub>T-</sub> V <sub>CC</sub> =4.5V	I <sub>OL</sub> =3mA			0.4		0.5	V
I <sub>O</sub>	Maximum output leak current	V <sub>I</sub> =V <sub>T+</sub> , V <sub>T-</sub> V <sub>CC</sub> =6V	V <sub>O</sub> =V <sub>CC</sub>			1.0		10.0	μA
			V <sub>O</sub> =GND			-1.0		-10.0	μA
I <sub>IH</sub>	High-level input current	V <sub>I</sub> =V <sub>CC</sub>	V <sub>CC</sub> =6V			0.1		1.0	μA
I <sub>IL</sub>	Low level input current	V <sub>I</sub> =GND	V <sub>CC</sub> =6V			-0.1		-1.0	μA
I <sub>CC</sub>	Static consumption current	V <sub>I</sub> =V <sub>CC</sub> , GND	V <sub>CC</sub> =6V			10.0		100.0	μA

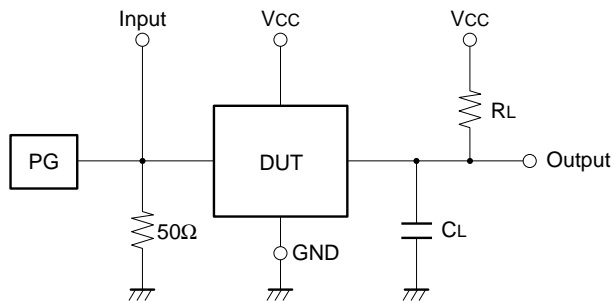
**SWITCHING CHARACTERISTICS** ( $V_{CC} = 5\text{V}$ )

Symbol	Parameter	Conditions	Limits					Unit
			T <sub>a</sub> =25°C			T <sub>a</sub> =-20~75°C		
			Min.	Typ.	Max.	Min.	Max.	
f <sub>max</sub>	Maximum repetition frequency	C <sub>L</sub> =50pF R <sub>L</sub> =1kΩ (Note 2)	2.5			1.9		MHz
t <sub>PLZ</sub>	Output "L-Z", "Z-L" propagation time				300		400	ns
t <sub>PZL</sub>	CLK-DO				300		400	ns
t <sub>PLZ</sub>	Output "L-Z", "Z-L" propagation time				300		400	ns
t <sub>PZL</sub>	CS-D1 to D16				300		400	ns
t <sub>PLZ</sub>	Output "L-Z" propagation time S-DO, D1 ~ D16				300		400	ns

**TIMING REQUIREMENTS** ( $V_{CC} = 5V$ )

Symbol	Parameter	Conditions	Limits					Unit
			$T_a=25^{\circ}C$			$T_a=-20\sim75^{\circ}C$		
			Min.	Typ.	Max.	Min.	Max.	
$t_w$	CLK, $\overline{CS}$ , $\overline{S}$ pulse width		200			260		ns
$t_{su}$	DI set up time for CLK		100			130		ns
	$\overline{CS}$ set up time for CLK		100			130		
	D1~D16 set up time for $\overline{CS}$		100			130		
$t_h$	DI hold time for CLK		100			130		ns
	$\overline{CS}$ hold time for CLK		100			130		
	D1~D16 hold time for $\overline{CS}$		100			130		
$t_{rec}$	$\overline{CS}$ recovery time for $\overline{S}$		100			130		ns

**Note 2: Test Circuit**



- (1) Characteristics (10%~90%) of pulse generator (PG)  
 $t_r=6ns, t_f=6ns$
- (2) Electrostatic capacitance  $C_L$  includes the floating capacitance of connection and probe input capacitance.

TIMING DIAGRAM

