M66008P/FP

16-BIT I/O EXPANDER

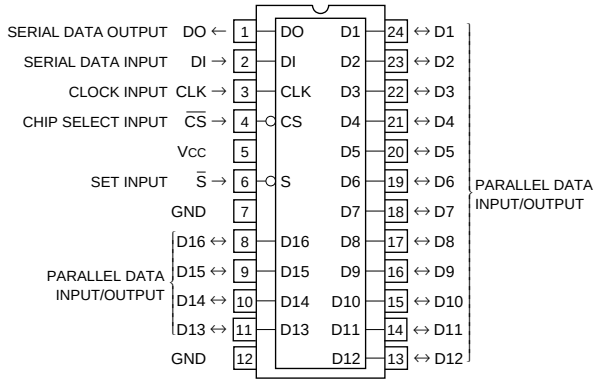
DESCRIPTION

The M66008 is a semiconductor integrated circuit providing the 16-bit serial input-parallel output and parallel input-serial output shift register function.
Independent built-in registers for serial input-parallel output and parallel input-serial output enable serial input data to be read into a shift register during output of serial data converted from parallel data. In addition, parallel data input/output pin can be placed in input or output mode in bits.
The M66008 is widely applicable to I/O port extension for MCU, data communication of serial bus system, etc.

FEATURES

- Two-way serial data communication with MCU
- Reading of serial data during parallel-serial data conversion
- Division of I/O bit in parallel data input/output
- Low power consumption of 50 µW/package maximum
  (Vcc=5V, Ta=25°C at time of standstill)
- Schmitt triggered input (DI, CLK, $\overline{S}$, $\overline{CS}$)
- Open drain output (DO, D1~D16)
- With parallel data input/output (D1~D16)
- Wide operating supply voltage range (Vcc=2~6V)
- Wide operating temperature range (Ta=–20~75°C)

PIN CONFIGURATION (TOP VIEW)

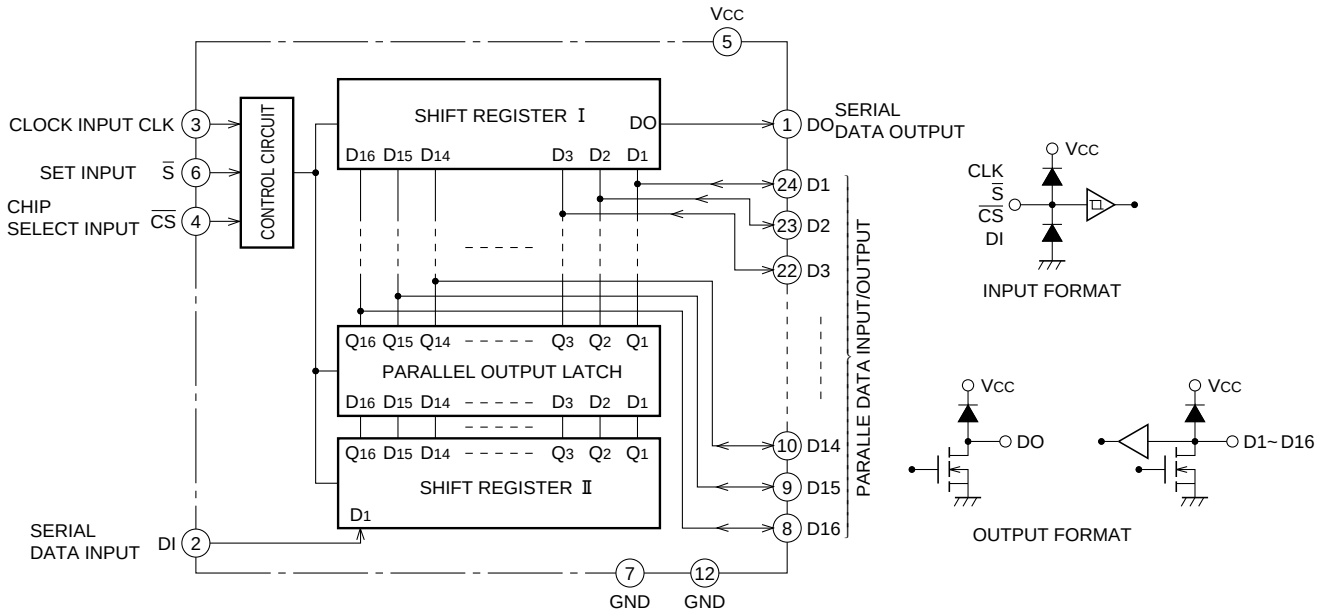


Outline 24P4D
24P2N-B

APPLICATION

Parallel/serial data conversion for MCU periphery, serial bus control by parallel/serial data conversion MCU, etc.

BLOCK DIAGRAM



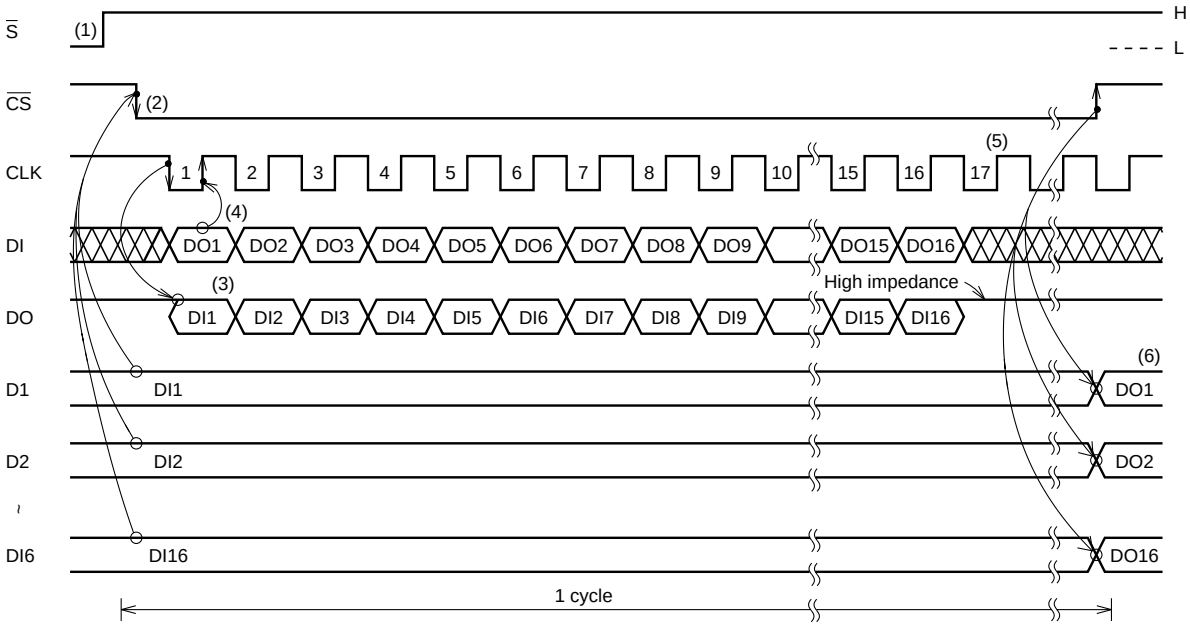
FUNCTION

The M66008 uses a silicon gate CMOS process to achieve low power consumption and high noise margin.
The M66008 independently forms a 16-bit serial input-parallel output shift register and a parallel input-serial output shift register to read serial input data during output of serial data converted from parallel data.
The operation for serial output of 16-bit parallel data and operation for reading serial data from MCU by changing $\overline{CS}$ from "H" to "L". That is, at a falling edge of $\overline{CS}$, 16-bit parallel data is latched and serial data is output from the DO pin in synchronization with 16-bit parallel data at a falling edge of shift clock. In addition, serial data from MCU is read into an internal shift register via the DI pin at a rising edge of shift clock. The 17th bit shift clock and later clocks are ignored.
When the reading operation is masked, the DO pin is placed in high impedance status. When $\overline{CS}$ changes from "L" to "H", 16-bit serial data read from the DI pin is output to pins D1 to D16 in parallel.
Since the output format of the parallel output pin is set to N-channel open drain output, write "H" data into a terminal placed in input mode.

OPERATION DESCRIPTION

(1) When power is turned on, DO and D1~D16 are indeterminate. However, they are placed in high impedance status by setting $\overline{S}$ to "L".
(2) The status of D1 to D16 is loaded to shift register Ⅰ at a falling edge of $\overline{CS}$.
(3) At a falling edge of CLK, 16-bit serial output of the data loaded in step (2) is sequentially performed from DO.
(4) At a rising edge of CLK, 16-bit serial data is written into shift register Ⅱ from DI.
(5) CLK of 17th bit and later is ignored and serial data cannot be written. DO is placed in high impedance status.
(6) At a rising edge of $\overline{CS}$, data written in step (4) is output to D1 to D16.
(7) Shift register Ⅰ loads data to be applied externally and AND data having the latched content to parallel output latch.
(8) When $\overline{CS}$ is activated before arrival of CLK at the 16th bit, parallel output latch outputs to D1 to D16 by latching the data that has been written into shift register Ⅱ. Shift registers Ⅰ and Ⅱ continues the shift operation until it arrives at the 16th bit of CLK and DO output serial data.
(9) Serial data is used to control the operation for switching input/output mode of D1 to D16. The pin set to "H" operates as an input pin.

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = –20 ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.5 ~ +7	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} + 0.5	V
I_{IK}	Input protection diode current	V_I<0V	–20	mA
		V_I>V_{CC}	20	
I_{OK}	Output incidental diode current	V_O<0V	–20	mA
		V_O>V_{CC}	20	
I_{GND}	Current/GND	GND	–64	mA
T_{stg}	Storage temperature		–65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	–20		75	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 2 ~ 6V unless otherwise noted)

Symbol	Parameter	Conditions		Limits					Unit
				T_a=25°C			T_a= –20~75°C		
				Min.	Typ.	Max.	Min.	Max.	
V_{T+}	Threshold voltage in positive direction	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20µA	$\overline{CS}$, CLK, DI	0.35 × V_{CC}		0.8 × V_{CC}	0.35 × V_{CC}	0.8 × V_{CC}	V
V_{T-}	Threshold voltage in negative direction	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20µA	$\overline{CS}$, DI	0.2 × V_{CC}		0.65 × V_{CC}	0.2 × V_{CC}	0.65 × V_{CC}	V
V_{IH}	High-level input voltage	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20µA	D1~D16	0.75 × V_{CC}			0.75 × V_{CC}		V
V_{IL}	Low-level input voltage	V_O=0.1V, V_{CC}–0.1V $\|I_O\|$=20µA	D1~D16			0.25 × V_{CC}		0.25 × V_{CC}	V
V_{OL}	Low-level output voltage	V_I=V_{T+}, V_{T-} V_{CC}=4.5V	I_{OL}=3mA			0.4		0.5	V
I_O	Maximum output leak current	V_I=V_{T+}, V_{T-} V_{CC}=6V	V_O=V_{CC}			1.0		10.0	µA
			V_O=GND			–1.0		–10.0	
I_{IH}	High-level input current	V_I=V_{CC}	V_{CC}=6V			0.1		1.0	µA
I_{IL}	Low level input current	V_I=GND	V_{CC}=6V			–0.1		–1.0	µA
I_{CC}	Static consumption current	V_I=V_{CC}, GND	V_{CC}=6V			10.0		100.0	µA

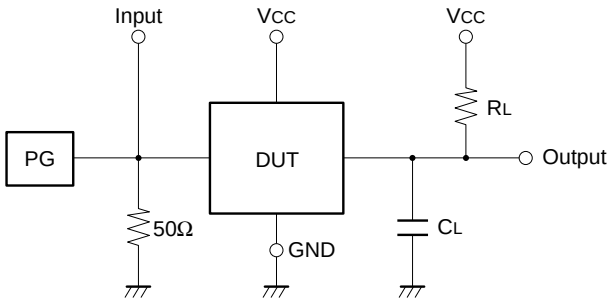
SWITCHING CHARACTERISTICS (V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits					Unit
			T_a=25°C			T_a= –20~75°C		
			Min.	Typ.	Max.	Min.	Max.	
f_{max}	Maximum repetition frequency	C_L=50pF R_L=1kΩ (Note 2)	2.5			1.9		MHz
t_{PLZ}	Output “L-Z”, “Z-L” propagation time CLK-DO				300		400	ns
t_{PZL}					300		400	ns
t_{PLZ}	Output “L-Z”, “Z-L” propagation time $\overline{CS}$-D1 to D16				300		400	ns
t_{PZL}					300		400	ns
t_{PLZ}	Output “L-Z” propagation time S-DO, D1 ~ D16				300		400	ns

TIMING REQUIREMENTS (V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits					Unit
			T_a=25°C			T_a= –20~75°C		
			Min.	Typ.	Max.	Min.	Max.	
t_w	CLK, $\overline{CS}$, $\overline{S}$ pulse width		200			260		ns
t_{su}	DI set up time for CLK		100			130		ns
	$\overline{CS}$ set up time for CLK		100			130		
	D1~D16 set up time for $\overline{CS}$		100			130		
t_h	DI hold time for CLK		100			130		ns
	$\overline{CS}$ hold time for CLK		100			130		
	D1~D16 hold time for $\overline{CS}$		100			130		
t_{rec}	$\overline{CS}$ recovery time for $\overline{S}$		100			130		ns

Note 2: Test Circuit



(1) Characteristics (10%~90%) of pulse generator (PG)
t_r=6ns, t_f=6ns
(2) Electrostatic capacitance C_L includes the floating capacitance of connection and probe input capacitance.

TIMING DIAGRAM