

**Amplifier, Power, 8W  
2.0-8.0 GHz**

**MAAP-000074-PKG001**  
Rev —  
Advance Datasheet

**Features**

- ◆ 8 Watt Saturated Output Power Level
- ◆ 2-Octave Bandwidth
- ◆ Variable Drain Voltage (4-10V) Operation
- ◆ MSAG Process

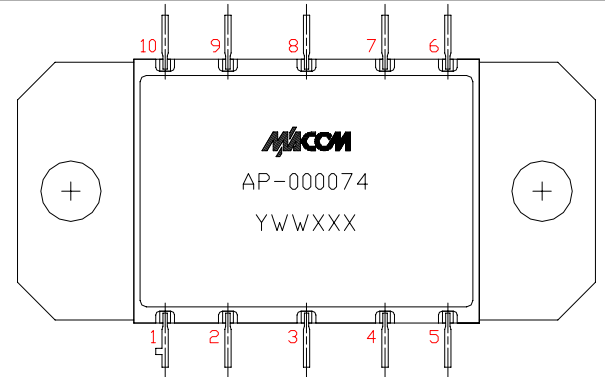
**Primary Applications**

- ◆ SatCom
- ◆ Radio Communications
- ◆ Radar
- ◆ Electronic Warfare

**Description**

The MAAP-000074-PKG001 is a 2-stage 8W power amplifier with on-chip bias networks in a 10 lead flange-mount ceramic package, allowing easy assembly. The package is hermetic and provides an excellent thermal path. This product is fully matched to 50 ohms on both the input and output. External DC blocking capacitors are not required since they are incorporated into the MMIC design. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG) Process, each device is 100% RF tested on wafer to ensure performance compliance.



Pin #	Description
1	VGG
2	N/C
3	RF IN
4	N/C
5	VGG
6	VDD
7	N/C
8	RF OUT
9	N/C
10	VDD

**Also Available in:**

Description	Die	Ceramic Pkg Sample Board	Die Sample Board
Part Number	MAAPGM0074-DIE	MAAP-000074-SMB001	MAAP-000074-SMB004

**Electrical Characteristics:**  $T_C = 30^{\circ}C^1$ ,  $Z_0 = 50 \Omega$ ,  $V_{DD} = 10V$ ,  $I_{DQ} = 2.1A^2$ ,  $P_{in} = 28 dBm$ ,  $R_G=40 \Omega$

Parameter	Symbol	Typical	Units
Bandwidth	f	2.0-8.0	GHz
Output Power	$P_{OUT}$	39	dBm
1-dB Compression Point	$P_{1dB}$	38	dBm
Small Signal Gain	G	14	dB
Input VSWR	VSWR	1.7:1	
Output VSWR	VSWR	2.2:1	
Gate Current	$I_{GG}$	3.5	mA
Drain Current, under RF Drive	$I_{DD}$	3.5	A
2 <sup>nd</sup> Harmonic, 2-4 GHz	2f	16.5	dBc
2 <sup>nd</sup> Harmonic, 6-8 GHz	2f	72	dBc

1.  $T_C$  = Case Temperature
2. Adjust  $V_{GG}$  between  $-2.6$  and  $-1.2V$  to achieve specified  $I_{DQ}$ .

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Visit [www.macom.com](http://www.macom.com) for additional data sheets and product information.

### Maximum Ratings <sup>3</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	P <sub>IN</sub>	33	dBm
Drain Supply Voltage	V <sub>DD</sub>	+12.0	V
Gate Supply Voltage	V <sub>GG</sub>	-3.0	V
Quiescent Drain Current (No RF)	I <sub>DQ</sub>	3.4	A
Quiescent DC Power Dissipated (No RF)	P <sub>DISS</sub>	34.2	W
Junction Temperature	T <sub>J</sub>	170	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

### Recommended Operating Conditions<sup>4</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V <sub>DD</sub>	4.0	10	10	V
Gate Voltage	V <sub>GG</sub>	-2.6	-2.2	-1.5	V
Input Power	P <sub>IN</sub>		28	30	dBm
Junction Temperature	T <sub>J</sub>			150	°C
Thermal Resistance	Θ <sub>JC</sub>				°C/W
Case Temperature	T <sub>C</sub>			Note 5	°C

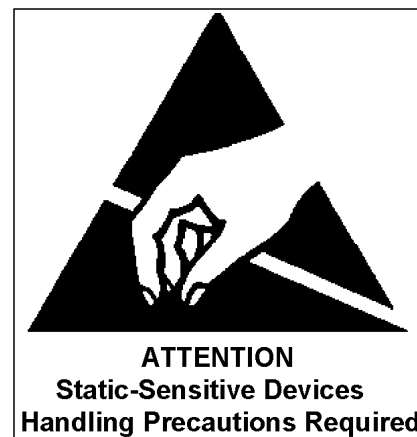
4. Operation outside of these ranges may reduce product reliability.

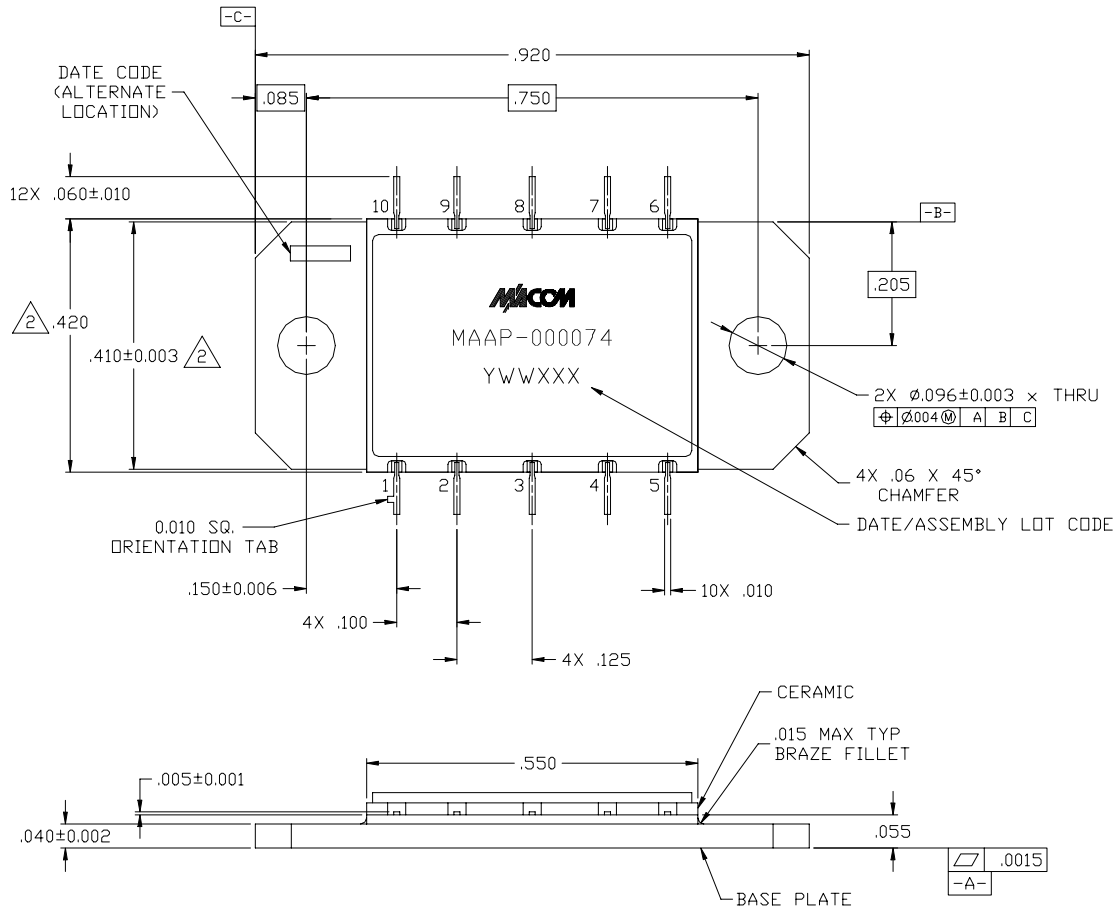
5. Case Temperature = 150°C — Θ<sub>JC</sub> \* V<sub>DD</sub> \* I<sub>DQ</sub>

### Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

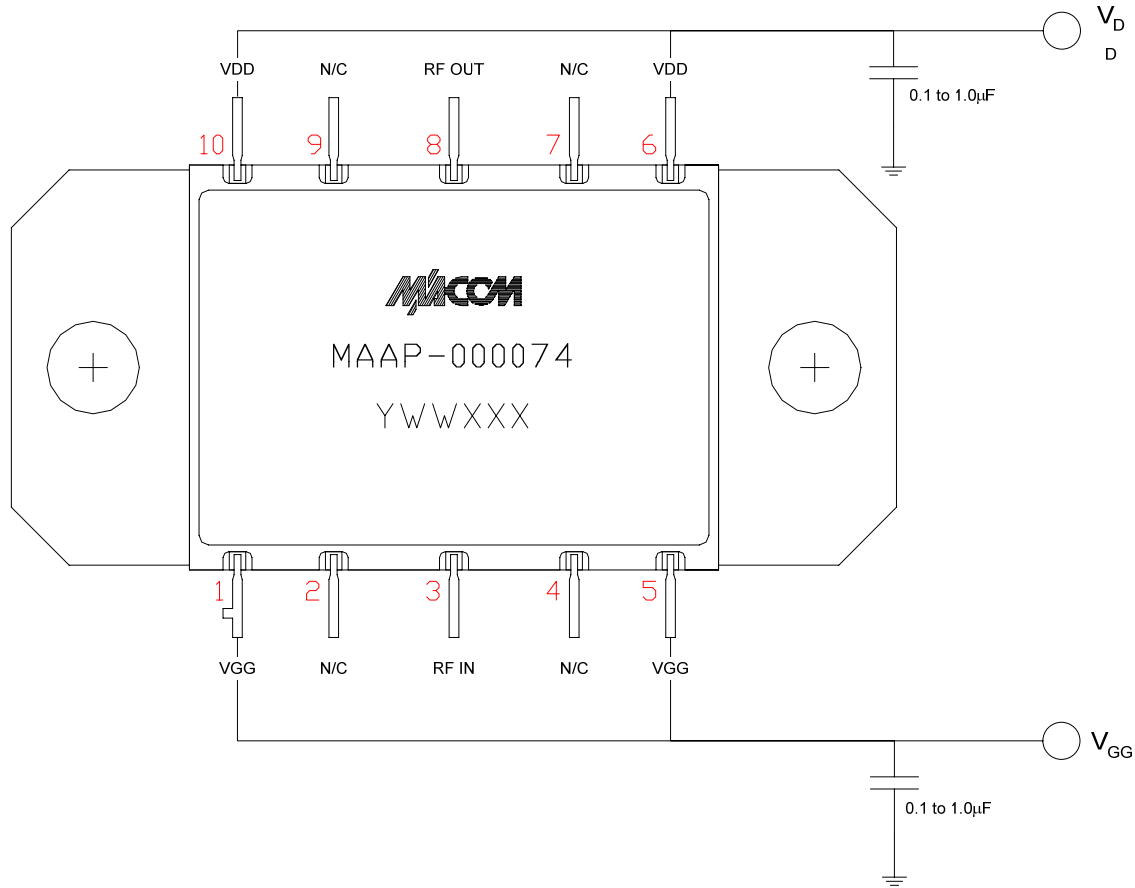
1. Apply V<sub>GG</sub> = -2.7 V, V<sub>DD</sub> = 0 V.
2. Ramp V<sub>DD</sub> to desired voltage, typically 10.0 V.
3. Adjust V<sub>GG</sub> to set I<sub>DQ</sub>, (approximately @ -2.2 V).
4. Set RF input.
5. Power down sequence in reverse. Turn V<sub>GG</sub> off last.





**Figure 1. Package Dimensions**

This is a high frequency, low thermal resistance package. The package consists of a cofired ceramic construction with a copper-tungsten base and iron-nickel-cobalt leads. The finish consists of electrolytic gold over nickel plate.



**Figure 2. Recommended Bias Configuration**

**Assembly Instructions:**

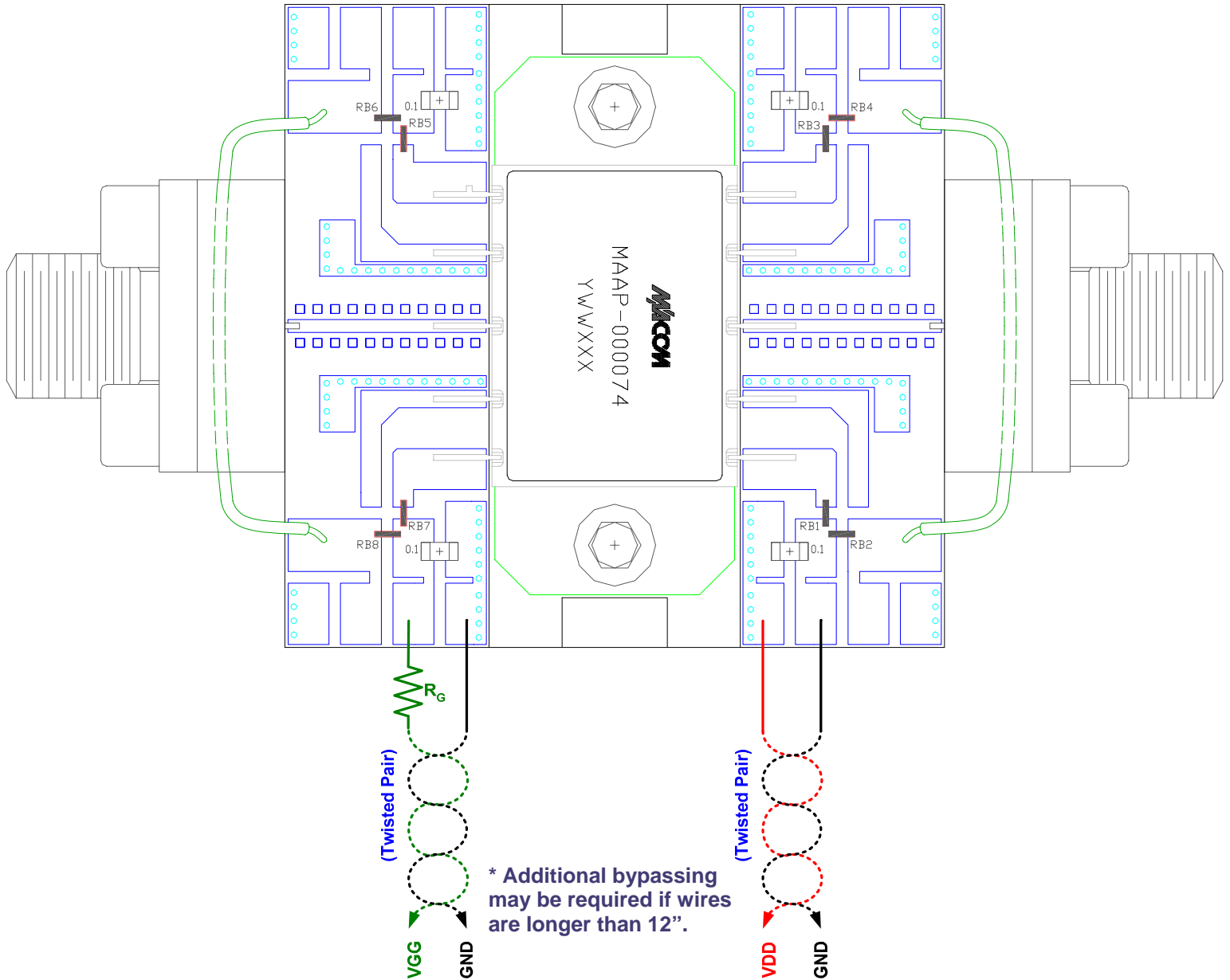
This flange mount style package provides a robust interface between a highly integrated GaAs MMIC device and a circuit board which may be assembled using conventional surface mount techniques. A thin shim made of a thermally and electrically conductive, ductile material must be used prior to installation of the ceramic package for proper thermal and electrical performance. Refer to **M/A-COM Application Note #M567\*** for more information regarding shim material and mounting screw torque requirements.

For applications where surface mount components are to be installed after the ceramic package installation, this package will not be damaged when subjected to typical convection or IR oven reflow profiles. Refer to **M/A-COM Application Note #M538\*** for maximum allowable reflow time and temperature. Alternatively, the package leads may be individually soldered. Whether an iron or hot gas soldering equipment is used, care should be taken to insure that the temperature is well controlled and electric static discharge (ESD) safe.

\* Application Notes are available upon request.

**Biassing Notes:**

- ◆ A negative bias must be applied to  $V_{GG}$  before applying a positive bias to  $V_{DD}$  to prevent damage to the amplifier.



**Figure 3. MAAP-000074-PKG001 Evaluation Board**