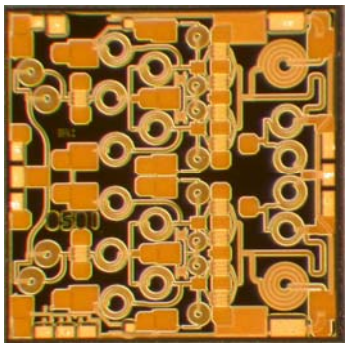
Amplifier, Power, S/C-Band, 1.6W 2.5-5.5 GHz

MAAPGM0035S-DIE
903179 —
Preliminary Information

Features

- **1.6 Watt Saturated Output Power Level**
- **Variable Drain Voltage (4-10V) Operation**
- **MSAG Process**
- **On-Chip Bias Ladder**



Description

The MAAPGM0035S-DIE is a 2-stage, 1.6 W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications. An on-chip bias ladder allows for fixed gate voltage or fixed small-signal drain current operation.

Each device is 100% RF tested on wafer to ensure performance compliance. The part is fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG®) Process. This process provides polyimide scratch protection.

Primary Applications

- WLL
- MMDS
- SatCom

Electrical Characteristics: T_B = 40°C[1], Z_0 = 50 Ω, V_{DD} = 8V, Idq= 600mA[2], P_{in} = 20 dBm

Parameter	Symbol	Typical	Units
Bandwidth	f	2.5-5.5	GHz
Output Power	P_{OUT}	32	dBm
Power Added Efficiency	PAE	34	%
1-dB Compression Point	P1dB	31	dBm
Small Signal Gain	G	17	dB
Input VSWR	VSWR	1.5:1	
Gate Current	I_{GG}	< 10	mA
Drain Current	I_{DD}	< 850	mA
Output Third Order Intercept	OTOI	42	dBm
Noise Figure	NF	7	dB
2nd Harmonic	2f	-10	dBc
3rd Harmonic	3f	-20	dBc

1. **T_B = MMIC Base Temperature**
2. **Adjust V_{GG} between –6.5 and –3.5V to achieve specified Idq.**

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• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
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Maximum Operating Conditions [3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	25.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-8V min. / -3V max.	V
Quiescent Drain Current (No RF)	I_{DQ}	790	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	6.3	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions

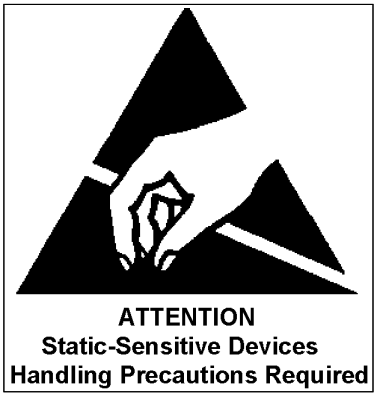
Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Supply Voltage, Fixed V_{GG} Operation	V_{GG}	-5.25	-5.0	-4.75	V
Gate Supply Voltage, Fixed I_{DQ} Operation	V_{GG}	-6.5	-5.0	-3.5	V
Input Power	P_{IN}		20.0	23.0	dBm
Junction Temperature	T_J			150	°C
Thermal Resistance	Θ_{JC}		12.7		°C/W
Package Base Temperature	T_B			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.
5. Maximum MMIC Base Temperature = 150°C — 12.7 °C/W * V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -5.0 V, V_{DD} = 0 V.
2. Ramp V_{DD} to desired voltage of 8 V.
3. Set RF input.
4. Power down sequence in reverse. Turn V_{GG} off last.



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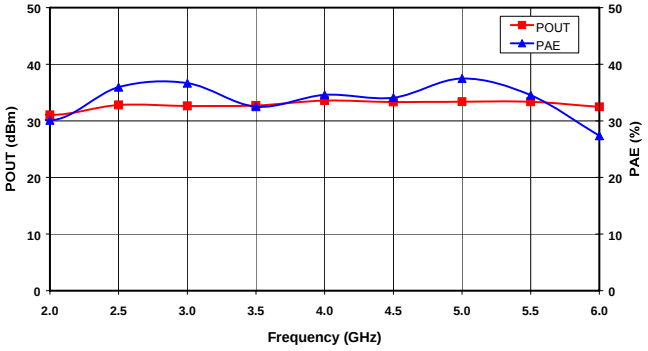

Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 8V and P_{in} = 20 dBm.

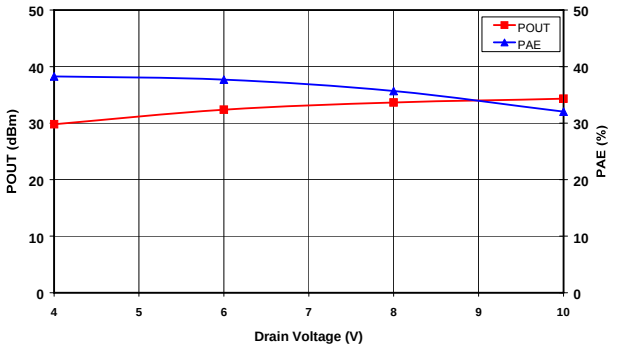

Figure 2. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at f_o = 4 GHz.

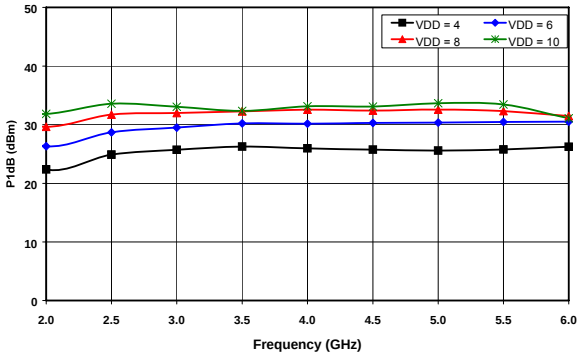

Figure 3. 1dB Compression Point vs. Drain Voltage

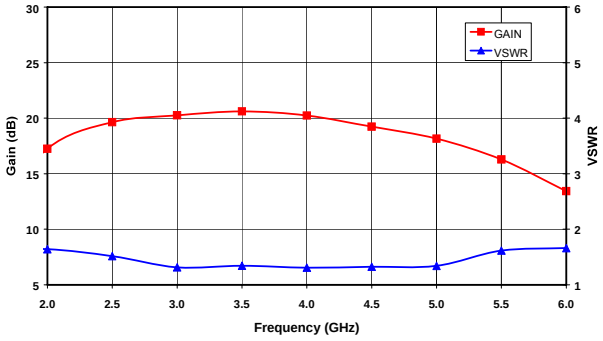

Figure 4. Small Signal Gain and VSWR vs. Frequency at V_{DD} = 8V.

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Mechanical Information

Chip Size: 3.000 x 3.000 x 0.075 mm (118 x 118 x 3 mils)

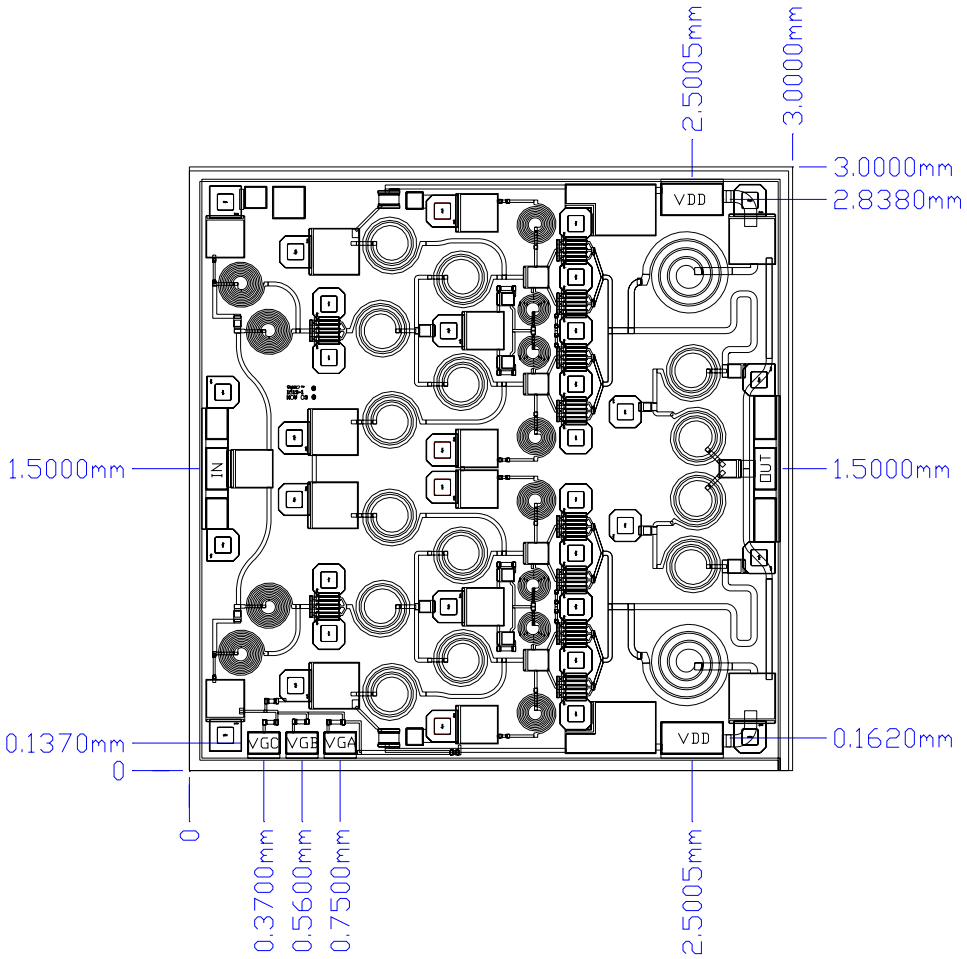

Figure 5. Die Layout

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VDD	300 x 150	12 x 6
DC Gate Supply Voltage VGG	150 x 100	6 x 4

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Assembly and Bonding Diagram

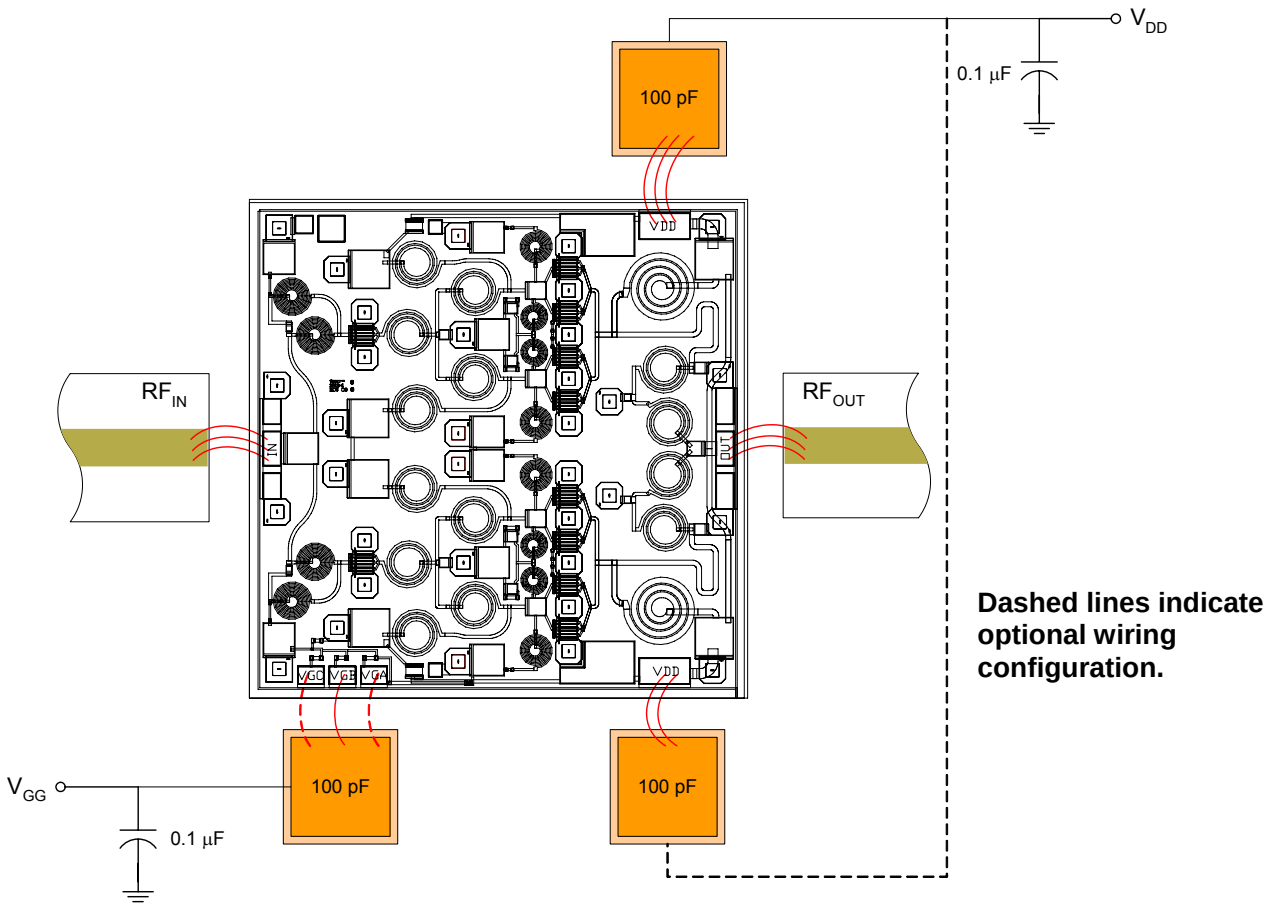

Figure 4. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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