



RF Power Field Effect Transistor LDMOS, 800—1700 MHz, 15W, 26V

1/11/06

Preliminary

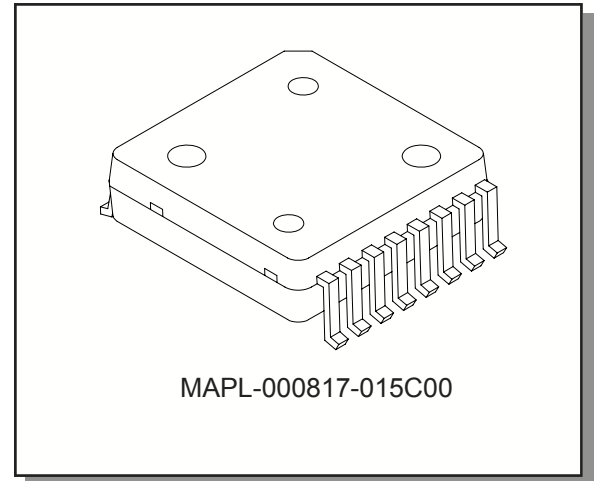
MAPL-000817-015C00



Features

- Designed for broadband commercial applications up to 1.7GHz
- High Gain, High Efficiency and High Linearity
- Typical P1dB performance at 960MHz, 26Vdc, CW
 - Typical Power Output: 16.5W
 - Gain: 16.5dB
 - Efficiency: 50%
 - 10:1 VSWR Ruggedness at 15W, 26Vdc, 960MHz

Package Style



Maximum Ratings

Parameter	Symbol	Rating	Units
Drain—Source Voltage	V_{DSS}	65	V _{dc}
Gate—Source Voltage	V_{GS}	+20, -20	V _{dc}
Total Power Dissipation @ T _c = 25 °C	P _d	31.25	W
Storage Temperature	T _{STG}	-65 to +150	°C
Junction Temperature	T _J	150	°C

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	4	°C/W

NOTE—**CAUTION**—MOS devices are susceptible to damage from electrostatic charge. Precautions in handling and packaging MOS devices should be observed.

Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS @ 25°C					
Drain-Source Breakdown Voltage ($V_{GS} = 0$ Vdc, $I_D = 30$ μ A dc)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate Threshold Voltage ($V_{ds} = 26$ Vdc, $I_d = 100$ mA)	$V_{GS(th)}$	2	—	5	Vdc
Gate Quiescent Voltage ($V_{ds} = 26$ Vdc, $I_d = 100$ mA)	$V_{DS(Q)}$	3	—	5	Vdc
Drain-Source On-Voltage ($V_{gs} = 10$ Vdc, $I_d = 1$ A)	$V_{DS(on)}$	—	0.25	—	Vdc
RF FUNCTIONAL TESTS @ 25°C (In M/A-COM Test Fixture) (1)					
Common Source Amplifier Gain ($V_{DD} = 26$ Vdc, $I_{DQ} = 100$ mA, $f = 960$ MHz, $P_{OUT} = 15$ W)	G_P	—	17	—	dB
Drain Efficiency ($V_{DD} = 26$ Vdc, $I_{DQ} = 100$ mA, $f = 960$ MHz, $P_{OUT} = 15$ W)	EFF (η)	—	50	—	%
Input Return Loss ($V_{DD} = 26$ Vdc, $I_{DQ} = 100$ mA, $f = 960$ MHz, $P_{OUT} = 15$ W)	IRL	—	-10	—	dB
Output VSWR Tolerance ($V_{DD} = 26$ Vdc, $I_{DQ} = 100$ mA, $f = 960$ MHz, $P_{OUT} = 15$ W, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			
Common Source Amplifier Gain ($V_{DD} = 26$ Vdc, $I_{DQ} = 100$ mA, $f = 1670$ MHz, $P_{OUT} = 15$ W)	G_P	—	12.5	—	dB
Drain Efficiency ($V_{DD} = 26$ Vdc, $I_{DQ} = 100$ mA, $f = 1670$ MHz, $P_{OUT} = 15$ W)	EFF (η)	—	50	—	%
Input Return Loss ($V_{DD} = 26$ Vdc, $I_{DQ} = 100$ mA, $f = 1670$ MHz, $P_{OUT} = 15$ W)	IRL	—	-10	—	dB

(1) Device specifications obtained on a Production Test Fixture.

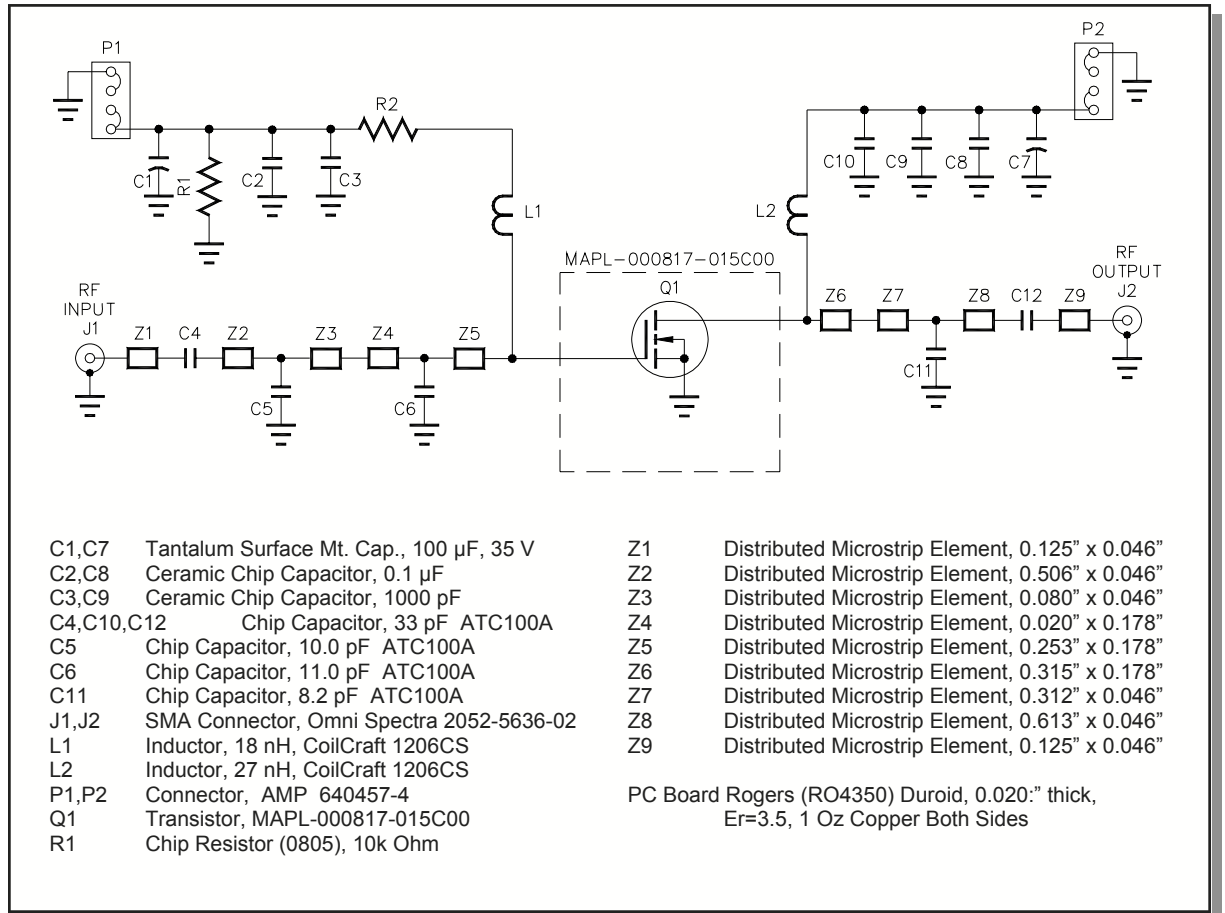


Figure 1. 920—960 MHz Test Fixture Schematic

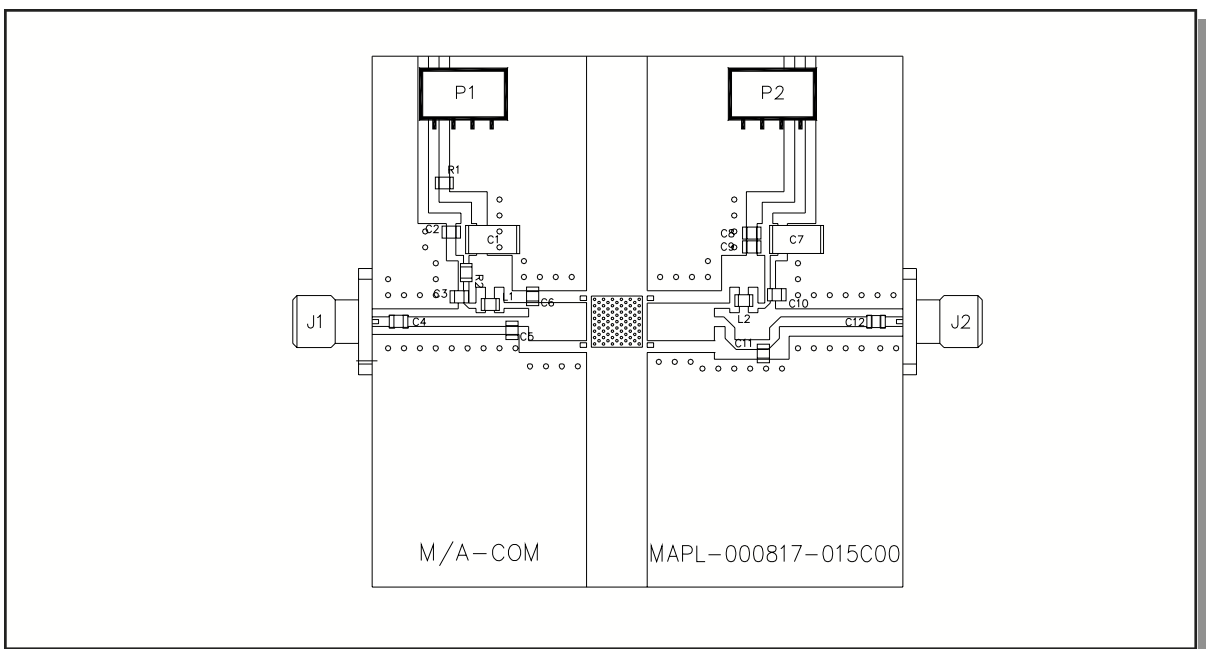


Figure 2. 920—960 MHz Test Fixture Component Layout

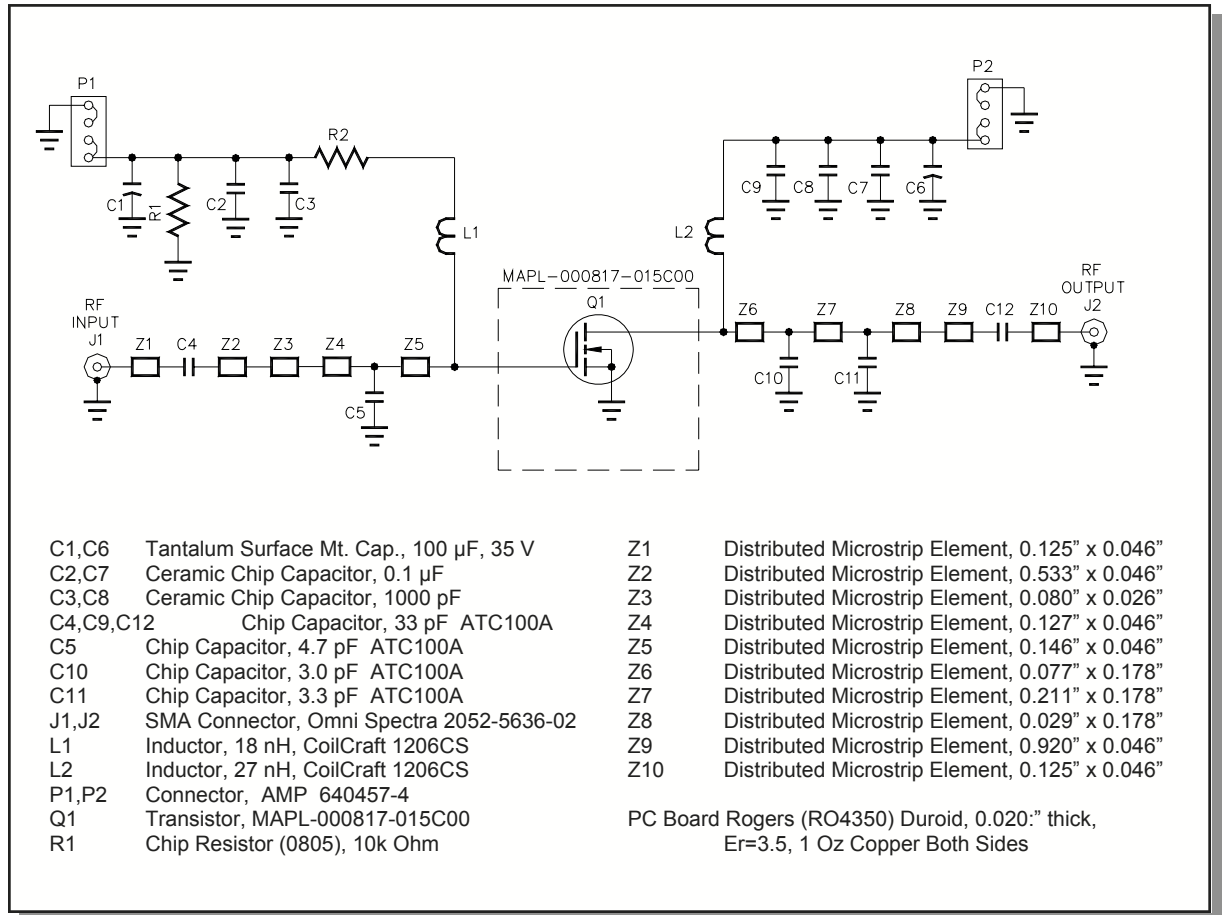


Figure 3. 1620-1670 MHz Test Fixture Schematic

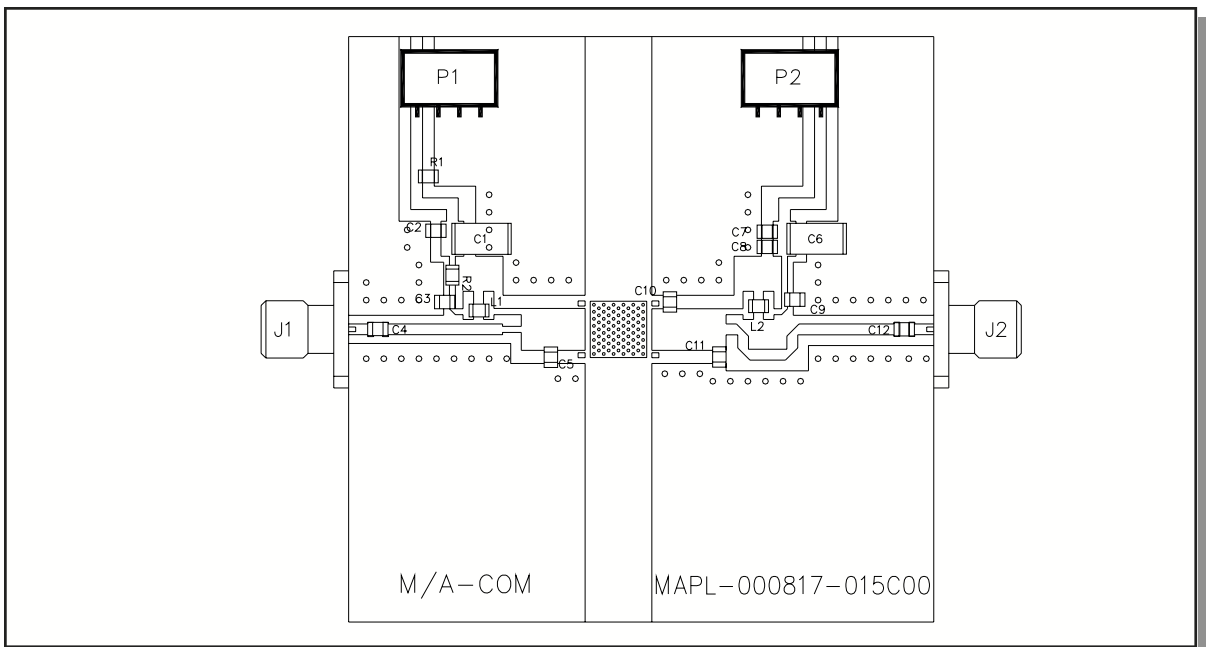


Figure 4. 1620—1670 MHz Test Fixture Component Layout

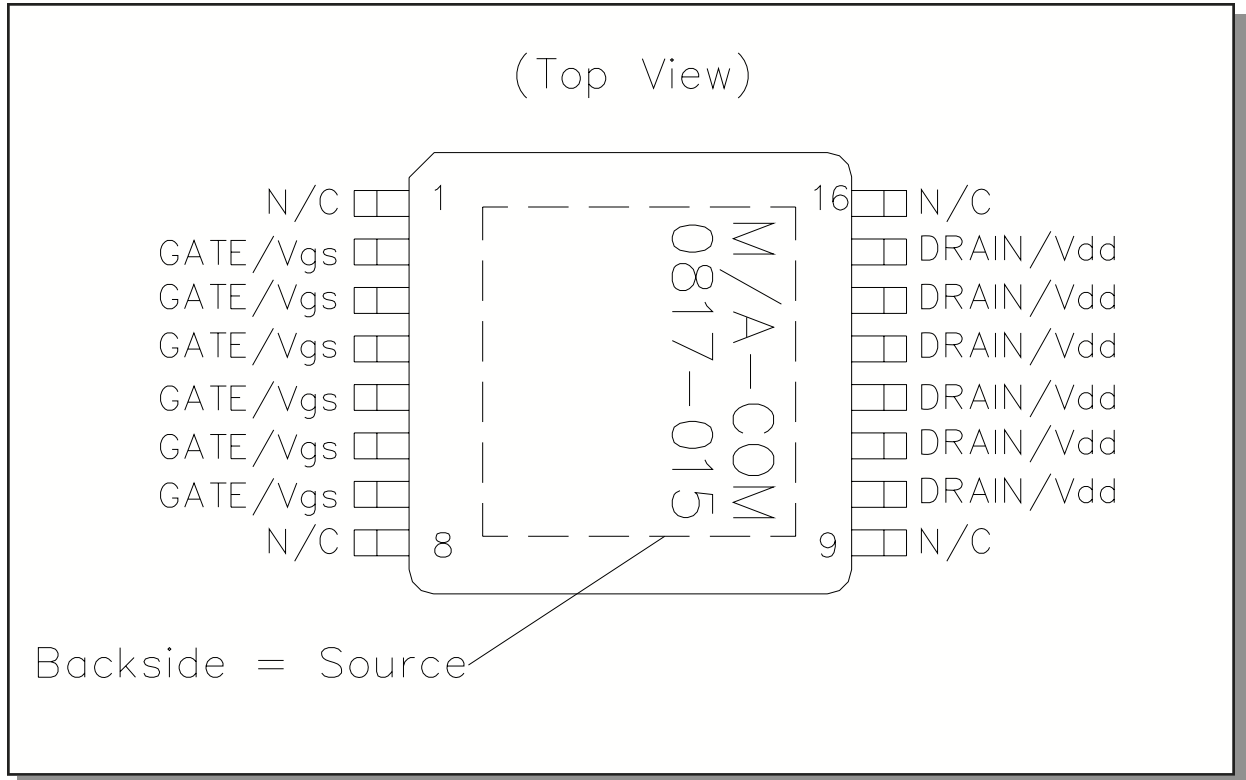
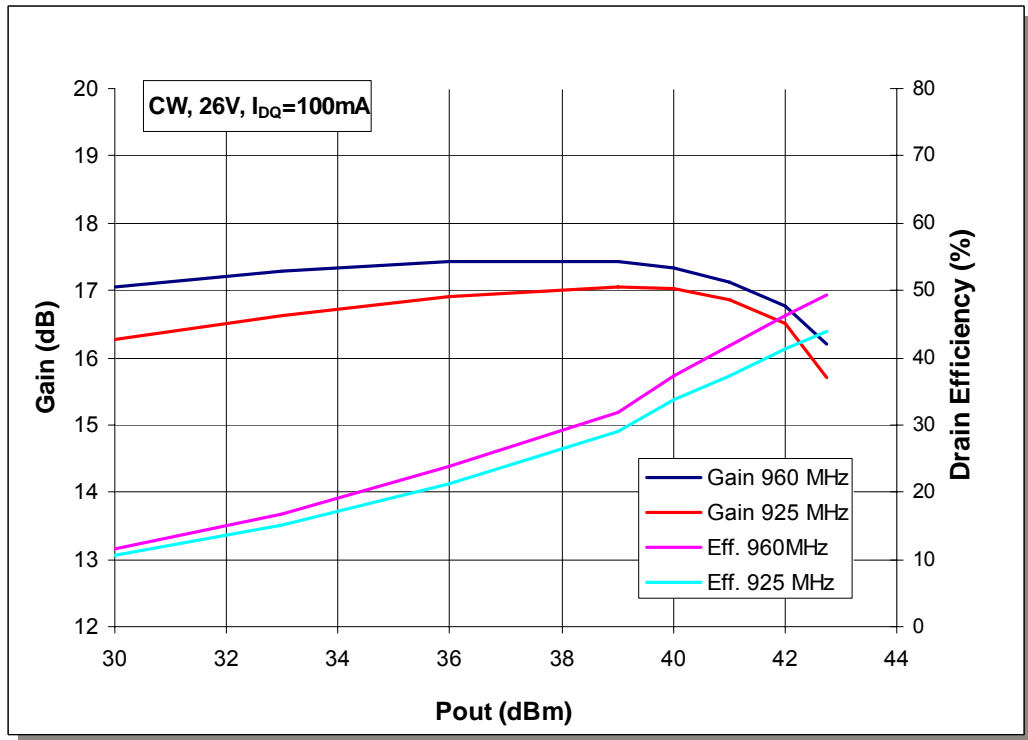
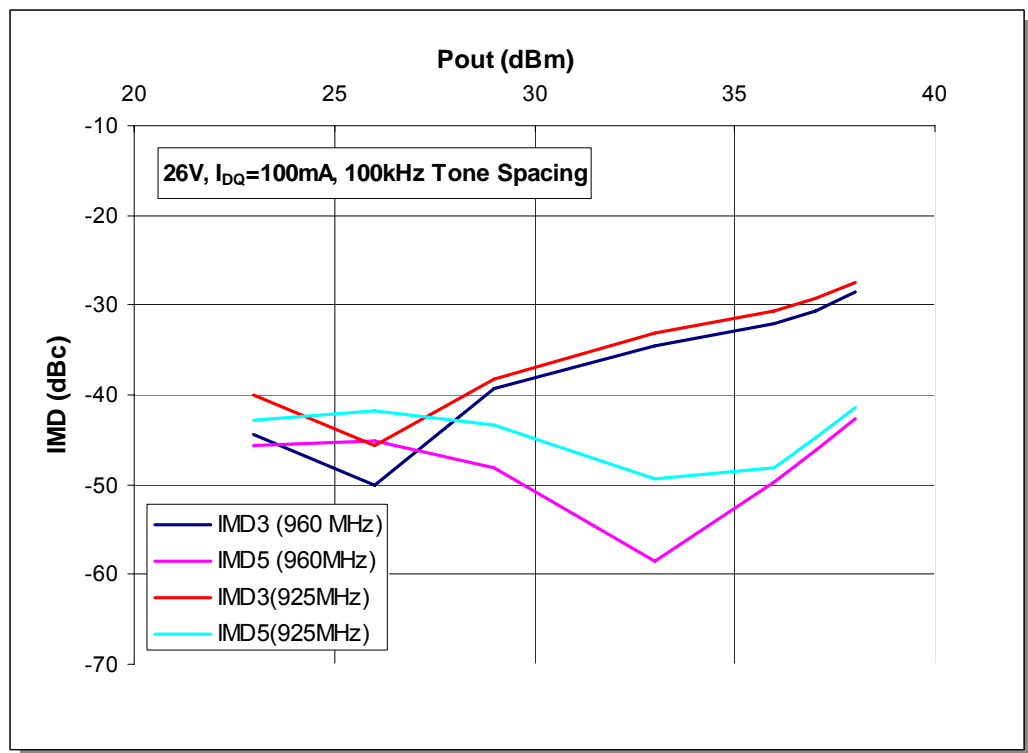


Figure 5. MAPL-000817-015C00 Pin Connections

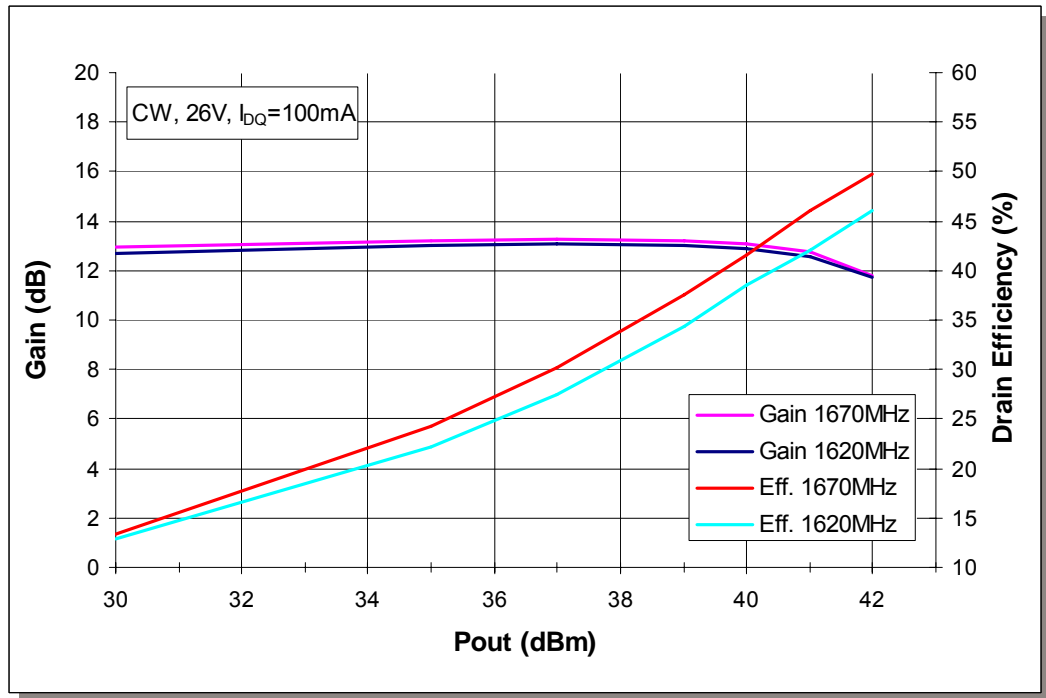
Preliminary



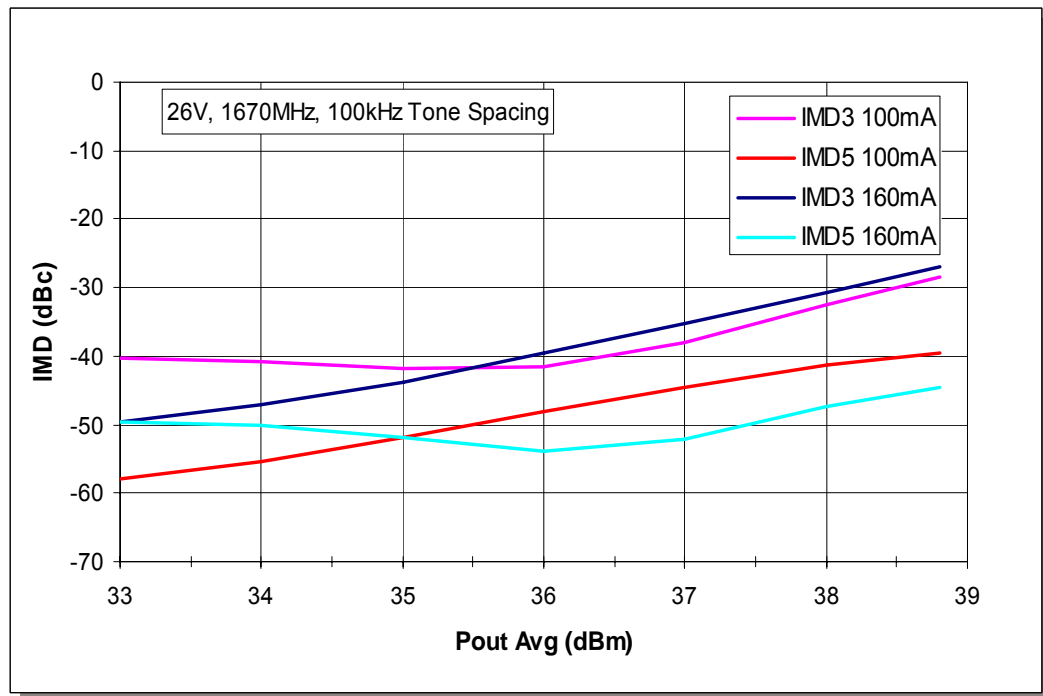
Graph 1. 925, 960MHz: CW Power Gain and Drain Efficiency vs. Output Power



Graph 2. 925, 960 MHz: 2 Tone Intermodulation Distortion vs. Output Power

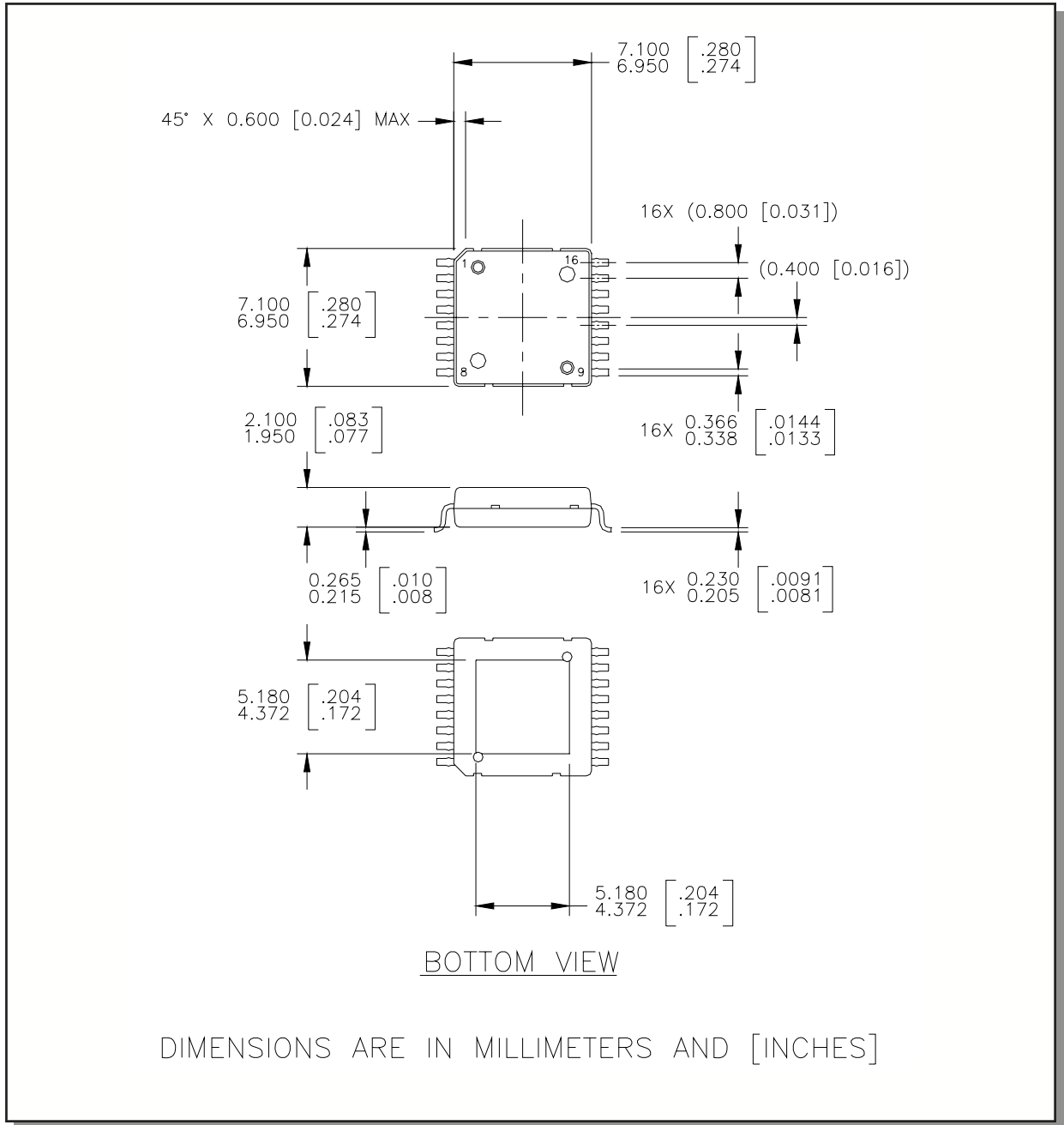


Graph 3. 1620, 1670MHz: CW Power Gain and Drain Efficiency vs. Output Power



Graph 4. 1620, 1670MHz: 2 Tone Intermodulation Distortion vs. Output Power

Package Dimensions



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