19-1981; Rev 1; 5/04

EVALUATION KIT AVAILABLE

12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

General Description

The MAX1420, 3.3V, 12-bit analog-to-digital converter (ADC) features a fully-differential input, pipelined, 12-stage ADC architecture with wideband track-and-hold (T/H) and digital error correction, incorporating a fully-differential signal path. The MAX1420 is optimized for low-power, high dynamic performance applications in imaging and digital communications. The converter operates from a single 3.3V supply, and consumes only 221mW. The fully-differential input stage has a small signal -3dB bandwidth of 400MHz and may be operated with single-ended inputs.

An internal 2.048V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure accommodates an internal reference, or externally applied buffered or unbuffered reference for applications that require increased accuracy and a different input voltage range.

In addition to low operating power, the MAX1420 features two power-down modes: reference power-down and shutdown mode. In reference power-down, the internal bandgap reference is deactivated, which results in a typical 2mA supply current reduction. A full shutdown mode is available to maximize power savings during idle periods.

The MAX1420 provides parallel, offset binary, CMOS-compatible three-state outputs.

The MAX1420 is available in a 7mm x 7mm x 1.4mm, 48-pin TQFP package, and is specified over the commercial (0°C to +70°C) and the extended industrial (-40°C to +85°C) temperature range.

Pin-compatible lower speed versions of the MAX1420 are also available. Please refer to the MAX1421 data sheet for 40Msps and the MAX1422 data sheet for 20Msps.

Applications

Medical Ultrasound Imaging

CCD Pixel Processing

IR Focal Plane Arrays

Radar

IF and Baseband Digitization

Functional diagram appears at end of data sheet.

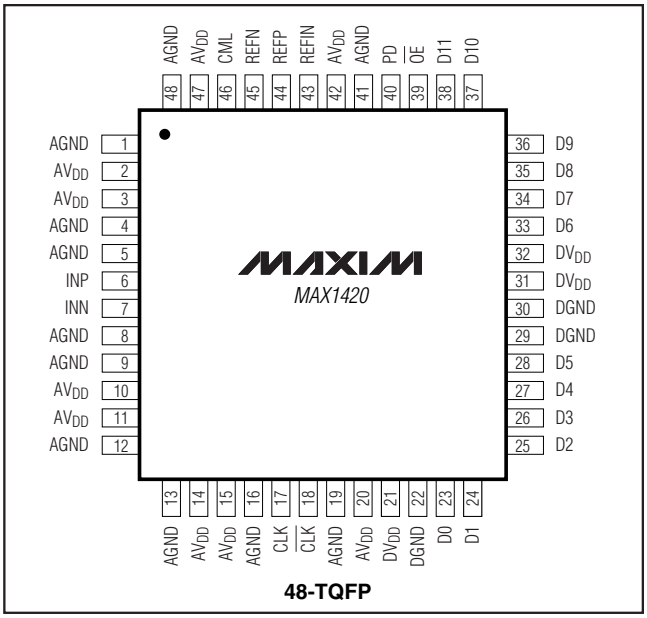
Features

- **3.3V Single Power Supply**
- **67dB SNR at f_{IN} = 5MHz**
- **66dB SNR at f_{IN} = 15MHz**
- **Internal 2.048V Precision Bandgap Reference**
- **Differential, Wideband Input T/H Amplifier**
- **Power-Down Modes**
  218mW (Reference Shutdown Mode)
  10µW (Shutdown Mode)
- **Space-Saving 48-Pin TQFP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1420CCM	0°C to +70°C	48 TQFP
MAX1420ECM	-40°C to +85°C	48 TQFP

Pin Configuration



48-TQFP

12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

ABSOLUTE MAXIMUM RATINGS

AV_{DD}, DV_{DD} to AGND .....-0.3V to +4V
DV_{DD}, AV_{DD} to DGND .....-0.3V to +4V
DGND to AGND .....-0.3V to +0.3V
INP, INN, REFP, REFN, REFIN,
CML, CLK, $\overline{CLK}$ .....(AGND - 0.3V) to (AV_{DD} + 0.3V)
D0–D11, $\overline{OE}$, PD .....(DGND - 0.3V) to (DV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 21.7mW/°C above +70°C).....1789mW

Operating Temperature Ranges
MAX1420CCM .....0°C to +70°C
MAX1420ECM .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input voltage at -0.5dBFS, internal reference, f_{CLK} = 62.5MHz (50% duty cycle); digital output load C_L = 10pF, ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	RES			12		Bits
Differential Nonlinearity	DNL	T_A = +25°C, no missing codes	-1		1	LSB
		T_A = T_{MIN} to T_{MAX}		±0.5		
Integral Nonlinearity	INL	T_A = T_{MIN} to T_{MAX}		±2		LSB
Mid-scale Offset	MSO		-3	.75	3	%FSR
Mid-scale Offset Temperature Coefficient	MSOTC			3 x 10^{-4}		%/°C
Gain Error	GE	Internal reference (Note 1)	-5	±0.1	5	%FSR
		External reference applied to REFIN (Note 2)	-5	±0.2	5	
		External reference applied to REFP, CML, and REFN (Note 3)	-1.5		1.5	
Gain Error Temperature Coefficient	GETC	External reference applied to REFP, CML, and REFN (Note 3)		100 x 106		%/°C
DYNAMIC PERFORMANCE (f_{CLK} = 60MHz, 4096-point FFT)						
Signal-to-Noise Ratio	SNR	f_{IN} = 5MHz		67		dB
		f_{IN} = 15MHz, T_A =+25°C	62	66		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 5MHz		72		dBc
		f_{IN} = 15MHz, T_A =+25°C	64	72		
Total Harmonic Distortion	THD	f_{IN} = 5MHz		-70		dBc
		f_{IN} = 15MHz, T_A =+25°C		-69	-62	
Signal-to-Noise and Distortion	SINAD	f_{IN} = 5MHz		64.5		dB
		f_{IN} = 15MHz, T_A =+25°C	58.5	63		
Effective Number of Bits	ENOB	f_{IN} = 5MHz		10.4		Bits
		f_{IN} = 15MHz		10.2		
Two-Tone Intermodulation Distortion	IMD	f_{IN1} = 11.566036MHz, f_{IN2} = 13.4119138MHz (Note 4)		-74		dBc

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input voltage at -0.5dBFS, internal reference, f_{CLK} = 62.5MHz (50% duty cycle); digital output load C_L = 10pF, ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Gain	DG			±1		%
Differential Phase	DP			±0.25		Degrees
ANALOG INPUTS (INP, INN, CML)						
Input Resistance	R_{IN}	Either input to ground		22		kΩ
Input Capacitance	C_{IN}	Either input to ground		4		pF
Common-Mode Input Level (Note 5)	V_{CML}			V_{AVDD} x 0.5		V
Common-Mode Input Voltage Range (Note 5)	V_{CMVR}			V_{CML} ± 5%		V
Differential Input Range	V_{IN}	V_{INP} - V_{INN} (Note 6)		±V_{DIFF}		V
Small-Signal Bandwidth	BW_{-3dB}	(Note 7)		400		MHz
Large-Signal Bandwidth	$FPBW_{-3dB}$	(Note 7)		150		MHz
Overvoltage Recovery	OVR	1.5 x FS input		1		Clock cycles
INTERNAL REFERENCE (REFIN bypassed with 0.22µF in parallel with 1nF)						
Common-Mode Reference Voltage	V_{CML}	At CML		V_{AVDD} _ 0.5		V
Positive Reference Voltage	V_{REFP}	At REFP		V_{CML} + 0.512		V
Negative Reference Voltage	V_{REFN}	At REFN		V_{CML} - 0.512		V
Differential Reference Voltage	V_{DIFF}	(Note 6)		1.024 ±5%		V
Differential Reference Temperature Coefficient	REFTC			±100		ppm/°C
EXTERNAL REFERENCE (V_{REFIN} = 2.048V)						
REFIN Input Resistance	R_{IN}	(Note 8)	5			kΩ
REFIN Input Capacitance	C_{IN}			10		pF
REFIN Reference Input Voltage	V_{REFIN}			2.048 ±10%		V
Differential Reference Voltage	V_{DIFF}	(Note 6)	0.92 x V_{REFIN}/2	V_{REFIN}/2	1.08 x V_{REFIN}/2	V
EXTERNAL REFERENCE (V_{REFIN} = 0, reference voltage applied to REFP, REFN, and CML)						
REFP, REFN, CML Input Current	I_{IN}		-200		200	µA
REFP, REFN, CML Input Capacitance	C_{IN}			15		pF

12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input voltage at -0.5dBFS, internal reference, f_{CLK} = 62.5MHz (50% duty cycle); digital output load C_L = 10pF, ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Reference Voltage Range	V_{DIFF}	(Note 6)		1.024 ±10%		V
CML Input Voltage Range	V_{CML}			1.65 ±10%		V
REFP Input Voltage Range	V_{REFP}			V_{CML} + $V_{DIFF}/2$		V
REFN Input Voltage Range	V_{REFN}			V_{CML} - $V_{DIFF}/2$		V
DIGITAL INPUTS (CLK, $\overline{CLK}$, PD, OE)						
Input Logic High	V_{IH}		0.7 x V_{DVDD}			V
Input Logic Low	V_{IL}				0.3 x V_{DVDD}	V
Input Current		CLK, $\overline{CLK}$		±330		µA
		PD	-20		20	
		OE	-20		20	
Input Capacitance				10		pF
DIGITAL OUTPUTS (D0–D11)						
Output Logic High	V_{OH}	I_{OH} = 200µA	V_{DVDD} - 0.5		V_{DVDD}	V
Output Logic Low	V_{OL}	I_{OL} = -200µA	0		0.5	V
Three-State Leakage			-10		10	µA
Three-State Capacitance				2		pF
POWER REQUIREMENTS						
Analog Supply Voltage	V_{AVDD}		3.135	3.3	3.465	V
Digital Supply Voltage	V_{DVDD}		2.7	3.3	3.63	V
Analog Supply Current	I_{AVDD}			67	78	mA
Analog Supply Current with Internal Reference in Shutdown		V_{REFIN} = 0		66	76	mA
Analog Shutdown Current		PD = D_{VDD}		10	20	µA
Digital Supply Current	I_{DVDD}			8		mA
Digital Shutdown Current		PD = V_{DVDD}			20	µA
Power Dissipation	P_{DISS}	Analog power dissipation		221	258	mW

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input voltage at -0.5dBFS, internal reference, f_{CLK} = 62.5MHz (50% duty cycle); digital output load C_L = 10pF, ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

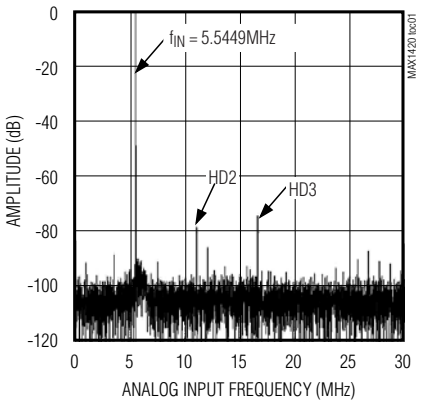
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation In Shutdown	P_{DISS}	PD = V_{DVDD}		10		µW
Power-Supply Rejection Ratio	PSRR	(Note 9)		±1		mV/V
TIMING CHARACTERISTICS						
Maximum Clock Frequency	f_{CLK}		60			MHz
Clock High	t_{CH}	Figure 6, clock period 16.667ns		8.33		ns
Clock Low	t_{CL}	Figure 6, clock period 16.667ns		8.33		ns
Pipeline Delay (Latency)		Figure 6		7		Clock cycles
Aperture Delay	t_{AD}	Figure 10		2		ns
Aperture Jitter	t_{AJ}	Figure 10		2		ps
Data Output Delay	t_{OD}	Figure 6	5	10	14	ns
Bus Enable Time	t_{BE}	Figure 5		5		ns
Bus Disable Time	t_{BD}	Figure 5		5		ns

Note 1: Internal reference, REFIN bypassed to AGND with a combination of 0.22µF in parallel with 1nF capacitor.
Note 2: External 2.048V reference applied to REFIN.
Note 3: Internal reference disabled. V_{REFIN} = 0, V_{REFP} = 2.162V, V_{CML} = 1.65V, and V_{REFN} = 1.138V.
Note 4: IMD is measured with respect to either of the fundamental tones.
Note 5: Specifies the common-mode range of the differential input signal supplied to the MAX1420.
Note 6: V_{DIFF} = V_{REFP} - V_{REFN}.
Note 7: Input bandwidth is measured at a -3dB level.
Note 8: V_{REFIN} is internally biased to 2.048V through a 10kΩ resistor.
Note 9: Measured as the ratio of the change in mid-scale offset voltage for a ±5% change in V_{AVDD}, using the internal reference.

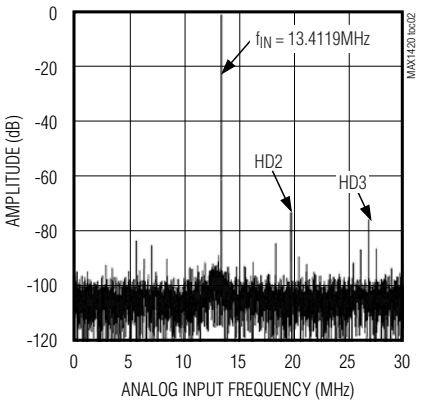
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input drive, A_{IN} = -0.5dBFS, f_{CLK} = 60.006MHz (50% duty cycle), digital output load C_L = 10pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

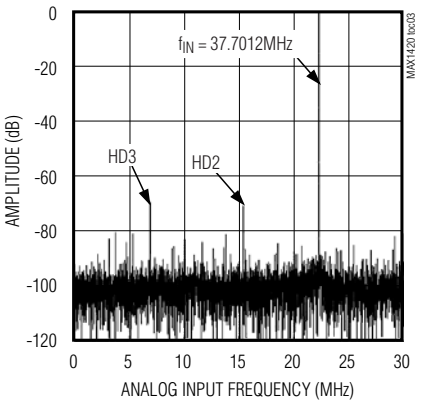
FFT PLOT (8192-POINT DATA RECORD)



FFT PLOT (8192-POINT DATA RECORD)



FFT PLOT (8192-POINT DATA RECORD)

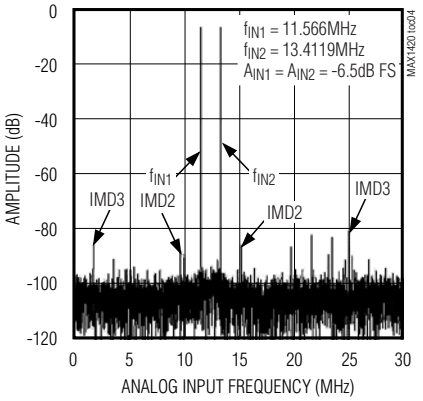


12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

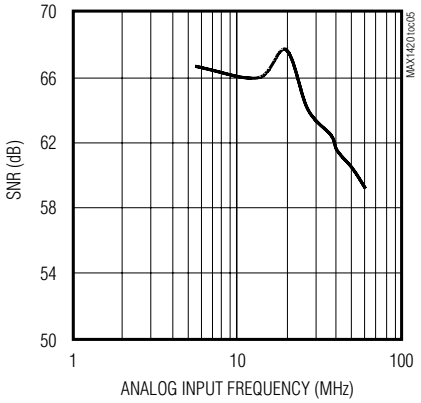
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input drive, A_{IN} = -0.5dBFS, f_{CLK} = 60.006MHz (50% duty cycle), digital output load C_L = 10pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

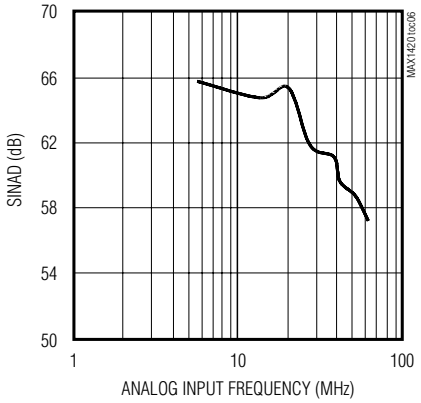
TWO-TONE IMD PLOT (8192-POINT DATA RECORD)



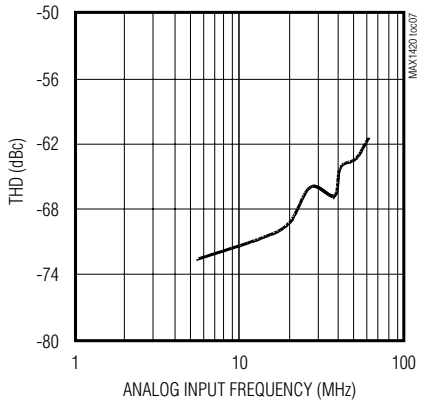
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



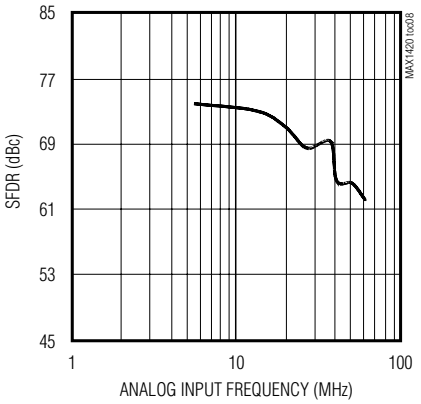
SIGNAL-TO-NOISE + DISTORTION vs. ANALOG INPUT FREQUENCY



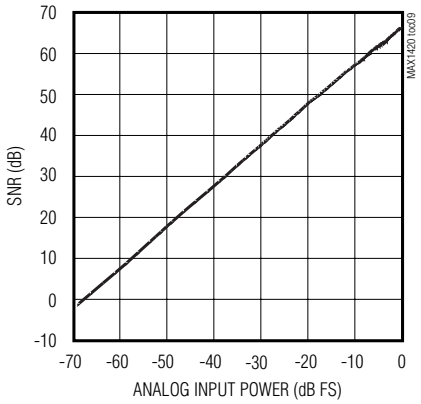
TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



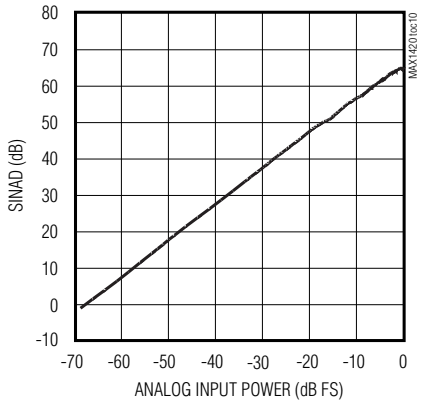
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



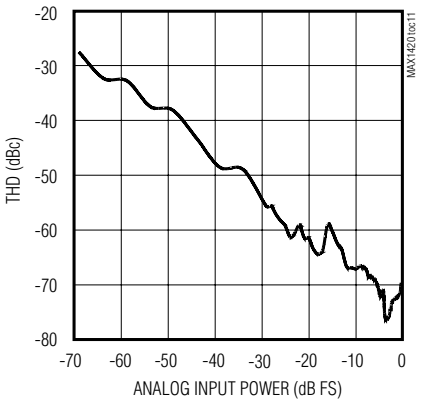
SIGNAL-TO-NOISE RATIO vs. INPUT POWER (f_{IN} = 15MHz)



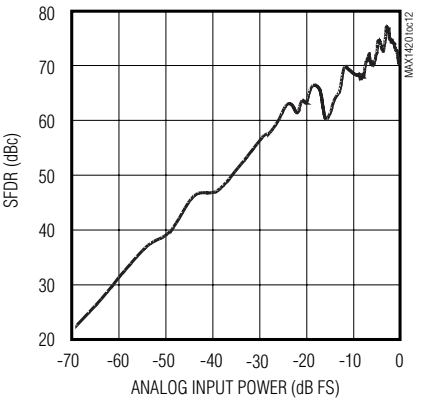
SIGNAL-TO-NOISE + DISTORTION vs. INPUT POWER (f_{IN} = 15MHz)



TOTAL HARMONIC DISTORTION vs. INPUT POWER (f_{IN} = 15MHz)



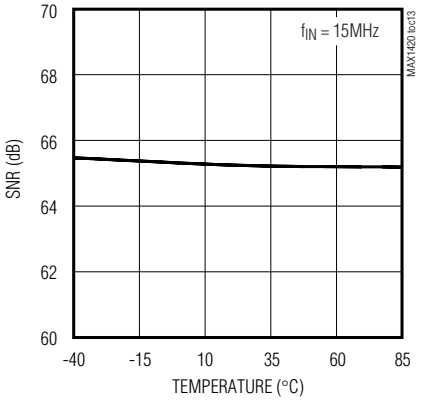
SPURIOUS-FREE DYNAMIC RANGE vs. INPUT POWER (f_{IN} = 15MHz)



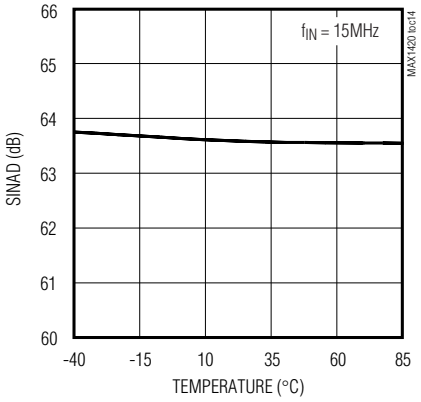
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input drive, A_{IN} = -0.5dBFS, f_{CLK} = 60.006MHz (50% duty cycle), digital output load C_L = 10pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

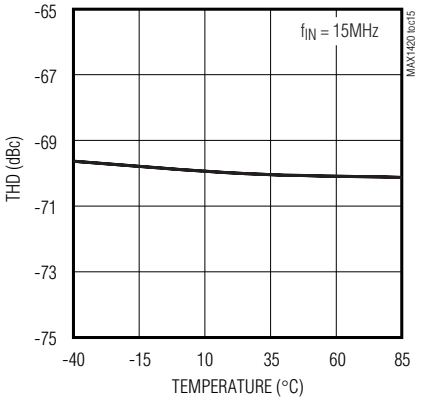
SIGNAL-TO-NOISE RATIO vs. TEMPERATURE



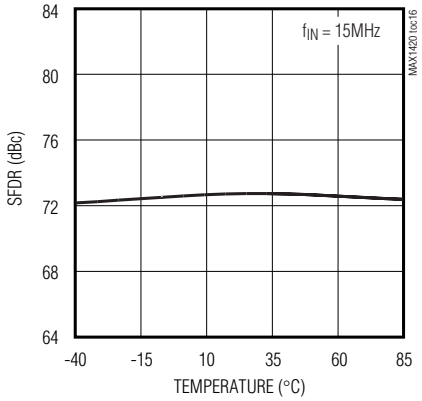
SIGNAL-TO-NOISE + DISTORTION vs. TEMPERATURE



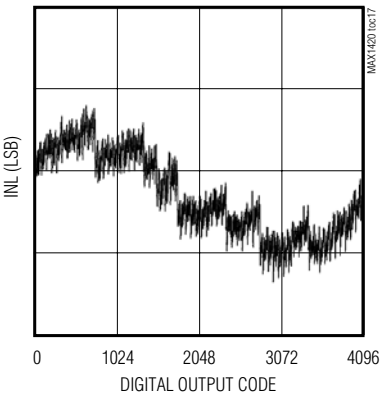
TOTAL HARMONIC DISTORTION vs. TEMPERATURE



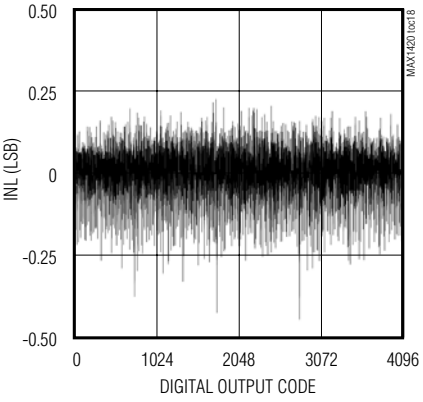
SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE



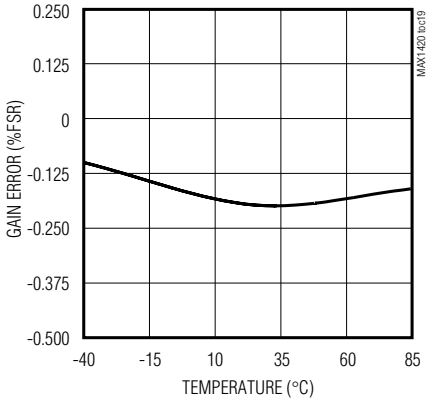
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



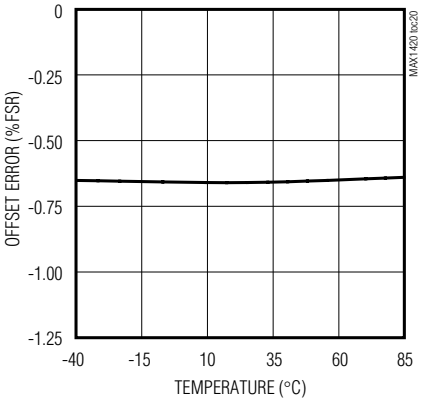
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



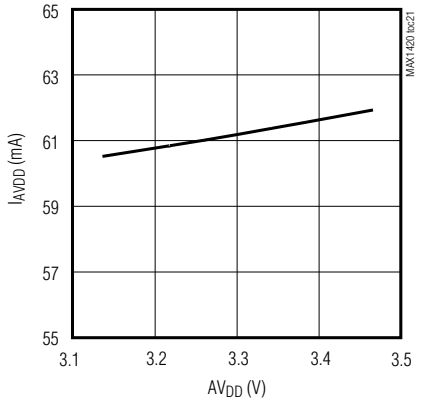
GAIN ERROR vs. TEMPERATURE, EXTERNAL REFERENCE V_{REFIN} = 2.048V



OFFSET ERROR vs. TEMPERATURE



ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE

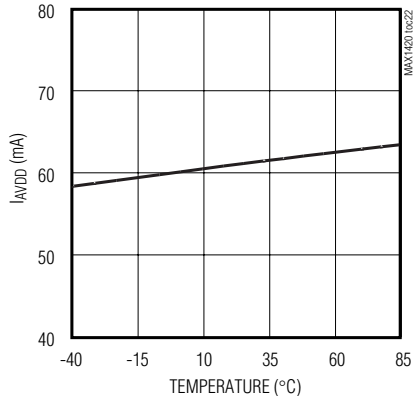


12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

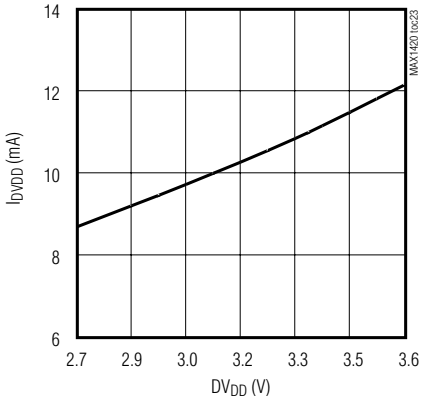
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, AGND = DGND = 0, V_{IN} = ±1.024V, differential input drive, A_{IN} = -0.5dBFS, f_{CLK} = 60.006MHz (50% duty cycle), digital output load C_L = 10pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

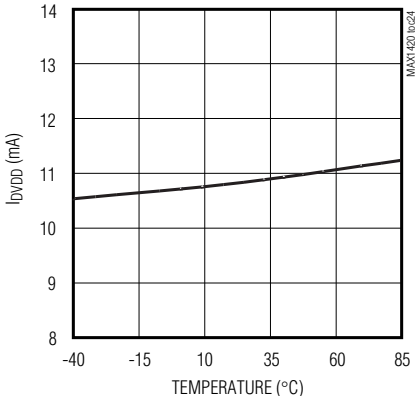
ANALOG SUPPLY CURRENT vs. TEMPERATURE



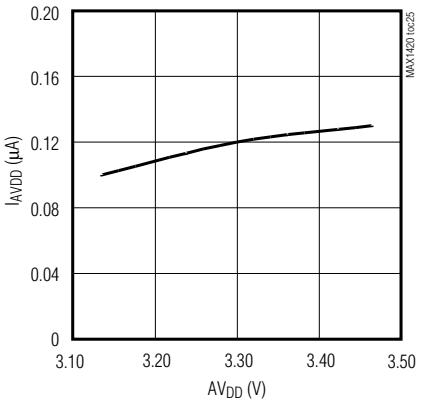
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



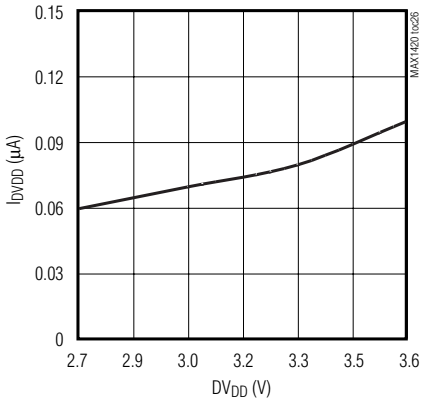
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



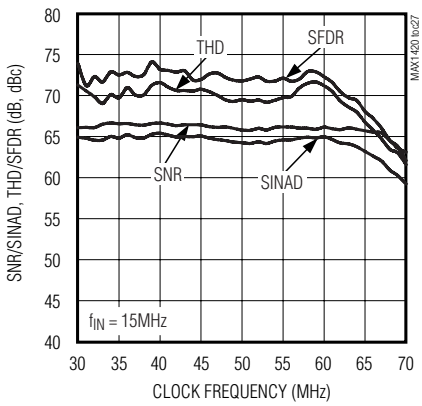
ANALOG POWER-DOWN CURRENT vs. ANALOG SUPPLY VOLTAGE



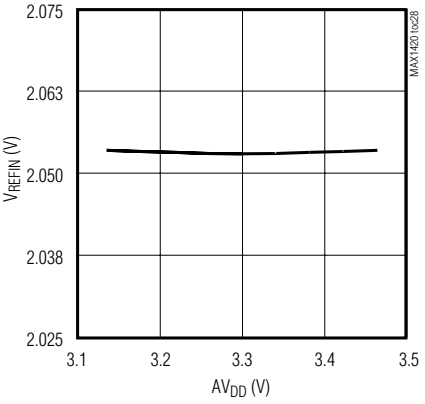
DIGITAL POWER-DOWN CURRENT vs. DIGITAL SUPPLY VOLTAGE



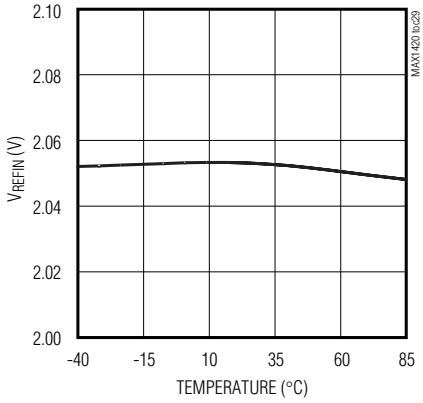
SNR/SINAD, THD/SFDR vs. CLOCK FREQUENCY



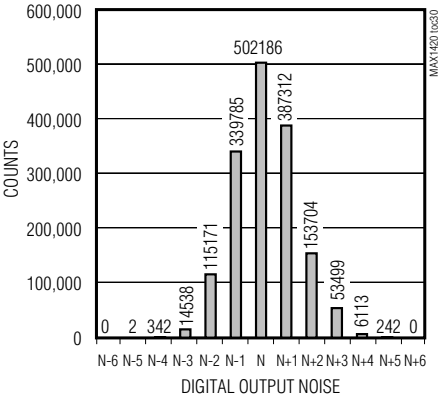
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



OUTPUT NOISE HISTOGRAM (DC INPUT)



Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 8, 9, 12, 13, 16, 19, 41, 48	AGND	Analog Ground. Connect all return paths for analog signals to AGND.
2, 3, 10, 11, 14, 15, 20, 42, 47	AV_{DD}	Analog Supply Voltage. For optimum performance, bypass to the closest AGND with a parallel combination of a 0.1µF and a 1nF capacitor. Connect a single 10µF and 1µF capacitor combination between A_{VDD} and A_{GND}.
6	INP	Positive Analog Signal Input
7	INN	Negative Analog Signal Input
17	CLK	Clock Frequency Input. Clock frequency input ranges from 100kHz to 60MHz.
18	$\overline{CLK}$	Complementary Clock Frequency Input. This input is used for differential clock inputs. If the ADC is driven with a single-ended clock, bypass $\overline{CLK}$ with a 0.1µF capacitor to AGND.
21, 31, 32	DV_{DD}	Digital Supply Voltage. For optimum performance, bypass to the closest DGND with a parallel combination of a 0.1µF and a 1nF capacitor. Connect a single 10µF and 1µF capacitor combination between D_{VDD} and D_{GND}.
22, 29, 30	DGND	Digital Ground
23–28	D0–D5	Digital Data Outputs. Data bits D0 through D5, where D0 represents the LSB.
33–38	D6–D11	Digital Data Outputs. D6 through D11, where D11 represents the MSB.
39	$\overline{OE}$	Output Enable Input. A logic “1” on $\overline{OE}$ places the outputs D0–D11 into a high-impedance state. A logic “0” allows for the data bits to be read from the outputs.
40	PD	Shutdown Input. A logic “1” on PD places the ADC into shutdown mode.
43	REFIN	External Reference Input. Bypass to AGND with a capacitor combination of 0.22µF in parallel with 1nF. REFIN can be biased externally to adjust reference levels and calibrate full-scale errors. To disable the internal reference, connect REFIN to AGND.
44	REFP	Positive Reference I/O. Bypass to AGND with a capacitor combination of 0.22µF in parallel with 1nF. With the internal reference disabled (REFIN = AGND), REFP should be biased to $V_{CML} + V_{DIFF} / 2$.
45	REFN	Negative Reference I/O. Bypass to AGND with a capacitor combination of 0.22µF in parallel with 1nF. With the internal reference disabled (REFIN = AGND), REFN should be biased to $V_{CML} - V_{DIFF} / 2$.
46	CML	Common-Mode Level Input. Bypass to AGND with a capacitor combination of 0.22µF in parallel with 1nF.

12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

Detailed Description

The MAX1420 uses a 12-stage, fully-differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Each sample moves through a pipeline stage every half-clock cycle, including the delay through the output latch. The latency is seven clock cycles.

A 2-bit (2-comparator) flash ADC converts the held-input voltage into a digital code. The following digital-to-analog converter (DAC) converts the digitized result back into an analog voltage, which is then subtracted from the original held-input signal. The resulting error signal is then multiplied by two, and the product is passed along to the next pipeline stage. This process is repeated until the signal has been processed by all 12 stages. Each stage provides a 1-bit resolution. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes.

Input Track-and-Hold Circuit

Figure 2 displays a simplified functional diagram of the input track-and-hold (T/H) circuit in both track-and-hold mode. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully-differential circuit passes the input signal to the two capacitors C2a and C2b through switches S4a and S4b. Switches S2a and S2b set the common mode for the operational transconductance amplifier (OTA) input, and open simultaneously with S1, sampling the input waveform. The resulting differential voltage is held on capacitors C2a and C2b. Switches S4a and S4b are then opened before S3a, S3b, S4C are closed. The OTA is used to charge capacitors C1a and C1b to the same values originally held on C2a and C2b. This value is then presented to the first stage quantizer and isolates the pipeline from the fast-changing input. The wide input bandwidth T/H amplifier allows the MAX1420 to track and sample/hold analog inputs of high frequencies beyond Nyquist. The analog inputs INP to INN can be driven either differentially or single-ended. Match the impedance of INP and INN and set the common-mode voltage to midsupply ($AV_{DD}/2$) for optimum performance.

Analog Input and Reference Configuration

The full-scale range of the MAX1420 is determined by the internally generated voltage difference between REFP ($AV_{DD}/2 + V_{REFIN}/4$) and REFN ($AV_{DD}/2 - V_{REFIN}/4$). The MAX1420's full-scale range is adjustable through REFIN, which provides high input impedance for this purpose. REFP, CML ($AV_{DD}/2$), and REFN are internally buffered low impedance outputs.

An internal 2.048V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure accommodates an internal reference, or externally applied buffered or unbuffered reference for appli-

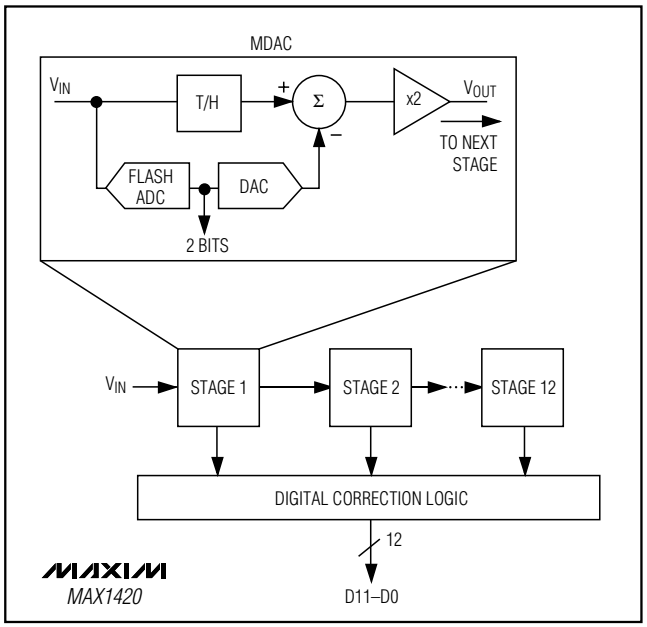


Figure 1. Pipelined Architecture—Stage Blocks

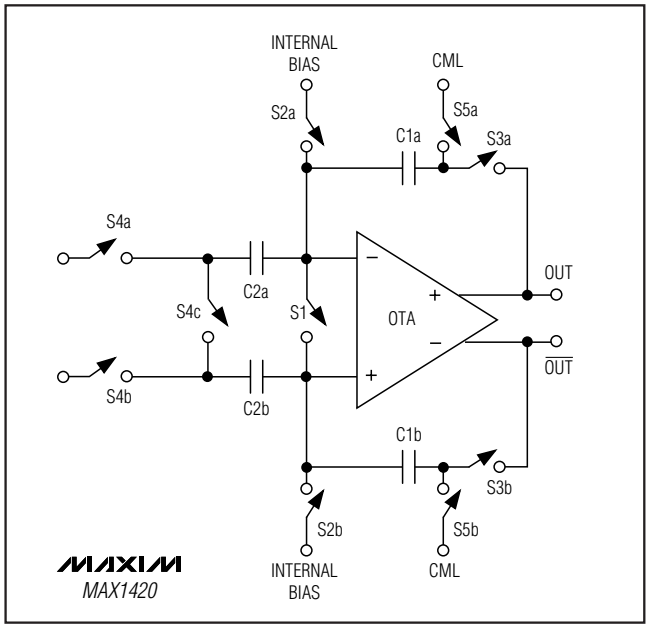


Figure 2. Internal Track-and-Hold Circuit

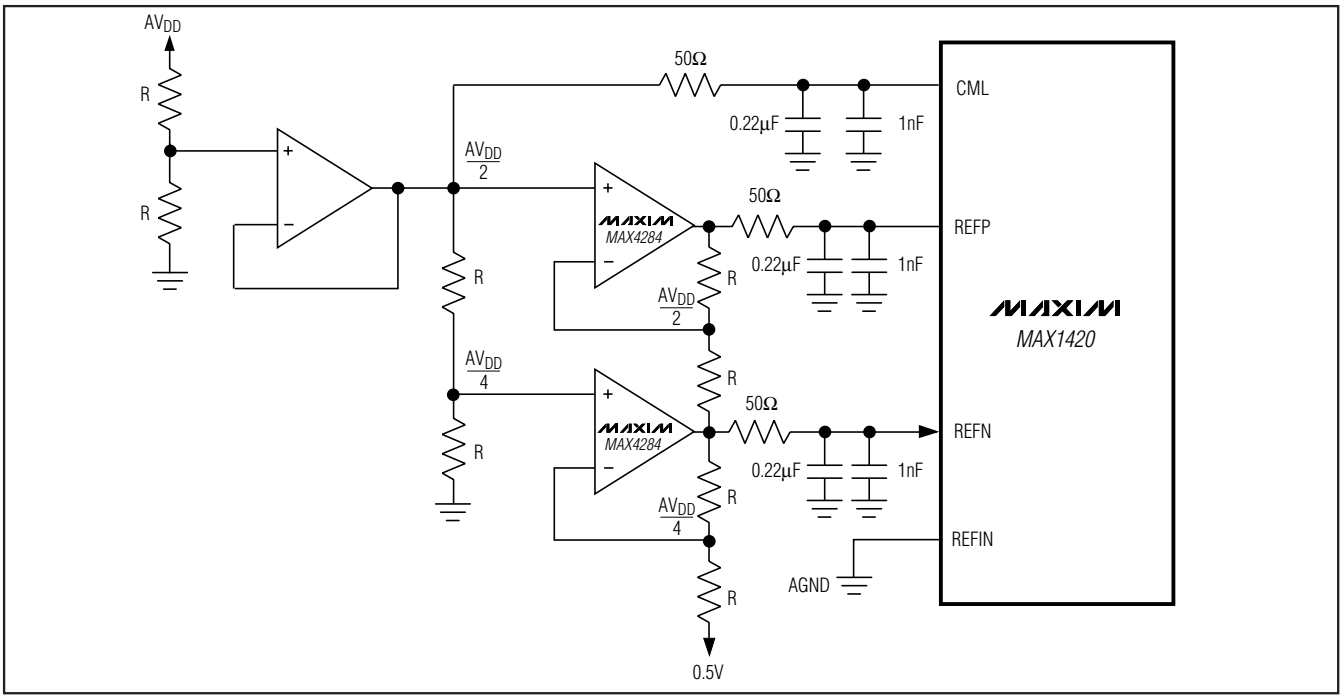


Figure 3. Unbuffered External Reference Drive—Internal Reference Disabled

cations that require increased accuracy and a different input voltage range.

The MAX1420 provides three modes of reference operation:

- Internal reference mode
- Buffered external reference mode
- Unbuffered external reference mode

In internal reference mode, the on-chip 2.048V bandgap reference is active and REFIN, REFP, CML, and REFN are left floating. For stability purposes, bypass REFIN, REFP, REFN and CML with a capacitor network of 0.22µF in parallel with a 1nF capacitor to AGND.

In buffered external reference mode, the reference voltage levels can be adjusted externally by applying a stable and accurate voltage at REFIN.

In unbuffered external reference mode, REFIN is connected to AGND, thereby deactivating the on-chip buffers of REFP, CML, and REFN. With their buffers shut down, these nodes become high impedance and can be driven by external reference sources, as shown in Figure 3.

Clock Inputs (CLK, $\overline{CLK}$)

The MAX1420's CLK and $\overline{CLK}$ inputs accept both differential and single-ended input operation and accept CMOS-compatible clock signals. If CLK is driven with a single-ended clock signal, bypass $\overline{CLK}$ with a 0.1µF capacitor to AGND. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (< 2ns). Sampling occurs on the rising edge of the clock signal, requiring this edge to have the lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the ADC according to the following relationship:

$$SNR_{dB} = 20 \times \log_{10} \frac{1}{2\pi \times f_{IN} \times t_{AJ}}$$

where f_{IN} represents the analog input frequency and t_{AJ} is the aperture jitter. Clock jitter is especially critical for high input frequency applications. The clock input should always be considered as an analog signal and routed away from any analog or digital signal lines.

The MAX1420 clock input operates with a voltage threshold set to $AV_{DD}/2$. Clock inputs must meet the specifications for high and low periods as stated in the *Electrical Characteristics*.

12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

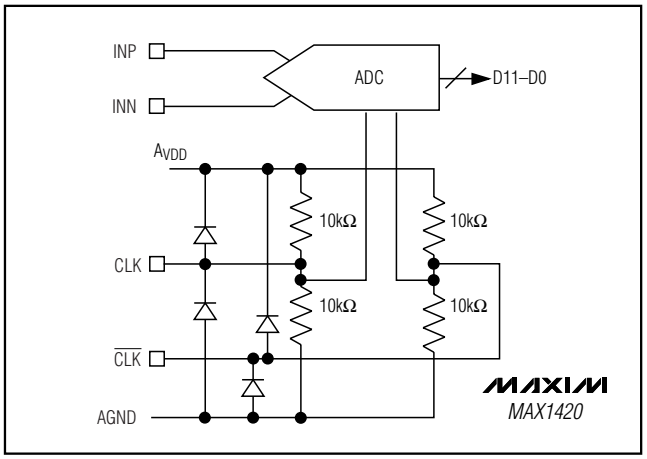


Figure 4. Simplified Clock Input Circuit

Figure 4 shows a simplified model of the clock input circuit. This circuit consists of two 10kΩ resistors to bias the common-mode level of each input. This circuit may be used to AC-couple the system clock signal to the MAX1420 clock input.

Output Enable ($\overline{OE}$), Power-Down (PD) and Output Data (D0–D11)

In addition to low operating power, the MAX1420 features two power-down modes: reference power-down and shutdown mode. In reference power-down, the internal bandgap reference is deactivated, which results in a typical 2mA supply current reduction. A full shutdown mode is available to maximize power savings during idle periods.

The MAX1420 provides parallel, offset binary, CMOS-compatible three-state outputs.

With $\overline{OE}$ high, the digital outputs enter a high-impedance state. If $\overline{OE}$ is held low with PD high, the outputs are latched at the last digital output code prior to the power-down. All data outputs, D0 (LSB) through D11 (MSB), are TTL/CMOS logic-compatible. There is a seven clock-cycle latency between any particular sample and its valid output data. The output coding is in offset binary format (Table 1).

The capacitive load on the digital outputs D0 through D11 should be kept as low as possible (≤10pF), to avoid large digital currents that could feed back into the analog portion of the MAX1420, thereby degrading its performance. The use of buffers (e.g., 74LVCH16244) on the digital outputs of the ADC can further isolate the digital outputs from heavy capacitive loads. To further improve the dynamic performance of the MAX1420, add small-series resistors of 100Ω to the digital output paths, close to the ADC.

Figure 5 displays the timing relationship between output enable and data output.

Table 1. MAX1420 Output Code for Differential Inputs

DIFFERENTIAL INPUT VOLTAGE*	DIFFERENTIAL INPUT	OFFSET BINARY
$V_{REF} \times 2047/2048$	+FULL SCALE - 1LSB	1111 1111 1111
$V_{REF} \times 2046/2048$	+FULL SCALE - 2LSB	1111 1111 1110
$V_{REF} \times 1/2048$	+ 1 LSB	1000 0000 0001
0	Bipolar Zero	1000 0000 0000
$-V_{REF} \times 1/2048$	- 1 LSB	0111 1111 1111
$-V_{REF} \times 2046/2048$	-FULL SCALE + 1 LSB	0000 0000 0001
$-V_{REF} \times 2047/2048$	-FULL SCALE	0000 0000 0000

** $V_{REF} = V_{REFP} - V_{REFN}$*

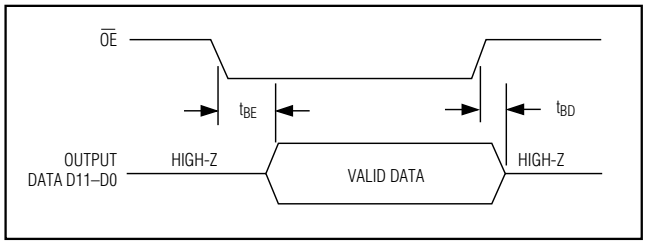


Figure 5. Output Enable Timing

System Timing Requirements

Figure 6 depicts the relationship between the clock input, analog input, and valid data output. The MAX1420 samples the analog input signal on the rising edge of CLK (falling edge of $\overline{CLK}$) and output data is valid seven clock cycles (latency) later.

Applications Information

Figure 7 depicts a typical application circuit containing a single-ended to differential converter. The internal reference provides an $AV_{DD}/2$ output voltage for level shifting purposes. The input is buffered and then split to a voltage follower and inverter. A lowpass filter at the input suppresses some of the wideband noise associated

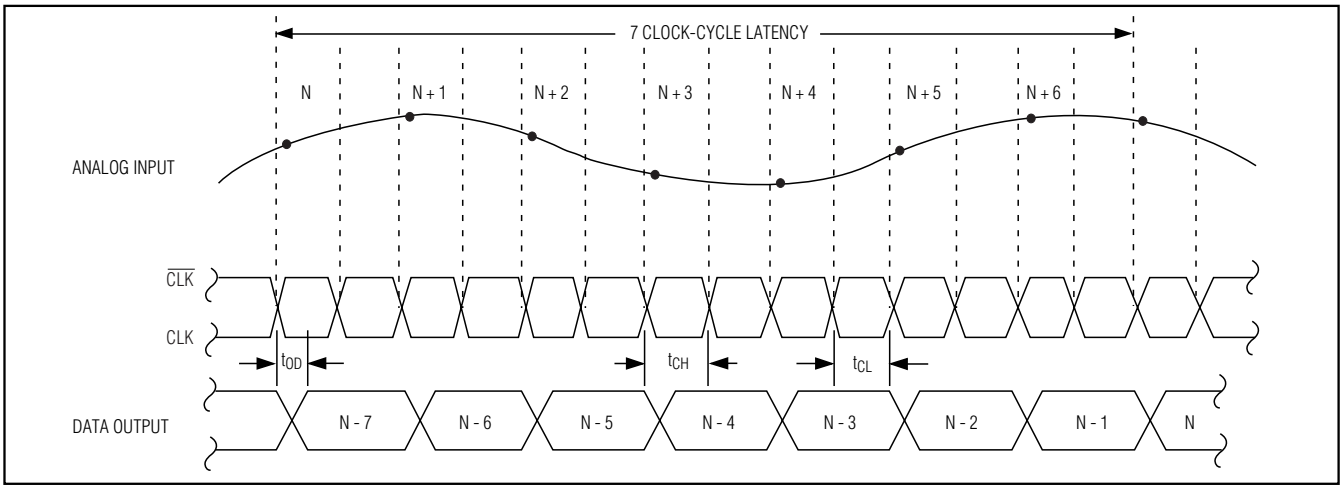


Figure 6. System and Output Timing Diagram

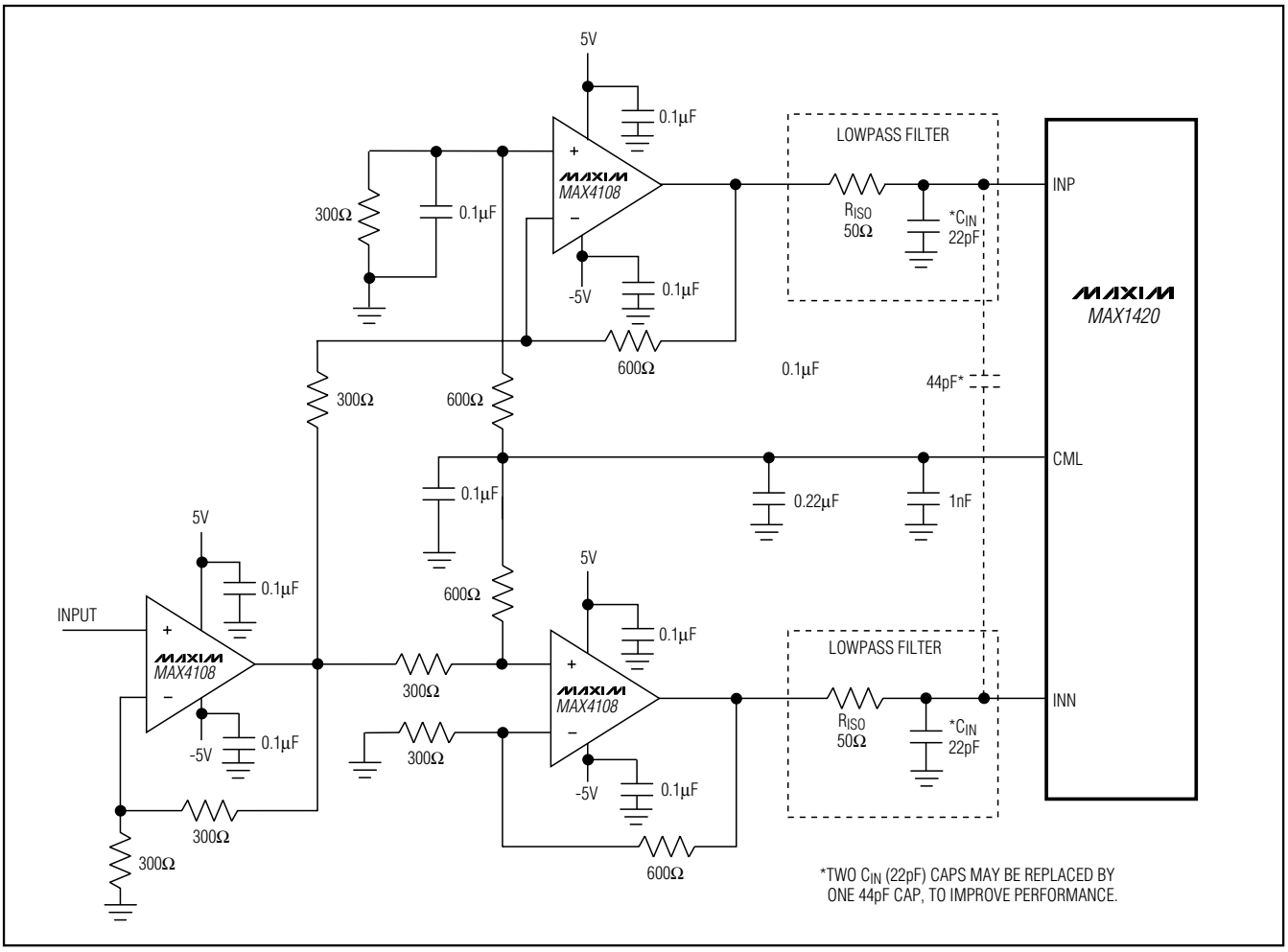


Figure 7. Typical Application Circuit for Single-Ended to Differential Conversion

12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

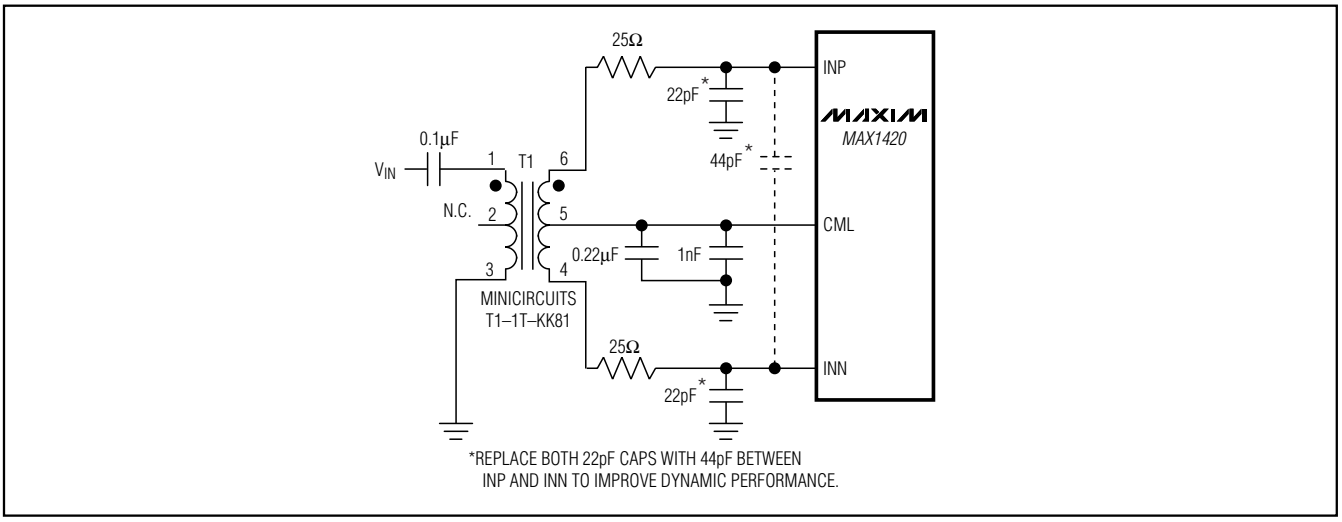


Figure 8. Using a Transformer for AC-Coupling

with high-speed op amps. Select the R_{ISO} and C_{IN} values to optimize the filter performance, to suit a particular application. For the application in Figure 7, an isolation resistor (R_{ISO}) of 50Ω is placed before the capacitive load to prevent ringing and oscillation. The 22pF C_{IN} capacitor acts as a small bypassing capacitor. Connecting C_{IN} from INN to INP may further improve dynamic performance.

Using Transformer Coupling

An RF transformer (Figure 8) provides an excellent solution to convert a single-ended signal to a fully differential signal, required by the MAX1420 for optimum performance. Connecting the center tap of the transformer to CML provides an $AV_{DD}/2$ DC level shift to the input. Although a 1:1 transformer is shown, a 1:2 or 1:4 step-up transformer may be selected to reduce the drive requirements.

In general, the MAX1420 provides better SFDR and THD with fully differential input signals over single-ended input signals, especially for very high input frequencies. In differential input mode, even-order harmonics are suppressed and each input requires only half the signal swing compared to single-ended mode.

Single-Ended AC-Coupled Input Signal

Figure 9 shows an AC-coupled, single-ended application, using a MAX4108 op amp. This configuration provides high speed, high bandwidth, low noise, and low distortion to maintain the integrity of the input signal.

Grounding, Bypassing, and Board Layout

The MAX1420 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, preferably on the same side of the board as the ADC, using surface-mount devices for minimum inductance. Bypass REFP, REFN, REFIN, and CML with a parallel network of 0.22µF capacitors and 1nF to AGND. AV_{DD} should be bypassed with a similar network of a 10µF bipolar capacitor in parallel with two ceramic capacitors of 1nF and 0.1µF. Follow the same rules to bypass the digital supply DV_{DD} to DGND. Multilayer boards with separate ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arrangement to match the physical location of the analog ground (AGND) and the digital ground (DGND) on the ADCs package. Join the two ground planes at a single point, such that the noisy digital ground currents do not interfere with the analog ground plane. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground plane (e.g., downstream output buffer or DSP ground plane). Route high-speed digital signal traces away from sensitive analog traces and remove digital ground and power planes from underneath digital outputs. Keep all signal lines short and free of 90 degree turns.

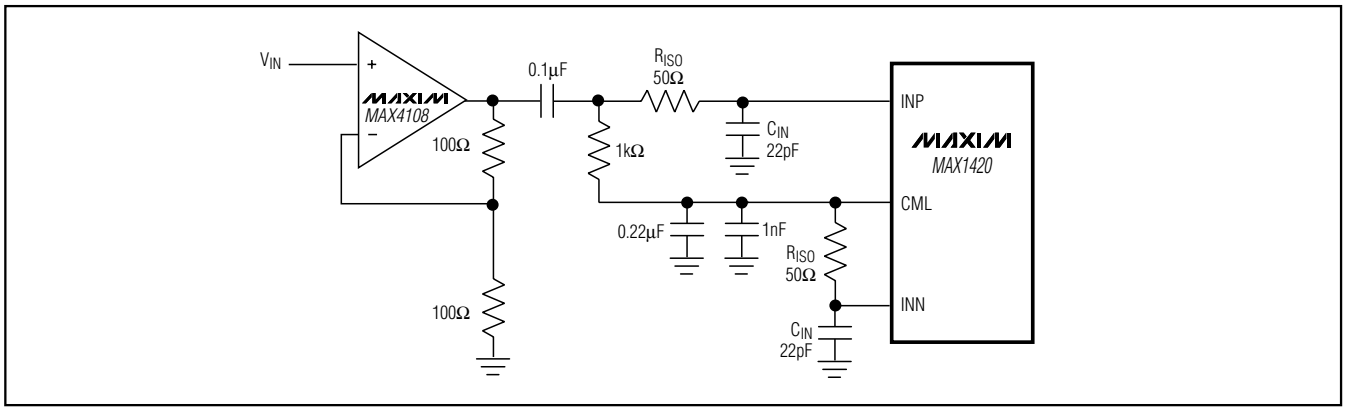


Figure 9. Single-Ended AC-Coupled Input Signal

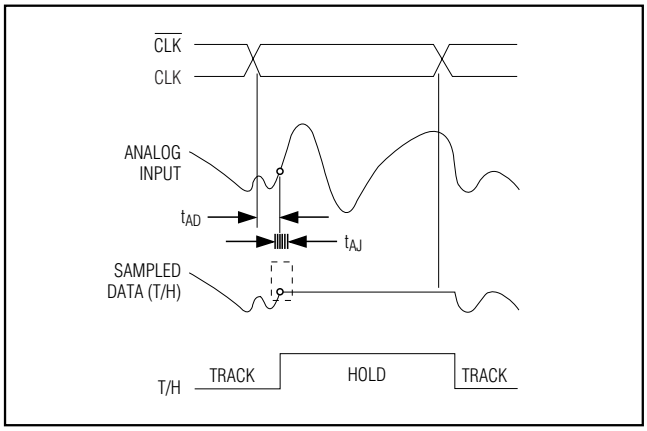


Figure 10. T/H Aperture Timing

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight-line. This straight-line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function once offset and gain errors have been nullified. The static linearity parameters for the MAX1420 are measured using the best straight-line fit method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step-width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes.

Dynamic Parameter Definitions

Aperture Jitter

Figure 10 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken (Figure 10).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADCs resolution (N-bits):

$$SNR_{MAX} = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, e.g., thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is computed from:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first four harmonics of the input signal to the fundamental itself. This is expressed as:

$$THDdB = 20 \times \log10 \left(\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2 \right)}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

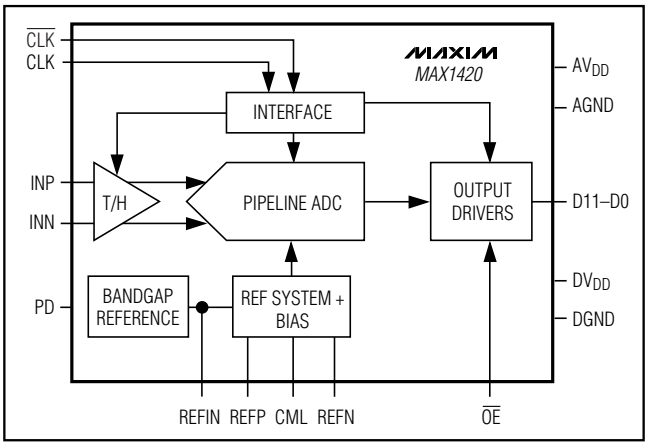
Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

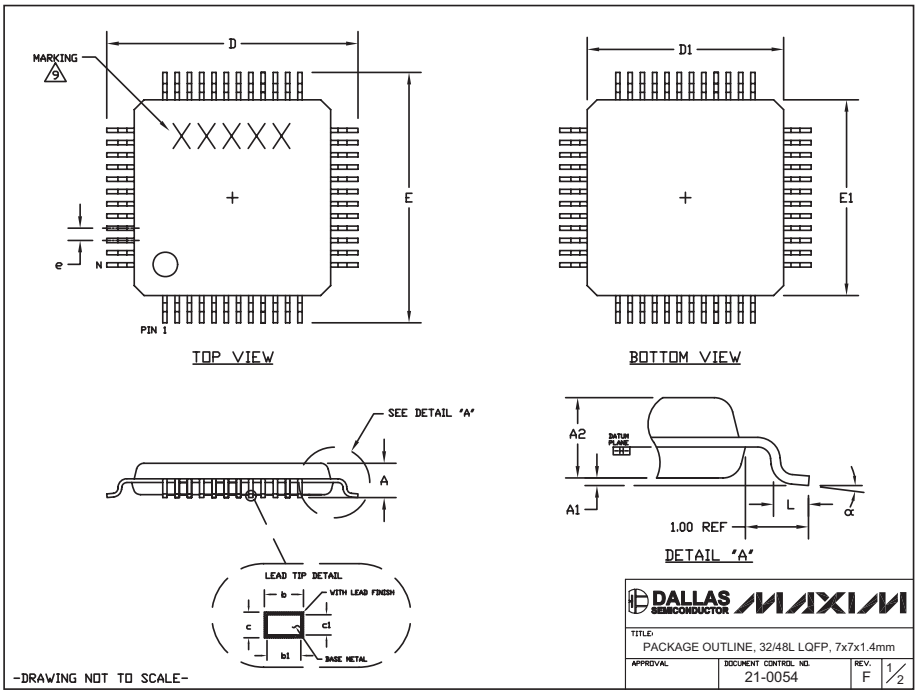
Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -6.5dB full scale.

Functional Diagram



Package Information



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

JEDEC VARIATION				
	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A1	0.05	0.15	0.05	0.15
A2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°
PKG. CODES	C32-1; C32-2; C48-1; C48-2; C48-3; C48-4F; C48-5; C48-6; C48-9F			

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DALLAS SEMICONDUCTOR MAXIM

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