19-2697; Rev 0; 12/02

MAXIM

Low-Jitter 155MHz/622MHz Clock Generator

General Description

The MAX3672 is a low-jitter 155MHz/622MHz reference clock generator IC designed for system clock distribution and frequency synchronization in OC-48 and OC-192 SONET/SDH and WDM transmission systems. The MAX3672 integrates a phase/frequency detector, an operational amplifier (op amp), prescaler dividers, and input/output buffers. Using an external VCO, the MAX3672 can be configured easily as a phase-lock loop with bandwidth programmable from 30Hz to 10kHz.

The MAX3672 operates from a single +3.3V or +5.0V supply and dissipates 150mW (typ) at 3.3V. The operating temperature range is -40°C to +85°C.

Applications

OC-12 to OC-192 SONET/WDM Transport Systems

Clock Jitter Clean-Up and Frequency Synchronization

Frequency Conversion

System Clock Distribution

Features

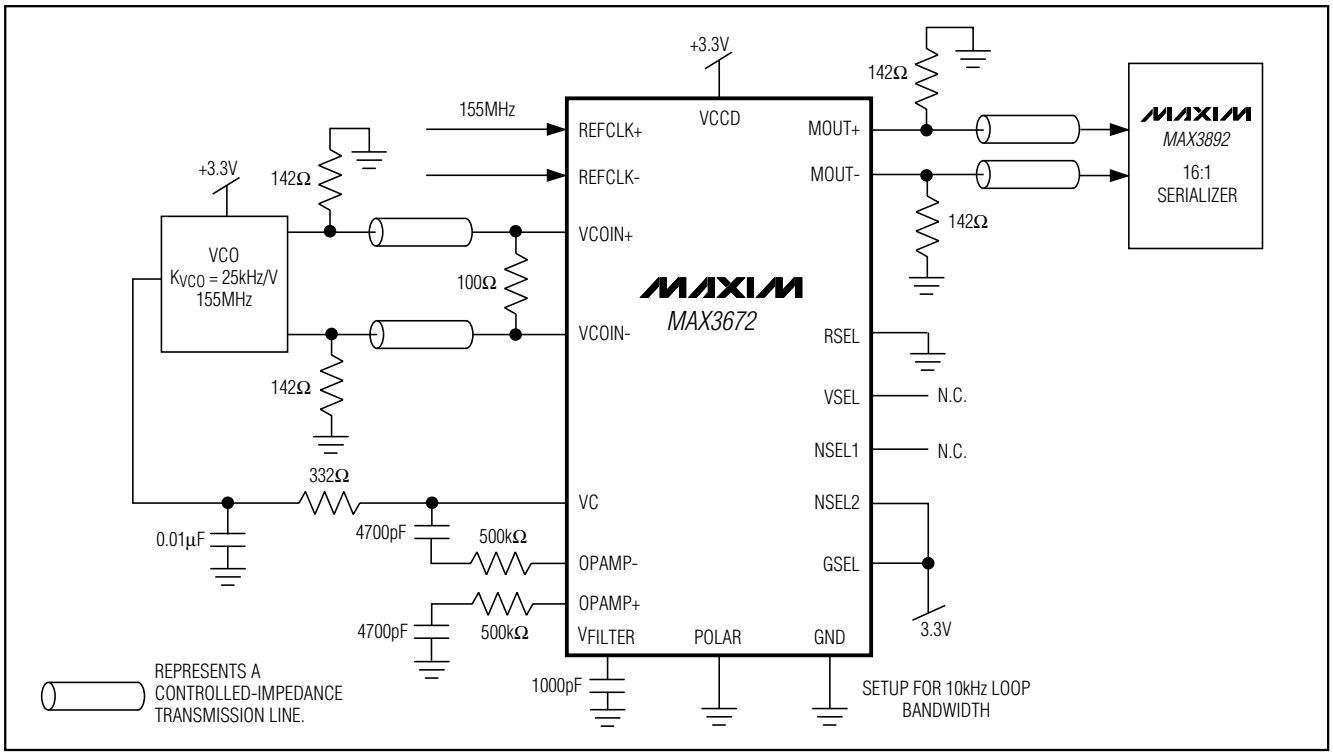
- **Single +3.3V or +5.0V Supply**
- **Power Dissipation: 150mW at +3.3V Supply**
- **External VCO Center Frequencies (f_{VCO}): 155MHz to 700MHz**
- **Reference Clock Frequencies: f_{VCO}, $f_{VCO}/2$, $f_{VCO}/4$, $f_{VCO}/8$, $f_{VCO}/32$**
- **Main Clock Output Frequency: f_{VCO}**
- **Optional Output Clock Frequencies: f_{VCO}, $f_{VCO}/2$, $f_{VCO}/4$, $f_{VCO}/8$**
- **Low Intrinsic Jitter: <0.4ps$_{RMS}$**
- **Loss-of-Lock Indicator**
- **PECL Clock Output Interface**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3672E/D	-40°C to +85°C	Dice*

**Dice are designed to operate from -40° to +85°C, but are tested and guaranteed at T_A = +25° only.*

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....-0.5V to +7.0V
Voltage at C2+, C2-, THADJ, CTH, NSEL1, NSEL2, GSEL, $\overline{LOL}$, RSEL, REFCLK-, REFCLK+, VSEL, VCOIN+, VCOIN-, VC, POLAR, PSEL1, PSEL2, COMP, OPAMP+, OPAMP- .....-0.5V to (V_{CC} + 0.5V)
Voltage at V_{FILTER} .....-0.5V to +3.0V
PECL Output Current (MOUT+, MOUT-, POUT+, POUT-).....56mA
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range. .....-65°C to +160°C
Die-Attach Process Temperature.....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10% or V_{CC} = +5.0V ±10%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 2)		50	72	mA
INPUT SPECIFICATIONS (REFCLK±, VCOIN±)						
Input High Voltage	V_{IH}		V_{CC} - 1.16		V_{CC} - 0.88	V
Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.48	V
Input Bias Voltage				V_{CC} - 1.3		V
Common-Mode Input Resistance			7.2	11.5	17.5	kΩ
Differential Input Resistance			12.0	21.0	32.5	kΩ
Differential Input Voltage Swing		AC-coupled	300		1900	mV_{P-P}
PECL OUTPUT SPECIFICATIONS						
Output High Voltage	V_{OH}	0°C to +85°C	V_{CC} - 1.025		V_{CC} - 0.88	V
		-40°C to 0°C	V_{CC} - 1.085		V_{CC} - 0.88	
Output Low Voltage	V_{OL}	0°C to +85°C	V_{CC} - 1.81		V_{CC} - 1.62	V
		-40°C to 0°C	V_{CC} - 1.83		V_{CC} - 1.556	
TTL SPECIFICATIONS						
Output High Voltage	V_{OH}	Sourcing 20µA	2.4		V_{CC}	V
Output Low Voltage	V_{OL}	Sinking 2mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V ±10% or V_{CC} = +5.0V ±10%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATIONAL AMPLIFIER SPECIFICATIONS (Note 3)						
Op Amp Output Voltage Range	V_O	V_{CC} = +3.3V ±10%	0.3		V_{CC} - 0.3	V
		V_{CC} = +5.0V ±10%	0.5		V_{CC} - 0.5	
Op Amp Input Offset Voltage	$\lvert V_{OS} \rvert$				3	mV
Op Amp Open-Loop Gain	A_{OL}			90		dB
PHASE FREQUENCY DETECTOR (PFD)/CHARGE-PUMP (CP) SPECIFICATIONS (Note 4)						
Full-Scale PFD/CP Output Current	$\lvert I_{PD} \rvert$	High gain	16.0	20	24.4	µA
		Low gain	4.0	5	6.2	
PFD/CP Offset Current		High gain			0.80	% $\lvert I_{PD} \rvert$
		Low gain			1.08	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10% or V_{CC} = +5.0V ±10%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OUTPUT SPECIFICATIONS						
Clock Output Frequency					700	MHz
Optional Clock Output Frequency		f_{VCO} = 622MHz		622/311/ 155/78		MHz
		f_{VCO} = 155MHz		155/78/ 38/19		
Clock Output Rise/Fall Time		Measured from 20% to 80%			280	ps
Clock Output Duty Cycle		(Note 6)	45		55	%
NOISE SPECIFICATIONS						
Random Noise Voltage at Loop-Filter Output	V_{NOISE}	Freq > 1kHz (Note 7)			1.14	$\mu V_{RMS}/\sqrt{Hz}$
Spurious Noise Voltage at Loop-Filter Output		(Note 8)		50		μV_{RMS}
Power-Supply Rejection at Loop-Filter Output	PSR	(Note 9)	30			dB
REFERENCE CLOCK INPUT SPECIFICATIONS						
Reference Clock Frequency				622/ 155/78/ 19	700	MHz
Reference Clock Duty Cycle			30		70	%

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V ±10% or V_{CC} = +5.0V ±10%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 5)

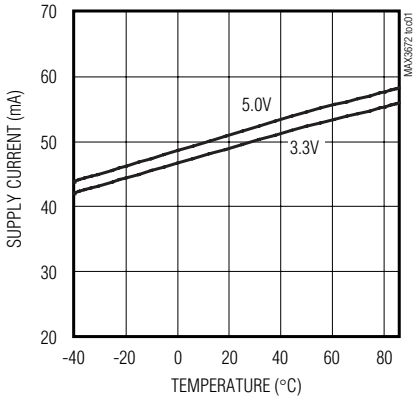
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PLL SPECIFICATIONS						
PLL Jitter Transfer Bandwidth	BW	(Note 10)	30		10,000	Hz
Jitter Transfer Peaking		$F_{JITTER} \leq BW$ (Note 11)			0.1	dB
OPAMP SPECIFICATION						
Unity-Gain Bandwidth				7		MHz
VCO INPUT SPECIFICATIONS						
VCO Input Frequency	f_{VCO}			622/155	700	MHz
VCO Input Slew Rate			0.5			V/ns

Note 1: Specifications at -40°C are guaranteed by design and characterization.
Note 2: Measured with PECL outputs unterminated.
Note 3: OPAMP specifications met with 10kΩ load to ground or 5kΩ load to V_{CC} (POLAR = 0 and POLAR = V_{CC}).
Note 4: PFD/CP currents are measured from pins OPAMP+ to OPAMP-. See Table 4 for gain settings.
Note 5: AC characteristics are guaranteed by design and characterization.
Note 6: Measured with 50% VCO input duty cycle.
Note 7: Random noise voltage at op amp output with 800kΩ resistor connected between VC and OPAMP-, PFD/CP gain (K_{PD}) = 5µA/UI, and POLAR = 0. Measured with the PLL open loop and no REFCLK or VCO input.
Note 8: Spurious noise voltage due to PFD/CP output pulses measured at op amp output with R_1 = 800kΩ, K_{PD} = 5µA/UI, and compare frequency 400 times greater than the higher-order pole frequency (see the *Design Procedure* section).
Note 9: PSR measured with a 100mV_{P-P} sine wave on V_{CC} in a frequency range from 100Hz to 2MHz. External resistors R_1 matched to within 1%, external capacitors C_1 matched to within 10%. Measured closed loop with PLL bandwidth set to 200Hz.
Note 10: The PLL 3dB bandwidth is adjusted from 30Hz to 10kHz by changing external components R_1 and C_1, by selecting the internal programmable divider ratio and phase-detector gain. Measured with VCO gain of 150ppm/V and C_1 limited to 2.2µF.
Note 11: When input jitter frequency is above PLL transfer bandwidth (BW), the jitter transfer function rolls off at -20dB/decade.

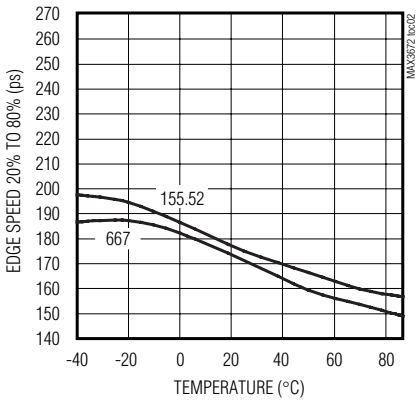
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

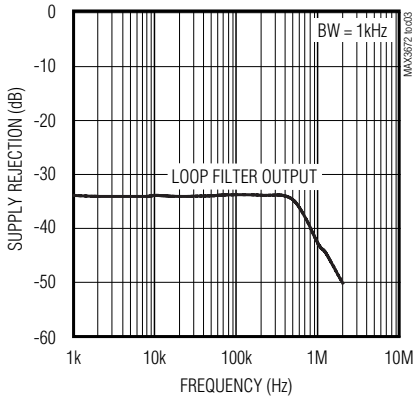
SUPPLY CURRENT vs. TEMPERATURE



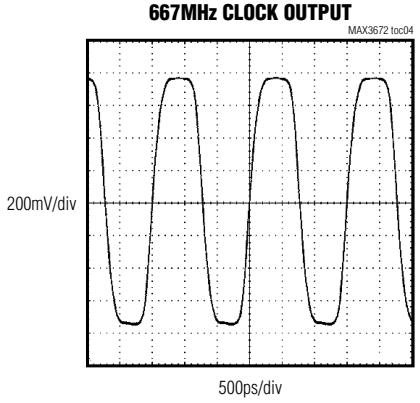
OUTPUT CLOCK EDGE SPEED vs. TEMPERATURE



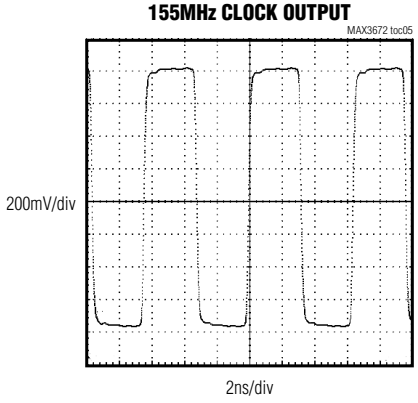
POWER-SUPPLY REJECTION vs. FREQUENCY



667MHz CLOCK OUTPUT



155MHz CLOCK OUTPUT

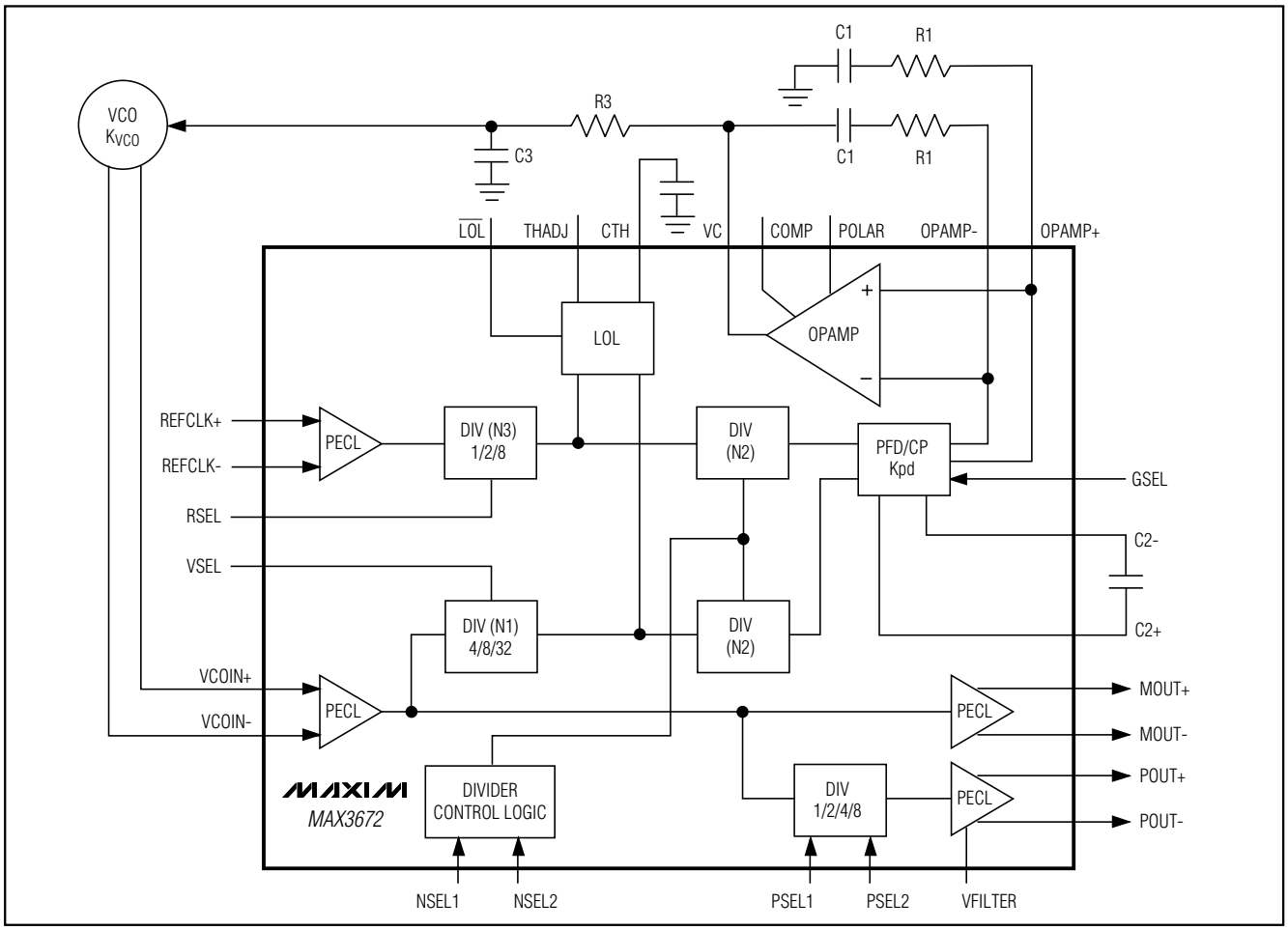


Low-Jitter 155MHz/622MHz Clock Generator

Pad Description

PAD	NAME	FUNCTION
1	C2+	Positive Filter Input. External capacitor connected between C2+ and C2- used for setting the higher order pole frequency (see the *Setting the Higher-Order Poles* section).
2	C2-	Negative Filter Input. External capacitor connected between C2+ and C2- used for setting the higher order pole frequency (see the *Setting the Higher-Order Poles* section).
3, 10, 16	VCCD	Positive Digital Supply Voltage
4	THADJ	Threshold Adjust Input. Used to adjust the loss-of-lock threshold (see the $\overline{LOL}$ *Setup* section).
5, 12, 18, 27, 33	GND	Ground
6	CTH	Threshold Capacitor Input. Connect capacitor connected between CTH and ground to control the loss-of-lock conditions (see the $\overline{LOL}$ *Setup* section).
7	NSEL1	Divide Selector 1 Input. Three-level pin used to set the frequency divider ratio (N_2) (Table 3).
8	NSEL2	Divide Selector 2 Input. Three-level pin used to set the frequency divider ratio (N_2) (Table 3).
9	GSEL	Gain Selector Input. Three-level pin used to set the phase-detector gain (Kpd) (Table 4).
11	$\overline{LOL}$	Loss of Lock. $\overline{LOL}$ signals a TTL low when the reference frequency differs from the VCO frequency. $\overline{LOL}$ signals a TTL high when the reference frequency equals the VCO frequency.
13	RSEL	Reference Clock Selector Input. Three-level pin used to set the pre-divider ratio (N_3) for the input reference clock (Table 1).
14	REFCLK+	Positive Reference Clock Input, PECL
15	REFCLK-	Negative Reference Clock Input, PECL
17	VSEL	VCO Clock Selector Input. Three-level pin used to set the pre-divider ratio (N_1) for the input VCO clock (Table 2).
19	POUT-	Negative Optional Clock Output, PECL
20	POUT+	Positive Optional Clock Output, PECL
21, 24	VCCO	Positive Supply Voltage for PECL Outputs
22	MOUT-	Negative Main Clock Output, PECL
23	MOUT+	Positive Main Clock Output, PECL
25	VCOIN-	Negative VCO Clock Input, PECL
26	VCOIN+	Positive VCO Clock Input, PECL
28	VFILTER	Optional Noise Filter. Connect an external capacitor to reduce PECL output noise (see the *Typical Application Circuit*).
29	VC	Control Voltage Output. The voltage output from the op amp that controls the VCO.
30	POLAR	Polarity Control of Op Amp Input. POLAR = GND for VCOs with positive-gain transfer. POLAR = V_{CC} for VCOs with negative-gain transfer.
31	PSEL1	Optional Clock Selector 1 Input. Sets the divider ratio for the optional clock output (Table 5).
32	PSEL2	Optional Clock Selector 2 Input. Sets the divider ratio for the optional clock output (Table 5).
34	VCCA	Positive Analog Supply Voltage for the Charge Pump and Op Amp
35	COMP	Compensation Control Input. Op Amp Compensation Reference Control Input. COMP = GND for VCOs whose control pin is V_{CC} referenced. COMP = V_{CC} for VCOs whose control pin is GND referenced.
36	OPAMP-	Negative Op Amp Input, POLAR = GND
37	OPAMP+	Positive Op Amp Input, POLAR = GND

Functional Diagram



Detailed Description

The MAX3672 contains all the blocks needed to form a PLL except for the VCO, which must be supplied separately. The MAX3672 consists of input buffers for the reference clock and VCO, input and output clock-divider circuitry, LOL detection circuitry phase detector, gain-control logic, a phase-frequency detector and charge pump, an op amp, and PECL output buffers.

This device is designed to clean up the noise on the reference clock input and provide a low-jitter system clock output. This device also supports frequency conversion.

Input Buffer for Reference Clock and VCO

The MAX3672 contains differential inputs for the reference clock and the VCO. These high impedance inputs can be DC-coupled and are internally biased with so that they can be AC-coupled (Figure 1 in the *Interface Schematic* section). A single-ended VCO or reference clock can also be applied.

Input and Output Clock-Divider Circuitry

The pre-dividers scale the input frequencies of the VCO and reference clock. Clock-divider ratios N1 and N3 must be chosen so that the output frequencies of the pre-dividers are equal. The maximum allowable pre-divider output frequency is 77.76MHz (Table 1).

The main dividers (N2) facilitate tuning the loop bandwidth by setting the frequency divider ratio. The divider control logic can be programmed to divide from 1 to 256 in binary multiples (Table 3). The POUT output buffer is preceded by a clock divider that scales the main clock output by 1, 2, 4, or 8 to provide an optional clock.

Low-Jitter 155MHz/622MHz Clock Generator

$\overline{LOL}$ Detection Circuitry

The MAX3672 incorporates a loss-of-lock ($\overline{LOL}$) monitor that consists of an XOR gate, filter, and comparator with adjustable threshold (see the *$\overline{LOL}$ Setup* section). A loss-of-lock condition is signaled with a TTL low when the reference clock frequency differs from the VCO frequency.

Phase-Frequency Detector and Charge Pump

The phase-frequency detector incorporated into the MAX3672 produces pulses proportional to the phase difference between the reference clock and the VCO input. The charge pump converts this pulse train to a current signal that is fed to the op amp. The phase detector gain can be set to either 5µA/UI or 20µA/UI with the GSEL input (Table 4).

Op Amp

The op amp is used to form an active PLL loop filter capable of driving the VCO control voltage input. Using the POLAR input, the op amp input polarity can be selected to work with VCOs having positive or negative gain-transfer functions. The COMP pin selects the op amp internal compensation. Connect COMP to ground if the VCO control voltage is V_{CC} referenced. Connect COMP to V_{CC} if the VCO control voltage is ground referenced.

Design Procedure

Setting Up the VCO and Reference Clock

The MAX3672 accepts a range of reference clock and VCO frequencies. The RSEL and VSEL inputs must be set so that the output frequencies of the reference clock and VCO pre-dividers are equal. Table 1 shows the divider ratios and pre-divider output frequencies for various reference clock and VCO frequencies.

Setting the Loop Bandwidth

To eliminate jitter present on the reference clock, the proper selection of loop bandwidth is critical. If the total output jitter is dominated by the noise at the reference clock input, then lowering the loop bandwidth will reduce system jitter. The loop bandwidth (K) is a function of the VCO gain (K_{VCO}), the gain of the phase detector (K_{PD}), the loop filter resistor (R_1), and the total feedback-divider ratio (N = N1 × N2). The loop bandwidth of the MAX3672 can be approximated by:

$$K = \frac{K_{PD} R_1 K_{VCO}}{2\pi N}$$

For stability, a zero must be added to the loop in the form of resistor R_1 in series with capacitor C_1 (see the *Functional Diagram*). The location of the zero can be approximated as:

$$f_Z = \frac{1}{2\pi R_1 C_1}$$

Because of the second-order nature of the PLL jitter transfer, peaking will occur and is proportional to f_Z/K. For certain applications, it may be desirable to limit jitter peaking in the PLL passband region to less than 0.1dB. This can be achieved by setting $f_Z \le K/100$.

A more detailed analysis of the loop filter is located in application note HFDN-13.0 on www.maxim-ic.com.

Table 1. VCO and Reference Clock Setup

F_{VOC} (MHz)	F_{REF} (MHz)	VSEL INPUT	VCO DIVIDER N1	RSEL INPUT	REFERENCE-CLOCK DIVIDER N3	PRE-DIVIDER OUTPUT FREQUENCY (MHz)
622.08	622.08	OPEN	8	GND	8	77.76
622.08	155.52	OPEN	8	OPEN	2	77.76
622.08	77.76	OPEN	8	V_{CC}	1	77.76
622.08	19.44	GND	32	V_{CC}	1	19.44
155.52	622.08	—	—	—	—	—
155.52	155.52	OPEN	8	GND	8	19.44
155.52	77.76	V_{CC}	4	OPEN	2	38.88
155.52	19.44	OPEN	8	V_{CC}	1	19.44

Table 2. RSEL and VSEL Settings

INPUT PIN VSEL	VCO DIVIDER N1	INPUT PIN RSEL	REFERENCE-CLOCK DIVIDER N3
V_{CC}	4	V_{CC}	1
OPEN	8	OPEN	2
GND	32	GND	8

Table 3. Divider Logic Setup

INPUT PIN NSEL1	INPUT PIN NSEL2	DIVIDER RATIO N_2
V_{CC}	V_{CC}	1
OPEN	V_{CC}	2
GND	V_{CC}	4
V_{CC}	OPEN	8
OPEN	OPEN	16
GND	OPEN	32
V_{CC}	GND	64
OPEN	GND	128
GND	GND	256

Table 4. Phase Detector Gain Setup

INPUT PIN GSEL	Kpd (µA/UI)
OPEN or V_{CC}	20
GND	5

Table 5. Optional Clock Setup

INPUT PIN PSEL1	INPUT PIN PSEL2	VCO TO POUT DIVIDER RATIO
V_{CC}	V_{CC}	1
GND	V_{CC}	2
V_{CC}	GND	4
GND	GND	8

Setting the Higher-Order Poles

Spurious noise is generated by the phase detector switching at the compare frequency, where $f_{COMPARE} = f_{VCO}/(N_1 \times N_2)$. Reduce the spurious noise from the digital phase detector by placing a higher-order pole (HOP) at a frequency much less than the compare frequency. The HOP should, however, be placed high enough in frequency that it does not decrease the overall loop-phase margin and impact jitter peaking. These two conditions can be met by selecting the HOP frequency to be $(K \times 4) < f_{HOP} < f_{COMPARE}$, where K is the loop bandwidth.

The HOP can be implemented either by providing a compensation capacitor C_2, which produces a pole at:

$$f_{HOP} = \frac{1}{2\pi(20k\Omega)(C_2)}$$

or by adding a lowpass filter, consisting of R_3 and C_3, directly on the VCO tuning port, which produces a pole at:

$$f_{HOP} = \frac{1}{2\pi R_3 C_3}$$

Using R_3 and C_3 might be preferable for filtering more noise in the PLL, but it might still be necessary to provide filtering through C_2 when using large values of R_1 and $N_1 \times N_2$, to prevent clipping in the op amp.

Setting the Optional Output

The MAX3672 optional clock output can be set to binary subdivisions of the main clock frequency. The PSEL1 and PSEL2 pins control the binary divisions. Table 5 shows the pin configuration and possible divider ratios.

Applications Information

PECL Interfacing

The MAX3672 outputs (MOUT+, MOUT-, POUT+, POUT-) are designed to interface with PECL signal levels and should be biased appropriately. Proper termination requires an external circuit that provides a Thevenin equivalent of 50Ω to VCC - 2.0V and controlled-impedance transmission lines. To ensure best performance, the differential outputs must have balanced loads. If the optional clock output is not used, the output can be left floating to save power.

Layout

The MAX3672 performance can be significantly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the reference and VCO clock signals. Power-supply decoupling should be placed as close to the die as possible. Take care to isolate the input from the output signals to reduce feedthrough.

VCO Selection

The MAX3672 is designed to accommodate a wide range of VCO gains, positive or negative transfer slopes, and V_{CC}-referenced or ground-referenced control voltages. These features allow the user a wide range of options in VCO selection; however, the proper VCO must be selected to allow the clock generator circuitry to operate at the optimum levels. When selecting

Interface Schematics

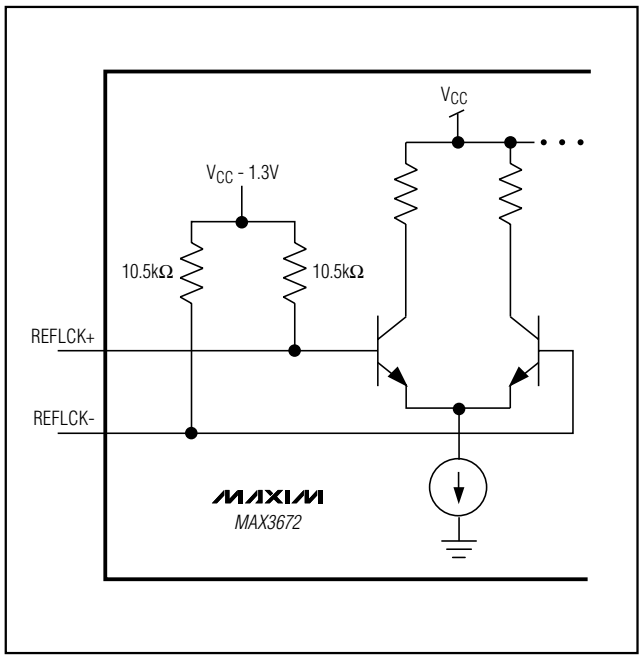


Figure 1. Input Interface

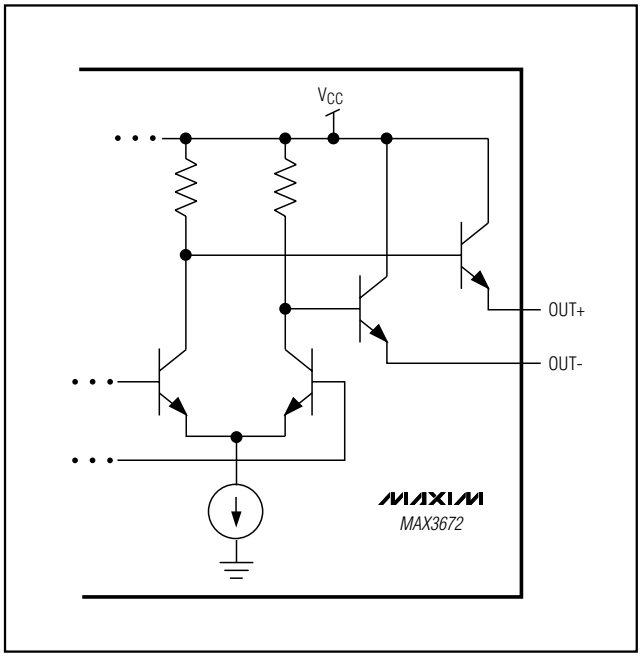


Figure 2. Output Interface

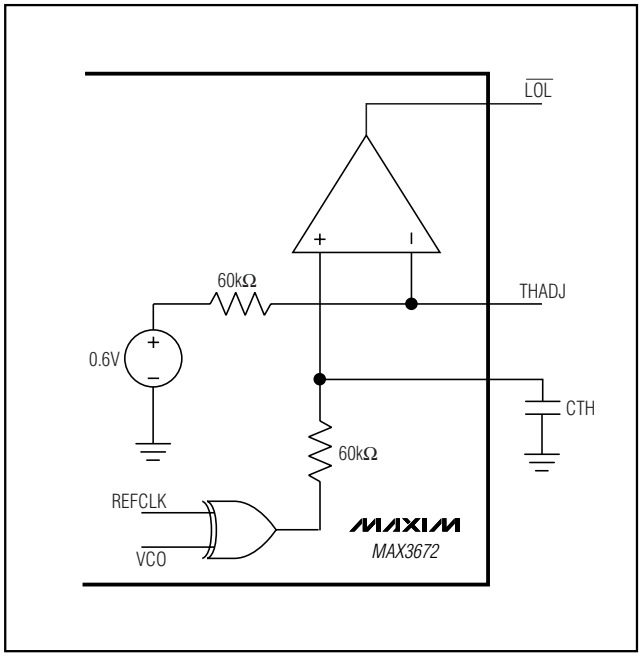


Figure 3. Loss-of-Lock Indicator

a VCO, the user needs to take into account the VCO's phase noise and modulation bandwidth. Phase noise is important because the phase noise above the PLL bandwidth is dominated by the VCO noise performance. The modulation bandwidth of the VCO contributes an additional higher-order pole (HOP) to the system and should be greater than the HOP set with the external filter components.

Noise Performance Optimization

Depending on the application, there are many different ways to optimize the PLL performance. The following are general guidelines to improve the noise on the system output clock.

1) If the reference clock noise dominates the total system-clock output jitter, then decreasing the loop bandwidth (K) reduces the output jitter.
2) If the VCO noise dominates the total system clock output jitter, then increasing the loop bandwidth (K) reduces the output jitter.
3) Smaller total divider ratio (N1 × N2), lower HOP, and smaller R_1 reduce the spurious output jitter.
4) Smaller R_1 reduces the random noise due to the op amp.

Bond Pad Coordinates

PAD	PAD COORDINATES (µm)	
	X	Y
1	50.8	1557.3
2	50.8	1408.8
3	50.8	1179.3
4	50.8	1028.1
5	50.8	874.2
6	50.8	720.4
7	50.8	566.5
8	50.8	412.6
9	50.8	258.7
10	266.8	50.8
11	420.7	50.8
12	574.6	50.8
13	728.5	50.8
14	882.4	50.8
15	1036.2	50.8
16	1190.1	50.8
17	1344	50.8
18	1549.2	50.8
19	1792.2	256
20	1792.2	409.9
21	1792.2	563.8
22	1792.2	717.7
23	1792.2	871.6
24	1792.2	1025.4
25	1792.2	1179.3
26	1792.2	1333.2
27	1792.2	1530.3
28	1792.2	1692.3
29	1565.4	1692.3
30	1411.5	1692.3
31	1257.6	1692.3
32	1103.7	1692.3
33	893.2	1692.3
34	685.3	1692.3
35	531.4	1692.3
36	377.5	1692.3
37	223.6	1692.3

$\overline{LOL}$ Setup

The $\overline{LOL}$ output indicates if the PLL has locked onto the reference clock using an XOR gate and comparator. The comparator threshold can be adjusted with THADJ, and the XOR gate output can be filtered with a capacitor between CTH and ground (Figure 3). When the voltage at pin CTH exceeds the voltage at pin THADJ, then the $\overline{LOL}$ output goes low and indicates that the PLL is not locked. Note that excessive jitter on the reference clock input at frequencies above the loop bandwidth may degrade LOL functionality.

The user can set the amount of frequency or phase difference between VCO and reference clock at which $\overline{LOL}$ indicates an out-of-lock condition. The frequency difference is called the beat frequency. The CTH pin can be connected to an external capacitor, which sets the lowpass filter frequency to approximately

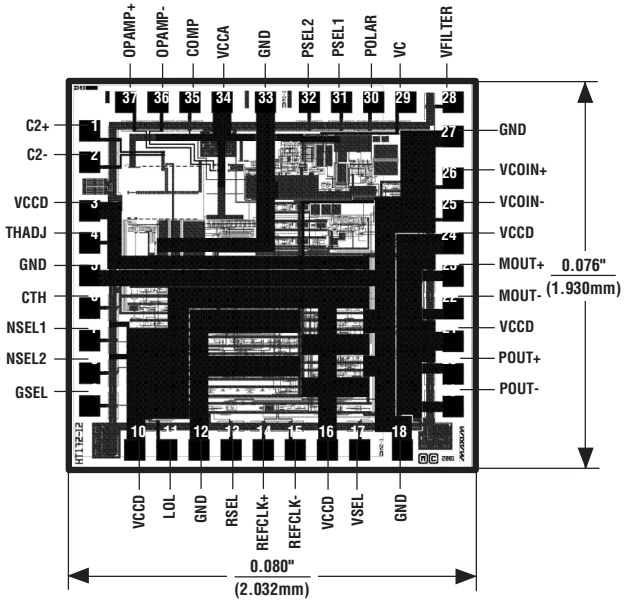
$$f_L = \frac{1}{2\pi C_{TH} 60k\Omega}$$

This lowpass filter frequency should be set about 10 times lower then the beat frequency to ensure that the filtered signal at CTH does not drop below the THADJ threshold voltage. Internal comparisons occur at the pre-divider output frequency (see Table 1 for VCO and reference clock setup). For example, assume the pre-divider output frequency is 19.44MHz. For a 1ppm sensitivity, the minimum beat frequency is 19Hz, and the filter should be set to 1.9Hz. Set CTH to 1.36uF.

The voltage at THADJ will determine the level at which the $\overline{LOL}$ output flags. THADJ is set to a default value of 0.6V which corresponds to a 45° phase difference. This value can be overridden by applying the desired threshold voltage to the THADJ input. The range of THADJ is 0V (0°) to 2.4V (180°).

Low-Jitter 155MHz/622MHz Clock Generator

Chip Topography



Chip Information

PROCESS: GST2
SUBSTRATE CONNECTED TO GND
DIE THICKNESS: 14 mils

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.