

+3.3V, 2.125Gbps/1.0625Gbps Fibre Channel Port Bypass ICs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}-0.5V to +5.0V
 Voltage at LOUT+, LOUT-,
 OUT+, OUT-.....($V_{CC} - 1.65V$) to ($V_{CC} + 0.5V$)
 Current Out of LOUT+, LOUT-, OUT+, OUT-..... $\pm 22mA$
 Voltage at SEL, LIN+, LIN-, IN+, IN-.....-0.5V to ($V_{CC} + 0.5V$)
 Differential Voltage at (LIN+ - LIN-), (IN+ - IN-)..... $\pm 2V$

Continuous Power Dissipation ($T_A = +70^\circ C$)
 16 QSOP (derate 8.3mW/ $^\circ C$ above $+70^\circ C$).....667mW
 Operating Temperature Range-40 $^\circ C$ to +85 $^\circ C$
 Storage Temperature Range-55 $^\circ C$ to 150 $^\circ C$
 Lead Soldering Temperature (soldering, 10sec).....+300 $^\circ C$

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to +3.6V, $T_A = 0^\circ C$ to +70 $^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	MAX3750 (Note 1)		57	84	mA
	MAX3751 (Note 1)		54	78	
Data Input Voltage Swing	Total differential signal, peak-to-peak	200		2200	mV
Differential Input Impedance		132	150	172	Ω
Output Voltage at LOUT \pm and OUT \pm	150 Ω load, total differential signal, peak-to-peak	1000		1600	mV
TTL Input Current		-10		10	μA
TTL Input Low		-0.3		0.8	V
TTL Input High		2		$V_{CC} + 0.3$	V

Note 1: Output currents included.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to +3.6V, $T_A = 0^\circ C$ to +70 $^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate	MAX3750		2.125		Gbps
	MAX3751		1.0625		
Data Input Voltage Swing	Total differential signal, peak-to-peak	200		2200	mV
Output Edge Speed IN \pm \rightarrow OUT \pm , IN \pm \rightarrow LOU \pm	MAX3750			160	ps
	MAX3751			325	
Deterministic Jitter IN \pm \rightarrow OUT \pm , IN \pm \rightarrow LOU \pm , LIN \pm \rightarrow OUT \pm	MAX3750, peak-to-peak (Notes 2, 4)		10		ps
	MAX3751, peak-to-peak (Notes 3, 4)		10		
Random Jitter IN \pm \rightarrow OUT \pm , IN \pm \rightarrow LOU \pm , LIN \pm \rightarrow OUT \pm	MAX3750, RMS (Note 2)			1.6	ps
	MAX3751, RMS (Note 3)			1.6	
Prop Delay IN \pm \rightarrow OUT \pm , IN \pm \rightarrow LOU \pm , LIN \pm \rightarrow OUT \pm	MAX3750		300		ps
	MAX3751		442		

Note 2: Input t_R and $t_F < 150ps$, 20% to 80%.

Note 3: Input t_R and $t_F < 300ps$, 20% to 80%.

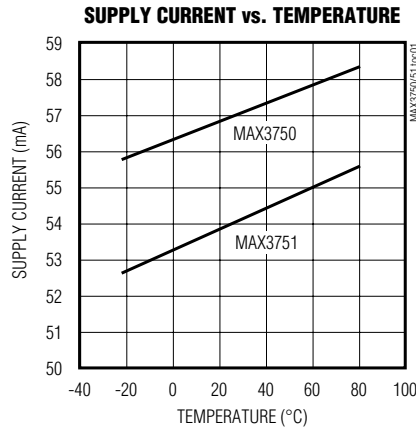
Note 4: Deterministic jitter is measured with 20 bits of the k28.5 pattern (00111110101100000101).

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MAX3750/MAX3751

Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 8, 16	GND	Electrical Ground
2	LOUT+	Noninverted Port Data Output
3	LOUT-	Inverted Port Data Output
6	OUT+	Noninverted Data Output
7	OUT-	Inverted Data Output
9	SEL	Select Input: SEL = Low: IN _± → OUT _± SEL = High: LIN _± → OUT _±
10	LIN-	Inverted Port Data Input
11	LIN+	Noninverted Port Data Input
12, 13	V _{CC}	Positive Supply Voltage
14	IN-	Inverted Data Input
15	IN+	Noninverted Data Input

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Circuit Description

A simplified block diagram of the single port bypass is shown in Figure 1. IN+ and IN- drive an input buffer (INBUFF) with 150Ω of internal differential input termination. INBUFF drives an output buffer (LOBUFF) and an input to a multiplexer (MUX).

A low TTL input at SEL selects the signal path of INBUFF through MUX to the output buffer (OUTBUFF). When SEL has a high TTL logic level present the signal path is into LIBUFF, through MUX, to OUTBUFF.

Low-Frequency Cutoff

The low-frequency cutoff is determined by the input resistance and the coupling capacitor as illustrated by the following equation:

$$f_c = 1 / (2\pi RC)$$

In a typical system where R = 150Ω and C = 100nF, resulting in f_c = 10kHz.

Layout Techniques

The MAX3750/MAX3751 are high-frequency products. The performance of the circuit is largely dependent upon layout of the circuit board. Use a multilayer circuit board with dedicated ground and VCC planes. Power supplies should be capacitively bypassed to the ground plane with surface-mount capacitors placed near the power-supply pins.

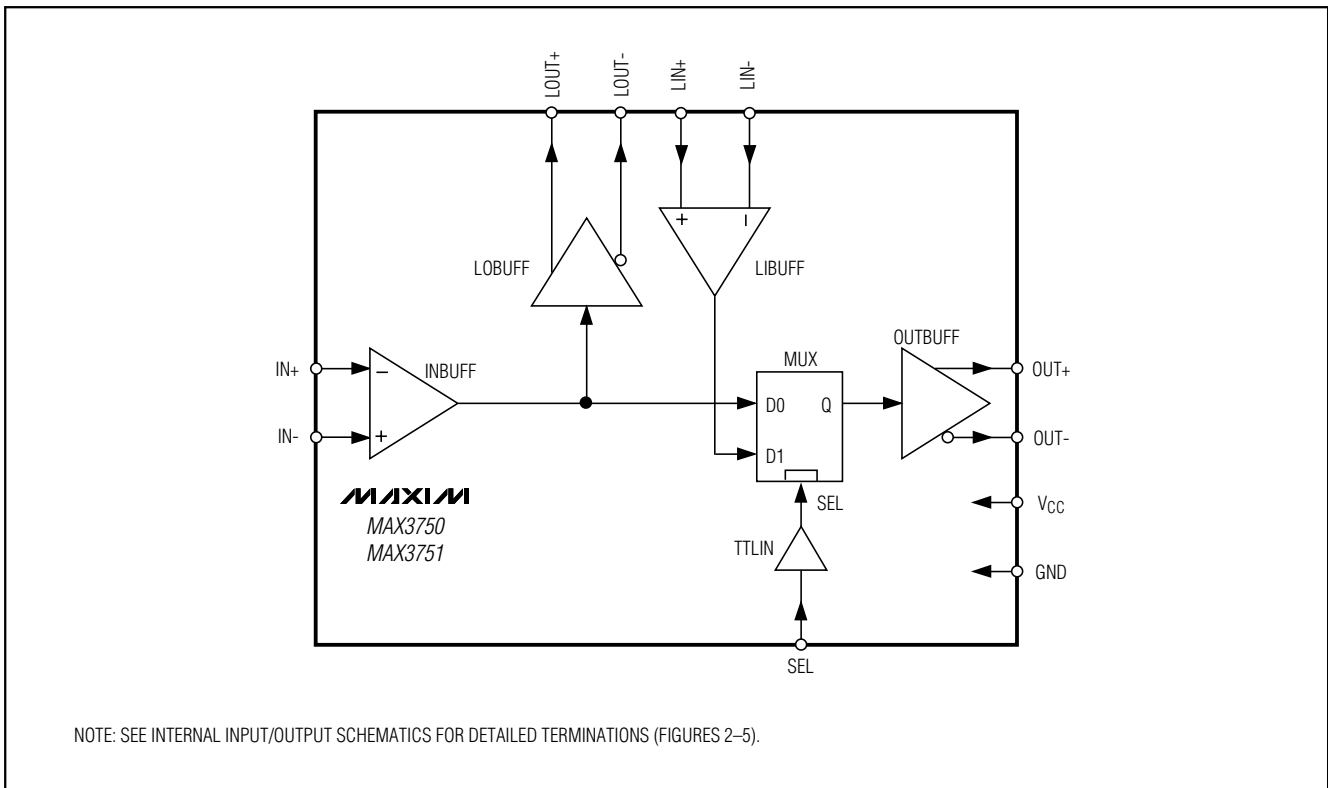


Figure 1. MAX3750/MAX3751 Block Diagram

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MAX3750/MAX3751

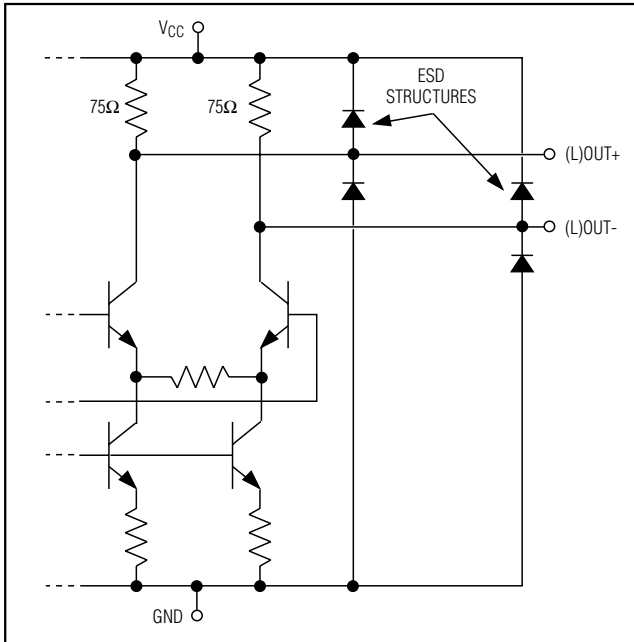


Figure 2. LOUT/OUT Pins Internal Input/Output Schematic

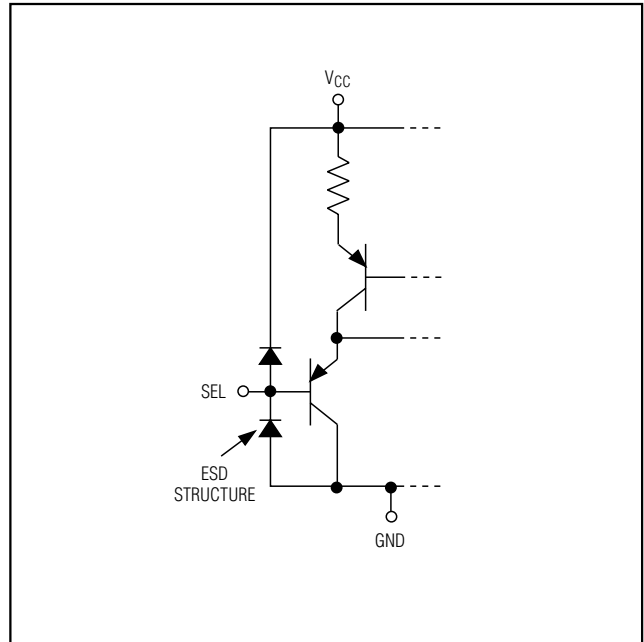


Figure 3. SEL Pin Internal Input/Output Schematic

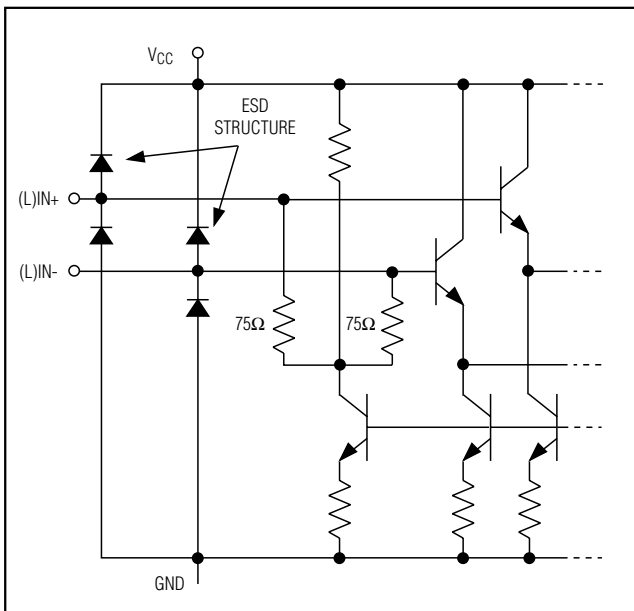


Figure 4. LIN/IN Pins Internal Input/Output Schematic

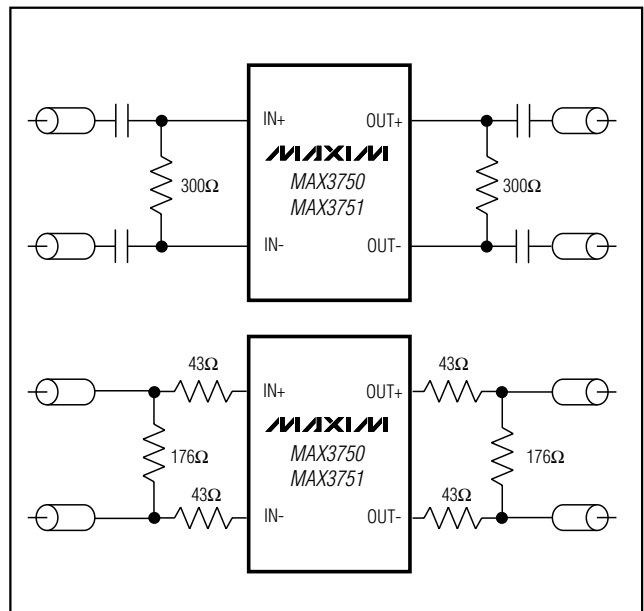
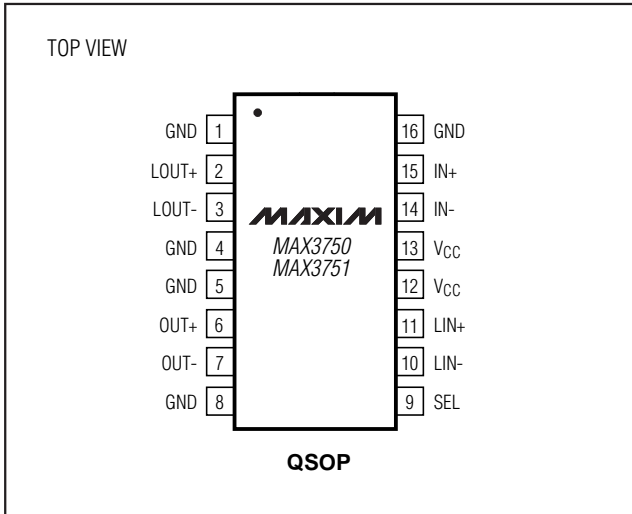


Figure 5. 50Ω Termination Applications

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Pin Configuration



Package Information

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

DIM	INCHES		MILLIMETERS		N
	MIN	MAX	MIN	MAX	
D	.189	.196	4.80	4.98	16
S	.0020	.0070	0.05	0.18	
X	.107	.123	2.72	3.12	
D	.337	.344	8.56	8.74	20
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28
S	.0250	.0300	0.635	0.762	
X	.271	.287	6.88	7.29	

VARIATIONS:

NOTES:

- D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
- HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
- CONTROLLING DIMENSIONS: INCHES.

PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH
APPROVAL: _____ DOCUMENT CTRL. NO: 21-0055 REV: B 1/1

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