MAXIM

Mono, 2W, Switch-Mode (Class D) Audio Power Amplifier

General Description

The MAX4295 mono, switch-mode (Class D) audio power amplifier operates from a single +2.7V to +5.5V supply. The MAX4295 has >85% efficiency and is capable of delivering 2W continuous power to a 4Ω load, making it ideal for portable multimedia and general-purpose high-power audio applications.

The MAX4295 features a total harmonic distortion plus noise (THD+N) of 0.4% (f_{OSC} = 125kHz), low quiescent current of 2.8mA, high efficiency, and clickless power-up and shutdown. The $\overline{SHDN}$ input disables the device and limits supply current to <1.5µA. Other features include a 1A current limit, thermal protection, and undervoltage lockout.

The MAX4295 reduces the number of required external components. Internal high-speed power-MOS transistors allow operation as a bridge-tied load (BTL) amplifier. The BTL configuration eliminates the need for isolation capacitors on the output. The frequency-selectable pulse-width modulator (PWM) allows the user to optimize the size and cost of the output filter.

The MAX4295 is offered in a space-saving 16-pin QSOP or narrow SO package.

Applications

- Palmtop/Notebook Computers
- PDA Audio
- Sound Cards
- Game Cards
- Boom Boxes
- AC Amplifiers
- Battery-Powered Speakers
- Cordless Phones
- Portable Equipment

Features

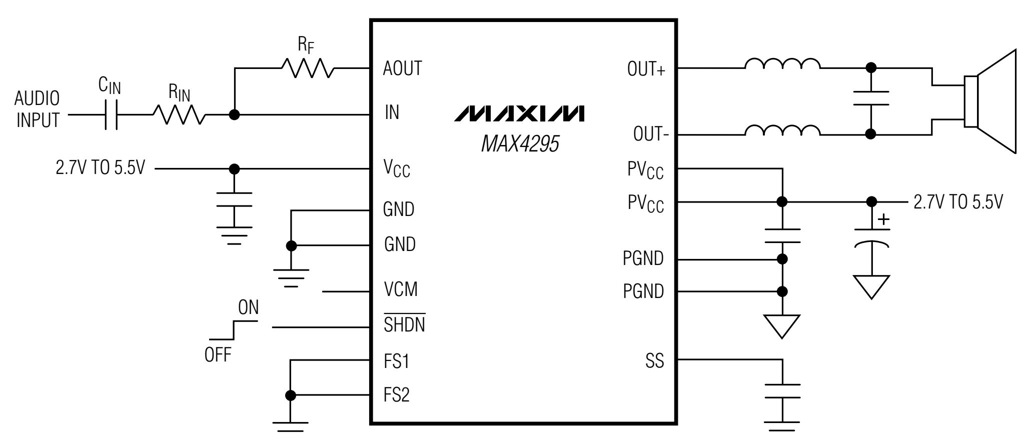
- **+2.7V to +5.5V Single-Supply Operation**
- **2W/Channel Output Power at 5V**
  0.7W/Channel Output Power at 3V
- **87% Efficiency (R_L = 4Ω, P_{OUT} = 2W)**
- **0.4% THD+N (R_L = 4Ω, f_{OSC} = 125kHz)**
- **Logic-Programmable PWM Frequency Selection (125kHz, 250kHz, 500kHz, 1MHz)**
- **Low-Power Shutdown Mode**
- **Clickless Transitions Into and Out of Shutdown**
- **1A Current Limit and Thermal Protection**
- **Available in Space-Saving Packages**
  16-Pin QSOP or Narrow SO

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4295EEE	-40°C to +85°C	16 QSOP
MAX4295ESE	-40°C to +85°C	16 Narrow SO

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



Mono, 2W, Switch-Mode (Class D) Audio Power Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{CC}, PV_{CC} to GND or PGND....................................-0.3V to +6V
PGND to GND...±0.3V
PV_{CC} to V_{CC} ....±0.3V
VCM, SS, AOUT, IN to GND.......................-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$, FS1, FS2 to GND ....-0.3V to +6V
OUT_ to PGND..-0.3V to (PV_{CC} + 0.3V)
Op Amp Output Short-Circuit
Duration (AOUT).........Indefinite Short Circuit to Either Supply
H-Bridge Short-Circuit
Duration (OUT_) ....Continuous Short Circuit to PGND, PV_{CC} or between OUT+ and OUT-

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.30mW/°C above +70°C)........667mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C)......696mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = PV_{CC} = +5V, $\overline{SHDN}$ = V_{CC}, FS1 = GND, FS2 = V_{CC} (f_{OSC} = 250kHz), input amplifier gain = -1V/V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage Range	(Note 2)		2.7		5.5	V
Quiescent Supply Current	Output load not connected			2.8	4	mA
Shutdown Supply Current	$\overline{SHDN}$ = GND			1.5	8	µA
Voltage at VCM Pin			0.285 × V_{CC}	0.3 × V_{CC}	0.315 × V_{CC}	V
PWM Frequency	FS1 = GND, FS2 = GND		105	125	145	kHz
	FS1 = GND, FS2 = V_{CC}		210	250	290	
	FS1 = V_{CC}, FS2 = GND		420	500	580	
	FS1 = V_{CC}, FS2 = V_{CC}		840	1000	1160	
PWM Frequency Change with V_{CC}	V_{CC} = 2.7V to 5.5V			±1	±3	kHz/V
Duty Cycle	V_{IN} = 0.06 × V_{CC}		10.2	12	13.8	%
	V_{IN} = 0.30 × V_{CC}		49.2	50	50.8	
	V_{IN} = 0.54 × V_{CC}		86.2	88	89.8	
Duty Cycle Change with V_{CC}	V_{IN} = 0.3 × V_{CC}, V_{CC} = 2.7V to 5.5V			±0.02	±0.15	%/V
Switch On-Resistance (each power device)	I_{OUT} = 150mA	V_{CC} = 5V		0.25	0.5	Ω
		V_{CC} = 2.7V		0.35	1.0	
H-Bridge Output Leakage	$\overline{SHDN}$ = GND			0	±5	µA
H-Bridge Current Limit				1		A
Soft-Start Capacitor Charging Current	V_{SS} = 0V		0.75	1.35	1.95	µA
Undervoltage Lockout			1.8	2.2	2.6	V
Thermal Shutdown Trip Point				145		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = PV_{CC} = +5V, $\overline{SHDN}$ = V_{CC}, FS1 = GND, FS2 = V_{CC} (f_{OSC} = 250kHz), input amplifier gain = -1V/V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range				0 to 0.6 x V_{CC}		V
Maximum Output Power	V_{CC} = +3V, f_{IN} = 1kHz	R_L = 8Ω		0.4		W
		R_L = 4Ω		0.7		
	V_{CC} = +5V, f_{IN} = 1kHz	R_L = 8Ω		1.2		
		R_L = 4Ω		2		
Total Harmonic Distortion Plus Noise	R_L = 4Ω, f_{IN} = 1kHz, P_O = 1W, f_{OSC} = 125kHz			0.4		%
Efficiency	MAX4295, R_L = 4Ω, f_{IN} = 1kHz, P_O = 2W			87		%
LOGIC INPUTS ($\overline{SHDN}$, FS1, FS2)						
Logic Input Current	V_{LOGIC} = 0 to V_{CC}			1	100	nA
Logic Input High Voltage			0.7 × V_{CC}			V
Logic Input Low Voltage					0.3 × V_{CC}	V
INPUT AMPLIFIER						
Input Offset Voltage				±0.5	±4	mV
V_{OS} Temp Coefficient				±5		µV/°C
Input Bias Current	(Note 3)			±0.05	±25	nA
Input Noise-Voltage Density	f = 10kHz			32		nV/√Hz
Input Capacitance				2.5		pF
Output Resistance				0.01		Ω
AOUT Disabled Mode Leakage Current	$\overline{SHDN}$ = GND, V_{AOUT} = 0 to V_{CC}			±0.1	±1	µA
Short-Circuit Current	AOUT to GND			8		mA
	AOUT to V_{CC}			65		
Large-Signal Voltage Gain	V_{OUT} = 0.2V to 4.6V, $R_{L(OPAMP)}$ = 10kΩ		78	115		dB
AOUT Voltage Swing	V_{DIFF} ≥ 10mV, $R_{L(OPAMP)}$ = 10kΩ	V_{CC} - V_{OH}		40	250	mV
		V_{OL}		40	100	
Gain-Bandwidth Product				1.25		MHz
Power-Supply Rejection	V_{CC} = +2.7V to +5.5V		66	90		dB
Maximum Capacitive Load	No sustained oscillations			200		pF

Note 1: All devices are 100% production tested at T_A = 25°C. All temperature limits are guaranteed by design.
Note 2: Supply Voltage Range guaranteed by PSRR of input amplifier, frequency, duty cycle, and H-bridge on-resistance.
Note 3: Guaranteed by design, not production tested.

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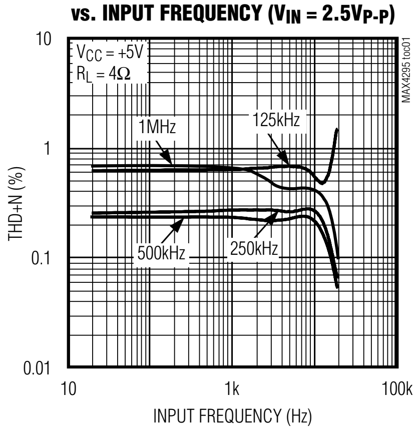
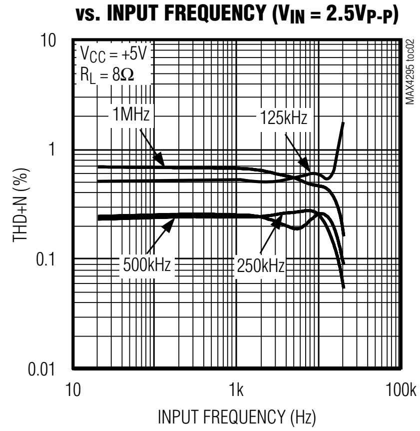
Typical Operating Characteristics

(V_{CC} = PV_{CC} = +3V, input amplifier gain = -1, $\overline{SHDN}$ = V_{CC} , T_A = +25°C, unless otherwise noted.)

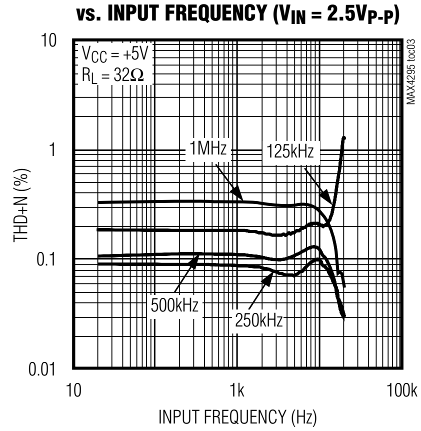
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT FREQUENCY (V_{IN} = 2.5V_{P-P})



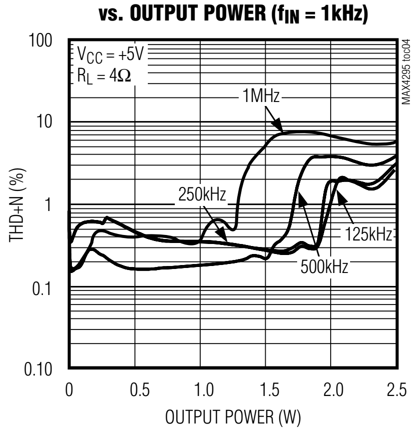
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT FREQUENCY (V_{IN} = 2.5V_{P-P})



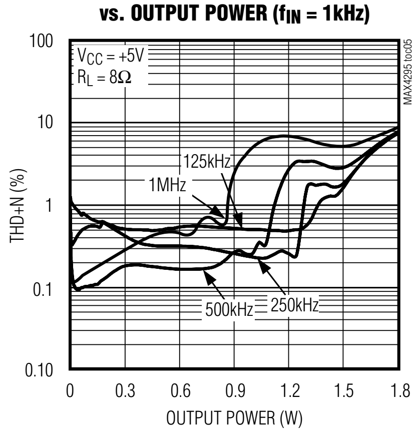
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT FREQUENCY (V_{IN} = 2.5V_{P-P})



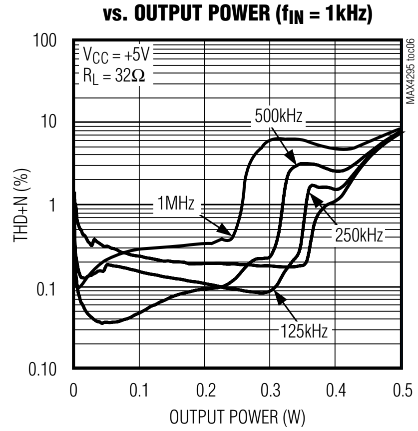
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 1kHz)



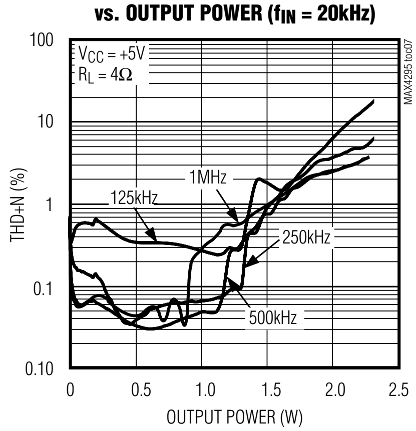
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 1kHz)



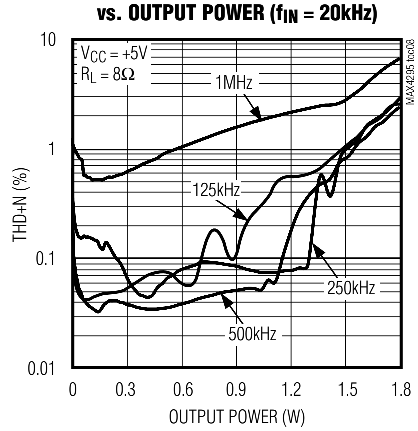
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 1kHz)



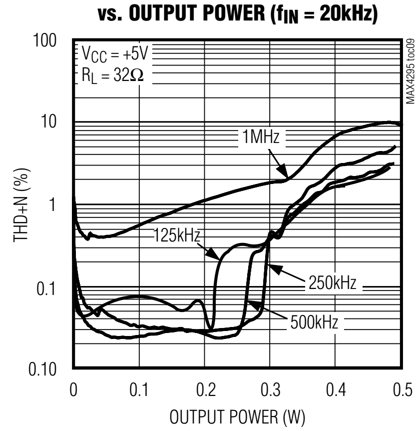
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 20kHz)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 20kHz)



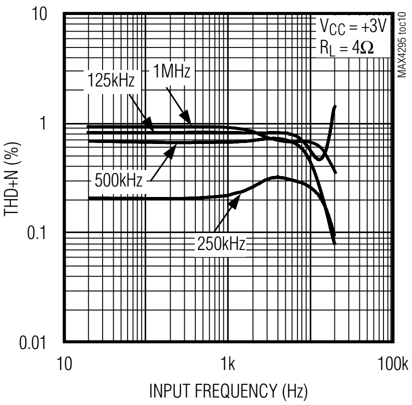
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 20kHz)



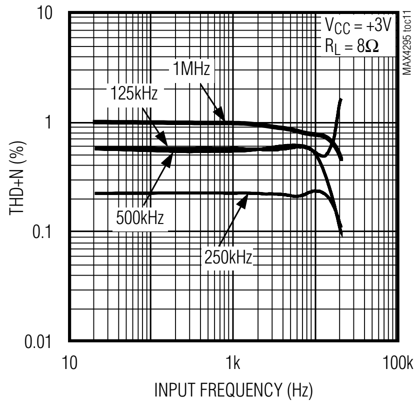
Typical Operating Characteristics (continued)

(V_{CC} = PV_{CC} = +3V, input amplifier gain = -1, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

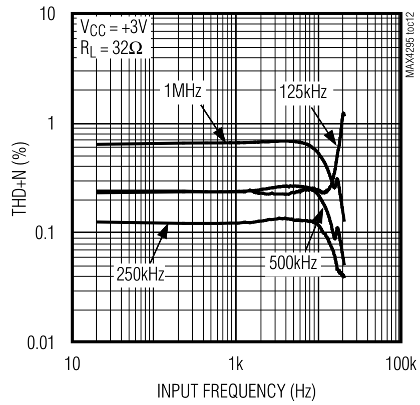
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT FREQUENCY (V_{IN} = 1.5V_{P-P})



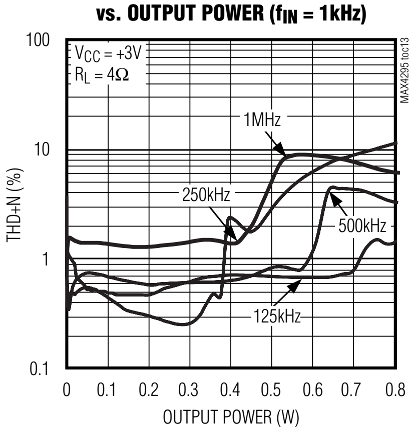
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT FREQUENCY (V_{IN} = 1.5V_{P-P})



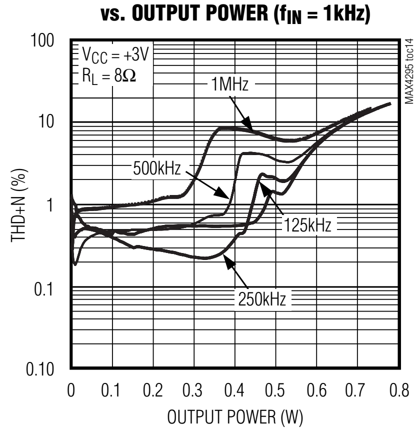
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT FREQUENCY (V_{IN} = 1.5V_{P-P})



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 1kHz)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 1kHz)



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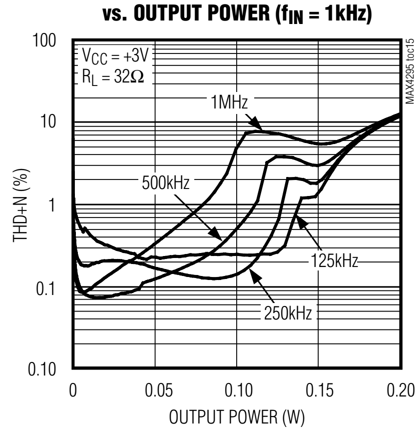
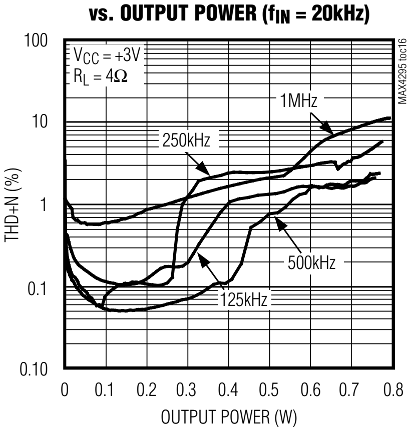
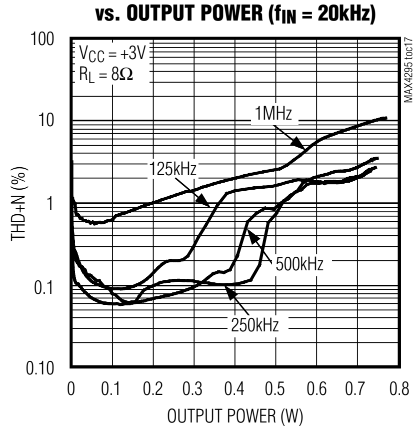


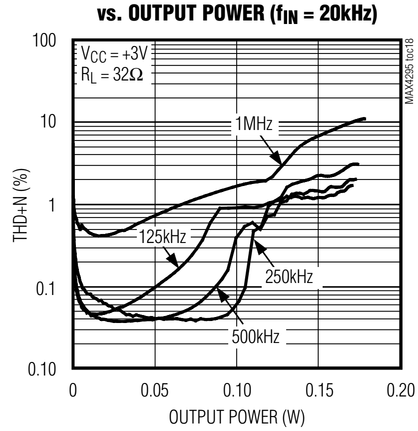
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 20kHz)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 20kHz)



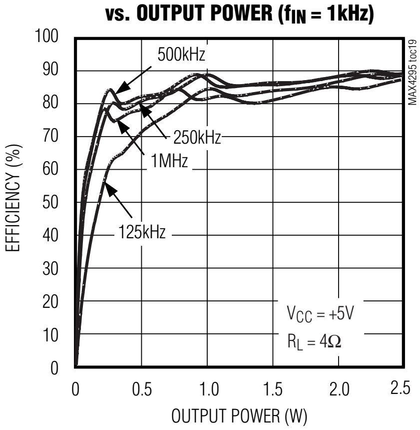
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (f_{IN} = 20kHz)



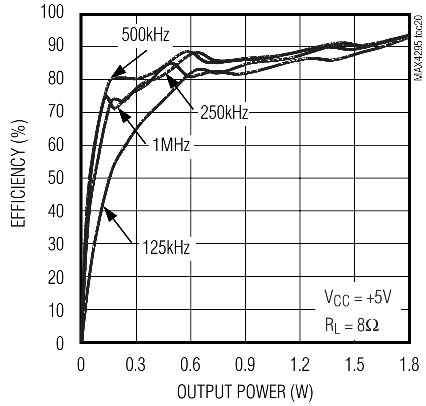
Typical Operating Characteristics (continued)

(V_{CC} = PV_{CC} = +3V, input amplifier gain = -1, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

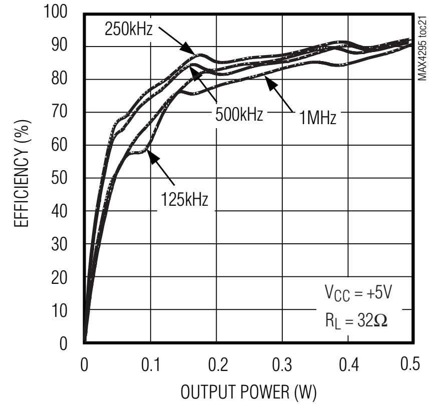
EFFICIENCY vs. OUTPUT POWER (f_{IN} = 1kHz)



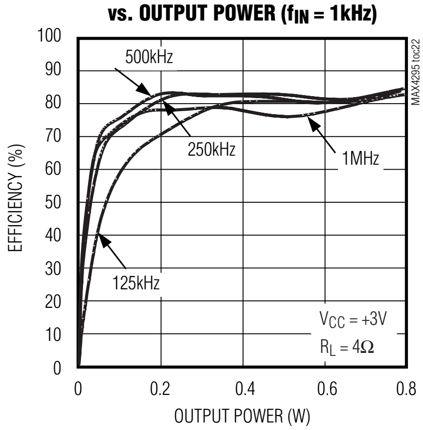
EFFICIENCY vs. OUTPUT POWER (f_{IN} = 1kHz)



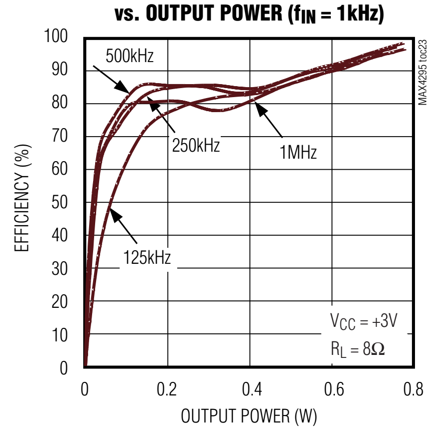
EFFICIENCY vs. OUTPUT POWER (f_{IN} = 1kHz)



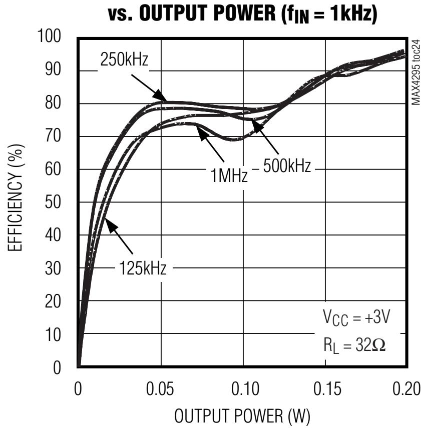
EFFICIENCY vs. OUTPUT POWER (f_{IN} = 1kHz)



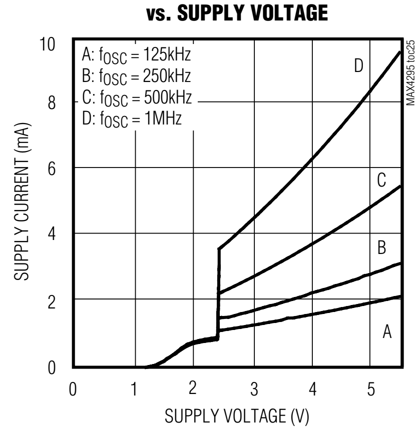
EFFICIENCY vs. OUTPUT POWER (f_{IN} = 1kHz)



EFFICIENCY vs. OUTPUT POWER (f_{IN} = 1kHz)

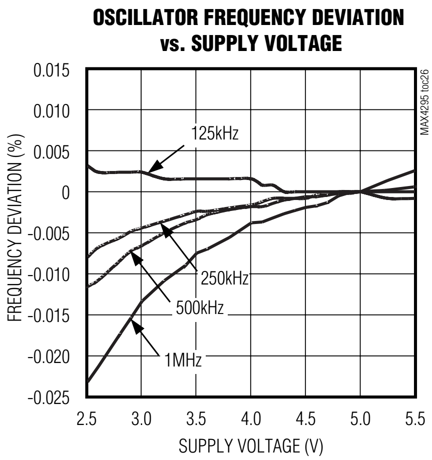


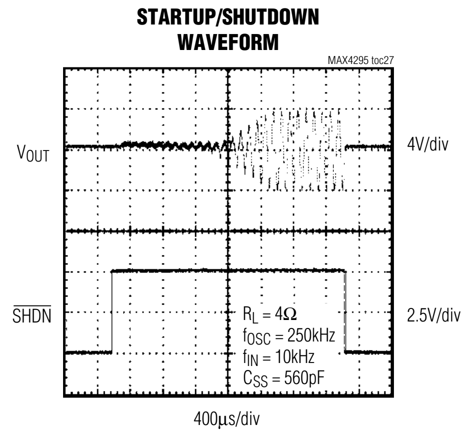
SUPPLY CURRENT vs. SUPPLY VOLTAGE



Typical Operating Characteristics (continued)

(V_{CC} = PV_{CC} = +3V, input amplifier gain = -1, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1, 12	GND	Analog Ground
2, 15	PV_{CC}	H-Bridge Power Supply
3	OUT+	Positive H-Bridge Output
4, 13	PGND	Power Ground
5	V_{CC}	Analog Power Supply
6	VCM	Audio Input Common-Mode Voltage. Do not connect. Minimize parasitic coupling to this pin.
7	IN	Audio Input
8	AOUT	Input Amplifier Output
9	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to V_{CC} for normal operation. Do not leave floating.
10	FS1	Frequency Select Input 1
11	FS2	Frequency Select Input 2
14	OUT-	Negative H-Bridge Output
16	SS	Soft-Start

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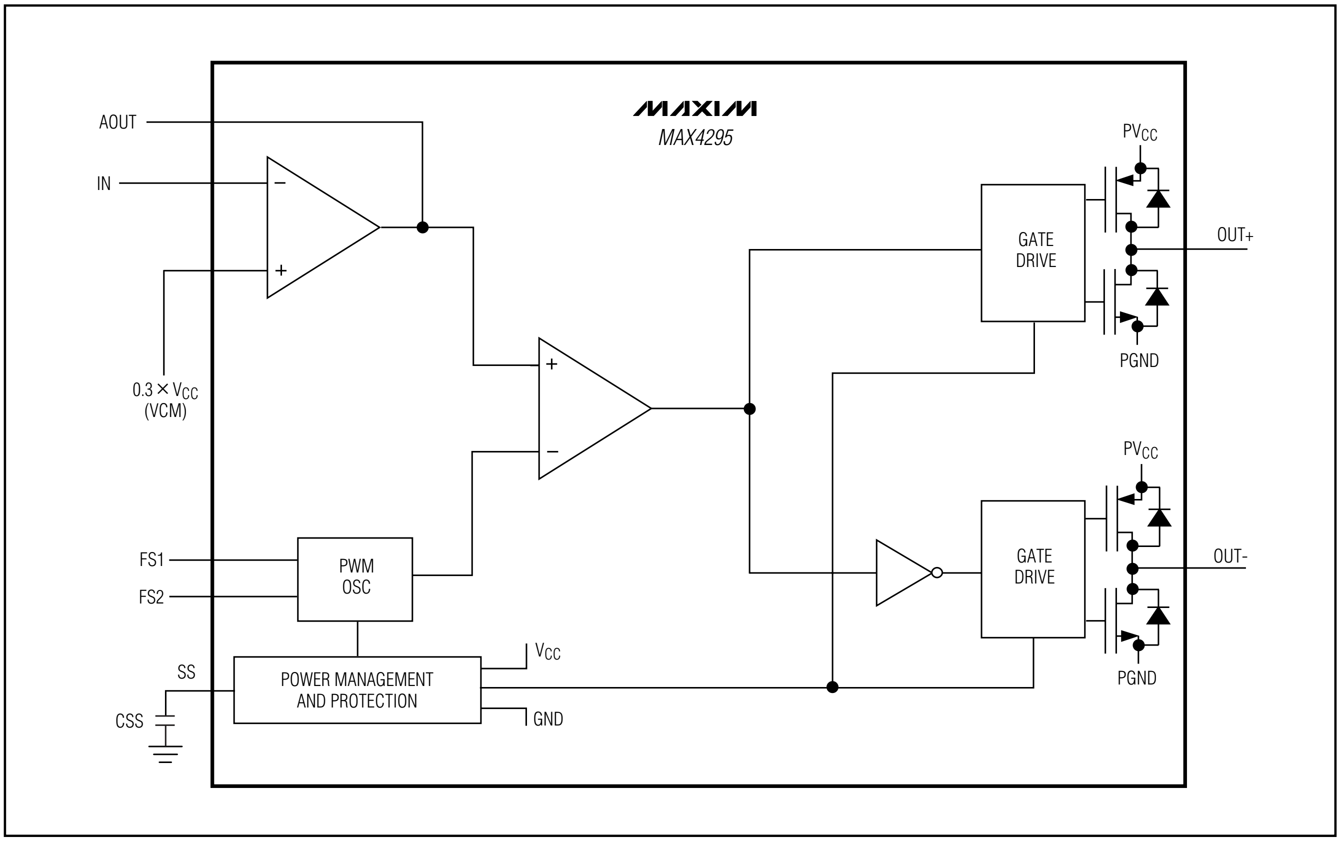


Figure 1. Functional Diagram

Detailed Description

The MAX4295 switch-mode, Class D audio power amplifier is intended for portable multimedia and general-purpose audio applications. Linear amplifiers in the 1W to 2W output range are inefficient; they overheat when operated near rated output power levels. The efficiency of linear amplifiers is <50% when the output voltage is equal to 1/2 the supply. The MAX4295 Class D amplifier achieves efficiencies of 87% or greater and is capable of delivering up to 2W of continuous maximum power to a 4Ω load. The lost power is due mainly to the on-resistance of the power switches and ripple current in the output.

In a Class D amplifier, a PWM controller converts the analog input to a variable pulse-width signal. The pulse width is proportional to the input voltage, ideally 0% for a 0V input signal and 100% for full-scale input voltages. A passive lowpass LC network filters the PWM output waveform to reconstruct the analog signal. The switching frequency is selected much higher than the maximum input frequencies so that intermodulation products are outside the input signal bandwidth. Higher switching frequencies also simplify the filtering requirements.

The MAX4295 consists of an inverting input operational amplifier, a PWM ramp oscillator, a controller that converts the analog input to a variable pulse-width signal, and a MOSFET H-bridge power stage (Figure 1). The control signal is generated by the PWM comparator; its pulse width is proportional to the input voltage. Ideally the pulse width varies linearly between 0% for a 0V input signal and 100% for full-scale input voltages (Figure 2). This signal controls the H-bridge. The switches work in pairs to reverse the polarity of the signal in the load. Break-before-make switching of the H-bridge MOSFETs by the driver circuit keeps supply current glitches and crowbar current in the MOSFETs at a low level. The output swing of the H-bridge is a direct function of the supply voltage. Varying the oscillator swing in proportion to the supply voltage maintains constant gain with varying supply voltage.

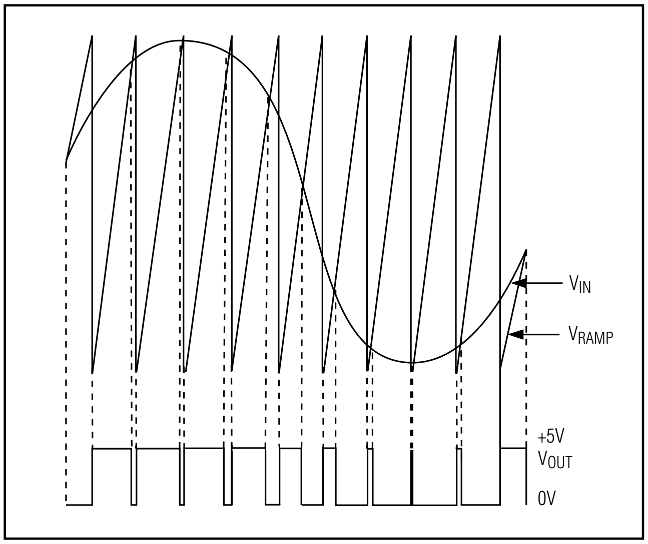


Figure 2. PWM Waveforms

FS1 and FS2 program the oscillator to a frequency of 125kHz, 250kHz, 500kHz, and 1MHz. The sawtooth oscillator swings between GND and 0.6 × V_{CC}. The input signal is typically AC-coupled to the internal input op amp, whose gain can be controlled through external feedback components. The common-mode voltage of the input amplifier is 0.3 × V_{CC} and is internally generated from the same resistive divider used to generate the 0.6 × V_{CC} reference for the PWM oscillator.

Current Limit

A current-limiting circuit in the H-bridge monitors the current in the H-bridge transistors and disables the H-bridge if the current in any of the H-bridge transistors exceeds 1A. The H-bridge is enabled after a period of 100µs. A continuous short circuit at the output results in a pulsating output.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX4295. When the junction temperature exceeds +145°C, the thermal detection disables the H-bridge transistors. The H-bridge transistors are enabled after the IC's junction temperature cools by 10°C. This results in a pulsating output under continuous thermal overload conditions. Junction temperature does not exceed the thermal overload trip point in normal operation, but only in the event of fault conditions, such as when the H-bridge outputs are short circuited.

Undervoltage Lockout

At low supply voltages, the MOSFETs in the H-bridge may have inadequate gate drive thus dissipating excessive power. The undervoltage lockout circuit prevents the device from operating at supply voltages below +2.2V.

Low-Power Shutdown Mode

The MAX4295 has a shutdown mode that reduces power consumption and extends battery life. Driving $\overline{SHDN}$ low disables the H-bridge, turns off the circuit, and places the MAX4295 in a low-power shutdown mode. Connect $\overline{SHDN}$ to V_{CC} for normal operation.

Applications Information

Component Selection

Gain Setting

External feedback components set the gain of the MAX4295. Resistors R_F and R_{IN} set the gain of the input amplifier to $-(R_F/R_{IN})$. The amplifier's noninverting input is connected to the internally generated 0.3 × V_{CC} (VCM) that sets the amplifier's common-mode voltage.

The amplifier's input bias current is low, ±50pA, and does not affect the choice of feedback resistors. The noise in the circuit increases as the value of R_F increases.

The optimum impedance seen by the inverting input is between 5kΩ and 20kΩ. The effective impedance is given by $(R_F \times R_{IN})/(R_F + R_{IN})$. For values of R_F > 50kΩ, a small capacitor (≈3pF) connected across R_F compensates for the pole formed by the input capacitance and the effective resistance at the inverting input.

Soft-Start (Clickless Startup)

The H-bridge is disabled under any of the following conditions:

- $\overline{SHDN}$ low
- H-bridge current exceeds the 1A current limit
- Thermal overload
- Undervoltage lockout

The circuit re-enters normal operation if none of the above conditions are present. A soft-start function prevents an audible pop on restart. An external capacitor connected to SS is charged by an internal 1.2µA current source and controls the soft-start rate. V_{SS} is held low while the H-bridge is disabled and allowed to ramp up to begin a soft-start. Until V_{SS} reaches $0.3 \times V_{CC}$, the H-bridge output is limited to a 50% duty cycle, independent of the input voltage. The H-bridge duty cycle is then gradually allowed to track the input signal at a rate determined by the ramp on SS. The soft-start cycle is complete after V_{SS} reaches $0.6 \times V_{CC}$. If the soft-start capacitor is omitted, the device starts up in approximately 100µs.

Input Filter

High-fidelity audio applications require gain flatness between 20Hz to 20kHz. Set the low-frequency cutoff point with an AC-coupling capacitor in series with the input resistor of the amplifier, creating a highpass filter (Figure 3). Assuming the input node of the amplifier is a virtual ground, the -3dB point of the highpass filter is determined by: $f_{LO} = 1/(2\pi \times R_{IN} \times C_{IN})$, where R_{IN} is the input resistor, and C_{IN} is the AC-coupling capacitor. Choose R_{IN} as described in the *Gain Setting* section. Choose C_{IN} such that the corner frequency is below 20Hz.

Frequency Selection

The MAX4295 has an internal logic-programmable oscillator controlled by FS1 and FS2 (Table 1). The oscillator can be programmed to frequencies of 125kHz, 250kHz, 500kHz, and 1MHz. The frequency should be chosen to best fit the application. As a rule of thumb, choose f_{OSC} to be 10 times the audio bandwidth. A lower switching frequency offers higher amplifier efficiency and lower THD but requires larger external filter components. A higher switching frequency reduces the size and cost of the filter components at the expense of THD and efficiency. In most applications, the optimal f_{OSC} is 250kHz.

Table 1. Frequency Select Logic

FS1	FS2	FREQUENCY (Hz)
1	1	1M
0	1	500k
1	0	250k
0	0	125k

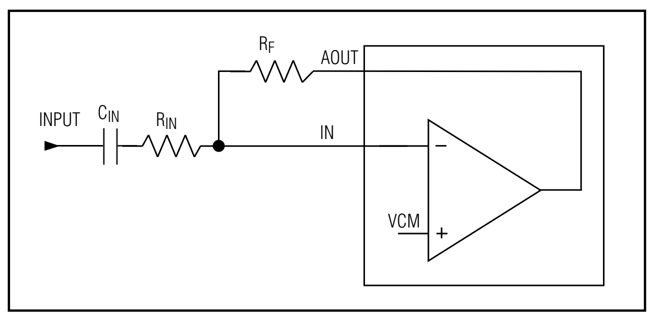


Figure 3. Input Amplifier Configuration

Output Filter

An output filter is required to attenuate the PWM switching frequency. Without the filter, the ripple in the load can substantially degrade efficiency and may cause interference problems with other electronic equipment.

A Butterworth lowpass filter is chosen for its flat passband and nice phase response, though other filter implementations may also be used. Three examples are presented below. The filter parameters for balanced 2-pole (Figure 4b) and 4-pole (Figure 4d) Butterworth filters are taken from *Electronic Filter Design Handbook* by Arthur B. Williams, McGraw Hill, Inc. These filter designs assume that the load is purely resistive and load impedance is constant over frequency. Calculation of filter component values should include the DC resistance of the inductors and take into account the worst-case load scenario:

• Single Ended 2-Pole Filter (Figure 4a)

$$C = 1 / (\sqrt{2} \times R_L \times \omega_O),\ L = \sqrt{2} \times R_L / \omega_O$$

where $\omega_O = 2 \times \pi \times f_O$ (f_O = filter cutoff frequency); choosing f_O = 30kHz and $R_L = 4\Omega$, C = 0.937µF, L = 30µH.

A single-ended 2-pole filter uses the minimum number of external components, but the load (speaker) sees the large common-mode switching voltage, which can increase power dissipation and cause EMI problems.

• Balanced 2-Pole (Figure 4b):

A balanced 2-pole filter does not have the common-mode swing problem of the single-ended filter.

$C = 2 / (\sqrt{2} \times R_L \times \omega_O)$, $L = (\sqrt{2} \times R_L)/(2 \times \omega_O)$; choosing f_O = 30kHz and $R_L = 4\Omega$, C1a = C1b = 2.0µF, L1a = L1b = 15µH.

A single capacitor connected across R_L, with a value of $C_L = 1/(\sqrt{2} \times R_L \times \omega_O)$, can be used in place of C1a and C1b. However, the configuration as shown gives an improved rejection to common-mode signal components of OUT+_ and OUT-_. If the single capacitor scheme is used, additional capacitors (Ca and Cb) can be added from each side of R_L, providing a high-frequency short to ground (Figure 4c). These capacitors should be approximately $0.2 \times C_L$.

• Balanced 4-Pole Filter (Figure 4d)

A balanced 4-pole filter is more effective in suppressing the switching frequency and its harmonics.

For the 4-pole Butterworth filter, the normalized values are: $L1_N = 1.5307$, $L2_N = 1.0824$, $C1_N = 1.5772$, $C2_N = 0.3827$.

The actual inductance and capacitance values for f_O = 30kHz and a bridge-tied load of $R_L = 4\Omega$ are given by:

$L1 = (L1_N \times R_L) / (2 \times \omega_O)$ = 16.24µH, $L2 = (L2_N \times R_L) / (2 \times \omega_O)$ = 11.5µH, $C1 = C1_N / (R_L \times \omega_O)$ = 2.1µF, $C2a = C2b = (2 \times C2_N) / (R_L \times \omega_O)$ = 1.0µF.

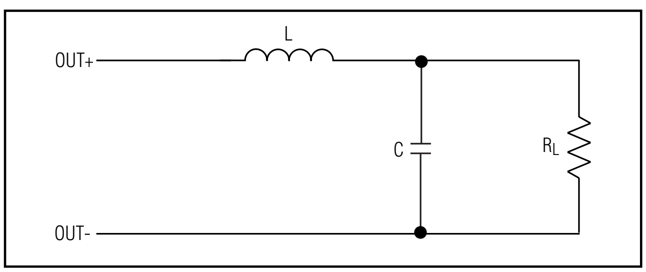


Figure 4a. Single-Ended 2-Pole Filter

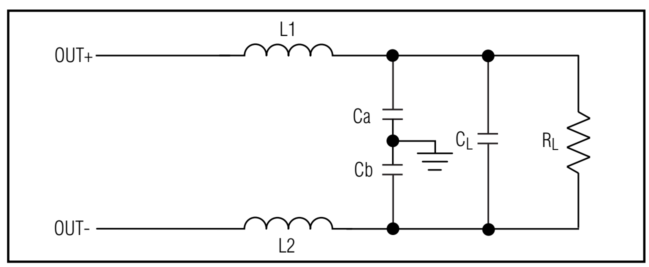


Figure 4c. Alternate Balanced 2-Pole Filter

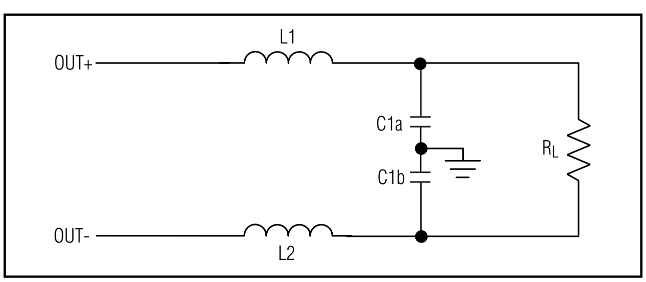


Figure 4b. Balanced 2-Pole Filter

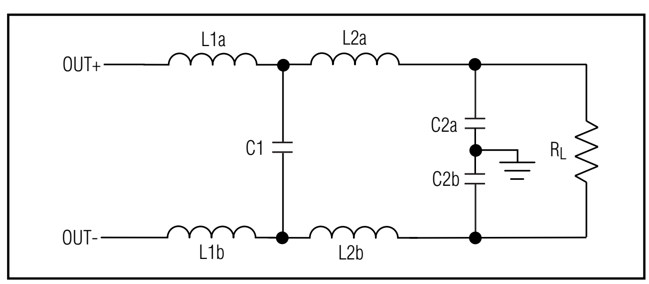


Figure 4d. Balanced 4-Pole Filter

Mono, 2W, Switch-Mode (Class D) Audio Power Amplifier

Filter Components

The inductor current rating should be higher than the peak current for a given output power requirement and should have relatively constant inductance over temperature and frequency. Typically, an open-core inductor is desirable since these types of inductors are more linear. Toroidal inductors without an air gap are not recommended. Q-shielded inductors may be required if the amplifier is placed in an EMI-sensitive system. The series resistance of the inductors will reduce the attenuation of the switching frequency and reduce efficiency due to the ripple current in the inductor.

The capacitors should have a voltage rating 2 to 3 times the maximum expected RMS voltage—allowing for high peak voltages and transient spikes—and be stable over temperature. Good quality capacitors with low equivalent series resistance (ESR) and equivalent series inductance (ESL) are necessary to achieve optimum performance. Low-ESR capacitors will decrease power dissipation. High ESL will shift the cutoff frequency, and high ESR will reduce filter rolloff.

Bridge-Tied Load/Single-Ended Configuration

The MAX4295 can be used as either a BTL or single-ended configured amplifier. The BTL configuration offers several advantages over a single-ended configuration. By driving the load differentially, the output voltage swing is doubled and the output power is quadrupled in comparison to a single-ended configuration. Because the differential outputs are biased at half supply, there is no DC voltage across the load, eliminating the need for large DC-blocking capacitors at the output.

The MAX4295 can be configured as a single-ended amplifier. In such a case, the load must be capacitively coupled to the filter to block the half-supply DC voltage from the load. The unused output pin must also be left open (Figure 5). Do not connect the unused output pin to ground.

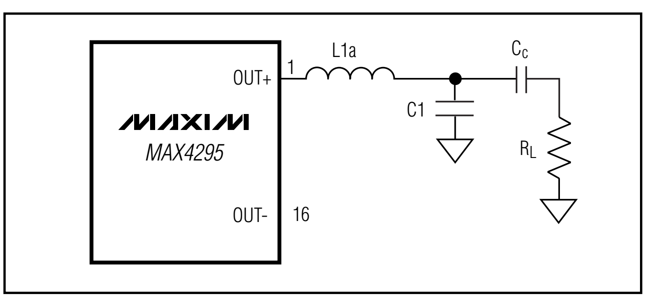


Figure 5. MAX4295 Single-Ended Configuration

Total Harmonic Distortion

The MAX4295 exhibits typical THD+N of <1% for input frequencies <10kHz. The PWM frequency affects THD performance. THD can be reduced by limiting the input bandwidth through the input highpass filter, choosing the lowest f_{OSC} possible, and carefully selecting the output filter and its components.

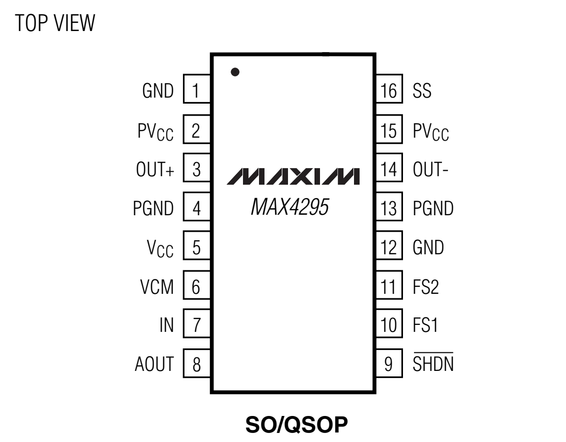
Bypassing and Layout Considerations

Distortion caused by supply ripple due to H-bridge switching can be reduced through proper bypassing of PV_{CC}. For optimal performance, a 330µF, low-ESR POSCAP capacitor to PGND and a 1µF ceramic capacitor to GND at each PV_{CC} input is suggested. Place the 1µF capacitor close to the PV_{CC} pin. Bypass V_{CC} with a 10µF capacitor in parallel with a 1µF capacitor to GND. Ceramic capacitors are recommended due to their low ESR.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the amplifier's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components as close as possible to the amplifier. Surface-mount components are recommended.

The MAX4295 requires two separate ground planes to prevent switching noise from the MOSFETs in the H-bridge from coupling into the rest of the circuit. PGND, the power ground, is utilized by the H-bridge and any external output components, while GND is used by the rest of the circuit. Connect the PGND and GND planes at only one point, as close to the power supply as possible. Any external components associated with the output of the MAX4295 must be connected to the PGND plane where applicable. Use the *Typical Operating Circuit* diagram as a reference. Refer to the evaluation kit manual for suggested component values, component suppliers, and layout.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 846

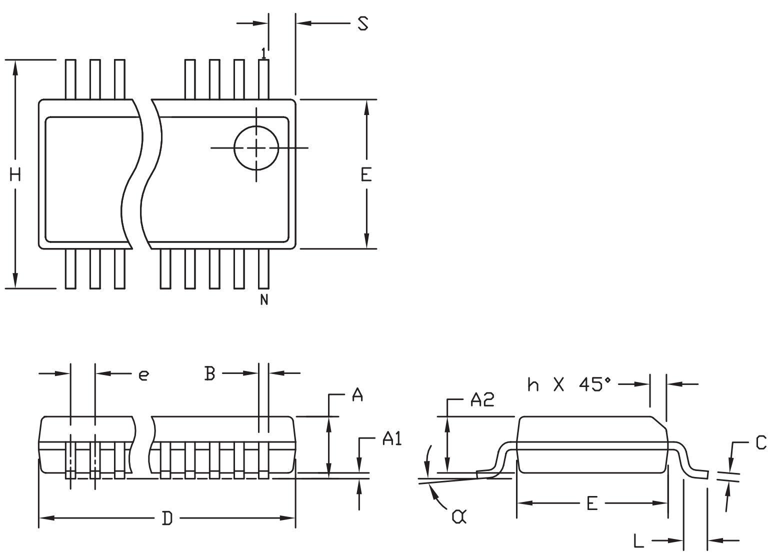
PROCESS: BiCMOS

Mono, 2W, Switch-Mode (Class D) Audio Power Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

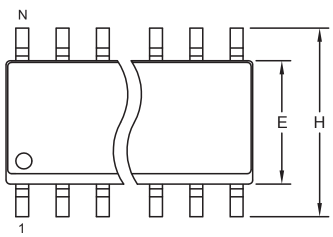
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

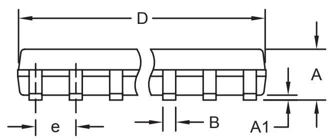
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



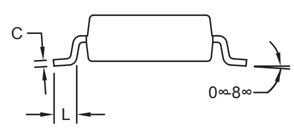
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1