19-2209; Rev 0; 10/01

MAXIM

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

General Description

The MAX4357 is a 32 x 16 highly integrated video crosspoint switch matrix with input and output buffers. This device operates from dual ±3V to ±5V supplies or from a single +5V supply. Digital logic is supplied from an independent single +2.7V to +5.5V supply. All inputs and outputs are buffered, with all outputs able to drive standard 75Ω reverse-terminated video loads.

The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface and initialized with a single update signal. The unique serial interface operates in two modes facilitating both fast updates and initialization. On power-up, all outputs are initialized in the disabled state to avoid output conflicts in large-array configurations.

Superior flexibility, high integration, and space-saving packaging make this nonblocking switch matrix ideal for routing video signals in security and video-on-demand systems.

The MAX4357 is available in a 128-pin TQFP package and specified over an extended -40°C to +85°C temperature range.

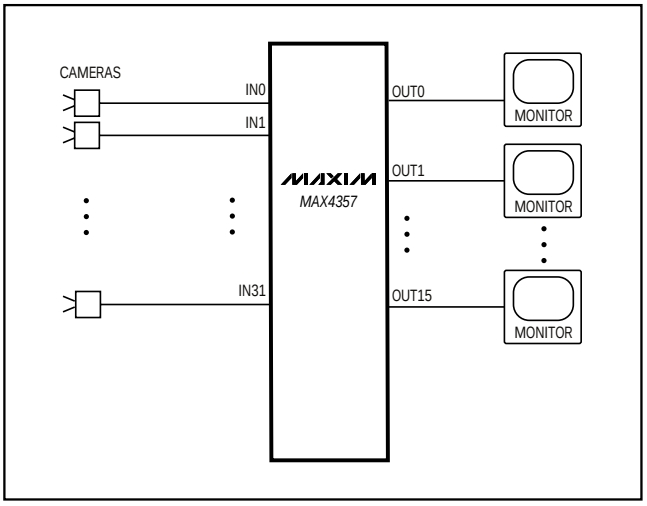
Applications

Security Systems

Video Routing

Video-On-Demand Systems

Typical Operating Circuit



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Features

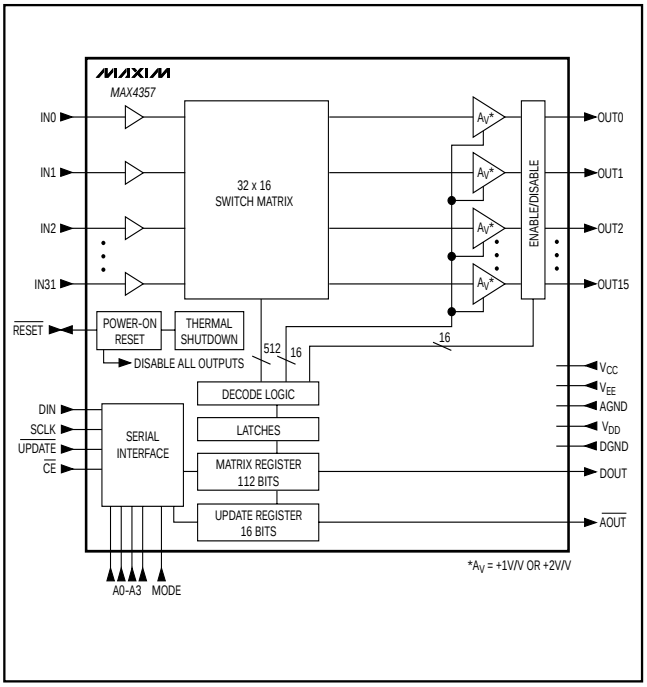
- **32 × 16 Nonblocking Matrix with Buffered Inputs and Outputs**
- **Operates from a ±3V, ±5V, or +5V Supply**
- **Each Output Individually Addressable**
- **Individually Programmable Output Buffer Gain (A_V = +1V/V or +2V/V)**
- **High-Impedance Output Disable for Wired-OR Connections**
- **0.1dB Gain Flatness to 12MHz**
- **Minimum -62dB Crosstalk, -110dB Isolation at 6MHz**
- **0.05%/0.1° Differential Gain/Differential Phase Error**
- **Low 220mW Power Consumption (0.43mW per Point)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4357ECD	-40°C to +85°C	128 TQFP

Pin Configuration appears at end of data sheet.

Functional Diagram



32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (V_{CC} - V_{EE}) .....+11V
Digital Supply Voltage (V_{DD} - DGND) .....+6V
Analog Supplies to Analog Ground
(V_{CC} - AGND) and (AGND - V_{EE}) ..... +6V
Analog Ground to Digital Ground .....-0.3V to +0.3V
IN_ Voltage Range ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
OUT_ Short-Circuit Duration to AGND, V_{CC}, or V_{EE}.....Indefinite
SCLK, $\overline{CE}$, $\overline{UPDATE}$, MODE, A_, DIN, DOUT,
$\overline{RESET}$, $\overline{AOUT}$.....(V_{DD} + 0.3V) to (DGND - 0.3V)
Current into Any Analog Input Pin (IN_) .....±50mA
Current into Any Analog Output Pin (OUT_).....±75mA
Continuous Power Dissipation (T_A = +70°C)
128-Pin TQFP (derate 25mW/°C above +70°C).....2W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±5V

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC} - V_{EE}	Guaranteed by PSRR test		4.5		10.5	V
Logic-Supply Voltage Range	V_{DD} to DGND			2.7		5.5	V
Gain (Note 1)	A_V	(V_{EE} + 2.5V) < $V_{IN\_}$ < (V_{CC} - 2.5V), A_V = +1V/V, R_L = 150Ω		0.97	0.995	1	V/V
		(V_{EE} + 2.5V) < $V_{IN\_}$ < (V_{CC} - 2.5V), A_V = +1V/V, R_L = 10kΩ		0.99	0.999	1	
		(V_{EE} + 3.75V) < $V_{IN\_}$ < (V_{CC} - 3.75V), A_V = +2V/V, R_L = 150Ω		1.92	1.996	2.08	
		(V_{EE} + 3.75V) < $V_{IN\_}$ < (V_{CC} - 3.75V) A_V = +2V/V, R_L = 10kΩ		1.94	2.008	2.06	
		(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V), A_V = +1V/V, R_L = 10kΩ		0.95	0.994	1	
Gain Matching (Channel to Channel)		R_L = 10kΩ			0.5	1.5	%
		R_L = 150Ω			0.5	2	
Temperature Coefficient of Gain	TC_{AV}				10		ppm/°C
Input Voltage Range	$V_{IN\_}$	A_V = +1V/V	R_L = 10kΩ	V_{EE} + 1		V_{CC} - 1.2	V
			R_L = 150Ω	V_{EE} + 2.5		V_{CC} - 2.5	
		A_V = +2V/V	R_L = 10kΩ	V_{EE} + 3		V_{CC} - 3.1	
			R_L = 150Ω	V_{EE} + 3.75		V_{CC} - 3.75	

DC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±5V (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Range	V_{OUT}	R_L = 10kΩ		V_{EE} + 1		V_{CC} - 1.2	V
		R_L = 150Ω		V_{EE} + 2.5		V_{CC} - 2.5	
Input Bias Current	I_B				4	11	µA
Input Resistance	$R_{IN\_}$	(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V)			10		MΩ
Output Offset Voltage	V_{OFFSET}	A_V = +1V/V			±5	±20	mV
		A_V = +2V/V			±10	±40	
Output Short-Circuit Current	I_{SC}	Sinking or sourcing, R_L = 1Ω			±40		mA
Enabled Output Impedance	Z_{OUT}	(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V)			0.2		Ω
Output Leakage Current, Disable Mode	I_{OD}	(V_{EE} + 1V) < $V_{OUT\_}$ < (V_{CC} - 1.2V)			0.004	1	µA
DC Power-Supply Rejection Ratio	PSRR	4.5V < (V_{CC} - V_{EE}) < 10.5V		60	70		dB
Quiescent Supply Current	I_{CC}	R_L = ∞	Outputs enabled, T_A = +25°C		100	150	mA
			Outputs enabled			175	
			Outputs disabled		55	75	
	I_{EE}	R_L = ∞	Outputs enabled, T_A = +25°C		95	150	
			Outputs enabled			175	
			Outputs disabled		50	75	
	I_{DD}				4	8	

DC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±3V

(V_{CC} = +3V, V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC} - V_{EE}	Guaranteed by PSRR test		4.5		10.5	V
Logic-Supply Voltage Range	V_{DD} to DGND			2.7		5.5	V
Gain (Note 1)	A_V	(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V), A_V = +1V/V, R_L = 150Ω		0.94	0.983	1	V/V
		(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V), A_V = +1V/V, R_L = 10kΩ		0.96	0.993	1	
		(V_{EE} + 2V) < $V_{IN\_}$ < (V_{CC} - 2.1V), A_V = +2V/V, R_L = 150Ω		1.92	1.985	2.08	
		(V_{EE} + 2V) < $V_{IN\_}$ < (V_{CC} - 2.1V) A_V = +2V/V, R_L = 10kΩ		1.94	2.00	2.06	
Gain Matching (Channel to Channel)		R_L = 10kΩ			0.5	1.5	%
		R_L = 150Ω			0.5	2	
Temperature Coefficient of Gain	TC_{AV}				10		ppm/°C
Input Voltage Range	$V_{IN\_}$	A_V = +1V/V	R_L = 10kΩ	V_{EE} + 1		V_{CC} - 1.2	V
			R_L = 150Ω	V_{EE} + 1		V_{CC} - 1.2	
		A_V = +2V/V	R_L = 10kΩ	V_{EE} + 2		V_{CC} - 2.1	
			R_L = 150Ω	V_{EE} + 2		V_{CC} - 2.1	
Output Voltage Range	V_{OUT}	R_L = 10kΩ		V_{EE} + 1		V_{CC} - 1.2	V
		R_L = 150Ω		V_{EE} + 1		V_{CC} - 1.2	
Input Bias Current	I_B				4	11	µA
Input Resistance	R_{IN}	(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V)			10		MΩ
Output Offset Voltage	V_{OFFSET}	A_V = +1V/V			±5	±20	mV
		A_V = +2V/V			±10	±40	

DC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±3V (continued)

(V_{CC} = +3V, V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{SC}	Sinking or sourcing, R_L = 1Ω			±40		mA
Enabled Output Impedance	Z_{OUT}	(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V)			0.2		Ω
Output Leakage Current, Disable Mode	I_{OD}	(V_{EE} + 1V) < $V_{OUT\_}$ < (V_{CC} - 1.2V)			0.004	1	µA
DC Power-Supply Rejection Ratio	PSRR	4.5V < (V_{CC} - V_{EE}) < 10.5V		60	75		dB
Quiescent Supply Current	I_{CC}	R_L = ∞	Outputs enabled		90		mA
			Outputs disabled		45		
	I_{EE}	R_L = ∞	Outputs enabled		85		
			Outputs disabled		40		
	I_{DD}				3		

DC ELECTRICAL CHARACTERISTICS—SINGLE SUPPLY +5V

(V_{CC} = +5V, V_{EE} = 0, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = +1.75V, A_V = +1V/V, R_L = 150Ω to AGND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	Guaranteed by PSRR test		4.5		5.5	V
Logic-Supply Voltage Range	V_{DD} to DGND			2.7		5.5	V
Gain (Note 1)	A_V	(V_{EE} + 1V) < V_{IN} < (V_{CC} - 2.5V), A_V = +1V/V, R_L = 150Ω		0.94	0.995	1	V
		(V_{EE} + 1V) < V_{IN} < (V_{CC} - 1.2V), A_V = +1V/V, R_L = 10kΩ		0.94	0.995	1	
Gain Matching (Channel to Channel)		R_L = 10kΩ			0.5	3	%
		R_L = 150Ω			0.5	3	
Temperature Coefficient of Gain	TC_{AV}				10		ppm/°C
Input Voltage Range	V_{IN}	A_V = +1V/V	R_L = 10kΩ	V_{EE} + 1		V_{CC} - 1.2	V
			R_L = 150Ω	V_{EE} + 1		V_{CC} - 2.5	
Output Voltage Range	V_{OUT}	A_V = +1V/V, R_L = 10kΩ		V_{EE} + 1		V_{CC} - 1.2	V
		A_V = +1V/V, R_L = 150Ω		V_{EE} + 1		V_{CC} - 2.5	

DC ELECTRICAL CHARACTERISTICS—SINGLE SUPPLY +5V (continued)

(V_{CC} = +5V, V_{EE} = 0, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = +1.75V, A_V = +1V/V, R_L = 150Ω to AGND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Bias Current	I_B				4	11	µA
Input Resistance	R_{IN}	V_{EE} + 1V < $V_{IN\_}$ < V_{CC} - 1.2V			10		MΩ
Output Offset Voltage	V_{OFFSET}	A_V = +1V/V			±10	±40	mV
Output Short-Circuit Current	I_{SC}	Sinking or sourcing, R_L = 1Ω			±35		mA
Enabled Output Impedance	Z_{OUT}	(V_{EE} + 1V) < $V_{IN\_}$ < (V_{CC} - 1.2V)			0.2		Ω
Output Leakage Current, Disable Mode	I_{OD}	(V_{EE} + 1V) < $V_{OUT\_}$ < (V_{CC} - 1.2V)			0.004	1	µA
DC Power-Supply Rejection Ratio	PSRR	4.5V < V_{CC} - V_{EE} < 5.5V	T_A = +25°C to +85°C	50	65		dB
			T_A = -40°C to +85°C	35			
Quiescent Supply Current	I_{CC}	R_L = ∞	Outputs enabled, T_A = +25°C		90		mA
			Outputs disabled		40		
	I_{EE}	R_L = ∞	Outputs enabled, T_A = +25°C		85		
			Outputs disabled		35		
	I_{DD}				4		

LOGIC-LEVEL CHARACTERISTICS

(V_{CC} - V_{EE}) = +4.5V to +10.5V, V_{DD} = +2.7V to +5.5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage High Level	V_{IH}	V_{DD} = +5.0V		3			V
		V_{DD} = +3V		2			
Input Voltage Low Level	V_{IL}	V_{DD} = +5.0V				0.8	V
		V_{DD} = +3V				0.6	
Input Current High Level	I_{IH}	V_I > 2V	Excluding $\overline{RESET}$	-1	0.01	1	µA
			$\overline{RESET}$	-30	-20		
Input Current Low Level	I_{IL}	V_I < 1V	Excluding $\overline{RESET}$	-1	0.01	1	µA
			$\overline{RESET}$	-300	-235		
Output Voltage High Level	V_{OH}	I_{SOURCE} = 1mA, V_{DD} = +5V		4.7	4.9		V
		I_{SOURCE} = 1mA, V_{DD} = +3V		2.7	2.9		
Output Voltage Low Level	V_{OL}	I_{SINK} = 1mA, V_{DD} = +5V			0.1	0.3	V
		I_{SINK} = 1mA, V_{DD} = +3V			0.1	0.3	
Output Current High Level	I_{OH}	V_{DD} = +5V, V_O = +4.9V		1	4		mA
		V_{DD} = +3V, V_{OUT} = +2.7V		1	8		
Output Current Low Level	I_{OL}	V_{DD} = +5V, V_O = +0.1V		1	4		mA
		V_{DD} = +3V, V_O = +0.3V		1	8		

AC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±5V

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	$V_{OUT\_}$ = 20mVp-p	A_V = +1V/V		95		MHz
			A_V = +2V/V		70		
Medium-Signal -3dB Bandwidth	BW_{MS}	$V_{OUT\_}$ = 200mVp-p	A_V = +1V/V		90		MHz
			A_V = +2V/V		70		
Large-Signal -3dB Bandwidth	BW_{LS}	$V_{OUT\_}$ = 2Vp-p	A_V = +1V/V		40		MHz
			A_V = +2V/V		50		
Small-Signal 0.1dB Bandwidth	$BW_{0.1dB-SS}$	$V_{OUT\_}$ = 20mVp-p	A_V = +1V/V		15		MHz
			A_V = +2V/V		15		
Medium-Signal 0.1dB Bandwidth	$BW_{0.1dB-MS}$	$V_{OUT\_}$ = 200mVp-p	A_V = +1V/V		15		MHz
			A_V = +2V/V		15		
Large-Signal 0.1dB Bandwidth	$BW_{0.1dB-LS}$	$V_{OUT\_}$ = 2Vp-p	A_V = +1V/V		12		MHz
			A_V = +2V/V		12		
Slew Rate	SR	$V_{OUT\_}$ = 2V step, A_V = +1V/V			150		Vµs
		$V_{OUT\_}$ = 2V step, A_V = +2V/V			160		

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

AC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±5V (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Settling Time	$t_{S\ 0.1\%}$	$V_{OUT\_}$ = 0 to 2V step	A_V = +1V/V		60		ns
			A_V = +2V/V		60		
Switching Transient (Glitch) (Note 3)		A_V = +1V/V			50		mV
		A_V = +2V/V			50		
AC Power-Supply Rejection Ratio		f = 100kHz			70		dB
		f = 1MHz			68		
Differential Gain Error (Note 4)		R_L = 1kΩ			0.01		%
		R_L = 150Ω			0.05		
Differential Phase Error (Note 4)		R_L = 1kΩ			0.03		Degrees
		R_L = 150Ω			0.1		
Crosstalk, All Hostile		f = 6MHz			-62		dB
Off-Isolation, Input-to-Output		f = 6MHz			-110		dB
Input Noise Voltage Density	e_n	BW = 6MHz			73		μV_{RMS}
Input Capacitance	C_{IN}				5		pF
Disabled Output Capacitance		Amplifier in disable mode			3		pF
Capacitive Load at 3dB Output Peaking					30		pF
Output Impedance	Z_{OUT}	f = 6MHz	Output enabled		3		Ω
			Output disabled		4k		

AC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±3V

(V_{CC} = +3V, V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	$V_{OUT\_}$ = 20mVp-p	A_V = +1V/V		90		MHz
			A_V = +2V/V		65		
Medium-Signal -3dB Bandwidth	BW_{MS}	$V_{OUT\_}$ = 200mVp-p	A_V = +1V/V		90		MHz
			A_V = +2V/V		65		
Large-Signal -3dB Bandwidth	BW_{LS}	$V_{OUT\_}$ = 2Vp-p	A_V = +1V/V		30		MHz
			A_V = +2V/V		35		
Small-Signal 0.1dB Bandwidth	$BW_{0.1dB-SS}$	$V_{OUT\_}$ = 20mVp-p	A_V = +1V/V		15		MHz
			A_V = +2V/V		15		
Medium-Signal 0.1dB Bandwidth	$BW_{0.1dB-MS}$	$V_{OUT\_}$ = 200mVp-p	A_V = +1V/V		15		MHz
			A_V = +2V/V		15		
Large-Signal 0.1dB Bandwidth	$BW_{0.1dB-LS}$	$V_{OUT\_}$ = 2Vp-p	A_V = +1V/V		12		MHz
			A_V = +2V/V		12		

AC ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES ±3V (continued)

(V_{CC} = +3V, V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	SR	$V_{OUT\_}$ = 2V step A_V = +1V/V			120		Vμs
		$V_{OUT\_}$ = 2V step A_V = +2V/V			120		
Settling Time	$t_{S\ 0.1\%}$	V_O = 0 to 2V step	A_V = +1V/V		60		ns
			A_V = +2V/V		60		
Switching Transient (Glitch) (Note 3)		A_V = +1V/V			15		mV
		A_V = +2V/V			20		
AC Power-Supply Rejection Ratio		f = 100kHz			60		dB
		f = 1MHz			40		
Differential Gain Error (Note 4)		R_L = 1kΩ			0.03		%
		R_L = 150Ω			0.2		
Differential Phase Error (Note 4)		R_L = 1kΩ			0.08		Degrees
		R_L = 150Ω			0.2		
Crosstalk, All Hostile		f = 6MHz			-63		dB
Off-Isolation, Input to Output		f = 6MHz			-112		dB
Input Noise Voltage Density	e_n	BW = 6MHz			73		$μV_{RMS}$
Input Capacitance	$C_{IN\_}$				5		pF
Disabled Output Capacitance		Amplifier in disable mode			3		pF
Capacitive Load at 3dB Output Peaking					30		pF
Output Impedance	z_{OUT}	f = 6MHz	Output enabled		3		Ω
			Output disabled		4k		

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

AC ELECTRICAL CHARACTERISTICS—SINGLE SUPPLY +5V

(V_{CC} = +5V, V_{EE} = 0, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 1.75V, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	$V_{OUT\_}$ = 20mVp-p			90		MHz
Medium-Signal -3dB Bandwidth	BW_{MS}	$V_{OUT\_}$ = 200mVp-p			90		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	$V_{OUT\_}$ = 1.5Vp-p			38		MHz
Small-Signal 0.1dB Bandwidth	$BW_{0.1dB-SS}$	$V_{OUT\_}$ = 20mVp-p			12		MHz
Medium-Signal 0.1dB Bandwidth	$BW_{0.1dB-MS}$	$V_{OUT\_}$ = 200mVp-p			12		MHz
Large-Signal 0.1dB Bandwidth	$BW_{0.1dB-LS}$	$V_{OUT\_}$ = 1.5Vp-p			12		MHz
Slew Rate	SR	$V_{OUT\_}$ = 2V step, A_V = +1V/V			100		V/µs
Settling Time	$t_{S\ 0.1\%}$	$V_{OUT\_}$ = 0 to 2V step			60		ns
Switching Transient (Glitch)					25		mV
AC Power-Supply Rejection Ratio		f = 100kHz			70		dB
		f = 1MHz			69		
Differential Gain Error (Note 4)		R_L = 1kΩ			0.03		%
		R_L = 150Ω			0.15		
Differential Phase Error (Note 4)		R_L = 1kΩ			0.06		Degrees
		R_L = 150Ω			0.2		
Crosstalk, All Hostile		f = 6MHz			-63		dB
Off-Isolation, Input-to-Output		f = 6MHz			-110		dB
Input Noise Voltage	e_n	BW = 6MHz			73		$µV_{RMS}$
Input Capacitance	$C_{IN\_}$				5		pF
Disabled Output Capacitance		Amplifier in disable mode			3		pF
Capacitive Load at 3dB Output Peaking					30		pF
Output Impedance	Z_{OUT}	f = 6MHz	Output enabled		3		Ω
			Output disabled		4k		

SWITCHING CHARACTERISTICS

((V_{CC} - V_{EE}) = +4.5V to +10.5V, V_{DD} = +2.7V to +5.5V, DGND = AGND = 0, $V_{IN\_}$ = 0 for dual supplies, $V_{IN\_}$ = +1.75V for single supply, R_L = 150Ω to AGND, C_L = 100pF, A_V = +1V/V, and T_A = T_{MIN} - T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay: $\overline{UPDATE}$ to Video Out	t_{PdUdVo}	V_{IN} = 0.5V step		200	450	ns
Delay: $\overline{UPDATE}$ to $\overline{AOUT}$	t_{PdUdAo}	MODE = 0, time to $\overline{AOUT}$ = low after $\overline{UPDATE}$ = low		30	200	ns
Delay: SCLK to DOUT Valid	t_{PdDo}	Logic state change in DOUT on active SCLK edge		30	200	ns
Delay: Output Disable	$t_{PdHOeVo}$	V_{OUT} = 0.5V, 1kΩ pulldown to AGND		300	800	ns
Delay: Output Enable	$t_{PdLOeVo}$	Output disabled, 1kΩ pulldown to AGND, V_{IN} = 0.5V		200	800	ns
Setup: $\overline{CE}$ to SCLK	t_{SuCe}				100	ns
Setup: DIN to SCLK	t_{SuDi}		100			ns
Hold Time: SCLK to DIN	t_{HdDi}		100			ns
Minimum High Time: SCLK	t_{MnHCk}		100			ns
Minimum Low Time: SCLK	t_{MnLCk}		100			ns
Minimum Low Time: $\overline{UPDATE}$	t_{MnLUd}		100			ns
Setup Time: $\overline{UPDATE}$ to SCLK	t_{SuHUd}	Rising edge of $\overline{UPDATE}$ to falling edge of SCLK	100			ns
Hold Time: SCLK to $\overline{UPDATE}$	t_{HdHUd}	Falling edge of SCLK to falling edge of $\overline{UPDATE}$	100			ns
Setup Time: MODE to SCLK	t_{SuMd}	Minimum time from clock edge to MODE with valid data clocking	100			ns
Hold Time: MODE to SCLK	t_{HdMd}	Minimum time from clock edge to MODE with valid data clocking	100			ns
Minimum Low Time: $\overline{RESET}$	t_{MnLRst}				300	ns
Delay: $\overline{RESET}$	t_{PdRst}	10kΩ pulldown to AGND			600	ns

Note 1: Associated output voltage may be determined by multiplying the input voltage by the specified gain (A_V) and adding output offset voltage.

Note 2: Logic-level characteristics apply to the following pins: DIN, DOUT, SCLK, $\overline{CE}$, $\overline{UPDATE}$, $\overline{RESET}$, A3–A0, MODE, and $\overline{AOUT}$.

Note 3: Switching transient settling time is guaranteed by the settling time (t_S) specification. Switching transient is a result of updating the switch matrix.

Note 4: Input test signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0 to 100IRE). IRE is a unit of video-signal amplitude developed by the International Radio Engineers: 140IRE = 1.0V.

Note 5: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

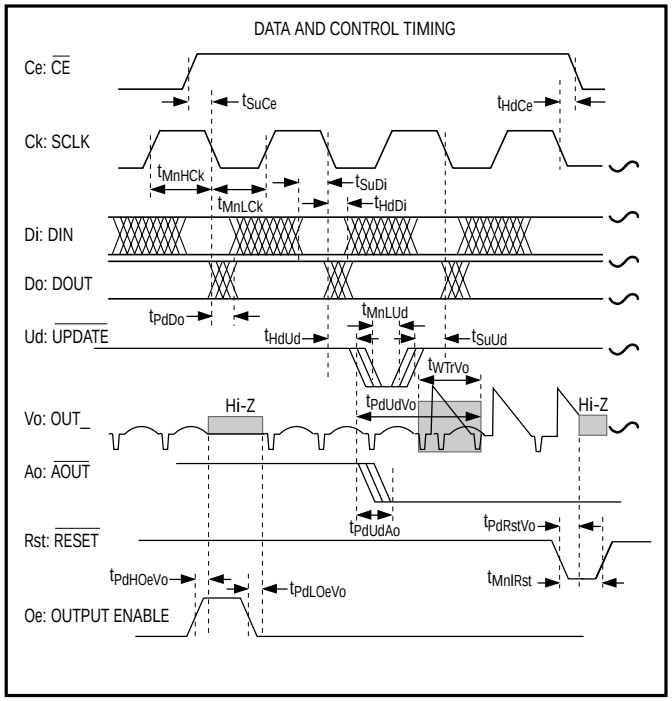
Symbol Definitions

SYMBOL	TYPE	DESCRIPTION
Ao	Signal	Address Valid Flag ($\overline{AOUT}$)
Ce	Signal	Clock Enable ($\overline{CE}$)
Ck	Signal	Clock (SCLK)
Di	Signal	Serial Data In (DIN)
Do	Signal	Serial Data Output (DOUT)
Md	Signal	MODE
Oe	Signal	Output Enable
Rst	Signal	Reset Input ($\overline{RESET}$)
Ud	Signal	$\overline{UPDATE}$
Vo	Signal	Video Out (OUT)
H	Property	High or Low-to-High Transition
Hd	Property	Hold
L	Property	Low or High-to-Low Transition
Mn	Property	Minimum
Mx	Property	Maximum
Pd	Property	Propagation delay
Su	Property	Setup
Tr	Property	Transition
W	Property	Width

Naming Conventions

- All parameters with time units are given a “t” designation, with appropriate subscript modifiers.
- Propagation delays for clocked signals are from the active edge of clock.
- Propagation delay for level-sensitive signals is from input to output at 50% point of a transition.
- Setup and Hold times are measured from 50% point of signal transition to 50% point of clocking signal transition.
- Setup time refers to any signal that must be stable before active clock edge, even if the signal is not latched or clocked itself.
- Hold time refers to any signal that must be stable during and after active clock edge, even if the signal is not latched or clocked.
- Propagation delays to unobservable internal signals are modified to set up and hold designations applied to observable I/O signals.

Timing Diagram



TIMING PARAMETER DEFINITIONS	
NAME	**DESCRIPTION**
t_{HdDi}	Hold Time: Clock to Data In
t_{MnHCk}	Min High Time: Clk
t_{MnLCk}	Min Low Time: Clk
t_{MnLUd}	Min Low Time: Update
t_{SuHUd}	Setup Time: UPDATE to Clk with UPDATE High
Not Valid	Setup Time: UPDATE to Clk with UPDATE Low
t_{HdHUd}	Hold Time: Clk to UPDATE with UPDATE high
Not Valid	Hold Time: Clk to UPDATE with UPDATE Low
t_{PdDiDo}	Asynchronous Delay: Data In to Data Out
t_{MnMd}	Min Low Time: MODE
t_{MxTr}	Max Rise Time: Clk, Update
t_{MnLRst}	Min Low Time: Reset
$t_{PdRstVo}$	Delay: Reset to Video Output

TIMING PARAMETER DEFINITIONS	
NAME	**DESCRIPTION**
t_{PdUdVo}	Delay: Update to Video Out
t_{PdUdAo}	Delay: UPDATE to Aout
t_{PdDo}	Delay: Clk to Data Out
$t_{PdHOeVo}$	Delay: Output Enable to Video Output (High: Disable)
$t_{PdLOeVo}$	Delay: Output Enable to Video Output (Low: Enable)
t_{SuCe}	Setup: Clock Enable to Clock
t_{SuDi}	Setup Time: Data In to Clock

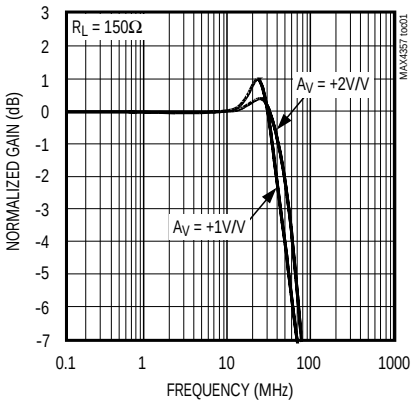
Figure 1. Timing Diagram

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

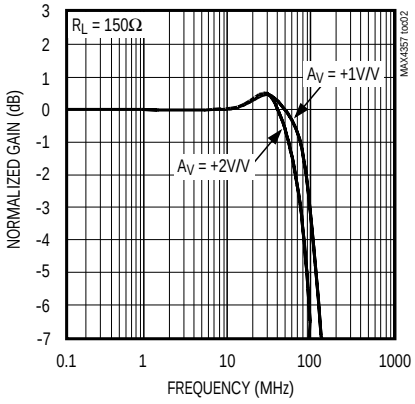
Typical Operating Characteristics—Dual Supplies ±5V

(V_{CC} = +5V and V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

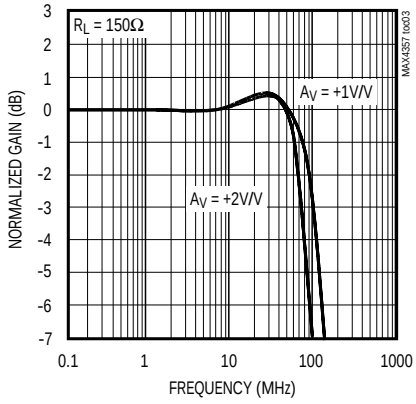
LARGE-SIGNAL FREQUENCY RESPONSE



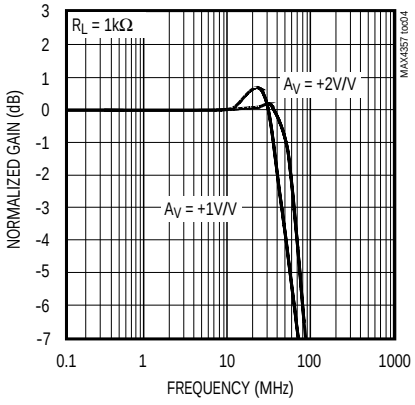
MEDIUM-SIGNAL FREQUENCY RESPONSE



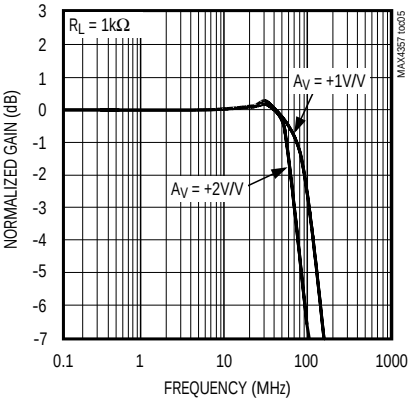
SMALL-SIGNAL FREQUENCY RESPONSE



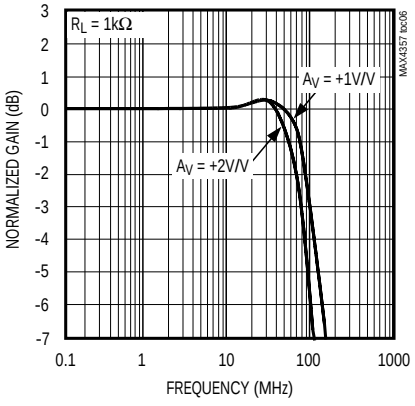
LARGE-SIGNAL FREQUENCY RESPONSE



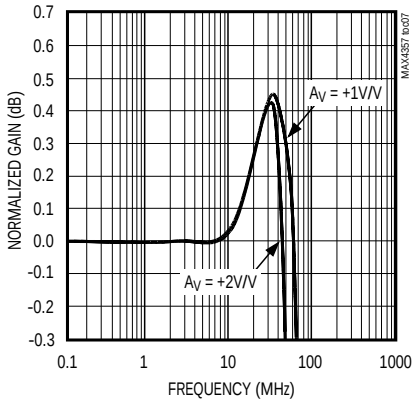
MEDIUM-SIGNAL FREQUENCY RESPONSE



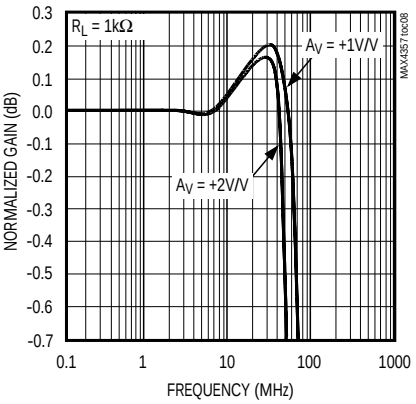
SMALL-SIGNAL FREQUENCY RESPONSE



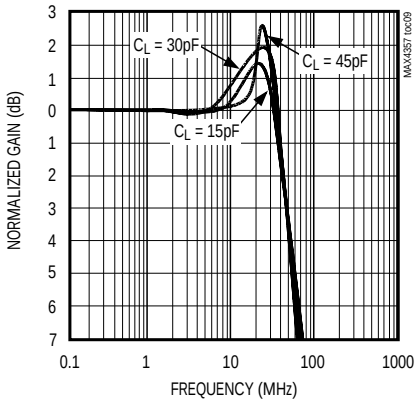
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



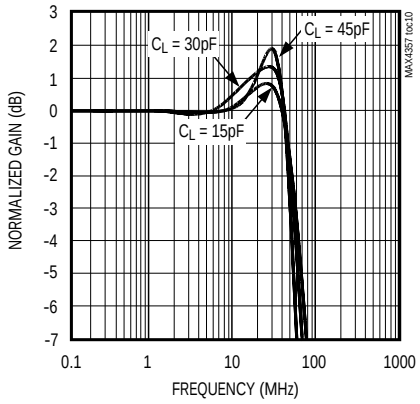
LARGE-SIGNAL FREQUENCY RESPONSE (A_V = +1V/V)



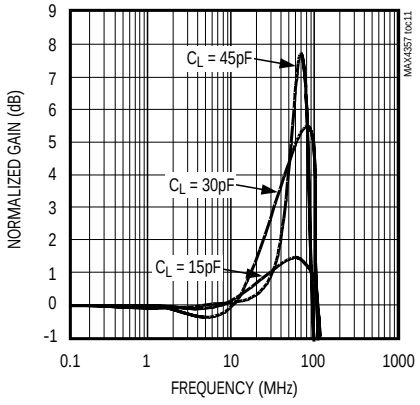
Typical Operating Characteristics—Dual Supplies ±5V (continued)

(V_{CC} = +5V and V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

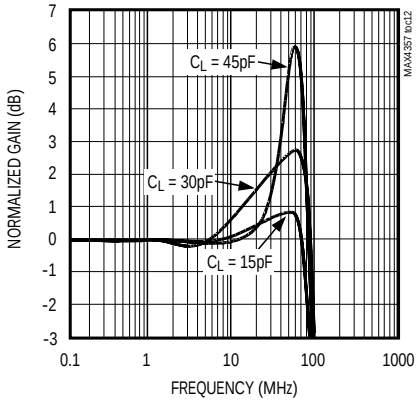
LARGE-SIGNAL FREQUENCY RESPONSE (A_V = +2V/V)



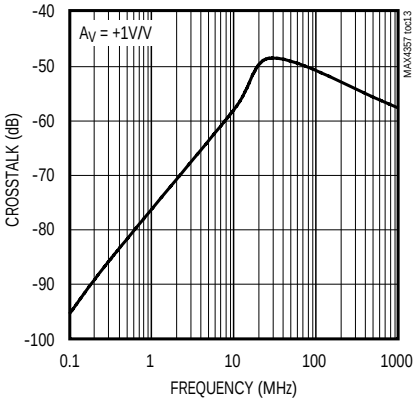
MEDIUM-SIGNAL FREQUENCY RESPONSE (A_V = +1V/V)



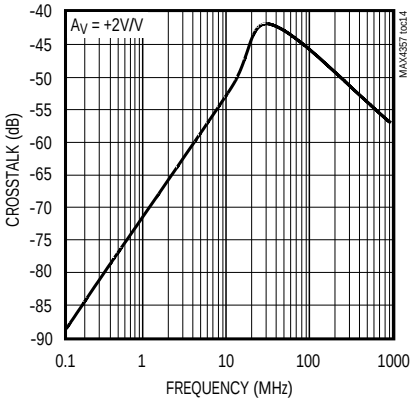
MEDIUM-SIGNAL FREQUENCY RESPONSE (A_V = +2V/V)



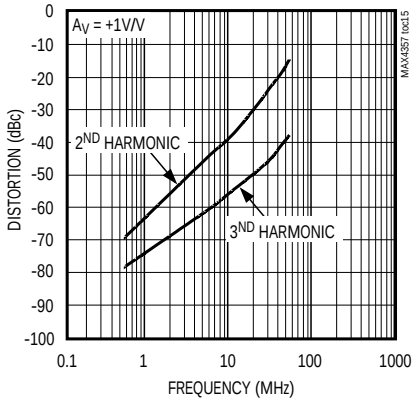
CROSSTALK vs. FREQUENCY



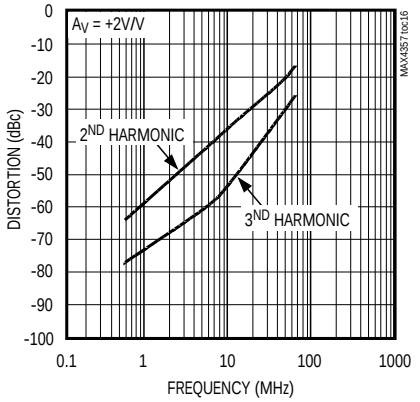
CROSSTALK vs. FREQUENCY



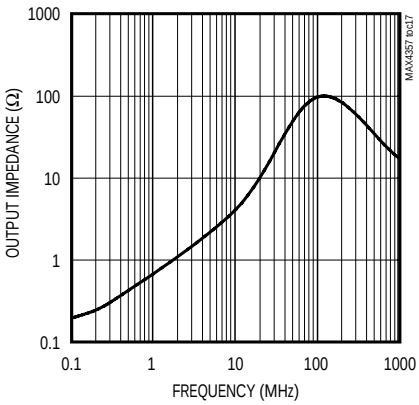
DISTORTION vs. FREQUENCY



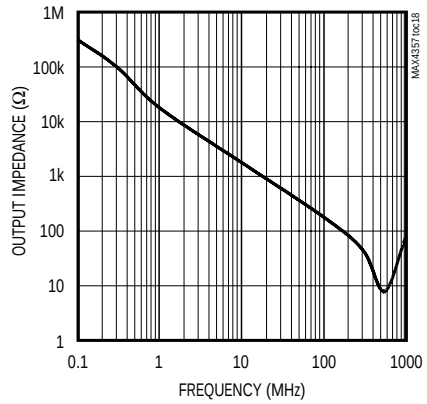
DISTORTION vs. FREQUENCY



ENABLED OUTPUT IMPEDANCE vs. FREQUENCY



DISABLED OUTPUT IMPEDANCE vs. FREQUENCY

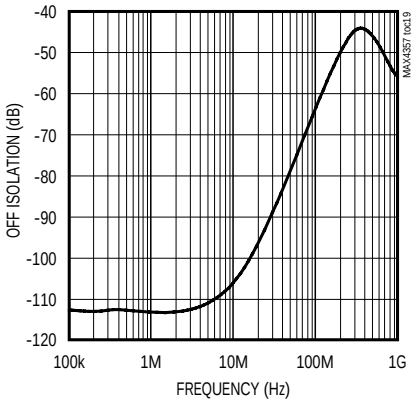


32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

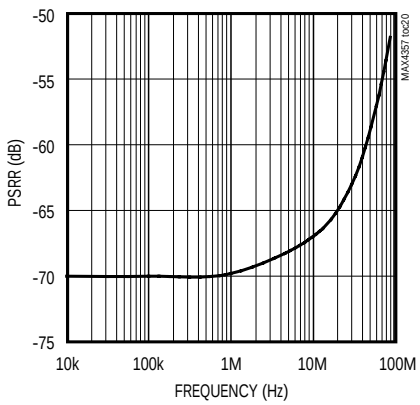
Typical Operating Characteristics—Dual Supplies ±5V (continued)

(V_{CC} = +5V and V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

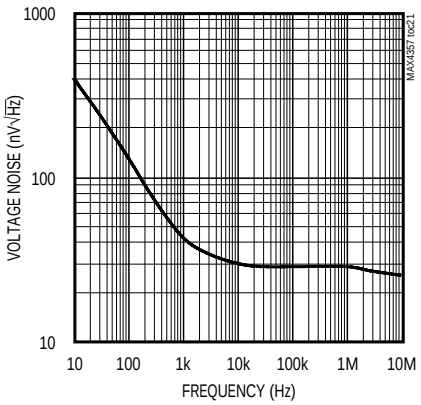
OFF-ISOLATION vs. FREQUENCY



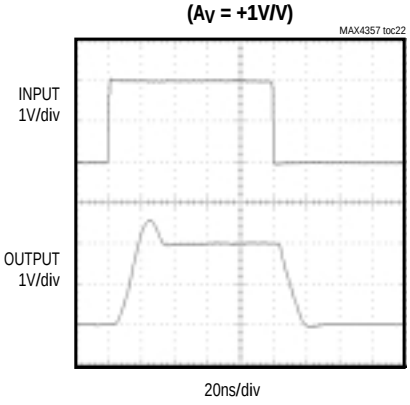
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



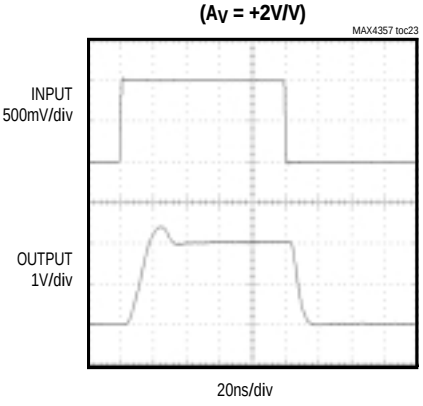
INPUT VOLTAGE NOISE vs. FREQUENCY



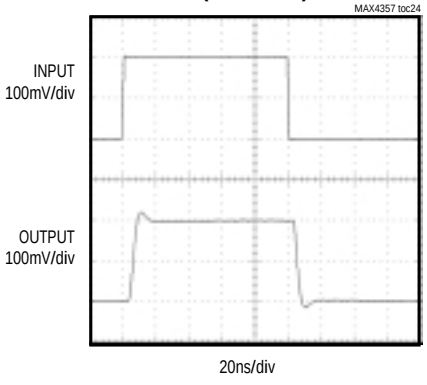
LARGE-SIGNAL PULSE RESPONSE (A_V = +1V/V)



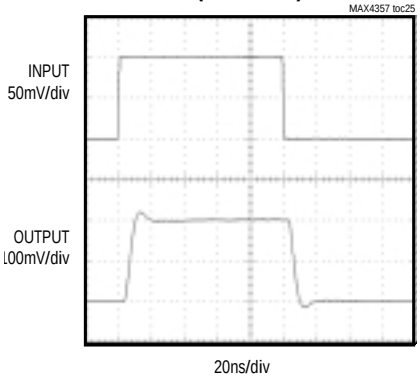
LARGE-SIGNAL PULSE RESPONSE (A_V = +2V/V)



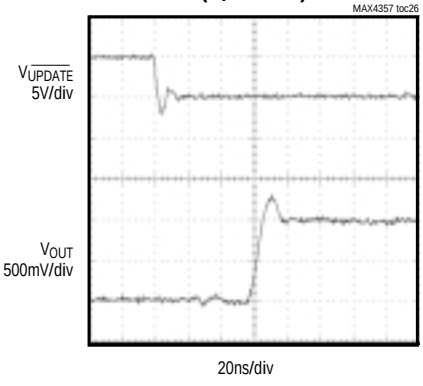
MEDIUM-SIGNAL PULSE RESPONSE (A_V = +1V/V)



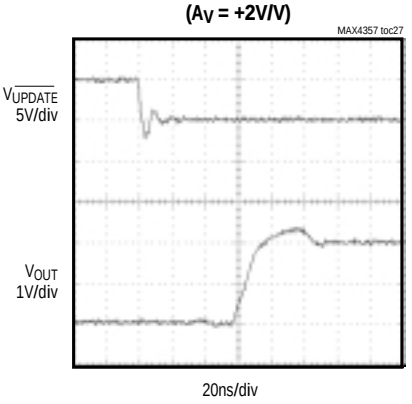
MEDIUM-SIGNAL PULSE RESPONSE (A_V = +2V/V)



SWITCHING TIME (A_V = +1V/V)



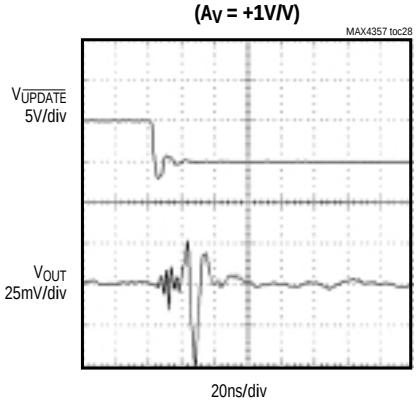
SWITCHING TIME (A_V = +2V/V)



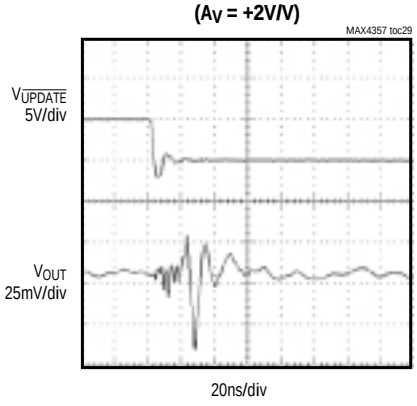
Typical Operating Characteristics—Dual Supplies ±5V (continued)

(V_{CC} = +5V and V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

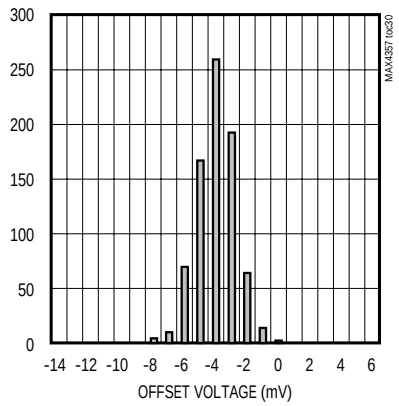
SWITCHING TRANSIENT (GLITCH) (A_V = +1V/V)



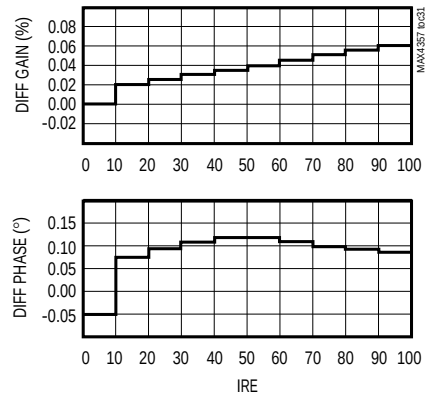
SWITCHING TRANSIENT (GLITCH) (A_V = +2V/V)



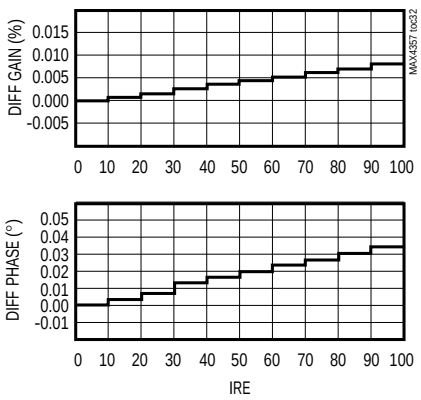
OFFSET VOLTAGE DISTRIBUTION



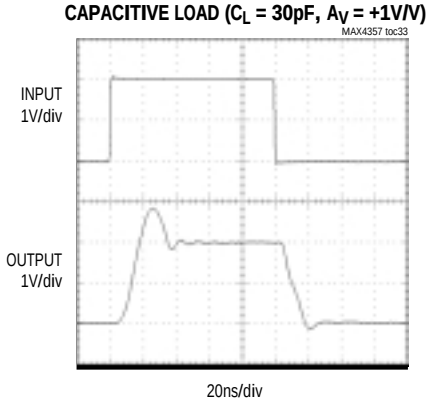
DIFFERENTIAL GAIN AND PHASE vs. DC VOLTAGE (R_L = 150Ω)



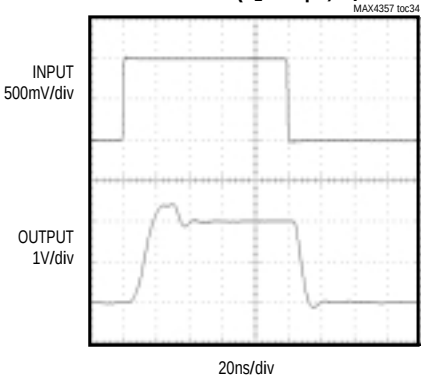
DIFFERENTIAL GAIN AND PHASE vs. DC VOLTAGE (R_L = 1kΩ)



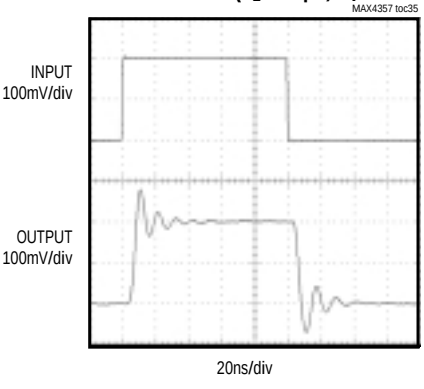
LARGE-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +1V/V)



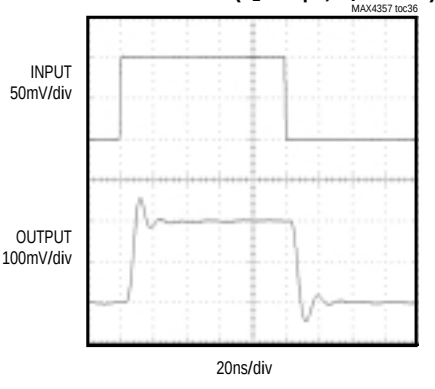
LARGE-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +2V/V)



MEDIUM-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +1V/V)



MEDIUM-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +2V/V)

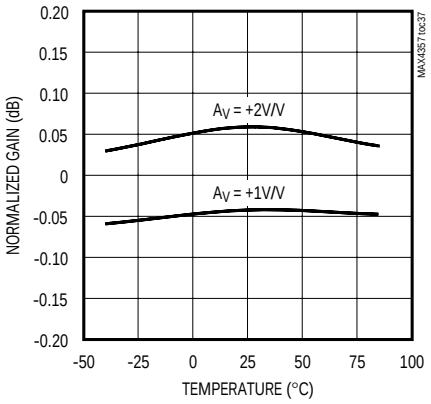


32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

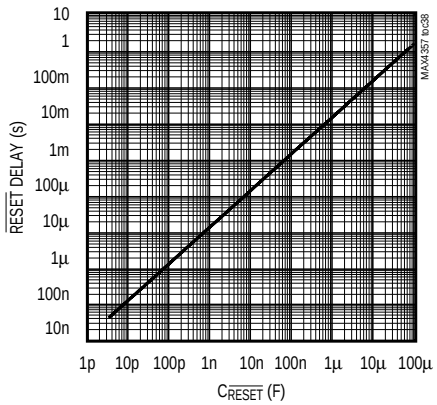
Typical Operating Characteristics—Dual Supplies ±5V (continued)

(V_{CC} = +5V and V_{EE} = -5V, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

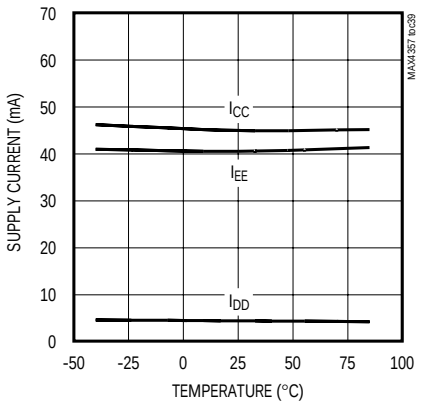
GAIN vs. TEMPERATURE



$\overline{RESET}$ DELAY vs. $\overline{RESET}$ CAPACITANCE



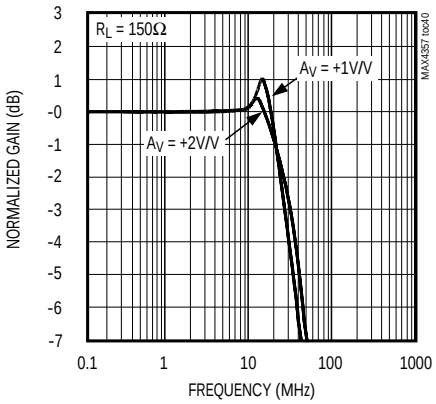
SUPPLY CURRENT vs. TEMPERATURE



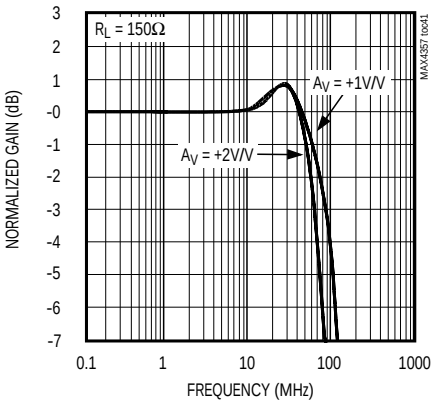
Typical Operating Characteristics—Dual Supplies ±3V

(V_{CC} = +3V and V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

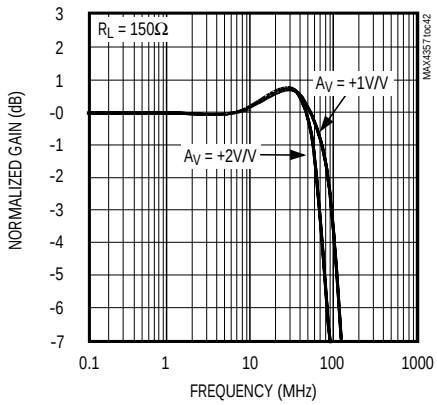
LARGE-SIGNAL FREQUENCY RESPONSE



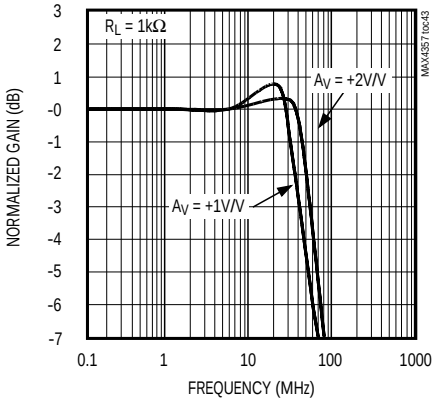
MEDIUM-SIGNAL FREQUENCY RESPONSE



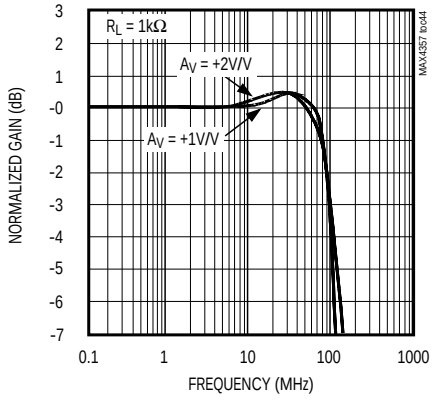
SMALL-SIGNAL FREQUENCY RESPONSE



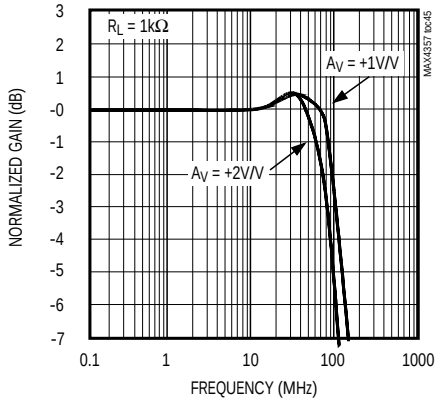
LARGE-SIGNAL FREQUENCY RESPONSE



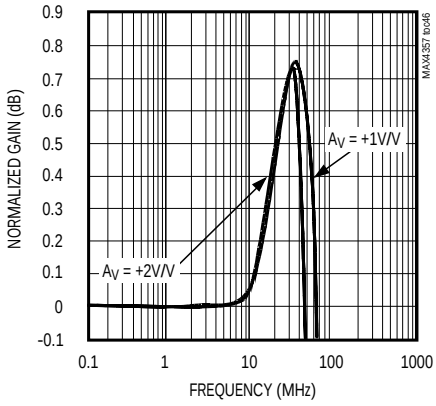
MEDIUM-SIGNAL FREQUENCY RESPONSE



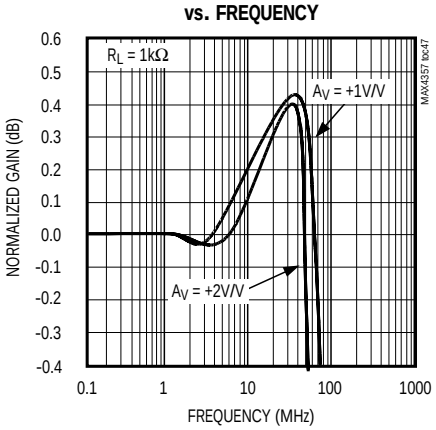
SMALL-SIGNAL FREQUENCY RESPONSE



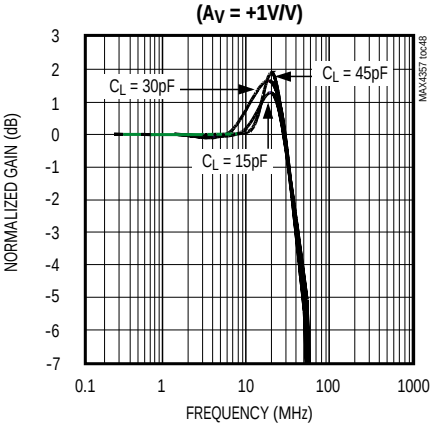
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



LARGE-SIGNAL FREQUENCY RESPONSE (A_V = +1V/V)

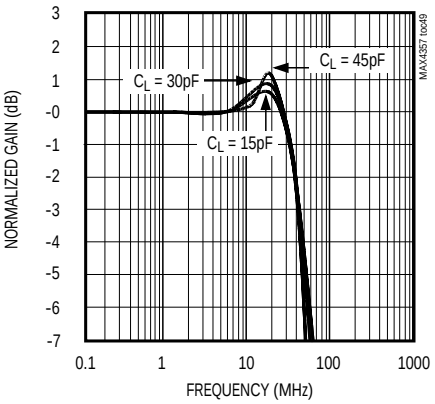


32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

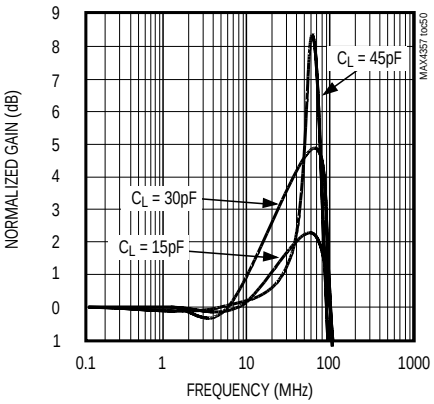
Typical Operating Characteristics—Dual Supplies ±3V (continued)

(V_{CC} = +3V and V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

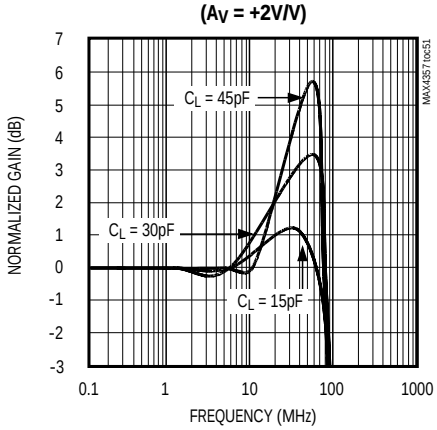
LARGE-SIGNAL FREQUENCY RESPONSE (A_V = +2V/V)



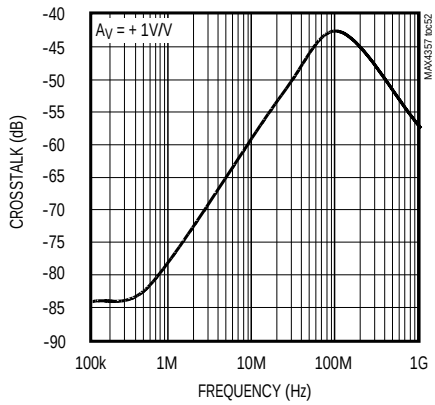
MEDIUM-SIGNAL FREQUENCY RESPONSE (A_V = +1V/V)



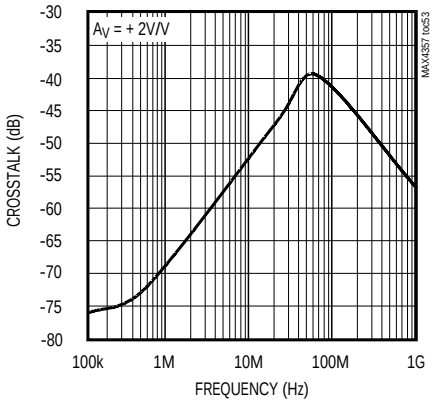
MEDIUM-SIGNAL FREQUENCY RESPONSE (A_V = +2V/V)



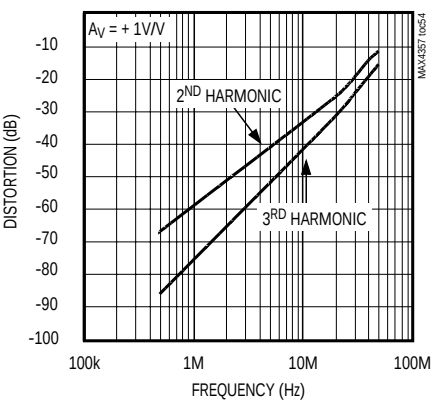
CROSSTALK vs. FREQUENCY



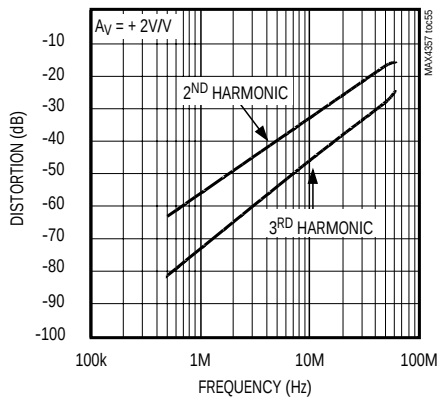
CROSSTALK vs. FREQUENCY



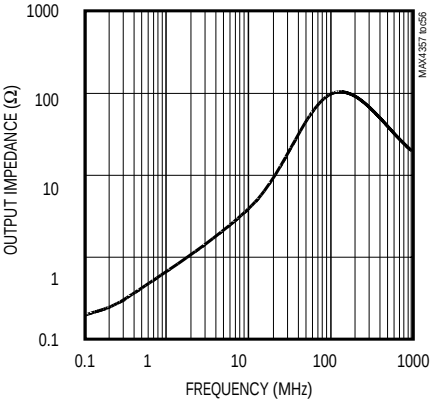
DISTORTION vs. FREQUENCY



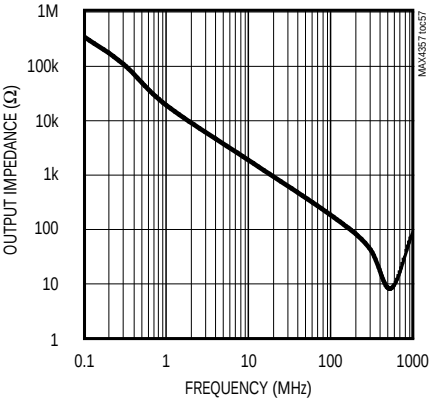
DISTORTION vs. FREQUENCY



ENABLED OUTPUT IMPEDANCE vs. FREQUENCY



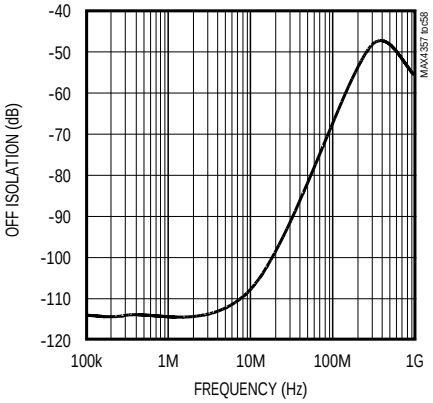
DISABLED OUTPUT IMPEDANCE vs. FREQUENCY



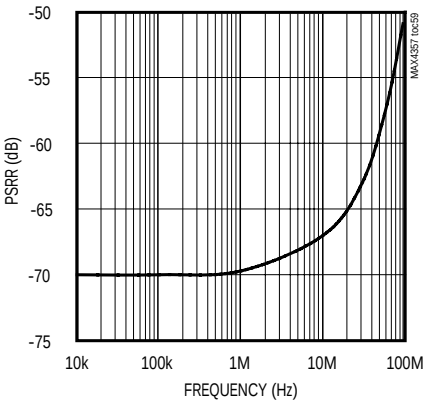
Typical Operating Characteristics—Dual Supplies ±3V (continued)

(V_{CC} = +3V and V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

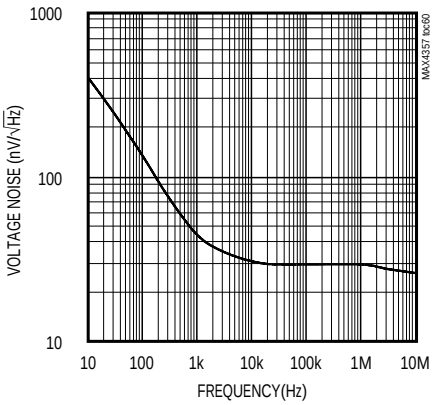
OFF-ISOLATION vs. FREQUENCY



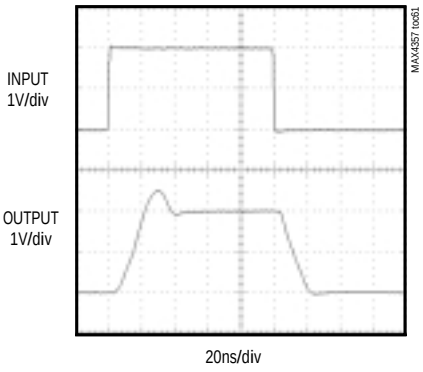
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



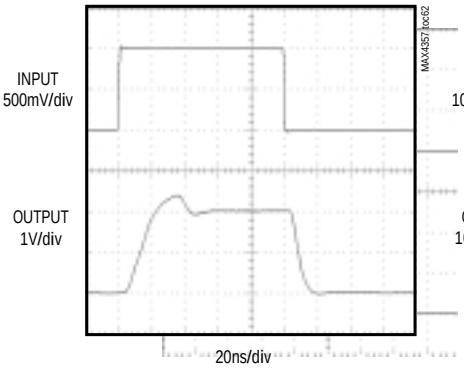
INPUT VOLTAGE NOISE vs. FREQUENCY



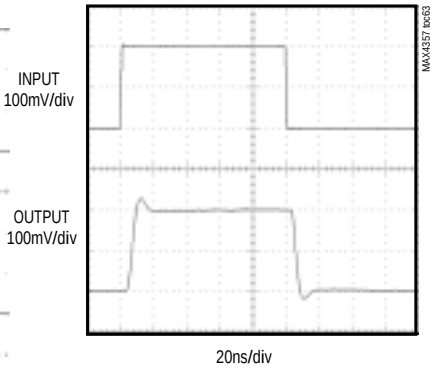
LARGE-SIGNAL PULSE RESPONSE (A_V = +1V/V)



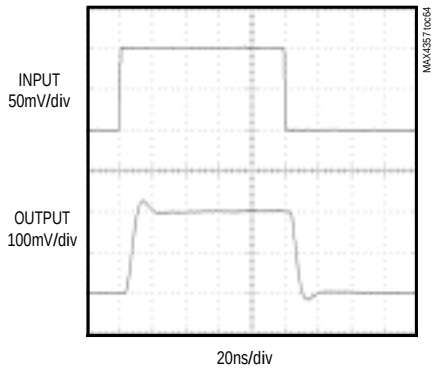
LARGE-SIGNAL PULSE RESPONSE (A_V = +2V/V)



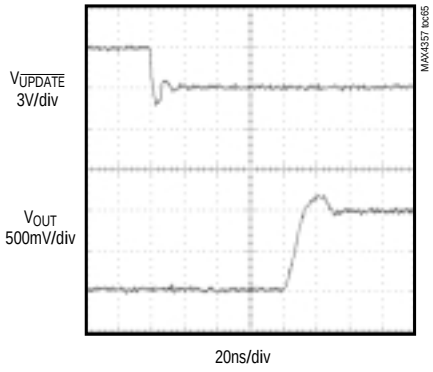
MEDIUM-SIGNAL PULSE RESPONSE (A_V = +1V/V)



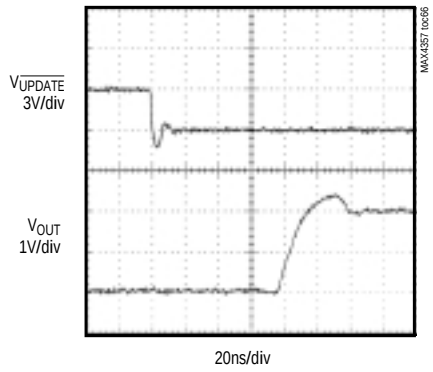
MEDIUM-SIGNAL PULSE RESPONSE (A_V = +2V/V)



SWITCHING TIME (A_V = +1V/V)



SWITCHING TIME (A_V = +2V/V)

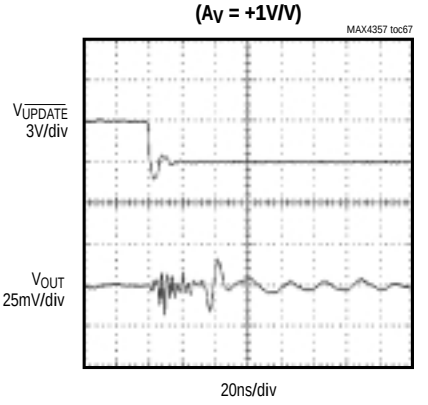


32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

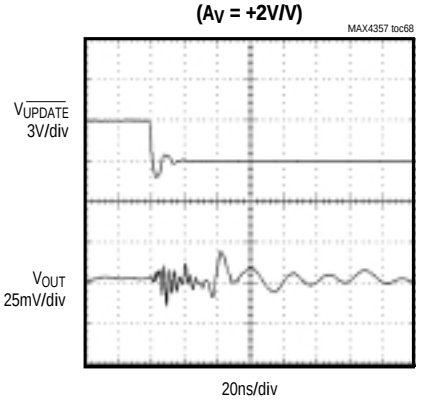
Typical Operating Characteristics—Dual Supplies ±3V (continued)

(V_{CC} = +3V and V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

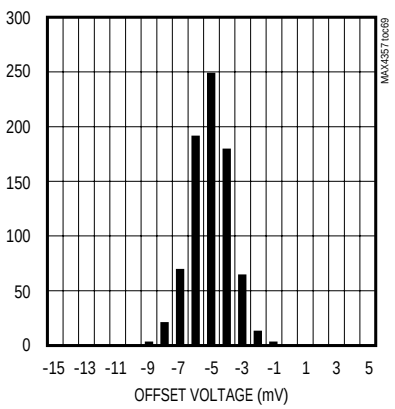
SWITCHING TRANSIENT GLITCH (A_V = +1V/V)



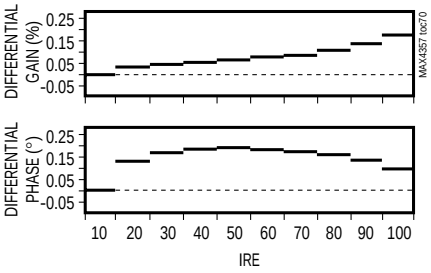
SWITCHING TRANSIENT GLITCH (A_V = +2V/V)



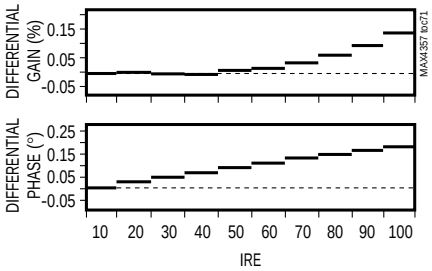
OFFSET VOLTAGE DISTRIBUTION



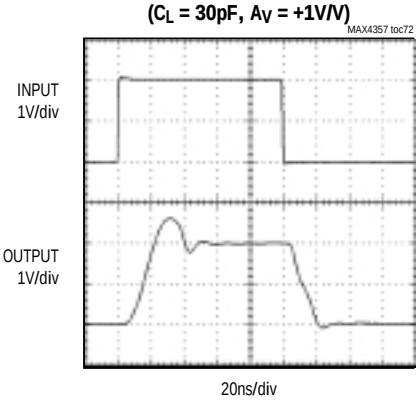
DIFFERENTIAL GAIN AND PHASE (R_L = 150Ω)



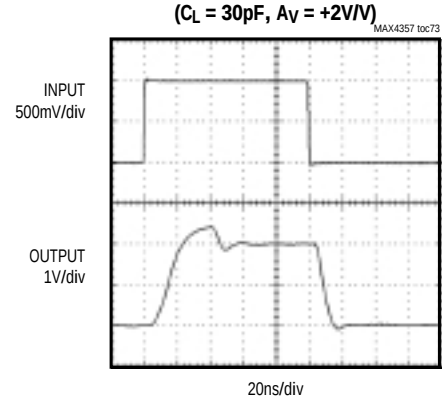
DIFFERENTIAL GAIN AND PHASE (R_L = 1kΩ)



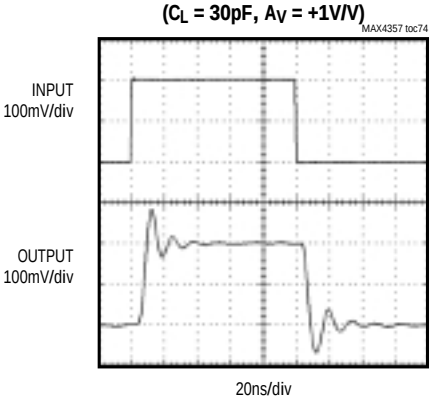
LARGE-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +1V/V)



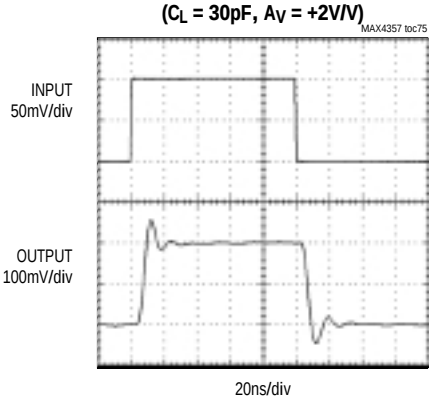
LARGE-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +2V/V)



MEDIUM-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +1V/V)



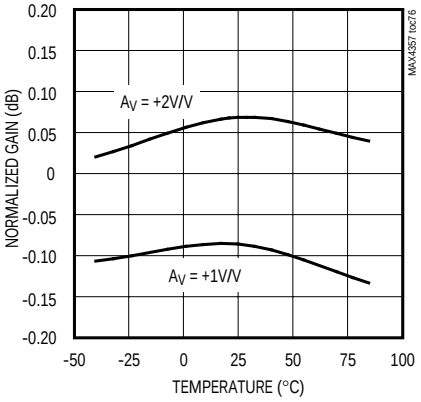
MEDIUM-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF, A_V = +2V/V)



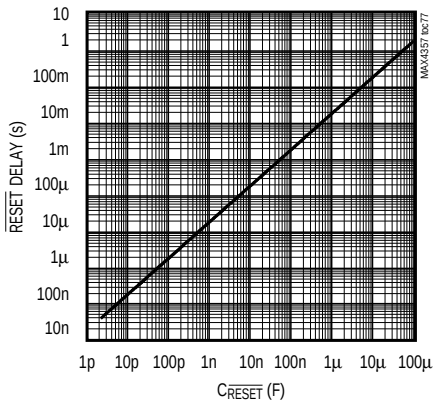
Typical Operating Characteristics—Dual Supplies ±3V (continued)

(V_{CC} = +3V and V_{EE} = -3V, V_{DD} = +3V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

GAIN vs. TEMPERATURE



$\overline{\text{RESET}}$ DELAY vs. $\overline{\text{RESET}}$ CAPACITANCE

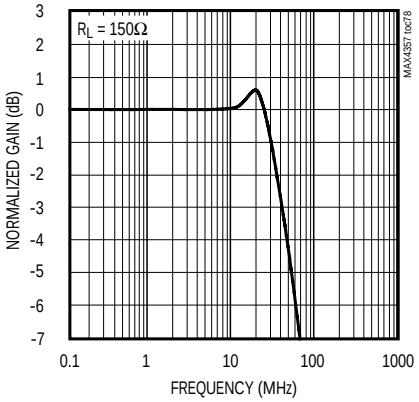


32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

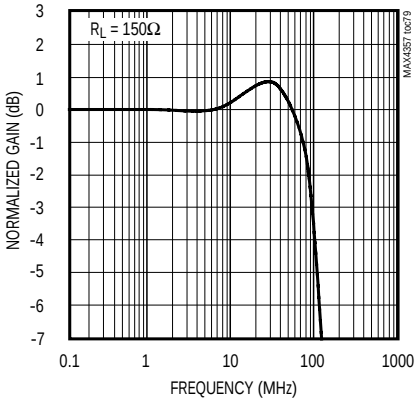
Typical Operating Characteristics—Single Supply +5V

(V_{CC} = +5V and V_{EE} = 0, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

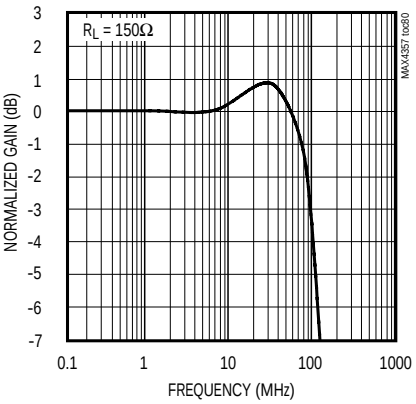
LARGE-SIGNAL FREQUENCY RESPONSE



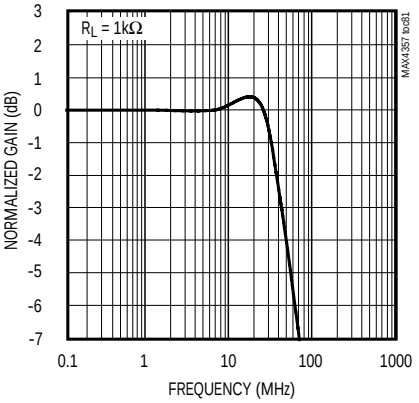
MEDIUM-SIGNAL FREQUENCY RESPONSE



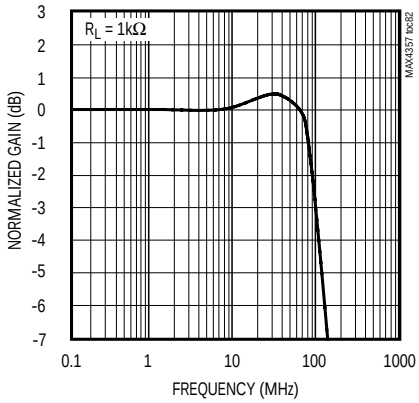
SMALL-SIGNAL FREQUENCY RESPONSE



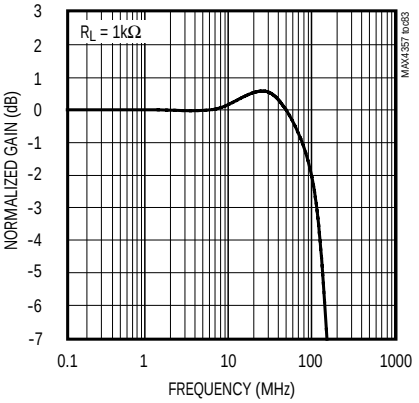
LARGE-SIGNAL FREQUENCY RESPONSE



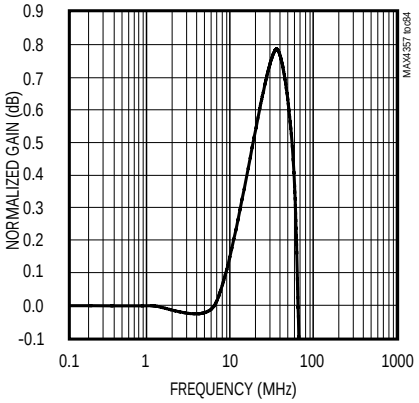
MEDIUM-SIGNAL FREQUENCY RESPONSE



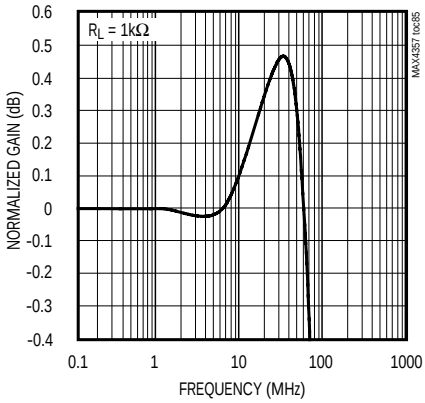
SMALL-SIGNAL FREQUENCY RESPONSE



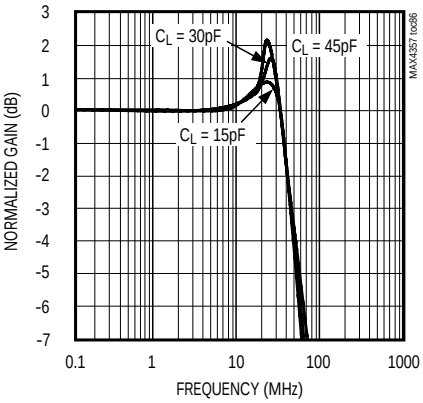
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



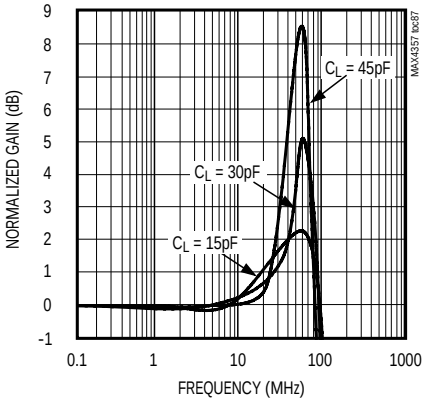
LARGE-SIGNAL FREQUENCY RESPONSE (A_V = +1V/V)



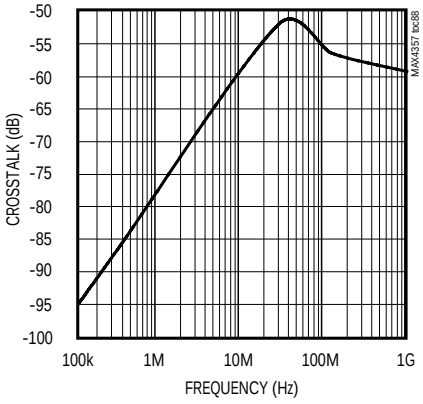
Typical Operating Characteristics—Single Supply +5V (continued)

(V_{CC} = +5V and V_{EE} = 0, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

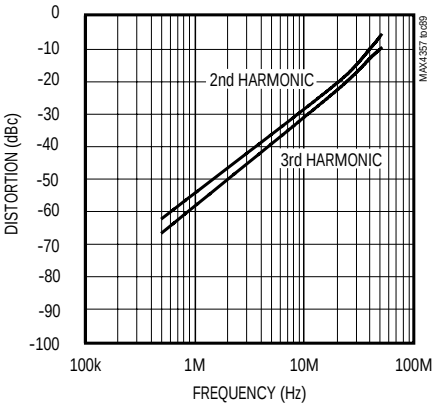
MEDIUM-SIGNAL FREQUENCY RESPONSE (A_V = +1V/V)



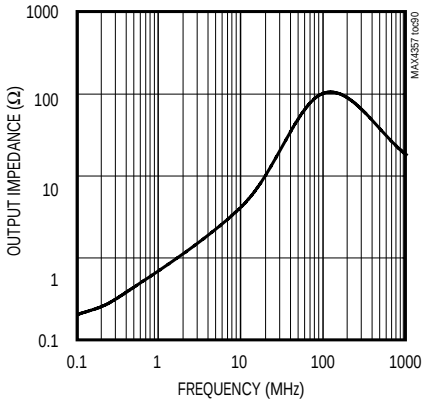
CROSSTALK vs. FREQUENCY



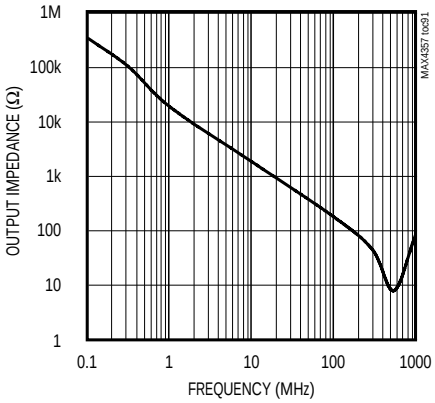
DISTORTION vs. FREQUENCY



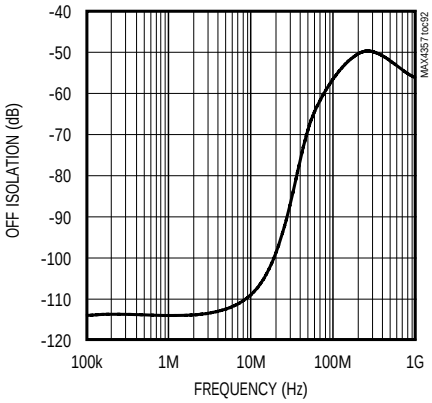
ENABLED OUTPUT IMPEDANCE vs. FREQUENCY



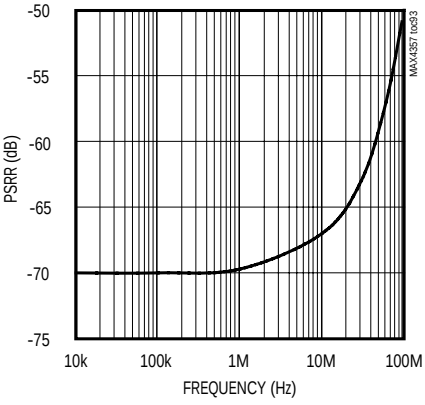
DISABLED OUTPUT IMPEDANCE vs. FREQUENCY



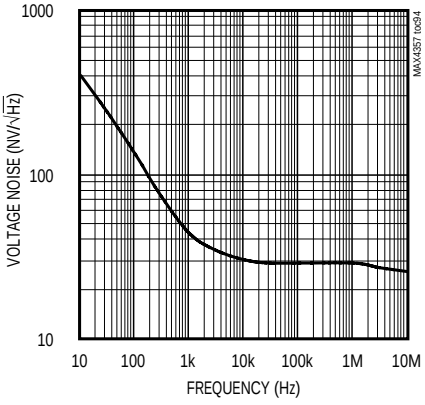
OFF-ISOLATION vs. FREQUENCY



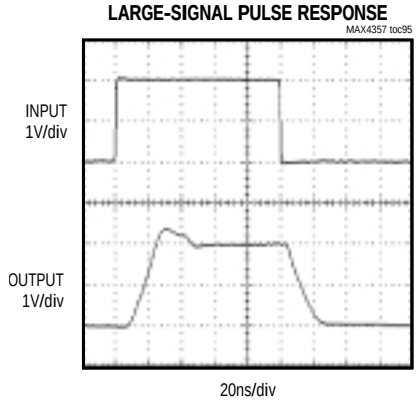
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



INPUT VOLTAGE NOISE vs. FREQUENCY



LARGE-SIGNAL PULSE RESPONSE

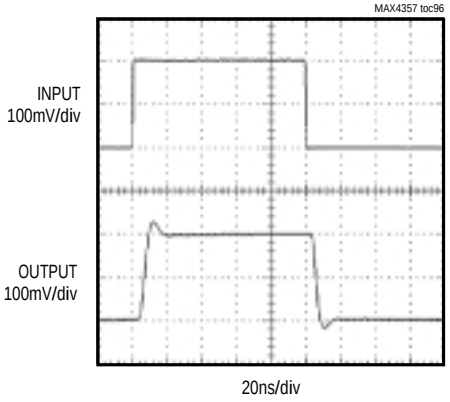


32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

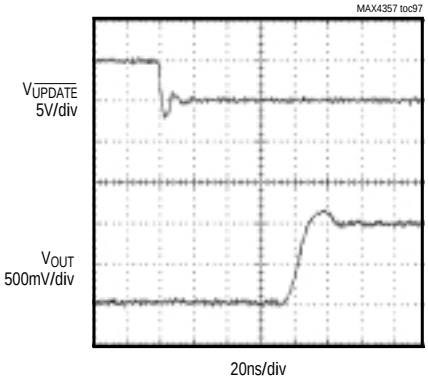
Typical Operating Characteristics—Single Supply +5V (continued)

(V_{CC} = +5V and V_{EE} = 0, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

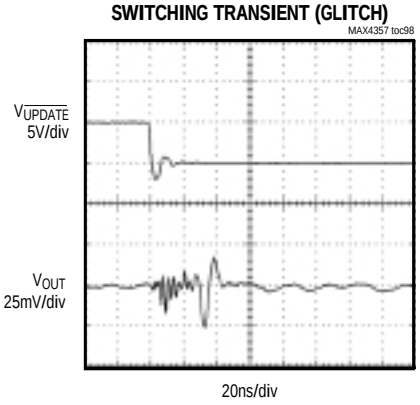
MEDIUM-SIGNAL PULSE RESPONSE



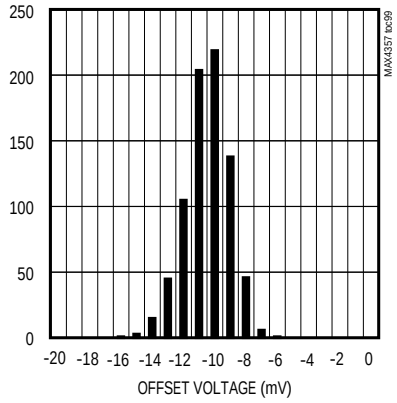
SWITCHING TIME



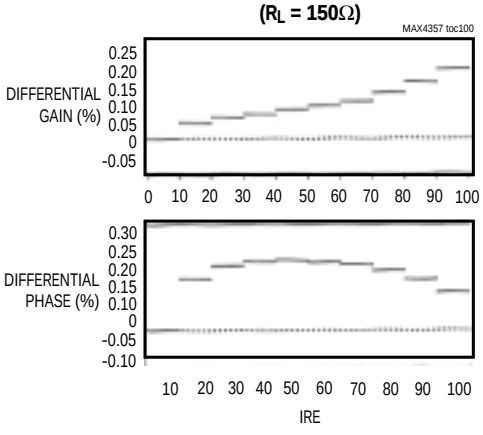
SWITCHING TRANSIENT (GLITCH)



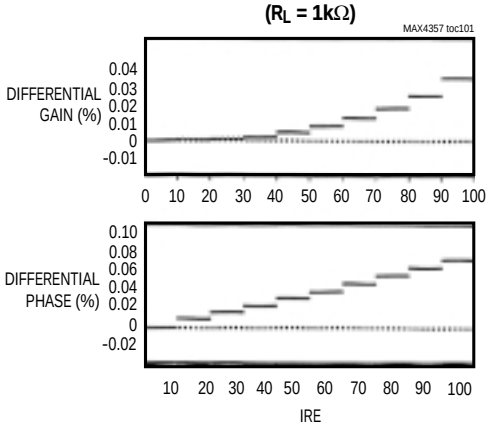
OFFSET VOLTAGE HISTOGRAM



DIFFERENTIAL GAIN AND PHASE (R_L = 150Ω)



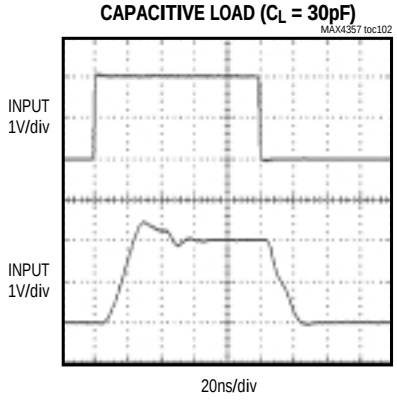
DIFFERENTIAL GAIN AND PHASE (R_L = 1kΩ)



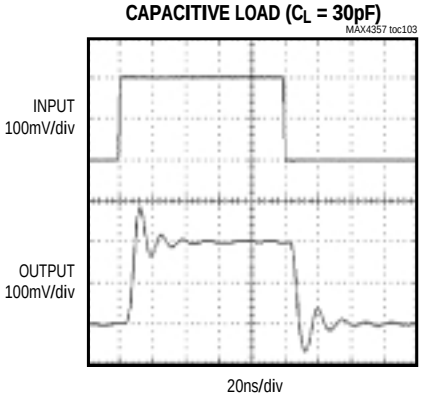
Typical Operating Characteristics—Single Supply +5V (continued)

(V_{CC} = +5V and V_{EE} = 0, V_{DD} = +5V, AGND = DGND = 0, $V_{IN\_}$ = 0, R_L = 150Ω to AGND, A_V = +1V/V, and T_A = +25°C, unless otherwise noted.)

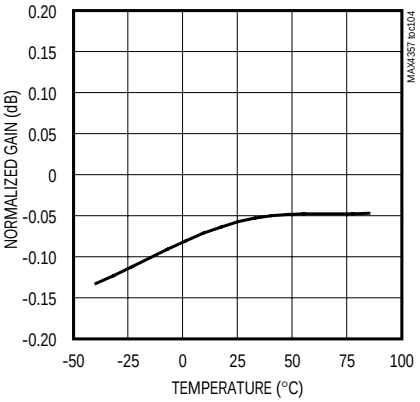
LARGE-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF)



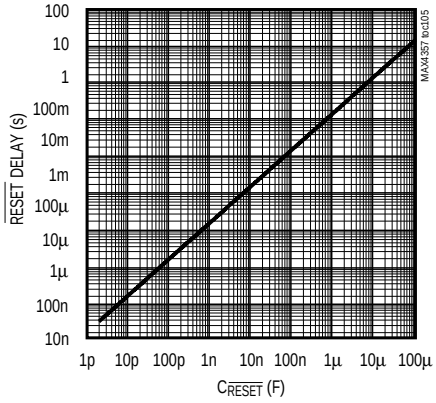
MEDIUM-SIGNAL PULSE RESPONSE WITH CAPACITIVE LOAD (C_L = 30pF)



GAIN vs. TEMPERATURE



$\overline{\text{RESET}}$ DELAY vs. $\overline{\text{RESET}}$ CAPACITANCE



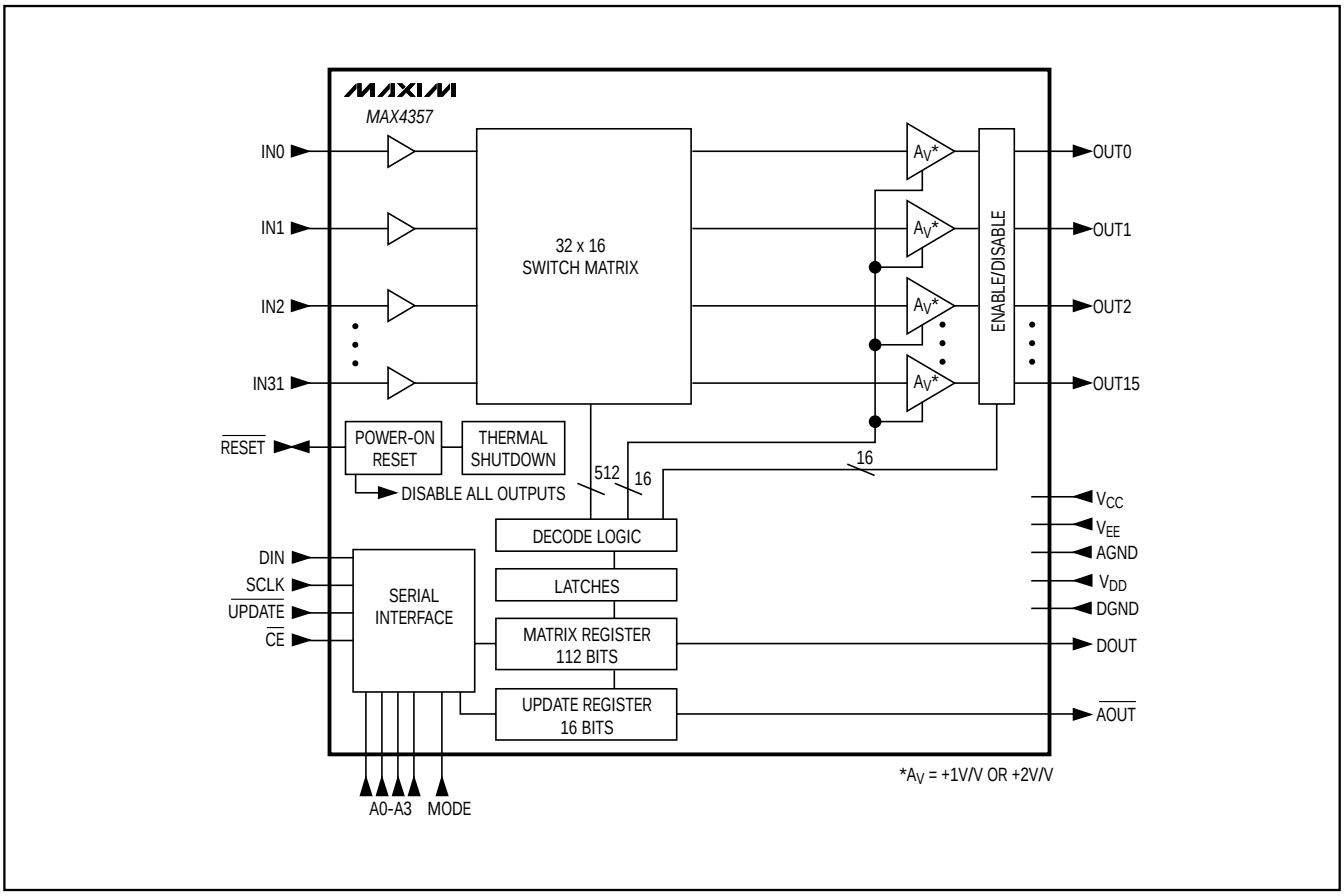
32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

Pin Description

PIN	NAME	FUNCTION
1, 69, 73, 77, 81, 85, 89, 93, 97	V_{EE}	Negative Analog Supply. Bypass each pin with a 0.1µF capacitor to AGND. Connect a single 10µF capacitor from one V_{EE} pin to AGND.
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 65, 66, 100, 102, 103, 104, 106, 108, 110, 112, 114, 116, 118, 120, 122, 124, 126, 128	AGND	Analog Ground
3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 37, 39, 41, 43, 105, 107, 109, 111, 113, 115, 117, 119, 121, 123, 125, 127,	IN0–IN31	Buffered Analog Inputs
35, 67, 71, 75, 79, 83, 87, 91, 95, 99	V_{CC}	Positive Analog Supply. Bypass each pin with a 0.1µF capacitor to AGND. Connect a single 10µF capacitor from one V_{CC} pin to AGND.
45	DGND	Digital Ground
46	$\overline{AOUT}$	Address Recognition Output. $\overline{AOUT}$ drives low after successful chip address recognition.
47–50	A3–A0	Address Programming Inputs. Connect to DGND or V_{DD} to select the address for Individual Output Address Mode (Table 3).
51	DOUT	Serial Data Output. In Complete Matrix Mode, data is clocked through the 112-bit Matrix Control Shift register. In Individual Output Address Mode, data at DIN passes directly to DOUT.
52	SCLK	Serial Clock Input
53	$\overline{CE}$	Clock Enable Input. Drive low to enable the serial data interface.
54	MODE	Serial Interface Mode Select Input. Drive high for Complete Matrix Mode (Mode 1), or drive low for Individual Output Address Mode (Mode 0).
55	$\overline{RESET}$	Asynchronous Reset Input/Output. Drive $\overline{RESET}$ low to initiate hardware reset. All matrix settings are set to power-up defaults and all analog outputs are disabled. Additional power-on reset delay may be set by connecting a small capacitor from $\overline{RESET}$ to DGND.
56	$\overline{UPDATE}$	Update Input. Drive $\overline{UPDATE}$ low to transfer data from mode registers to the matrix switch.
57	DIN	Serial Data Input. Data is clocked in on the falling edge of SCLK.
58–63, 101	N.C.	No Connection. Not internally connected. Connect to AGND.
64	V_{DD}	Digital Logic Supply. Bypass V_{DD} with a 0.1µF capacitor DGND.
68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88, 90, 92, 94, 96, 98	OUT0–OUT15	Buffered Analog Outputs. Gain is individually programmable for A_V = +1V/V or A_V = +2V/V through the serial interface. Outputs may be individually disabled (high impedance). On power-up, or assertion of $\overline{RESET}$, all outputs are disabled.

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

Functional Diagram



Detailed Description

The MAX4357 is a highly integrated 32 x 16 nonblocking video crosspoint switch matrix. All inputs and outputs are buffered, with all outputs able to drive standard 75Ω reverse-terminated video loads.

A three-wire interface programs the switch matrix and initializes with a single update signal. The unique serial interface operates in one of two modes, Complete Matrix Mode (Mode 1) or Individual Output Address Mode (Mode 0).

The signal path of the MAX4357 is from the buffered inputs (IN0–IN31), through the switching matrix, buffered by the output amplifiers, and presented at the outputs (OUT0–OUT15) (*Functional Diagram*). The other functional blocks are the serial interface and control logic. Each of the functional blocks is described in detail in the sections following.

Analog Outputs

The MAX4357 outputs are high-speed amplifiers capable of driving 150Ω (75Ω back-terminated) loads. The gain, A_V = +1V/V or +2V/V, is selectable through programming bit 5 of the serial control word. Amplifier compensation is automatically optimized to maximize the bandwidth for each gain selection. Each output can be individually enabled and disabled through bit 6 of the serial control word. When disabled, the output is high impedance presenting typically 4kΩ load, and 3pF output capacitance, allowing multiple outputs to be connected together for building large arrays. On power-up (or asynchronous $\overline{RESET}$), all outputs are initialized in the disabled state to avoid output conflicts in large array configurations. The programming and operation of the MAX4357 is output referred. Outputs are configured individually to connect to any one of the 32 analog inputs, programmed to the desired gain (A_V = +1V/V or +2V/V), and enabled or disabled in a high-impedance state.

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

Table 1. Operation Truth Table

$\overline{CE}$	$\overline{UPDATE}$	SCLK	DIN	DOUT	MODE	$\overline{AOUT}$	$\overline{RESET}$	OPERATION/COMMENTS
1	X	X	X	X	X	X	1	No change in logic.
0	1	↓	D_i	D_{i-112}	1	1	1	Data at DIN is clocked on negative edge of SCLK into 112-bit Complete Matrix Mode register. DOUT supplies original data in 112 SCLK pulses later.
0	0	X	X	X	1	1	1	Data in serial 112-bit Complete Matrix Mode register is transferred into parallel latches, which control the switching matrix.
0	1	↓	D_i	D_i	0	1	1	Data at DIN is routed to Individual Output Address Mode shift register. DIN is also connected directly to DOUT so that all devices on the serial bus may be addressed in parallel.
0	0	X	D_i	D_i	0	0	1	4-bit chip address A3–A0 is compared to D14–D11. If equal, remaining 11 bits in Individual Output Address Mode register are decoded, allowing reprogramming for a single output. $\overline{AOUT}$ signals successful individual matrix update.
X	X	X	X	X	X	X	0	Asynchronous reset. All outputs are disabled. Other logic remains unchanged.

Note: *X = Don't care*

Analog Inputs

The MAX4357 offers 32 analog input channels. Each input is buffered before the crosspoint matrix switch, allowing one input to cross-connect up to 16 outputs. The input buffers are voltage-feedback amplifiers with high-input impedance and low-input bias current. This allows the use of very simple input clamp circuits.

Switch Matrix

The MAX4357 has 512 individual T-switches making a 32 × 16 switch matrix. The switching matrix is 100% nonblocking, which means that any input may be routed to any output. The switch matrix programming is output-referred. Each output may be connected to any one of the 32 analog inputs. Any one input can be routed to all 16 outputs with no signal degradation.

Digital Interface

The digital interface consists of the following pins: DIN, DOUT, SCLK, $\overline{AOUT}$, $\overline{UPDATE}$, $\overline{CE}$, A3–A0, MODE, and $\overline{RESET}$. DIN is the serial-data input; DOUT is the serial-data output.

SCLK is the serial-data clock that clocks data into the data input registers (Figure 3). Data at DIN is loaded in at each falling edge of SCLK. DOUT is the data shifted out of the 112-bit Complete Matrix Mode register (Mode = 1). DIN passes directly to DOUT when in Individual Output Address Mode (Mode = 0).

The falling edge of $\overline{UPDATE}$ latches the data and programs the matrix. When using Individual Output Address Mode, the address recognition output $\overline{AOUT}$ drives low when control-word bits D14 to D11 match the address programming inputs (A3–A0) and $\overline{UPDATE}$ is low (Table 1). Table 1 is the operation truth table.

Programming the Matrix

The MAX4357 offers two programming modes: Individual Output Address Mode and Complete Matrix Mode. These two distinct programming modes are selected by toggling a single MODE pin high or low. Both modes operate with the same physical board layout. This flexibility allows initial programming of the IC by daisy-chaining and sending one long data word

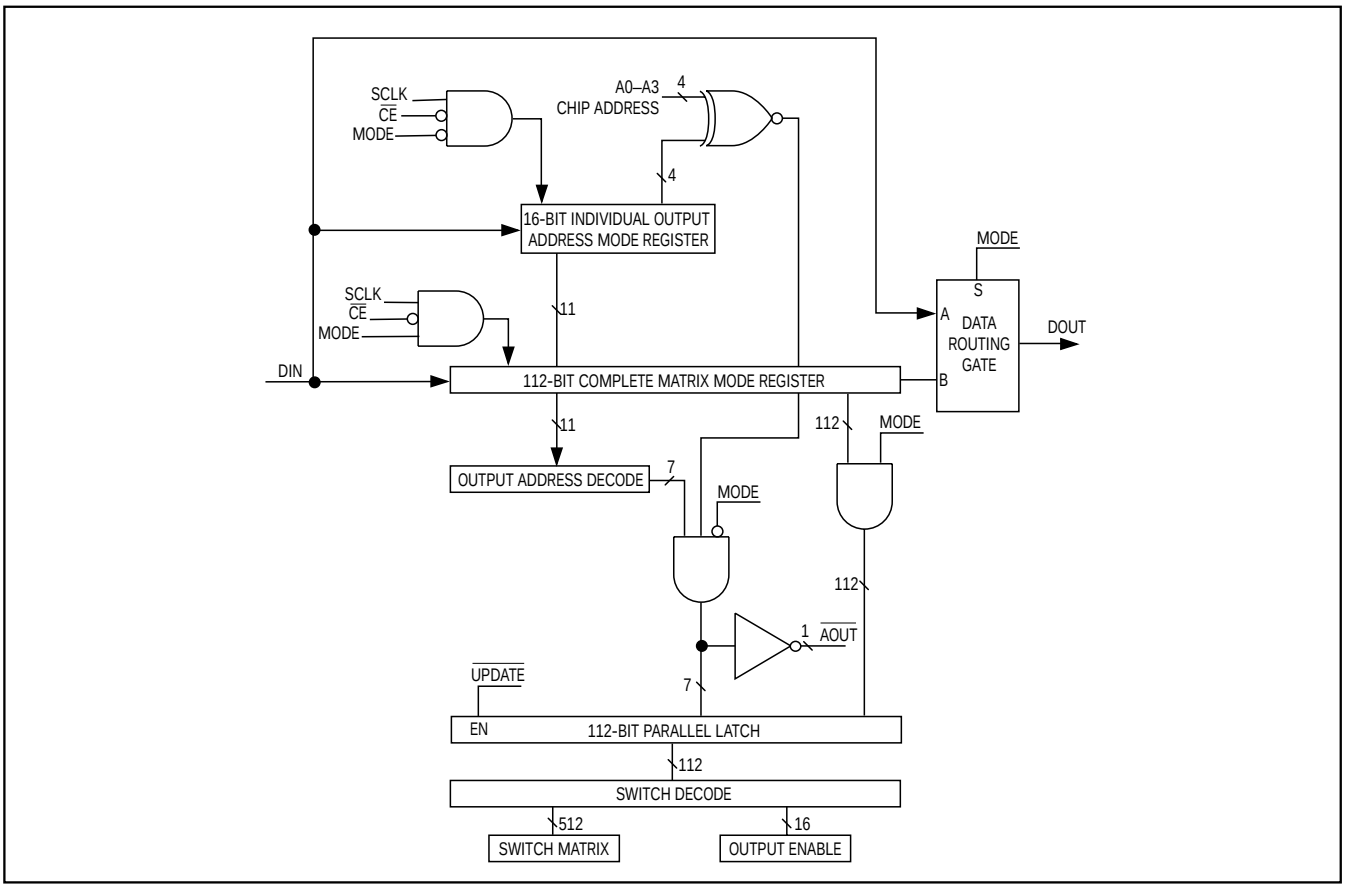


Figure 2. Serial Interface Block Diagram

while still being able to immediately address and update individual outputs in the matrix.

Individual Output Address Mode (MODE = 0)

Drive MODE to logic low to select Mode 0. Individual outputs are programmed through the serial interface with a single 16-bit control word. The control word consists of a don't care MSB, the chip address bits, output address bits, an output enable/disable bit, an output gain-set bit, and input address bits (Table 2 through Table 6, and Figure 2).

In Mode 0, data at DIN passes directly to DOUT through the data routing gate (Figure 3). In this configuration, the 16-bit control word is simultaneously sent to all chips in an array of up to 16 addresses.

Complete Matrix Mode (MODE = 1)

Drive MODE to logic high to select Mode 1. A single 112-bit control word, consisting of sixteen 7-bit control words, programs all outputs. The 112-bit control word's first 7-bit control word (MSBs) programs output 15, and the last 7-bit control word (LSBs) programs output 0 (Table 7 and Figures 4 and 5). Data clocked into the 112-bit Complete Matrix Mode register is latched on the falling edge of $\overline{UPDATE}$, and the outputs are immediately updated.

Initialization String

Complete Matrix Mode (Mode = 1) is convenient for programming the matrix at power-up. In a large matrix consisting of many MAX4357s, all the devices can be programmed by sending a single bit stream equal to n x 112 bits where n is the number of MAX4357 devices on the bus. The first 112-bit data word programs the last MAX4357 in line (see *Matrix Programming* section).

$\overline{RESET}$

The MAX4357 features an asynchronous bidirectional $\overline{RESET}$ with an internal 20kΩ pullup resistor to V_{DD}. When $\overline{RESET}$ is pulled low either by internal circuitry, or

Table 2. 16-Bit Serial Control Word Bit Assignments (Mode 0: Individual Output Address Mode)

BIT	NAME	FUNCTION
15 (MSB)	X	Don't care
14	IC Address A3	MSB of selected chip address
13	IC Address A2	MSB of selected chip address
12	IC Address A1	MSB of selected chip address
11	IC Address A0	LSB of selected chip address
10	Output Address B3	MSB of output buffer address
9	Output Address B2	MSB of output buffer address
8	Output Address B1	MSB of output buffer address
7	Output Address B0	LSB of output buffer address
6	Output Enable	Enable bit for output, 0 = disable, 1 = enable
5	Gain Set	Gain select for output buffer, 0 = gain of +1V/V, 1 = gain of +2V/V
4	Input Address 4	MSB of input channel select address
3	Input Address 3	MSB of input channel select address
2	Input Address 2	MSB of input channel select address
1	Input Address 1	MSB of input channel select address
0 (LSB)	Input Address 0	LSB of input channel select address

driven externally, the analog output buffers are latched into a high-impedance state. After $\overline{RESET}$ is released, the output buffers remain disabled. The outputs may be enabled by sending a new 112-bit data word or a 16-bit individual output address word. A reset is initiated from any of three sources. $\overline{RESET}$ can be driven low by external circuitry to initiate a reset, or $\overline{RESET}$ can be pulled low by internal circuitry during power-up (power-on reset) or thermal shutdown.

Since driving $\overline{RESET}$ low only clears the output-buffer-enable bit in the matrix control latches, $\overline{RESET}$ can be used to disable all outputs simultaneously. If no new data has been loaded into the 112-bit Complete Matrix Mode register, a single $\overline{UPDATE}$ restores the previous matrix control settings.

Power-On Reset

The power-on reset ensures all output buffers are in a disabled state when power is initially applied. A V_{DD} voltage comparator generates the power-on reset. When the voltage at V_{DD} is less than 2.5V, the power-on reset comparator pulls $\overline{RESET}$ low through internal circuitry. As the digital-supply voltage ramps up crossing 2.5V, the MAX4357 holds $\overline{RESET}$ low for 40ns (typ). Connecting a small capacitor from $\overline{RESET}$ to DGND extends the power-on reset delay (see the $\overline{RESET}$ Delay vs. $\overline{RESET}$ Capacitance graph in the *Typical Operating Characteristics)*.

Thermal Shutdown

The MAX4357 features thermal shutdown protection with temperature hysteresis. When the die temperature exceeds +150°C, the MAX4357 pulls $\overline{RESET}$ low, disabling the output buffer. When the die cools by 20°C, the $\overline{RESET}$ pulldown is deasserted, and output buffers remain disabled until the device is programmed again.

Applications Information

Building Large Video-Switching Systems

The MAX4357 can be easily used to create larger switching matrices. The number of ICs required to implement the matrix is a function of the number of input channels, the number of outputs required, and whether the array needs to be nonblocking or not. The most straightforward technique for implementing nonblocking matrices is to arrange the building blocks in a grid. The inputs connect to each vertical bank of devices in parallel with the other banks. The outputs of each building block in a vertical column connect together in a wired-OR configuration. Figure 6 shows a 128-input, 32-output, nonblocking array using eight MAX4357 crosspoint devices.

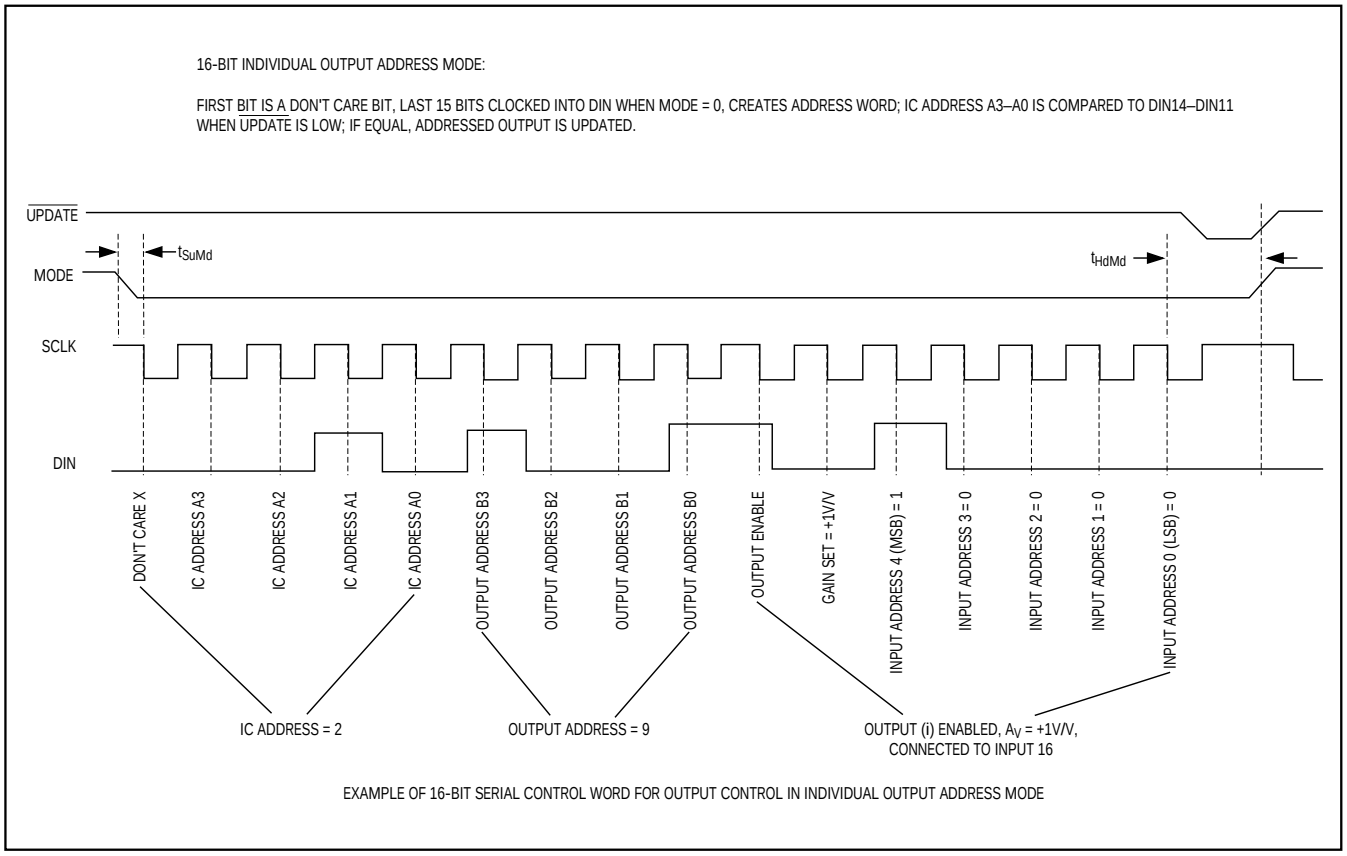


Figure 3. Mode 0, Individual Output Address Mode Timing and Programming Example

The wire-OR connection of the outputs shown in the diagram is possible because the outputs of the IC devices can be placed in a disabled, or high-impedance-output state. This disable state of the output buffers is designed for a maximum impedance vs. frequency while maintaining a low output capacitance. These characteristics minimize the adverse loading effects from the disabled outputs. Larger arrays are constructed by extending this connection technique to more devices.

Driving a Capacitive Load

Figure 6 shows an implementation requiring many outputs to be wired together. This creates a situation where each output buffer sees not only the normal load impedance, but also the disabled impedance of all the other outputs. This impedance has a resistive and a capacitive component. The resistive components reduce the total effective load for the driving output. Total capacitance is the sum of the capacitance of all the disabled outputs and is a function of the size of the matrix. Also, as the size of the matrix increases, the length of the PC board traces increases, adding more capacitance. The output buffers have been designed to drive more than 30pF of capacitance while still maintaining a good AC response. Depending on the size of the array, the capacitance seen by the output can exceed this amount. There are several ways to improve the situation. The first is to use more building-block crosspoint devices to reduce the number of outputs that need to be wired together (Figure 7).

In Figure 7, the additional devices are placed in a second bank to multiplex the signals. This reduces the number of wired-OR connections. Another solution is to put a small resistor in series with the output before the capacitive load to limit excessive ringing and oscillations. Figure 8 shows the Optimal Isolation Resistor vs. Capacitive Load graph. A lowpass filter is created from the series resistor and parasitic capacitance to ground. A single R-C does not affect the performance at video

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

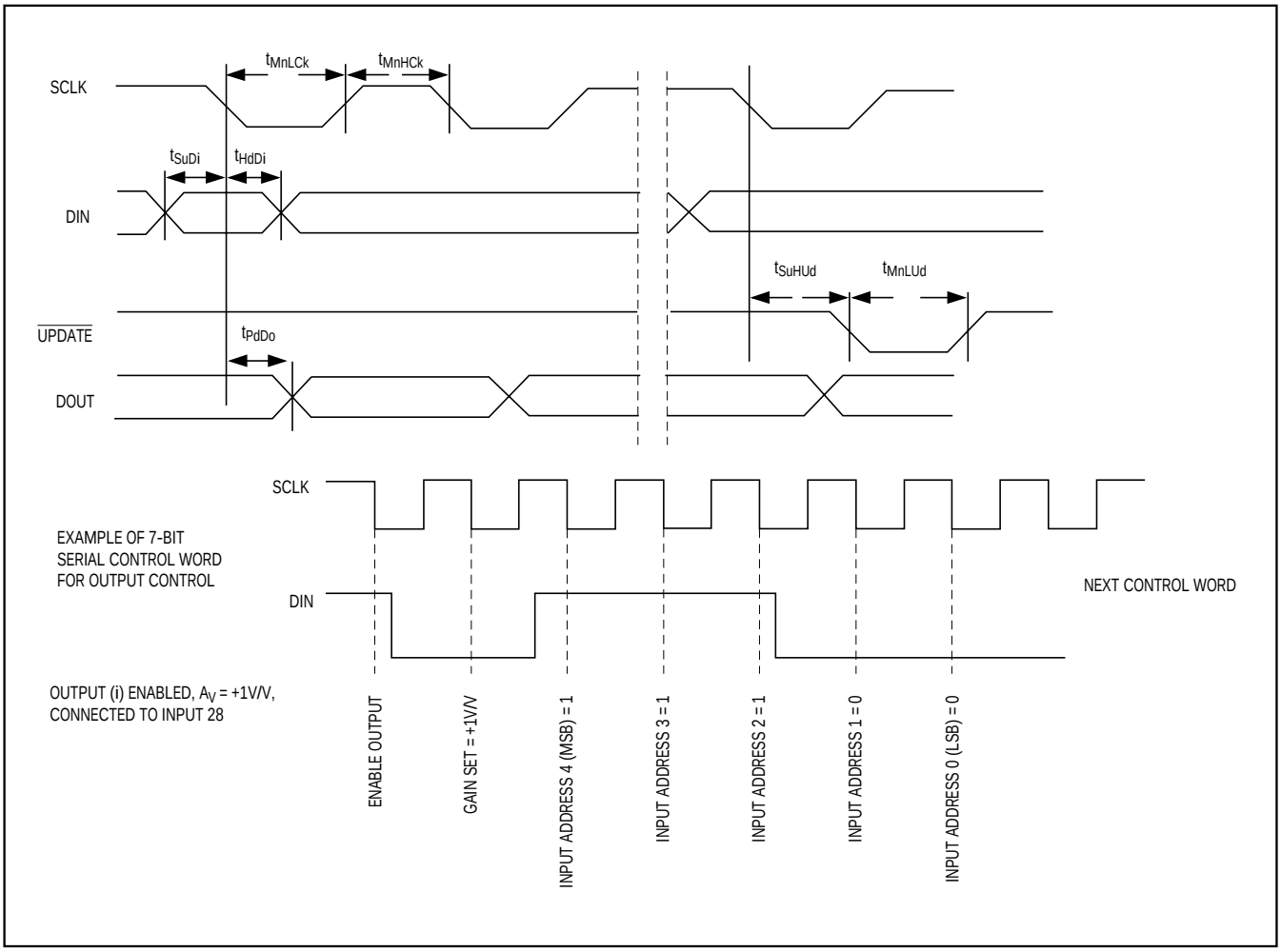


Figure 4. 7-Bit Control Word and Programming Example (Mode 1: Complete Matrix Mode)

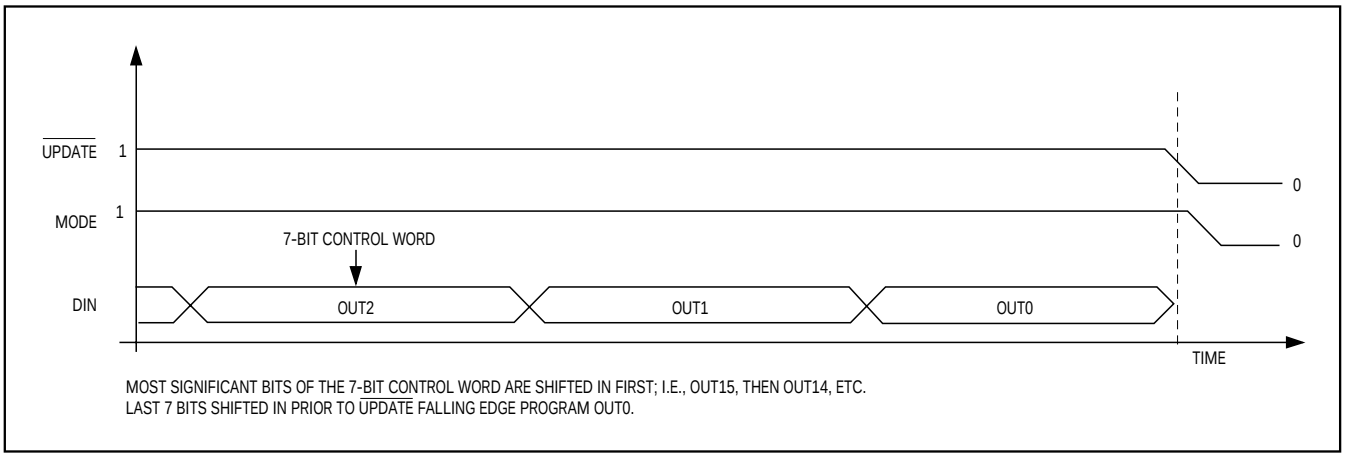


Figure 5. Mode 1: Complete Matrix Mode Programming

Table 3. Chip Address Programming for 16-Bit Control Word (Mode 0: Individual Output Address Mode)

IC ADDRESS BIT				ADDRESS	
A3 (MSB)	A2	A1	A0 (LSB)	CHIP ADDRESS (HEX)	CHIP ADDRESS (DECIMAL)
0	0	0	0	0h	0
0	0	0	1	1h	1
0	0	1	0	2h	2
0	0	1	1	3h	3
0	1	0	0	4h	4
0	1	0	1	5h	5
0	1	1	0	6h	6
0	1	1	1	7h	7
1	0	0	0	8h	8
1	0	0	1	9h	9
1	0	1	0	Ah	10
1	0	1	1	Bh	11
1	1	0	0	Ch	12
1	1	0	1	Dh	13
1	1	1	0	Eh	14
1	1	1	1	Fh	15

Table 4. Chip Address A3–A0 Pin Programming

PIN				ADDRESS	
A3	A2	A1	A0	CHIP ADDRESS (HEX)	CHIP ADDRESS (DECIMAL)
DGND	DGND	DGND	DGND	0h	0
DGND	DGND	DGND	V_{DD}	1h	1
DGND	DGND	V_{DD}	DGND	2h	2
DGND	DGND	V_{DD}	V_{DD}	3h	3
DGND	V_{DD}	DGND	DGND	4h	4
DGND	V_{DD}	DGND	V_{DD}	5h	5
DGND	V_{DD}	V_{DD}	DGND	6h	6
DGND	V_{DD}	V_{DD}	V_{DD}	7h	7
V_{DD}	DGND	DGND	DGND	8h	8
V_{DD}	DGND	DGND	V_{DD}	9h	9
V_{DD}	DGND	V_{DD}	DGND	Ah	10
V_{DD}	DGND	V_{DD}	V_{DD}	Bh	11
V_{DD}	V_{DD}	DGND	DGND	Ch	12
V_{DD}	V_{DD}	DGND	V_{DD}	Dh	13
V_{DD}	V_{DD}	V_{DD}	DGND	Eh	14
V_{DD}	V_{DD}	V_{DD}	V_{DD}	Fh	15

Table 5. Output Selection Programming

OUTPUT ADDRESS BIT				SELECTED OUTPUT
B3 (MSB)	B2	B1	B0 (LSB)	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

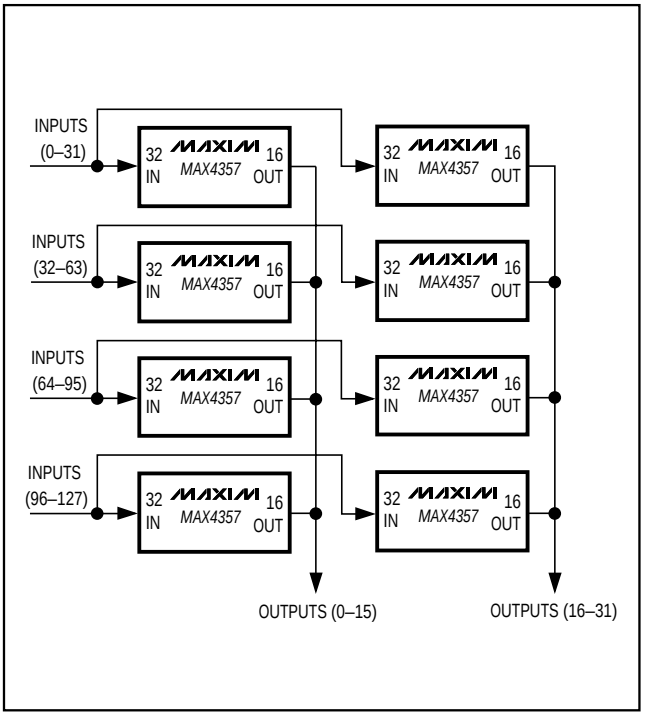


Figure 6. 128 x 32 Nonblocking Matrix Using 32 x 16 Crosspoint Devices

frequencies, but in a very large system, there may be many R-Cs cascaded in series. The cumulative effect is a slight rolling off of the high frequencies, causing a "softening" of the picture. There are two solutions to achieve higher performance. One way is to design the PC board traces associated with the outputs such that they exhibit some inductance. By routing the traces in a repeating "S" configuration, the traces that are nearest each other will exhibit a mutual inductance increasing the total inductance. This series inductance causes the amplitude response to increase or peak at higher frequencies, offsetting the rolloff from the parasitic capacitance. Another solution is to add a small-value inductor to the output.

Crosstalk and Board Routing Issues

Improper signal routing causes performance problems. The MAX4357 has a typical crosstalk rejection of -62dB at 6MHz. A bad PC board layout degrades the crosstalk rejection by 20dB or more. To achieve the best crosstalk performance:

1) Place ground isolation between long critical signal PC board trace runs. These traces act as a shield to potential interfering signals. Crosstalk can be degraded from parallel traces, as well as directly above and below on adjoining PC board layers.

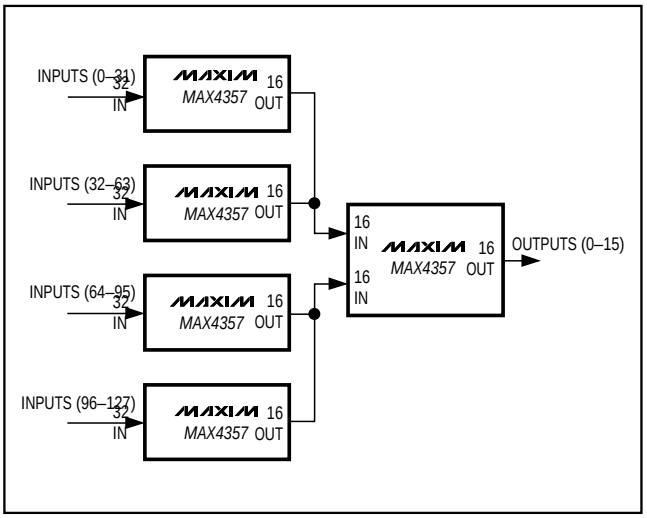


Figure 7. 128 x 16 Nonblocking Matrix with Reduced Capacitive Loading

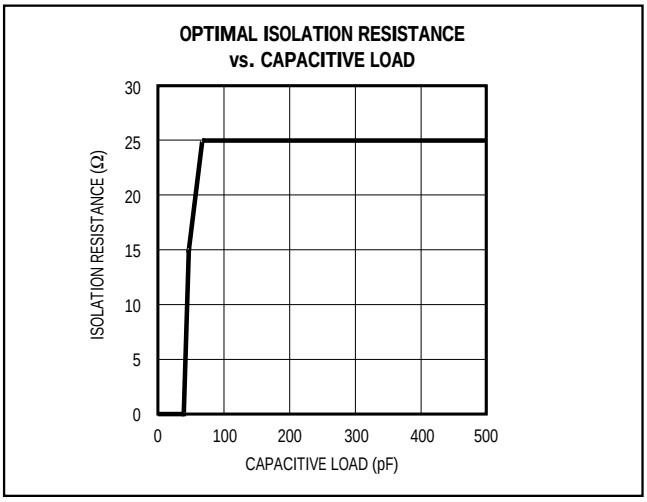


Figure 8. Optimal Isolation Resistor vs. Capacitive Load

2) Maintain controlled-impedance traces. Design as many of the PC board traces as possible to be 75Ω transmission lines. This lowers the impedance of the traces, reducing a potential source of crosstalk. More power dissipates due to the output buffer driving a lower impedance.

3) Minimize ground current interaction by using a good ground plane strategy.

In addition to crosstalk, another key issue of concern is isolation. Isolation is the rejection of undesirable feedthrough from input to output with the output disabled. The MAX4357 achieves a -110dB isolation at 6MHz by selecting the pinout configuration such that the inputs and outputs are on opposite sides of the package. Coupling through the power supply is a function of the quality and location of the supply bypassing. Use appropriate low-impedance components and locate them as close as possible to the IC. Avoid routing the inputs near the outputs.

Table 6. Input Selection Programming

INPUT ADDRESS BIT					SELECTED INPUT
B4 (MSB)	B3	B2	B1	B0 (LSB)	
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	0	0	1	25
1	1	0	1	0	26
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Table 7. 7-Bit Serial Control Word Bit Assignments (Mode 1: Complete Matrix Mode Programming)

BIT	NAME	FUNCTION
6 (MSB)	Output Enable	Enable bit for output, 0 = disable, 1 = enable.
5	Gain Set	Gain select for output buffer, 0 = gain of +1V/V, 1 = gain of +2V/V.
4	Input Address 4	MSB of input channel select address
3	Input Address 3	MSB of input channel select address
2	Input Address 2	MSB of input channel select address
1	Input Address 1	MSB of input channel select address
0 (LSB)	Input Address 0	LSB of input channel select address

Power-Supply Bypassing

The MAX4357 operates from a single +5V or dual ±3V to ±5V supply. For single-supply operation, connect all V_{EE} pins to ground and bypass all power-supply pins with a 0.1µF capacitor to ground. For dual-supply systems, bypass all supply pins to ground with 0.1µF capacitors.

Power in Large Systems

The MAX4357 has been designed to operate with split supplies down to ±3V or a single supply of +5V. Operating at the minimum supply voltages reduces the power dissipation by as much 40% to 50%. At ±5V, the MAX4357 consumes 220mW (0.43mW/point).

Driving a PC Board Interconnect or Cable (A_V = +1V/V or +2V/V)

The MAX4357 output buffers can be programmed to either A_V = +1V/V or +2V/V. The +1V/V configuration is typically used when driving short-length (less than 3cm), high-impedance “local” PC board traces. To drive a cable or a 75Ω transmission line trace, program the gain of the output buffer to +2V/V and place a 75Ω resistor in series with the output. The series termination resistor and the 75Ω load impedance act as a voltage-divider that divides the video signal in half. Set the gain to +2V/V to transmit a standard 1V video signal down a cable. The series 75Ω resistor is called the back-match, reverse termination, or series termination. This 75Ω resistor reduces reflections and provides isolation, increasing the output-capacitive-driving capability.

Matrix Programming

The MAX4357's unique digital interface simplifies programming multiple MAX4357 devices in an array. Multiple devices are connected with DOUT of the first device connecting to DIN of the second device, and so on (Figure 9). Two distinct programming modes, Individual Output Address Mode (MODE = 0) and Complete Matrix Mode (MODE = 1) are selected by toggling a single MODE control pin high or low. Both modes operate with the same physical board layout. This allows initial programming of the IC by daisy-chaining and sending one long data word while still being able to immediately address and update individual locations in the matrix.

Individual Output Address Mode (Mode = 0)

In Individual Output Address Mode, the devices are connected in a serial-bus configuration, with the data-routing gate (Figure 3) connecting DIN to DOUT, making each device a virtual node on the serial bus. A single 16-bit control word is sent to all devices simultaneously. Only the device with the corresponding chip address responds to the programming word and updates its output. In this mode the chip address is set through hardware pin strapping of A3–A0. The host communicates with the device by sending a 16-bit word consisting of 1 don’t-care bit, 4-chip address bits, and 11 bits of data to make the word exactly 2 bytes in length. The 11 data bits are broken down into 4 bits to select the output to be programmed; 1 bit to set the output enable, 1 bit to set gain, and 5 bits to the select the input to be connected to that output. In this method, the matrix is programmed one output at a time.

Complete Matrix Mode (Mode = 1)

In Complete Matrix Mode, the devices are connected in a daisy-chain fashion where n × 112 bits are sent to program the entire matrix, where n = the number of MAX4357 devices connected in series. The data word is structured such that the first bit is the LSB of the last device in the chain and the last data bit is the MSB of the first device in the chain. The total length of the data word is equal to the number of crosspoint devices to be

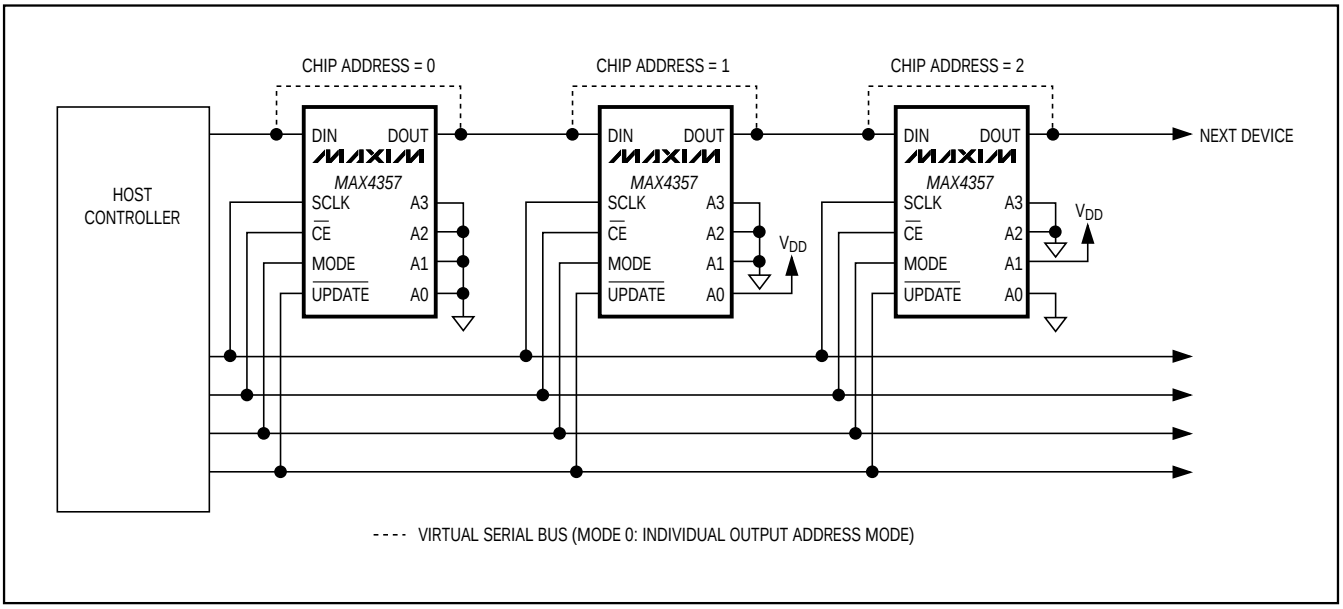


Figure 9. Matrix Mode Programming

programmed in series times 112 bits per crosspoint device. This programming method is most often used at startup to initially configure the switching matrix.

Operating at +5V Single-Supply with A_V = +1V/V or +2V/V

The MAX4357 guarantees operation with a single +5V supply and a gain of +1V/V for standard video-input signals (1Vp-p). To implement a complete video matrix switching system capable of gain = +2V/V while operating with a +5V single supply, combine the MAX4357 crosspoint switch with Maxim's low-cost, high-performance video amplifiers optimized for single +5V supply operation (Figure 10). The MAX4450 single and MAX4451 dual op amps are unity-gain-stable devices that combine high-speed performance with Rail-to-Rail® outputs. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications). The MAX4450 is available in the ultra-small 5-pin SC70 package, while the MAX4451 is available in a space-saving 8-pin SOT23 package. The MAX4383 is a quad op amp available in a 14-pin TSSOP package. The MAX4380/MAX4381/MAX4382/MAX4384 offer individual high-impedance output disable, making these amplifiers suitable for wired-OR connections.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

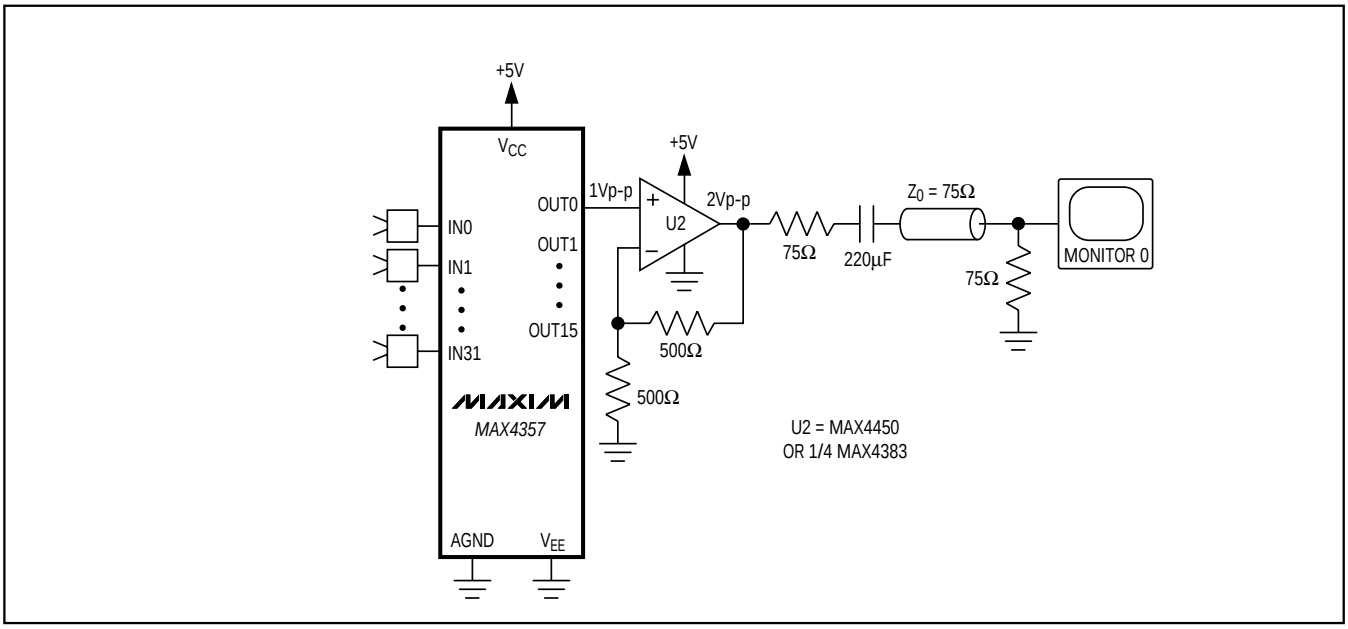


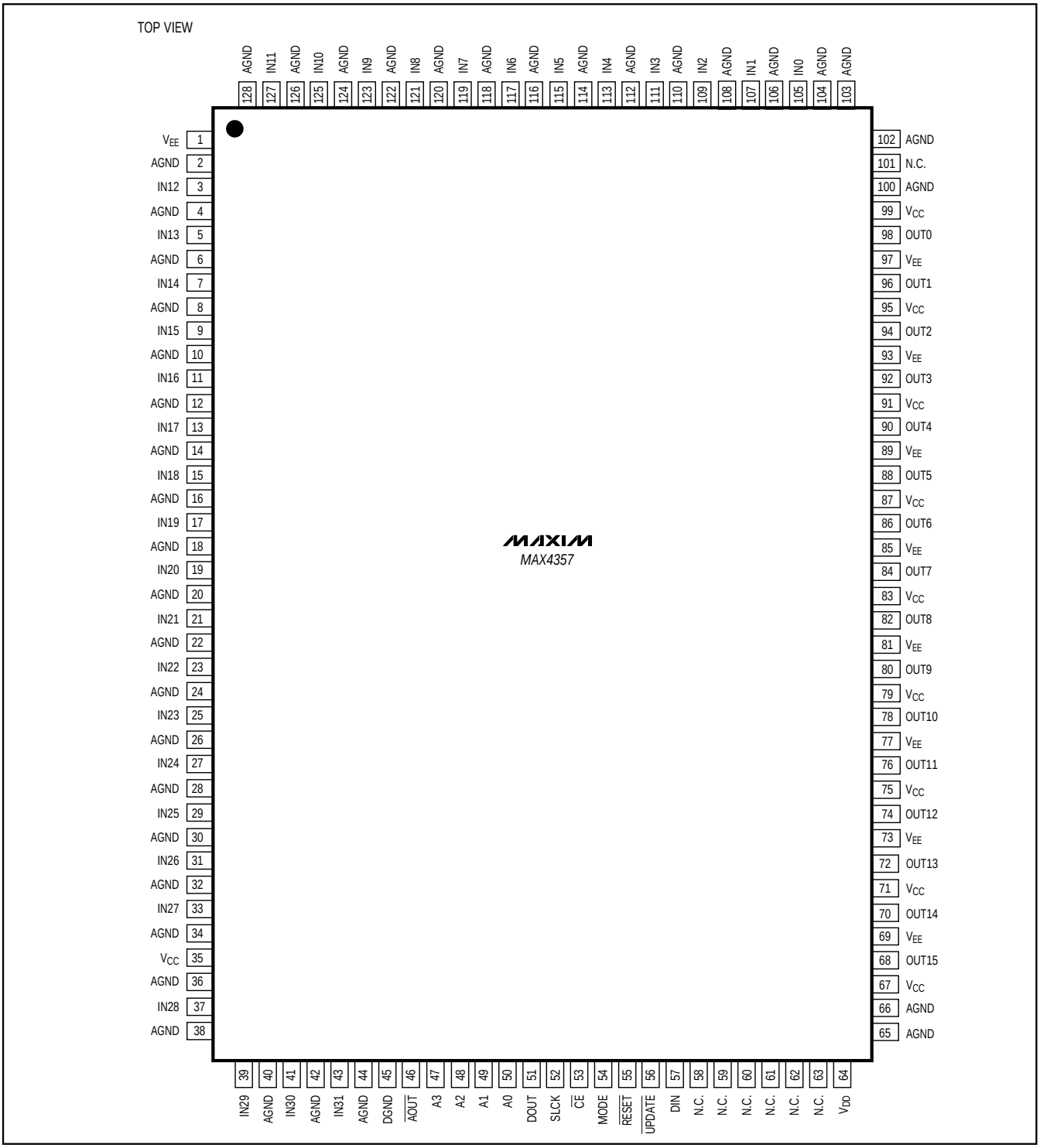
Figure 10. Typical Single +5V Supply Application

Chip Information

TRANSISTOR COUNT: 39,133

PROCESS: BiCMOS

Pin Configuration



32 x 16 Nonblocking Video Crosspoint Switch with I/O Buffers

Package Information

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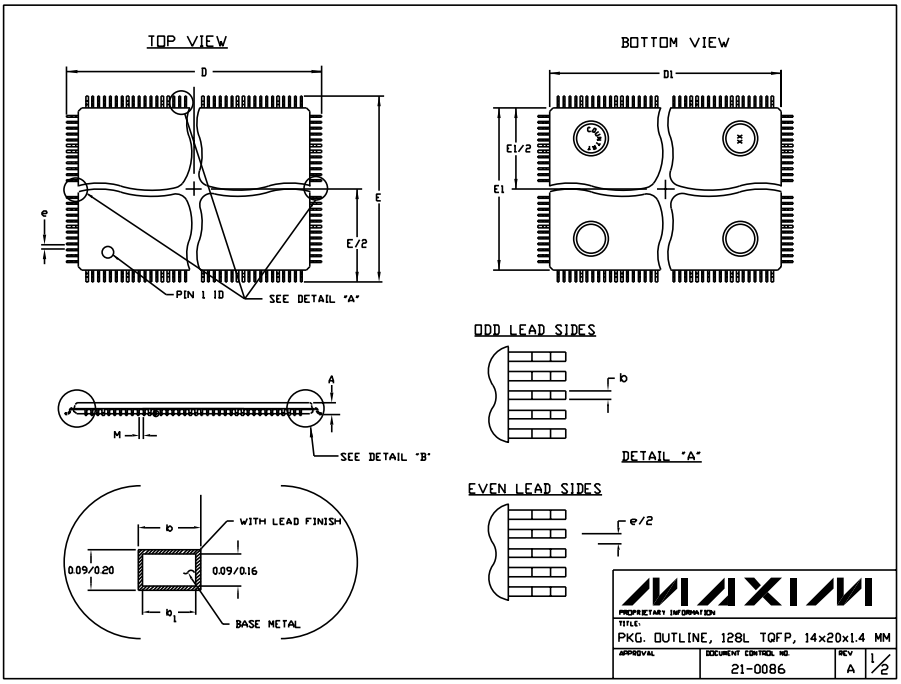
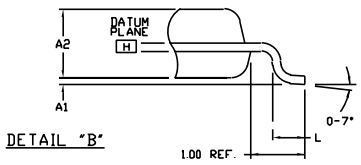


NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [H] LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. PACKAGE TOP DIMENSIONS ARE SMALLER THAN THE BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

SYMBOL	TQFP PACKAGE VARIATION ALL DIMENSIONS IN MILLIMETERS	
	128L, 14x20x1.4	
	MIN.	MAX.
A	—	1.60
A_1	0.05	0.15
A_2	1.35	1.45
D	22.00 BSC.	
D_1	20.00 BSC.	
E	16.00 BSC.	
E_1	14.00 BSC.	
L	0.45	0.75
M	0.14	—
N	128	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23



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APPROVAL
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21-0086
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