19-6144; Rev 0; 12/11

EVALUATION KIT AVAILABLE

MAX44268

1.3mm x 1.3mm, Low-Power Dual Comparator with Reference

General Description

The MAX44268 is an ultra-small and low-power dual comparator ideal for battery-powered applications such as cell phones, notebooks, and portable medical devices that have extremely aggressive board space and power constraints. The comparator is available in a miniature 1.3mm x 1.3mm, 9-bump WLP package, making it the industry's smallest dual comparator.

The IC can be powered from supply rails as low as 1.8V and up to 5.5V. It also features a 1.236V ±1% reference and a 0.7µA typical supply current per comparator. It has a rail-to-rail input structure and a unique output stage that limits supply current surges while switching. This design also minimizes overall power consumption under dynamic conditions. The IC has open-drain outputs, making it suitable for mixed voltage systems. The IC also features internal filtering to provide high RF immunity. It operates over a -40°C to +85°C temperature.

Applications

Smartphones
Notebooks
Two-Cell Battery-Powered Devices
Battery-Operated Sensors
Ultra-Low-Power Systems
Portable Medical Mobile Accessories

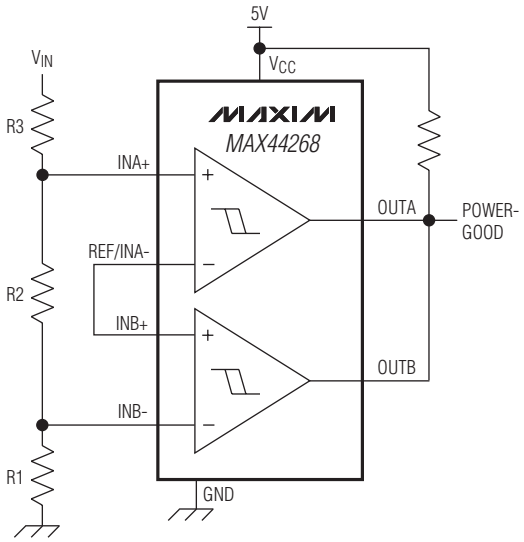
Features

- **Ultra-Low Power Consumption**
  - **0.7µA per Comparator**
- **Ultra-Small 1.3mm x 1.3mm WLP Package**
- **Internal 1.236V ±1% Reference**
- **Guaranteed Operation Down to V_{CC} = 1.8V**
- **Input Common-Mode Voltage Range Extends 200mV Beyond-the-Rails**
- **6V Tolerant Inputs Independent of Supply**
- **Open-Drain Outputs**
- **Internal Filters Enhance RF Immunity**
- **Crowbar-Current-Free Switching**
- **Internal Hysteresis for Clean Switching**
- **No Output Phase Reversal for Overdriven Inputs**

***Ordering Information** appears at end of data sheet.*

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX44268.related**.*

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... -0.3V to +6V
INA+, REF/INA-, INB+, INB- to GND ..... -0.3V to +6V
Output Voltage to GND (OUT_) ..... -0.3V to +6V
Output Current (OUT_) ..... ±50mA
Output Short-Circuit Duration (OUT_) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 11.9mW/°C above T_A = +70°C) 952mW
Continuous Input Current into Any Pin ..... ±20mA
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 84°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{GND} = 0V, V_{IN-} = V_{IN+} = 1.236V, R_{PULLUP} = 100kΩ to V_{CC}, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Input-Referred Hysteresis	V_{HYS}	(V_{GND} - 0.2V) ≤ V_{CM} ≤ (V_{CC} + 0.2V) (Note 3)			4	6	mV
Input Offset Voltage	V_{OS}	V_{GND} - 0.2V ≤ V_{CM} ≤ V_{CC} + 0.2V (Note 4)	T_A = +25°C		0.15	5	mV
			-40°C ≤ T_A ≤ +85°C			10	
Input Bias Current	I_B	T_A = +25°C			0.15		nA
		T_A = -40°C to +85°C			0.2		
Output-Voltage Swing Low	V_{OL}	V_{CC} = 1.8V, I_{SINK} = 1mA	T_A = +25°C		105	200	mV
			-40°C ≤ T_A ≤ +85°C			300	
		V_{CC} = 5V, I_{SINK} = 6mA	T_A = +25°C		285	350	
			-40°C ≤ T_A ≤ +85°C			450	
Input Voltage Range	V_{CM}	Inferred from V_{OS} test		V_{GND} - 0.2V		V_{CC} + 0.2V	V
Output Short-Circuit Current	I_{SC}	Sinking, V_{OUT} = V_{CC}	V_{CC} = 1.8V		3		mA
			V_{CC} = 5V		30		
Output Leakage Current	I_{LEAK}	V_{CC} = 5.5V, V_{OUT} = 5.5V			0.2		nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{IN-} = V_{IN+} = 1.236V, R_{PULLUP} = 100kΩ to V_{CC}, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS						
Propagation Delay High to Low (Note 5)	t_{PHL}	Input overdrive = ±100mV, V_{CC} = 5V		6		µs
		Input overdrive = ±100mV, V_{CC} = 1.8V		7		
		Input overdrive = 100mV, V_{CC} = 1.8V, Comparator A		10		
		Input overdrive = ±20mV, V_{CC} = 5V		14		
		Input overdrive = ±20mV, V_{CC} = 1.8V		19		
Propagation Delay Low to High (Note 5)	t_{PLH}	Input overdrive = ±100mV, V_{CC} = 5V		38		µs
		Input overdrive = ±100mV, V_{CC} = 1.8V		13		
		Input overdrive = ±20mV, V_{CC} = 5V		39		
		Input overdrive = ±20mV, V_{CC} = 1.8V		20		
Fall Time	t_F	C_{LOAD} = 15pF		0.2		µs
POWER SUPPLY						
Supply Voltage Range	V_{CC}	Guaranteed from PSRR tests	1.8		5.5	V
Power-Supply Rejection Ratio	PSRR	V_{CC} = 1.8V to 5.5V	60	80		dB
Supply Current Per Comparator	I_{CC}	V_{CC} = 1.8V, T_A = +25°C		0.6	0.95	µA
		V_{CC} = 5V, T_A = +25°C		0.7	1.15	
		V_{CC} = 5V, -40°C ≤ T_A ≤ +85°C			1.4	
Power-Up Time	t_{ON}			1		ms
Reference Voltage	V_{REF}	T_A = +25°C, 1%	1.224	1.236	1.248	V
		-40°C < T_A < +85°C	1.205		1.267	
Reference Voltage Temperature Coefficient	TC_{VREF}	T_A = +25°C, 1%		40		ppm/°C
Reference Output Voltage Noise	e_N	10Hz to 1kHz, C_{REF} = 1nF		75		$µV_{RMS}$
		10Hz to 6kHz, C_{REF} = 1nF		130		
Reference Line Regulation	$\Delta V_{REF}/\Delta V_{CC}$	V_{CC} = 1.8V to 5.5V		0.35		mV/V
Reference Load Regulation	$\Delta V_{REF}/\Delta I_{OUT}$	0 < I_{OUT} < 100nA		0.05		mV/nA

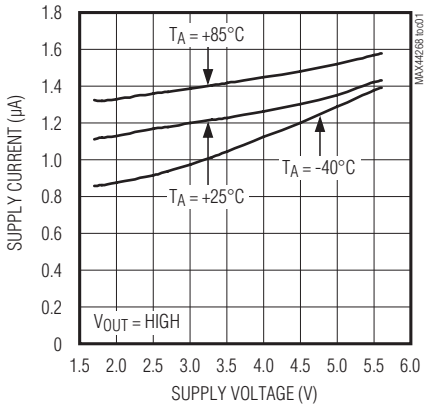
Note 2: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 3: Hysteresis is the input voltage difference between the two switching points.
Note 4: V_{OS} is the average of the positive and negative trip points minus V_{REF}.
Note 5: Overdrive is defined as the voltage above or below the switching points.

1.3mm x 1.3mm, Low-Power Dual Comparator with Reference

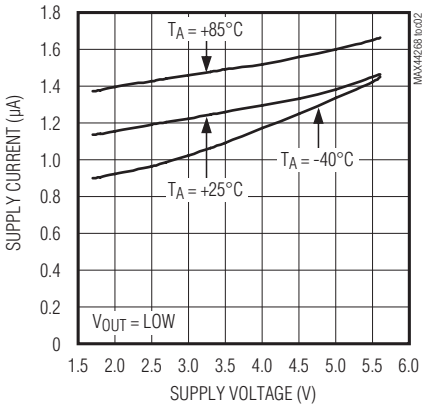
Typical Operating Characteristics

(V_{CC} = 5V, V_{GND} = 0V, V_{IN-} = V_{IN+} = 1.236V, R_{PULLUP} = 100kΩ to V_{CC}, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

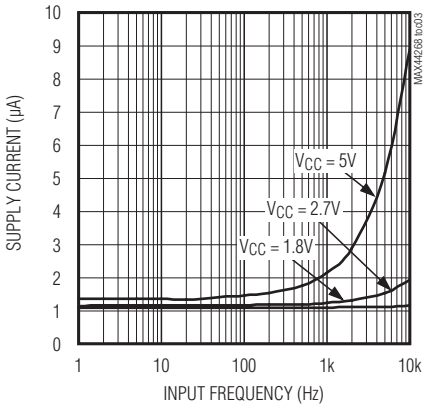
SUPPLY CURRENT vs. SUPPLY VOLTAGE



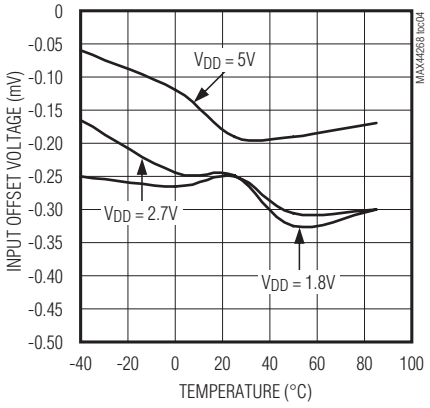
SUPPLY CURRENT vs. SUPPLY VOLTAGE



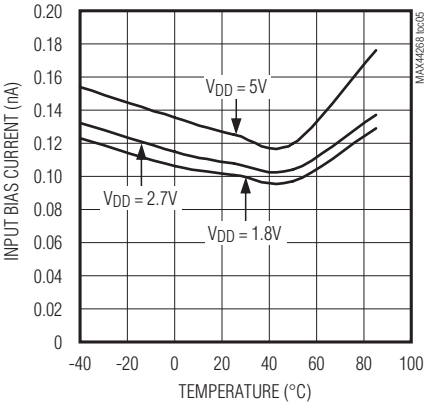
SUPPLY CURRENT vs. TRANSITION FREQUENCY ($V_{OVERDRIVE}$ = 20mV)



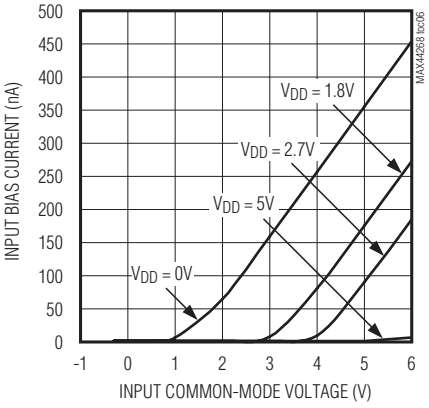
INPUT OFFSET VOLTAGE vs. TEMPERATURE



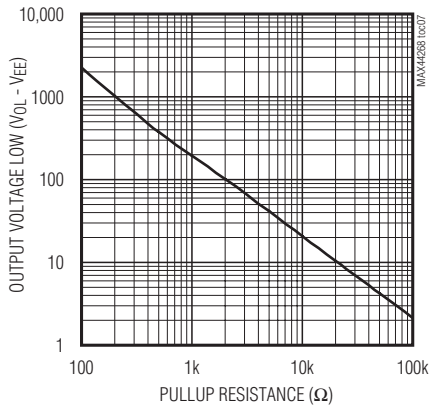
INPUT BIAS CURRENT vs. TEMPERATURE



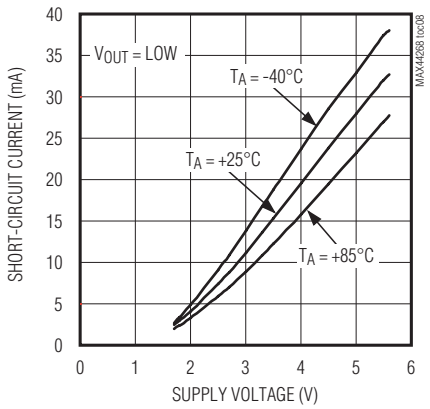
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



OUTPUT VOLTAGE LOW vs. PULLUP RESISTANCE



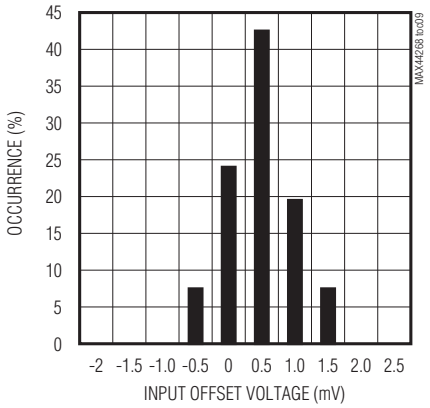
SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



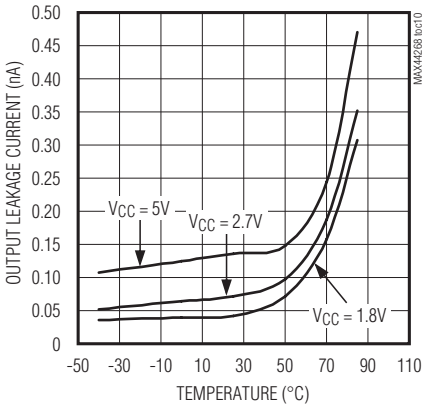
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{IN-} = V_{IN+} = 1.236V, R_{PULLUP} = 100kΩ to V_{CC}, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

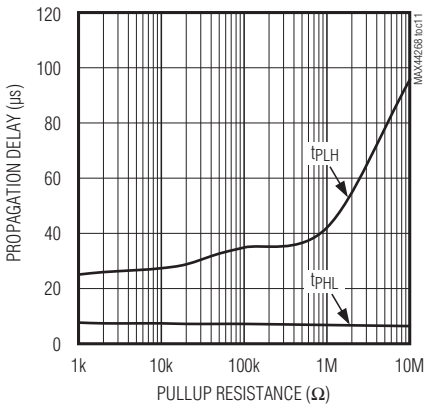
INPUT OFFSET VOLTAGE HISTOGRAM



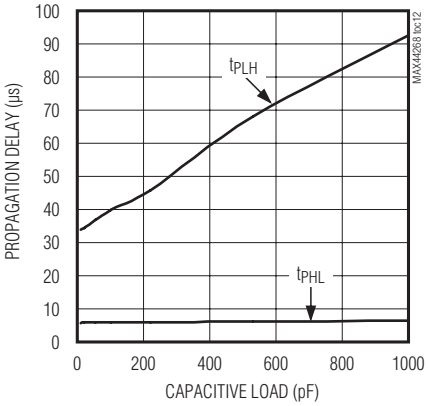
LEAKAGE CURRENT vs. TEMPERATURE



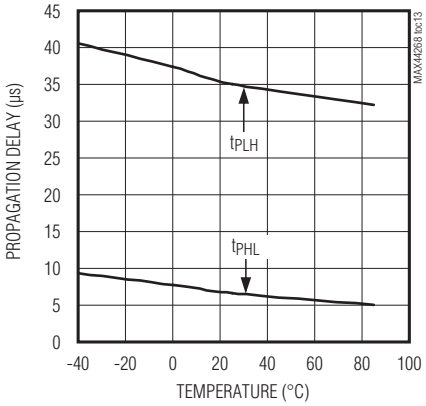
PROPAGATION DELAY vs. PULLUP RESISTANCE



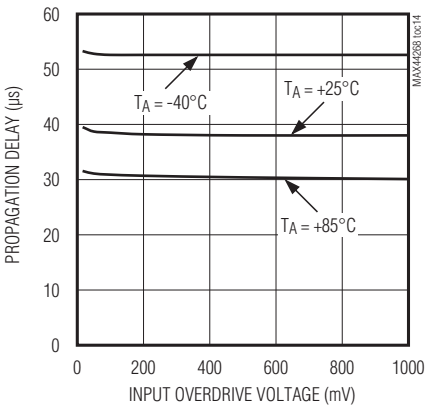
PROPAGATION DELAY vs. CAPACITIVE LOAD



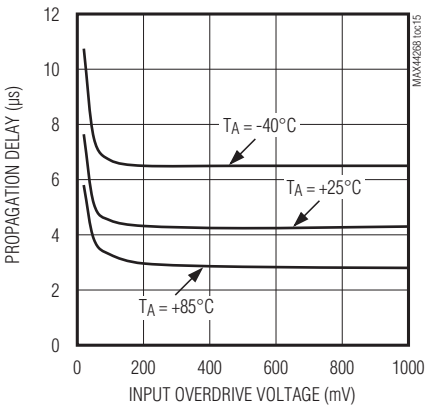
PROPAGATION DELAY vs. TEMPERATURE ($V_{OVERDRIVE}$ = 100mV, V_{DD} = 5V)



PROPAGATION DELAY vs. INPUT OVERDRIVE (t_{PLH})



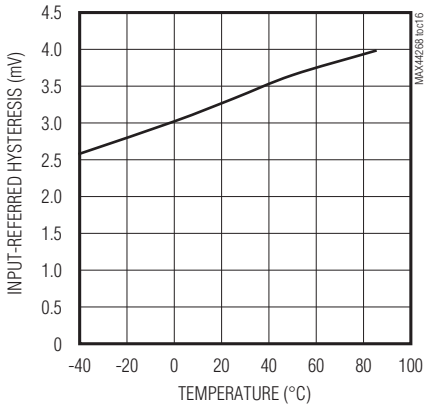
PROPAGATION DELAY vs. INPUT OVERDRIVE (t_{PLH})



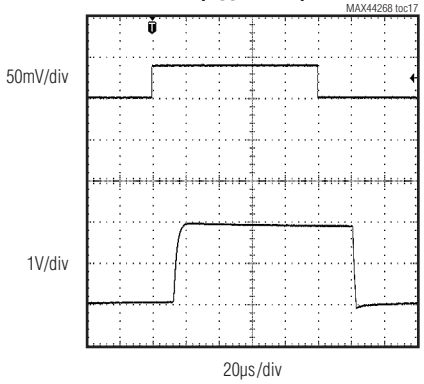
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{IN-} = V_{IN+} = 1.236V, R_{PULLUP} = 100kΩ to V_{CC}, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

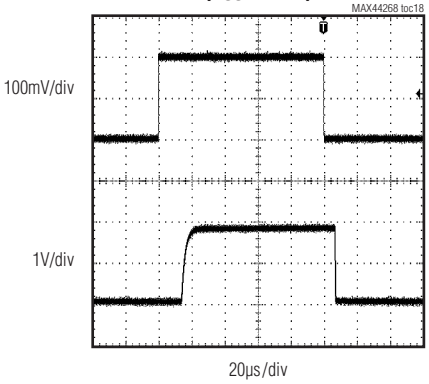
INPUT-REFERRED HYSTERESIS vs. TEMPERATURE



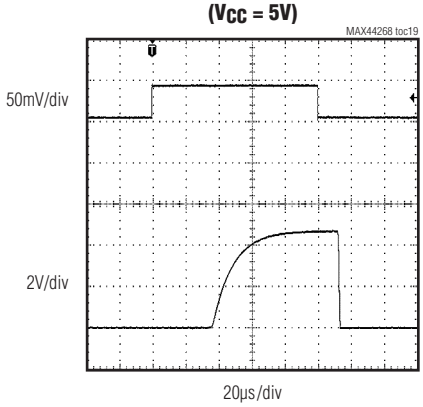
SMALL-SIGNAL TRANSIENT RESPONSE (V_{CC} = 1.8V)



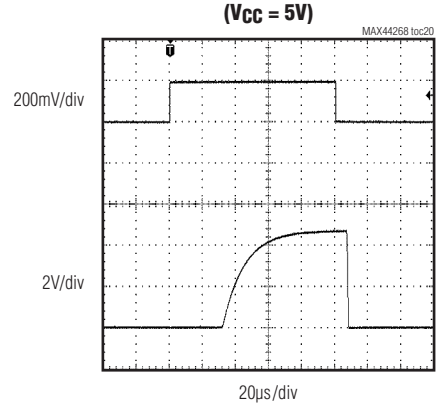
LARGE-SIGNAL TRANSIENT RESPONSE (V_{CC} = 1.8V)



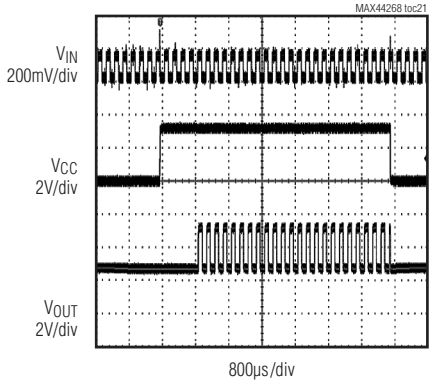
SMALL-SIGNAL TRANSIENT RESPONSE (V_{CC} = 5V)



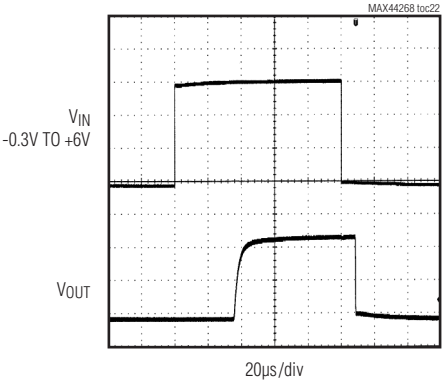
LARGE-SIGNAL TRANSIENT RESPONSE (V_{CC} = 5V)



POWER-UP RESPONSE



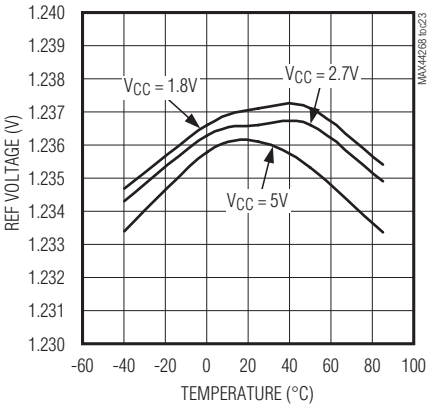
NO OUTPUT PHASE REVERSAL



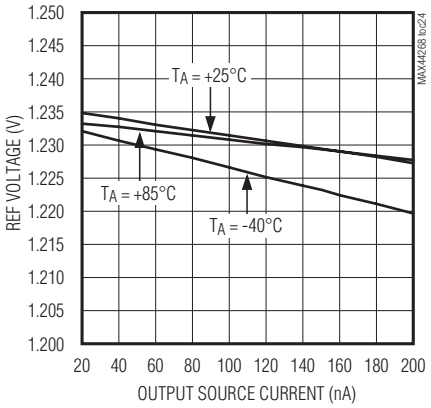
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, V_{IN-} = V_{IN+} = 1.236V, R_{PULLUP} = 100kΩ to V_{CC}, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.)

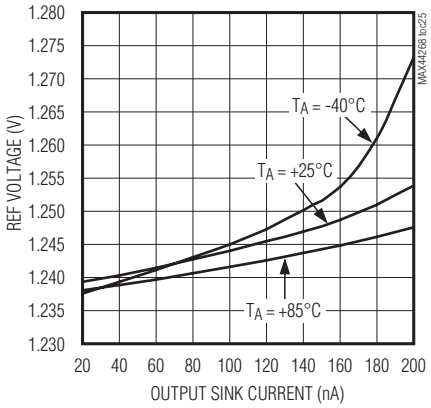
REF VOLTAGE vs. TEMPERATURE



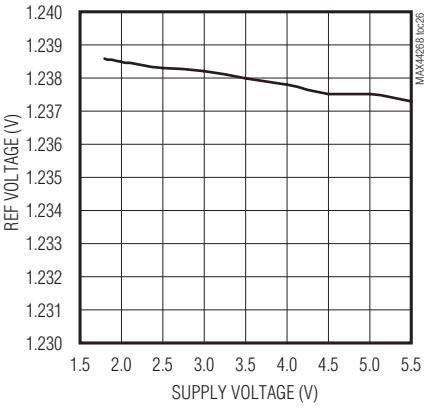
REF VOLTAGE vs. REF SOURCE CURRENT AND TEMPERATURE



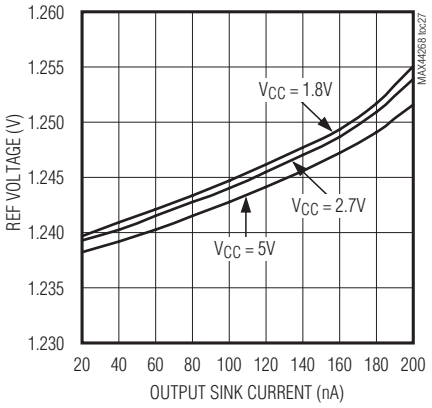
REF VOLTAGE vs. REF SINK CURRENT AND TEMPERATURE



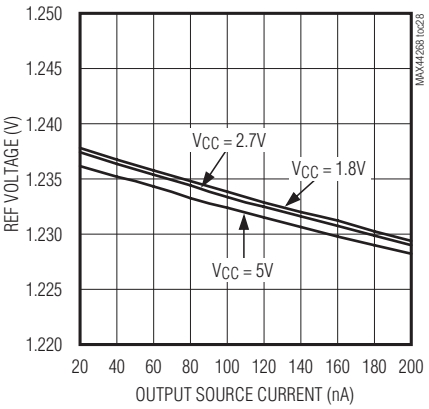
REF VOLTAGE vs. SUPPLY VOLTAGE



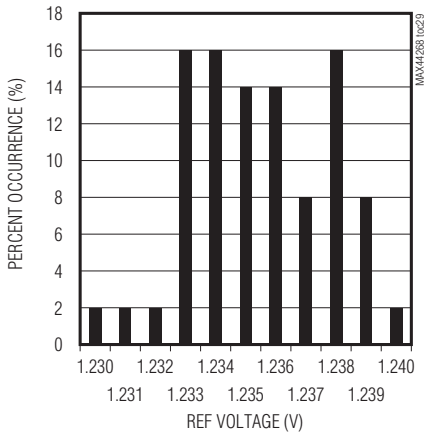
REF VOLTAGE vs. REF SINK CURRENT



REF VOLTAGE vs. REF SOURCE CURRENT

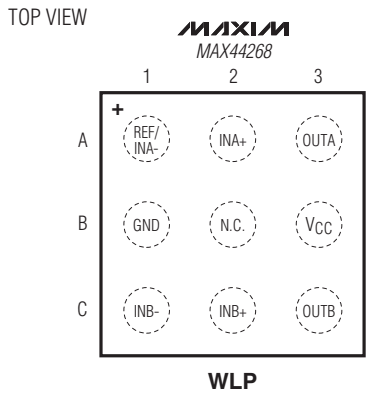


REF VOLTAGE DRIFT HISTOGRAM



1.3mm x 1.3mm, Low-Power Dual Comparator with Reference

Bump Configuration



WLP

Bump Description

PIN	NAME	FUNCTION
A1	REF/INA-	Reference Output/Comparator A Inverting Input
A2	INA+	Comparator A Noninverting Input
A3	OUTA	Comparator A Output
B1	GND	Negative Supply Voltage. Bypass to GND with a 1.0µF capacitor.
B2	N.C.	No Connection
B3	V_{CC}	Positive Supply Voltage. Bypass to GND with a 1.0µF capacitor.
C1	INB-	Comparator B Inverting Input
C2	INB+	Comparator B Noninverting Input
C3	OUTB	Comparator B Output

Detailed Description

The MAX44268 is a general-purpose dual comparator for battery-powered devices where area, power, and cost constraints are crucial. The IC can operate with a low 1.8V supply rail typically consuming 0.7µA quiescent current per comparator. This makes it ideal for mobile and very low-power applications. The IC's common-mode input voltage range extends 200mV beyond-the-rails. An internal 4mV hysteresis ensures clean output switching, even with slow-moving input signals.

Input Stage Structure

The input common-mode voltage range extends from (V_{GND} - 0.2V) to (V_{CC} + 0.2V). The comparator operates at any different input voltage within these limits with low input bias current. Input bias current is typically 0.15nA if the input voltage is between the supply rails. The device also features a 1.236V reference voltage output on the inverting input of comparator A.

The IC features a unique input ESD structure that can handle voltages from -0.3V to +6V independent of supply voltage. This allows for the device to be powered down with a signal still present on the input without damaging the part. This feature is useful in applications where one of the inputs has transient spikes that exceed the supply rails.

No Output Phase Reversal for Overdriven Inputs

The IC's design is optimized to prevent output phase reversal if both the inputs are within the input common-mode voltage range. If one of the inputs is outside the input common-mode voltage range, then output phase reversal does not occur as long as the other input is kept within the valid input common-mode voltage range. This behavior is shown in the No Output Phase Reversal graph in the *Typical Operating Characteristics* section.

Open-Drain Output

The IC features an open-drain output, enabling greater control of speed and power consumption in the circuit design. The output logic level is also independent from the input, allowing for simple level translation.

RF Immunity

The IC has very high RF immunity due to on-chip filtering of RF sensitive nodes. This allows the IC to hold its output state even in the presence of high amounts of RF noise. This improved RF immunity makes the IC ideal for mobile wireless devices.

Applications Information

Hysteresis

Many comparators oscillate in the linear region of operation because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal or very close to the voltage on the other input.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal and the output trips, the hysteresis effectively causes one comparator input to move quickly past the other. This takes the input out of the region where oscillation occurs. This provides clean output transitions for noisy, slow-moving input signals. The IC has an internal hysteresis of 4mV. Additional hysteresis can be generated with three resistors using positive feedback (Figure 2).

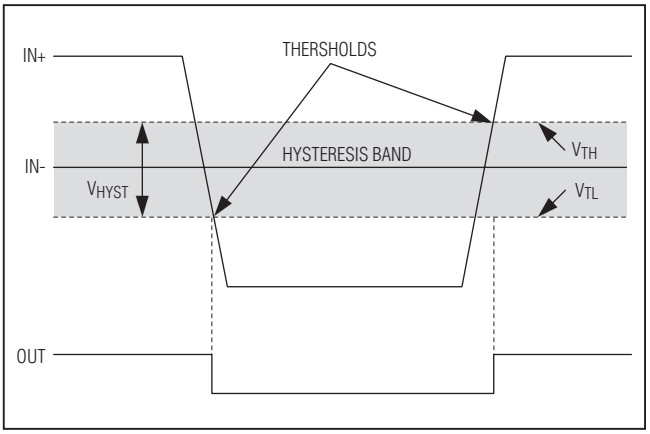


Figure 1. Threshold Hysteresis Band (Not to Scale)

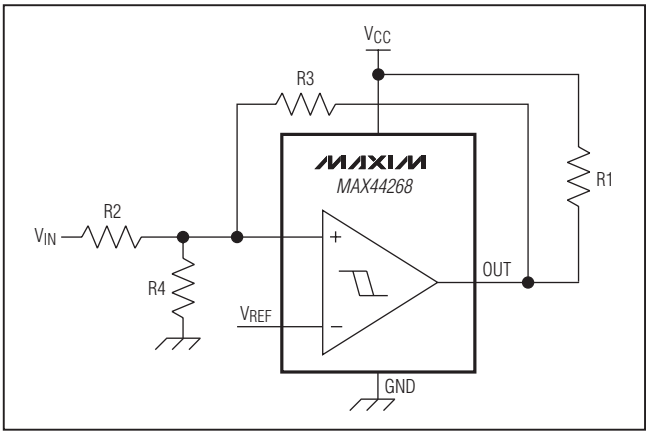


Figure 2. Adding Hysteresis with External Resistors

Use the following procedure to calculate resistor values.

1) Select R3. Input bias current at IN_+ is less than 15nA. To minimize errors caused by the input bias current, the current through R3 should be at least 1.5µA. Current through R3 at the trip point is (V_{REF} - V_{OUT})/R3. Considering the two possible output states in solving for R3 yields two formulas:

   R3 = V_{REF}/IR3 and R3 = [(V_{CC} - V_{REF})/IR3] - R1

   Use the smaller of the two resulting resistor values. For example, for V_{CC} = 5V, IR3 = -1.5µA, R1 = 200kΩ, and a V_{REF} = 1.236V, the two resistor values are 827kΩ and 1.5MΩ. Therefore, for R3 choose the standard value of 825kΩ.

2) Choose the hysteresis band required (V_{HB}). In this example, the V_{HB} = 50mV.

3) Calculate R2 according to the following equation:

$$R2 = (R1 + R3)\left(\frac{V_{HB}}{V_{CC} + (V_{REF} \times R1)/R3}\right)$$

For this example, insert the value:

$$R2 = (200k\Omega + 0.825M\Omega)\left(\frac{50mV}{5.3}\right) = 9.67k\Omega$$

For this example, choose standard value R2 = 9.76kΩ.

4) Choose the trip point for V_{IN} rising (V_{THR}) in such a way that:

$$V_{THR} > V_{REF}\left(1 + \frac{V_{HB}}{V_{CC}}\right)$$

   V_{THR} is the threshold voltage at which the comparator switches its output from low to high, as V_{IN} rises above the trip point. For this example, choose V_{THR} = 3V.

5) Calculate R4 as follows:

$$R4 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R2}\right) - \left(\frac{1}{R2}\right) - \left(\frac{1}{R3}\right)}$$

$$R4 = \frac{1}{\left(\frac{3}{1.236V \times 9.76}\right) - \left(\frac{1}{9.76}\right) - \left(\frac{1}{825}\right)} = 6.93k\Omega$$

For this example, choose a standard value of 6.98kΩ.

6) Verify the trip voltages and hysteresis as follows:

$$V_{THR} = V_{REF} \times R2\left(\left(\frac{1}{R2}\right) + \left(\frac{1}{R3}\right) + \left(\frac{1}{R4}\right)\right)$$

$$V_{THF} = V_{REF} \times R2\left(\left(\frac{1}{R2}\right) + \left(\frac{1}{R1 + R3}\right) + \left(\frac{1}{R4}\right)\right)$$

$$- \frac{R2}{R1 + R3} \times V_{CC}$$

The hysteresis network in Figure 2 can be simplified if the reference voltage is chosen to be at midrail and the trip points of the comparator are chosen to be symmetrical about the reference voltage. Use the circuit in Figure 3 if the reference voltage can be designed to be at the center of the hysteresis band. For the symmetrical case, follow the same steps outlined in the paragraph above to calculate the resistor values except that in this case, resistor R4 approaches infinity (open). So in the previous example, using comparator B with V_{REF} = 2.5V, if V_{THR} = 2.525V and V_{THF} = 2.475V then using the above formulas, results in R1 = 200kΩ, R2 = 9.09kΩ, and R3 = 825kΩ, R4 = not installed.

Logic-Level Translator

Due to the open-drain output of the IC, the device can translate between two different logic levels (Figure 4). If the internal 4mV hysteresis is not sufficient, then external resistors can be added to increase the hysteresis as shown in Figure 2 and Figure 3.

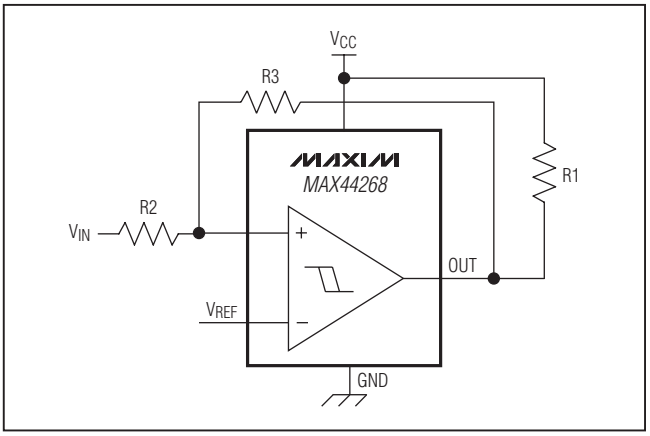


Figure 3. Simplified External Hysteresis Network if V_{REF} is at the Center of the Hysteresis Band

Power-On-Reset Circuit

The IC can be used to make a power-on-reset circuit as displayed in Figure 5. The negative input provides the ratiometric reference with respect to the power supply and is created by a simple resistive divider. Choose reasonably large values to minimize the power consumption in the resistive divider. The positive input provides the power-on delay time set by the time constant of the RC circuit formed by R2 and C1. This simple circuit can be used to power up the system in a known state after ensuring that the power supply is stable. Diode D1 provides a rapid reset in the event of unexpected power loss. If using comparator A, R3 and R4 are not populated and REF settles in approximately 100µs.

Relaxation Oscillator

The IC can also be used to make a simple relaxation oscillator (Figure 6) using comparator B. By adding the RC circuit R5 and C1, a standard Schmidt Trigger circuit referenced to a set voltage is converted into an astable multivibrator. As shown in Figure 7, IN- is a sawtooth waveform with capacitor C1 alternately charging and discharging through resistor R5. The external hysteresis network formed by R1 to R4 defines the trip voltages as:

$$V_{T\_RISE} = V_{CC}\left(\frac{R3 \times R4}{R2R3 + R2R4 + R3R4}\right)$$

$$V_{T\_FALL} = V_{CC}\left(\frac{R4R5(R1+R2+R3) + R1R3R4}{R4R5(R1+R2+R3) + R1R3R4 + R2(R1R3 + R3R5 + R1R5)}\right)$$

Using the basic time domain equations for the charging and discharging of an RC circuit, the logic-high time, logic-low time, and frequency can be calculated as:

$$t_{LOW} = R5C1 \ln\left(\frac{V_{T\_FALL}}{V_{T\_RISE}}\right)$$

Since the comparator's output is open drain, it goes to high impedance corresponding to logic-high. So, when the output is at logic-high, the C1 capacitor charges through the resistor network formed by R1 to R5. An accurate calculation of t_{HIGH} would have involved applying thevenin's theorem to compute the equivalent thevenin voltage ($V_{THEVENIN}$) and thevenin resistance

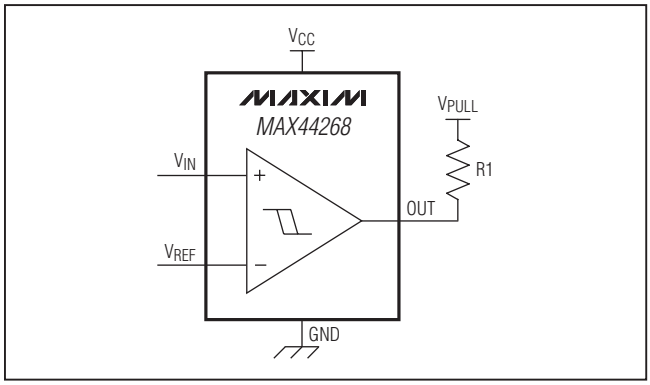


Figure 4. Logic-Level Translator

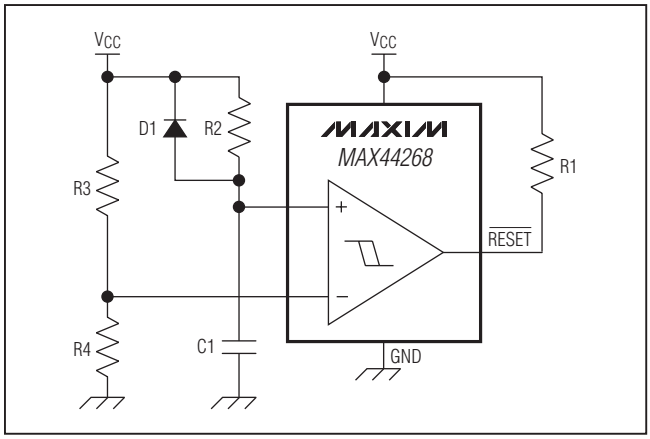


Figure 5. Power-On Reset Circuit

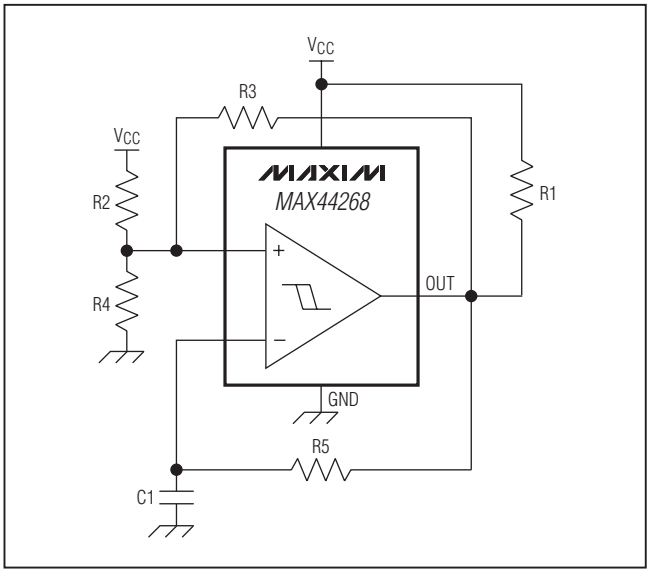


Figure 6. Relaxation Oscillator

($R_{THEVENIN}$) in series with the capacitor C1. t_{HIGH} can then be computed using the basic time domain equations for the charging RC circuit as:

$$t_{HIGH} = R_{THEVENIN}\, C1 \ln\left(\frac{V_{THEVENIN} - V_{T\_RISE}}{V_{THEVENIN} - V_{T\_FALL}}\right)$$

$$R_{THEVENIN} = [(R2 \,||\, R4) + R3] \,||\, R1 + R5$$

$$V_{THEVENIN} = \frac{V_{CC}\,[(R2 \,||\, R4) + R3]}{(R2 \,||\, R4) + R3 + R1} + \frac{V_{CC} \times R4}{R2 + R4} \times \frac{R1}{(R2 \,||\, R4) + R3 + R1}$$

The t_{HIGH} calculation can be simplified by selecting the component values in such a way that R3 >> R1 and R5 >> R1. This ensures that the output of the comparator goes close to V_{CC} when at logic-high (that is, $V_{THEVENIN}$ ~ V_{CC} and $R_{THEVENIN}$ ~ R5). With this selection, t_{HIGH} can be approximated as:

$$t_{HIGH} = R5C1 \ln\left(\frac{V_{CC} - V_{T\_RISE}}{V_{CC} - V_{T\_FALL}}\right)$$

The frequency of the relaxation oscillator is:

$$f = \frac{1}{t_{HIGH} + t_{LOW}} = \frac{1}{R5C1 \ln\left(\frac{V_{T\_FALL}\,(V_{CC} - V_{T\_RISE})}{V_{T\_RISE}\,(V_{CC} - V_{T\_FALL})}\right)}$$

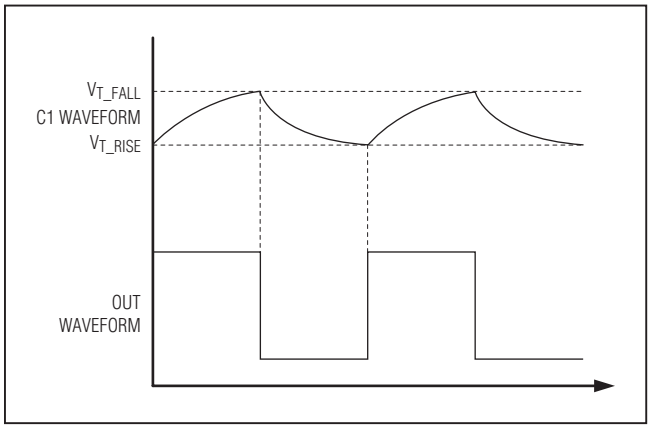


Figure 7. Relaxation Oscillator Waveforms

Window Detector Circuit

The IC is ideal for window detectors (undervoltage/overvoltage detectors). *Typical Application Circuit* shows a simple window detector circuit. By changing the values of R1, R2, and R3 different voltage threshold values can be chosen. For this example, assume a single-cell Li+ battery with a 2.9V end-of-life charge, a peak charge of 4.2V, and a nominal value of 3.6V. OUTA provides an active-low undervoltage indication, and OUTB provides an active-low overvoltage indication. The open-drain outputs of both the comparators are wired ORed to give an active-high power-good signal.

The design procedure is as follows:

1) Select R1. The input bias current into INB- is less than 15nA, so the current through R1 should exceed 1.5µA for the thresholds to be accurate. In this example, choose R1 = 825kΩ (1.236V/1.5µA).
2) Calculate R2 + R3. The overvoltage threshold should be 4.2V when V_{IN} is rising. The design equation is as follows:

$$R2 + R3 = R1 \times \left[\left(\frac{V_{OTH}}{V_{REF}}\right) - 1\right]$$
$$= 825 \times \left[\left(\frac{4.2}{1.236}\right) - 1\right]$$
$$= 1969k\Omega$$

3) Calculate R2. The undervoltage threshold should be 2.9V when V_{IN} is falling. The design equation is as follows:

$$R2 = (R1 + R2 + R3) \times \left(\frac{V_{REF}}{V_{UTH}}\right) - R1$$
$$= \left((825 + 1969) \times (1.236/2.9)\right) - 825$$
$$= 370k\Omega$$

For this example, choose a 374kΩ standard value 1% resistor.

4) Calculate R3:

$$R3 = (R2 + R3) - R2$$
$$= 1969k\Omega - 374k\Omega$$
$$= 1.595M\Omega$$

For this example, choose a 1.58MΩ standard value 1% resistor.

Board Layout and Bypassing

Use 1.0µF bypass capacitors from V_{CC} to GND. To maximize performance, minimize stray inductance by putting this capacitor close to the V_{CC} pin and reducing trace lengths. Use 1nF bypass capacitors from REF/INA- to GND as close as possible to the IC. Do not route noisy traces near REF/INA-.

Jack Detect

The IC can be used to detect peripheral devices connected to a circuit using comparator B. This includes a simple jack-detect scheme for cell phone applications. Figure 8 shows how the device can be used in conjunction with an external reference to detect an accessory ID input. The open-drain output of the devices allows the output logic level to be controlled independent of the peripheral device's load, making interfacing and controlling external devices as simple as monitoring a few digital inputs on a microcontroller or codec.

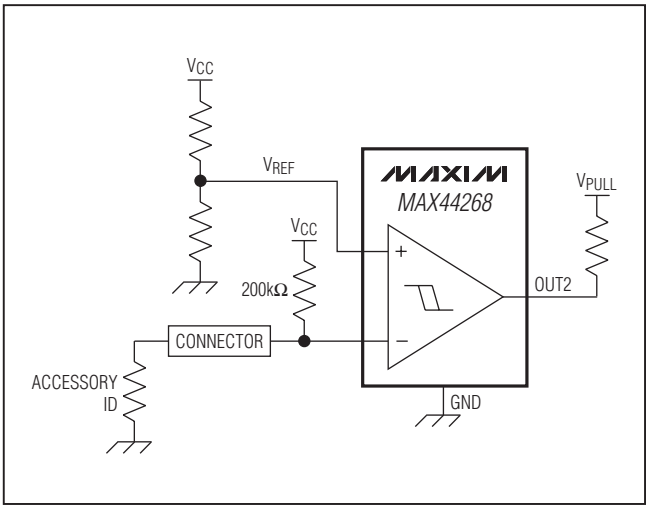


Figure 8. Jack Detector Circuit

Chip Information

PROCESS: BiCMOS

Ordering Information

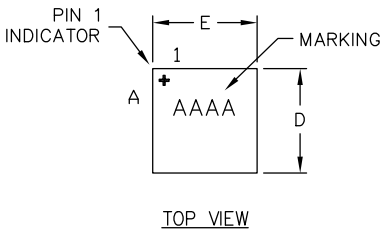
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44268EWL+T	-40°C to +85°C	9 WLP	+AJK

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

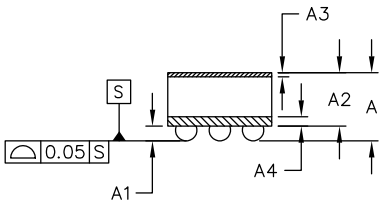
Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91B1-6	**21-0430**	Refer to **Application Note 1891**



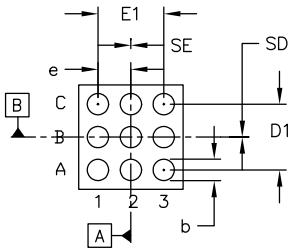
TOP VIEW



SIDE VIEW

COMMON DIMENSIONS	
A	0.64±0.05
A1	0.21±0.03
A2	0.43 REF
A3	0.025 BASIC
A4	0.07 BASIC
b	ø0.26±0.03
D1	0.80 BASIC
E1	0.80 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W91B1+6	1.22	1.30	1.22	1.30	NONE



BOTTOM VIEW

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.

MAXIM

TITLE:
PACKAGE OUTLINE
9 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0430	B	1/1

-DRAWING NOT TO SCALE-

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—