# Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches 


#### Abstract

General Description The MAX4514/MAX4515 are single-pole/single-throw (SPST), CMOS, low-voltage, single-supply analog switches with very low switch on-resistance. The MAX4514 is normally open (NO). The MAX4515 is normally closed (NC). These CMOS switches can operate continuously with a single supply between +2 V and +12 V . Each switch can handle rail-to-rail analog signals. The off-leakage current maximum is only 1 nA at $+25^{\circ} \mathrm{C}$ or 20 nA at $+85^{\circ} \mathrm{C}$. All digital inputs have 0.8 V to 2.4 V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a +5 V supply. For pin-compatible parts for use with dual supplies, see the MAX4516/MAX4517.


## Applications

Battery-Operated Equipment
Audio and Video Signal Routing
Low-Voltage Data-Acquisition Systems
Communications Circuits
PCMCIA Cards
Cellular Phones
Modems

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* Available in SOT23-5 Package
* +2V to +12V Single-Supply Operation
- Guaranteed On-Resistance:
    20\Omega with +5V Supply
    10\Omega with +12V Supply
- Guaranteed Low Off-Leakage Currents:
    1nA at +25*
    20nA at +85'C
- Guaranteed Low On-Leakage Currents:
    2nA at +25*'C
    40nA at +85 ' C
- Low Charge Injection: 10pC
* Fast Switching Speed: toN = 150ns, toFF = 100ns
Break-Before-Make Operation: toN > tofF at +5V
- TTL/CMOS-Logic Compatible with +5V Supply
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Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
| :--- | :--- | :--- |
| MAX4514CPA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX4514CSA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 SO |
| MAX4514CUK | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 5 SOT23-5 |
| MAX4514C/D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice $^{*}$ |

Ordering Information continued at end of data sheet.
*Contact factory for dice specifications.

Pin Configurations

TOP VIEW


| INPUT | SWITCH STATE |  |
| :---: | :---: | :---: |
|  | MAX4514 | MAX4515 |
| LOW | OFF | ON |
| HIGH | ON | OFF |



SOT23-5

## Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)


Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—+5V Supply

$\left(\mathrm{V}+=+4.5 \mathrm{~V}\right.$ to $+5.5 \mathrm{~V}, \mathrm{~V}_{\text {INH }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {INL }}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. $)$

| PARAMETER | SYMBOL | CONDITIONS |  |  | MIN | TYP (Note 2) | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |  |
| Analog Signal Range | $\mathrm{V}_{\mathrm{CO}}, \mathrm{V}_{\mathrm{NO}}$, $\mathrm{V}_{\mathrm{NC}}$ |  |  |  | 0 |  | V+ | V |
| COM to NO or NC On-Resistance | Ron | $\begin{aligned} & \mathrm{V}+=5 \mathrm{~V}, \mathrm{VCOM}=3.5 \mathrm{~V}, \\ & \mathrm{I} C O M=1 \mathrm{~mA} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 10 | 20 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ | MAX |  |  | 25 |  |
| COM to NO or NC On-Resistance Flatness | $\Delta \mathrm{RON}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}=1 \mathrm{~V}, 2 \mathrm{~V}, 3 \mathrm{~V} ; \\ & \mathrm{ICOM}=1 \mathrm{~mA} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 1 | 3 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ | MAX |  |  | 5 |  |
| NO or NC Off-Leakage Current (Note 3) | INO(OFF) <br> INC(OFF) | V+ = 5.5V, <br> $V_{C O M}=1 V$, <br> $\mathrm{V}_{\mathrm{NO}}$ or $\mathrm{V}_{\mathrm{NC}}=4.5 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -1 | 0.01 | 1 | nA |
|  |  |  | $\begin{aligned} & \mathrm{T}_{A}=\mathrm{T}_{\mathrm{MIN}} \\ & \text { to } \mathrm{T}_{\mathrm{MAX}} \end{aligned}$ | C, E | -20 |  | 20 |  |
|  |  |  |  | M | -100 |  | 100 |  |
| COM Off-Leakage Current (Note 3) | ICOM(OFF) | $\mathrm{V}+=5.5 \mathrm{~V},$ <br> $\mathrm{VCOM}=4.5 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{NO}}$ or $\mathrm{V}_{\mathrm{NC}}=1 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -1 | 0.01 | 1 | nA |
|  |  |  | $\begin{aligned} & \mathrm{T}_{A}=\mathrm{T}_{\mathrm{MIN}} \\ & \text { to } \mathrm{T}_{\text {MAX }} \end{aligned}$ | C, E | -20 |  | 20 |  |
|  |  |  |  | M | -100 |  | 100 |  |
| COM On-Leakage Current (Note 3) | ICOM(ON) | $\begin{aligned} & V_{+}=5.5 \mathrm{~V}, \\ & V_{C O M}=4.5 \mathrm{~V}, \\ & V_{N O} \text { or } V_{N C}=4.5 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -2 | 0.01 | 2 | nA |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$$\text { to } \mathrm{T}_{\mathrm{MAX}}$ | C, E | -40 |  | 40 |  |
|  |  |  |  | M | -200 |  | 200 |  |
| DIGITAL I/O |  |  |  |  |  |  |  |  |
| Input Logic High | VIH |  |  |  | 2.4 |  | V+ | V |
| Input Logic Low | VIL |  |  |  | 0 |  | 0.8 | V |
| Input Current Logic High or Low | $\mathrm{IIH}_{\text {, IIL }}$ | V IN $=\mathrm{V}+, \mathrm{OV}$ |  |  | -1 | 0.03 | 1 | $\mu \mathrm{A}$ |
| SWITCH DYNAMIC CHARACTERISTICS |  |  |  |  |  |  |  |  |
| Turn-On Time | ton | Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 30 | 150 | ns |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ | max |  |  | 240 |  |
| Turn-Off Time | toff | Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 20 | 100 | ns |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  |  | 150 |  |

# Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches 

## ELECTRICAL CHARACTERISTICS—+5V Supply (continued)

$\left(\mathrm{V}+=+4.5 \mathrm{~V}\right.$ to $+5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{INH}}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. $)$

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | $\begin{aligned} & \text { TYP } \\ & \text { (Note 2) } \end{aligned}$ | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SWITCH DYNAMIC CHARACTERISTICS |  |  |  |  |  |  |  |
| Charge Injection (Note 4) | Q | $\begin{aligned} & C_{L}=1 \mathrm{nF}, \mathrm{~V}_{\mathrm{NO}}=0 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{S}}=0 \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \text {, Figure } 1 \end{aligned}$ |  |  | 2 | 10 | pC |
| Off Isolation | VISO | $\begin{aligned} & \mathrm{RL}=50 \Omega, C \mathrm{C}=15 \mathrm{pF}, \\ & \mathrm{~V}_{\mathrm{NO}}=1 \mathrm{~V}_{\mathrm{RMS}}, \mathrm{f}=100 \mathrm{kHz}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \text {, Figure } 3 \end{aligned}$ |  |  | $\leq-90$ |  | dB |
| NO or NC Off Capacitance | CNO(OFF), $\mathrm{C}_{\mathrm{NC} \text { (OFF) }}$ | $f=1 \mathrm{MHz}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Figure 4 |  |  | 14 |  | pF |
| COM Off Capacitance | CCOM(OFF) | $\mathrm{f}=1 \mathrm{MHz}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Figure 4 |  |  | 14 |  | pF |
| COM On Capacitance | Ccom(ON) | $f=1 \mathrm{MHz}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Figure 4 |  |  | 30 |  | pF |
| POWER SUPPLY |  |  |  |  |  |  |  |
| V+ Supply Current | I+ | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ or $\mathrm{V}_{+}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 |  | 1 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {Min }}$ to TMAX | -10 |  | 10 |  |

## ELECTRICAL CHARACTERISTICS—+12V Supply

$\left(\mathrm{V}+=+11.4 \mathrm{~V}\right.$ to $+12.6 \mathrm{~V}, \mathrm{VINH}^{2}=5 \mathrm{~V}, \mathrm{~V}$ INL $=0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. $)$

| PARAMETER | SYMBOL | CONDITIONS |  |  | MIN | TYP <br> (Note 2) | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |  |
| Analog Signal Range | $\mathrm{V}_{\mathrm{COM}}, \mathrm{V}_{\mathrm{NO}}$, VNC |  |  |  | 0 |  | V+ | V |
| COM to NO or NC On-Resistance | Ron | $\mathrm{VCOM}=10 \mathrm{~V}, \mathrm{ICOM}=1 \mathrm{~mA}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 5 | 10 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  |  | 15 |  |
| NO, NC Off-Leakage Current (Note 3) | I(NO)OFF I(NC)OFF | $\begin{aligned} & V_{+}=12.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{COM}}=1 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=10 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -2 |  | 2 | nA |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ <br> to TMAX | C, E | -50 |  | 50 |  |
|  |  |  |  | M | -200 |  | 200 |  |
| COM Off-Leakage Current (Note 3) | ICOM(OFF) | $\begin{aligned} & V_{+}=12.6 \mathrm{~V}, V_{C O M}=10 \mathrm{~V} \\ & V_{\text {NO }} \text { or } V_{N C}=1 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -2 |  | 2 | nA |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ <br> to TMAX | C, E | -50 |  | 50 |  |
|  |  |  |  | M | -200 |  | 200 |  |
| COM On-Leakage Current (Note 3) | ICOM(ON) | $\begin{aligned} & V_{+}=12.6 \mathrm{~V}, V_{C O M}=10 \mathrm{~V}, \\ & V_{\text {NO }} \text { or } V_{N C}=10 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -4 |  | 4 | nA |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ <br> to TMAX | C, E | -100 |  | 100 |  |
|  |  |  |  | M | -400 |  | 400 |  |
| DIGITAL I/O |  |  |  |  |  |  |  |  |
| Input Logic High | VINH |  |  |  | 5 |  | V+ | V |
| Input Logic Low | VINL |  |  |  | 0 |  | 0.8 | V |
| Input Current Logic High or Low | l/nH, lint | V IN $=\mathrm{V}+, \mathrm{OV}$ |  |  | -1 | 0.03 | 1 | $\mu \mathrm{A}$ |
| POWER SUPPLY |  |  |  |  |  |  |  |  |
| V+ Supply Current | I+ | $\mathrm{IN}=0 \mathrm{~V}$ or $\mathrm{V}+$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | -2 |  | 2 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  | -20 |  | 20 |  |

## Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—+3V Supply
$\left(\mathrm{V}+=+3 \mathrm{~V}\right.$ to $+3.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP <br> (Note 2) | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |
| Analog Signal Range | $\mathrm{V}_{\mathrm{COM}}, \mathrm{V}_{\mathrm{NO}}$, $\mathrm{V}_{\mathrm{NC}}$ |  |  | 0 |  | V+ | V |
| COM to NO or NC On-Resistance | Ron | $\begin{aligned} & \mathrm{V}_{\mathrm{COM}}=1.5 \mathrm{~V}, \mathrm{I}_{\mathrm{NO}}=1 \mathrm{~mA}, \\ & \mathrm{~V}+=3 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 20 | 50 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 75 |  |
| DIGITAL I/O |  |  |  |  |  |  |  |
| Input Logic High | VINH |  |  | 2.4 |  | V+ | V |
| Input Logic Low | VINL |  |  | 0 |  | 0.80 | V |
| Input Current Logic High or Low | linh, linL | V IN $=\mathrm{V}+, \mathrm{OV}$ |  | -1 | 0.03 | 1 | $\mu \mathrm{A}$ |
| SWITCH DYNAMIC CHARACTERISTICS |  |  |  |  |  |  |  |
| Turn-On Time (Note 4) | ton | Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 45 | 150 | ns |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 240 |  |
| Turn-Off Time (Note 4) | toff | Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 30 | 100 | ns |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 150 |  |
| Charge Injection (Note 4) | Q | $C L=1 n F$, Figure 1 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 4 | 10 | pC |
| POWER SUPPLY |  |  |  |  |  |  |  |
| V+ Supply Current | I+ | $\mathrm{IN}=0 \mathrm{~V}$ or $\mathrm{V}+$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 |  | 1 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -10 |  | 10 |  |

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Leakage parameters are $100 \%$ tested at maximum-rated hot operating temperature, and are guaranteed by correlation at $+25^{\circ} \mathrm{C}$.
Note 4: Guaranteed, not production tested.
Note 5: SOT packaged parts are $100 \%$ tested at $+25^{\circ} \mathrm{C}$. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at $+25^{\circ} \mathrm{C}$.

Typical Operating Characteristics
( $\mathrm{V}+=+5 \mathrm{~V}, \mathrm{GND}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)


# Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches 

## Typical Operating Characteristics (continued)

$\left(\mathrm{V}+=+5 \mathrm{~V}, \mathrm{GND}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)


Pin Description

| PIN |  |  | MAME | FUNCTION |  |
| :---: | :---: | :---: | :---: | :---: | :--- |
| MAX4514 | MAX4515 |  |  |  |  |
| DIP/SO | SOT23-5 | DIP/SO | SOT23-5 |  |  |
| 1 | 1 | 1 | 1 | COM | Analog Switch Common Terminal |
| $2,3,5$ | - | $2,3,5$ | - | N.C. | No Connection (Not Internally Connected) |
| 4 | 5 | 4 | 5 | V+ | Positive Supply-Voltage Input (Analog and Digital) |
| 6 | 4 | 6 | 4 | IN | Digital Control Input |
| 7 | 3 | 7 | 3 | GND | Ground |
| 8 | 2 | - | - | NO | Analog Switch (Normally Open) |
| - | - | 8 | 2 | NC | Analog Switch (Normally Cosed) |

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.

# Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches 

# Applications Information <br> Power-Supply Considerations 

The MAX4514/MAX4515 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both $\mathrm{V}+$ and GND. One of these diodes conducts if any analog signal exceeds $V+$ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the $V+$ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.
There is no connection between the analog-signal paths and V+ or GND.
V+ and GND also power the internal logic and logiclevel translators. The logic-level translators convert the logic levels to switched V+ and GND signals to drive the analog signal gates.

## Logic-Level Thresholds

The logic-level thresholds are CMOS/TTL compatible when $V+$ is +5 V . As $\mathrm{V}_{+}$is raised, the level threshold increases slightly. When $\mathrm{V}+$ reaches +12 V , the level threshold is about 3.0V-above the TTL guaranteed high-level minimum of 2.8 V , but still compatible with CMOS outputs.
Do not connect the MAX4514/MAX4515's V+ to +3V and then connect the logic-level pins to logic-level signals that operate from +5 V supply. Output levels can exceed +3 V and violate the absolute maximum ratings, damaging the part and/or external circuits.

High-Frequency Performance
In $50 \Omega$ systems, signal response is reasonably flat up to 250 MHz (see Typical Operating Characteristics). Above 20 MHz , the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10 MHz , off isolation is about -45 dB in $50 \Omega$ systems, decreasing (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation decrease. Off isolation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams


Figure 1. Charge Injection

## Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches

Test Circuits/Timing Diagrams (continued)


Figure 2. Switching Times


Figure 3. Off-Isolation and On-Loss


Figure 4. NO, NC, and COM Capacitance

# Low-Voltage, Low-On-Resistance, SPST, CMOS Analog Switches 

_Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
| :--- | :--- | :--- |
| MAX4514EPA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX4514ESA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 SO |
| MAX4514EUK | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 5 SOT23-5 |
| MAX4514MJA | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 8 CERDIP** |
| MAX4515CPA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX4515CSA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 SO |
| MAX4515CUK | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 5 SOT23-5 |
| MAX4515C/D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice* |
| MAX4515EPA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX4515ESA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 SO |
| MAX4515EUK | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 5 SOT23-5 |
| MAX4515MJA | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 8 CERDIP** |

*Contact factory for dice specifications
** Contact factory for availability.

Chip Topography


TRANSISTOR COUNT: 19 SUBSTRATE IS INTERNALLY CONNECTED TO V+

Tape-and-Reel Information


Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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