19-3944; Rev 1; 5/06

EVALUATION KIT AVAILABLE

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

General Description

The MAX5088/MAX5089 high-frequency, DC-DC converters with an integrated n-channel power MOSFET provide up to 2A of load current. The MAX5088 includes an internal power MOSFET to enable the design of a nonsynchronous buck topology power supply. The MAX5089 is for the design of a synchronous buck topology power supply. These devices operate from a 4.5V to 5.5V or 5.5V to 23V input voltage and a 200kHz to 2.2MHz resistor-programmable switching frequency. The voltage-mode architecture with a peak switch current-limit scheme provides stable operation up to a 2.2MHz switching frequency. The MAX5088 includes a clock output for driving a second DC-DC converter 180° out-of-phase and a power-on-reset ($\overline{\text{RESET}}$) output. The MAX5089 includes a power-good output and a synchronous rectifier driver to drive an external low-side MOSFET in the buck converter configuration for high efficiency.

The MAX5088/MAX5089 protect against overcurrent conditions by utilizing a peak current limit as well as overtemperature shutdown providing a very reliable and compact power source for point-of-load regulation applications. Additional features include synchronization, internal digital soft-start, and an enable input. The MAX5088/MAX5089 are available in a thermally enhanced, space-saving 16-pin TQFN (5mm x 5mm) package and operate over the -40°C to +125°C temperature range.

Applications

xDSL Modem Power Supply

Automotive Radio Power Supply

Servers and Networks

IP Phones/WLAN Access Points

Selector Guide

PART	CONFIGURATION	FEATURES
MAX5088ATE	Nonsynchronous Buck	$\overline{\text{RESET}}$ Output, Clock Output
MAX5089ATE	Synchronous Buck	PGOOD Output, Synchronous FET Driver

Pin Configurations continued at end of data sheet.

Features

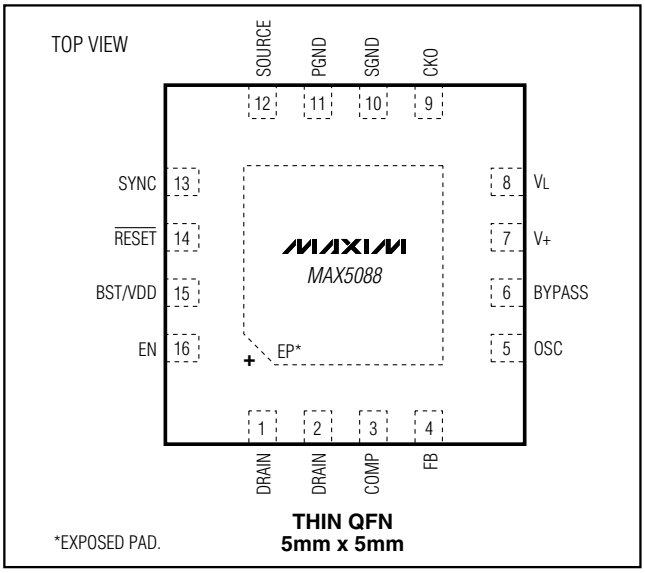
- **4.5V to 5.5V or 5.5V to 23V Input Voltage Range**
- **Output Voltage Adjustable Down to 0.6V**
- **2A Output Current**
- **Synchronous Rectifier Driver Output (MAX5089) for Higher Efficiency**
- **Resistor-Programmable Switching Frequency from 200kHz to 2.2MHz**
- **External Synchronization and Enable (On/Off) Inputs**
- **Clock Output for Driving Second Converter 180° Out-Of-Phase (MAX5089)**
- **Integrated 150mΩ High-Side n-Channel Power MOSFET**
- **Power-On Reset Output (MAX5088)/Power-Good Output (MAX5089)**
- **Short-Circuit Protection**
- **Thermal-Shutdown Protection**
- **Thermally Enhanced 16-Pin TQFN Package Dissipates 2.7W**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5088ATE+	-40°C to +125°C	16 TQFN	T1655-2
MAX5089ATE+	-40°C to +125°C	16 TQFN	T1655-2

+Denotes lead-free package.

Pin Configurations



2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

ABSOLUTE MAXIMUM RATINGS

V+ to PGND .....-0.3V to +25V
BST/VDD, DRAIN to SGND .....-0.3V to +30V
SGND to PGND .....-0.3V to +0.3V
BST/VDD to SOURCE .....-0.3V to +6V
SOURCE to SGND .....-0.6V to +25V
SOURCE or DRAIN Maximum Peak Current .....5A for 1ms
V_L to SGND .....-0.3V to the lower of +6V and (V+ + 0.3V)
SYNC, EN, DL, CKO, OSC, COMP, FB to SGND .....-0.3V to (V_L + 0.3V)
BYPASS, CKO, OSC, COMP, FB, EN, SYNC, RESET, PGOOD Maximum Input Current .....±50mA

$\overline{RESET}$, PGOOD to SGND .....-0.3V to +6V
BYPASS to SGND .....-0.3V to +2.2V
V_L and BYPASS Short-Circuit Duration to SGND .....Continuous
Continuous Power Dissipation* (T_A = +70°C)
16-Pin TQFN (derate 33mW/°C above +70°C) 2666mW
Package Thermal Resistance (junction to case) .....1.7°C/W
Operating Temperature Range .....-40°C to +125°C
Junction Temperature Range .....-65°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*As per JEDEC51 Standard (multilayer board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = V_L = 5V or V+ = 5.5V to 23V, V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Circuits of Figures 5 and 6. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V+		5.5		23.0	V
		V+ = V_L	4.5		5.5	V
V+ Operating Supply Current	I_Q	V+ = 12V, V_{FB} = 0.8V, R_{OSC} = 10kΩ, no switching		1.8	2.5	mA
V+ Standby Supply Current	I_{STBY}	V+ = 12V, V_{EN} = 0V, PGOOD (MAX5089), $\overline{RESET}$, CKO unconnected (MAX5088), R_{OSC} = 10kΩ		1	1.4	mA
Efficiency	η	Nonsynchronous (MAX5088), f_{SW} = 1.25MHz, V+ = 12V, I_{OUT} = 1.5A, V_{OUT} = 3.3V		79		%
		Synchronous (MAX5089), f_{SW} = 300kHz, V+ = 12V, I_{OUT} = 1.5A, V_{OUT} = 3.3V		90		
V_L REGULATOR (V_L)/BYPASS OUTPUT (BYPASS)						
V_L Undervoltage Lockout	V_{UVLO}	V_L falling		4.1	4.3	V
V_L Undervoltage Lockout Hysteresis	V_{HYST}			137		mV
V_L Output Voltage	V_L	V+ = 5.5V to 23V, I_{VL} = 0 to 40mA	5.0	5.2	5.5	V
BYPASS Output Voltage	V_{BYPASS}	V+ = V_L = 5.2V	1.98	2	2.02	V
BYPASS Load Regulation	ΔV_{BYPASS}	I_{BYPASS} steps from 0 to 50µA, V+ = V_L = 5.2V	0	1.2	10	mV

ELECTRICAL CHARACTERISTICS (continued)

(V+ = V_L = 5V or V+ = 5.5V to 23V, V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Circuits of Figures 5 and 6. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SOFT-START							
Digital Soft-Start Period		Internal 6-bit DAC			4096		Clock periods
Soft-Start Steps					64		Steps
ERROR AMPLIFIER (FB and COMP)							
FB to COMP Transconductance	g_M			1.20	1.8	2.75	mS
FB Input Bias Current	I_{FB}					250	nA
FB Input Voltage Set Point	V_{FB}			0.5940	0.601	0.6095	V
COMP Sink-and-Source Current Capability	I_{COMP}			100	150		µA
INTERNAL MOSFETs							
On-Resistance n-Channel Power MOSFET	R_{ON}	V+ = V_L = 5.2V, I_{SINK} = 100mA			0.150	0.302	Ω
Leakage Current	I_{LEAK}	V_{EN} = 0V, V_{DRAIN} = 23V, SOURCE = PGND				20	µA
Minimum Output Current	I_{OUT}	V_{OUT} = 3.3V, V+ = 12V (Note 2)			2		A
Current Limit	I_{LIMIT}			2.2	2.8	3.5	A
On-Resistance Internal Low-Side Switch	R_{ONLSW}	I_{SWITCH} = 50mA, V+ = V_L = 5.2V			20	38	Ω
SYNCHRONOUS RECTIFIER DRIVER (DL) (MAX5089 Only)							
On-Resistance nMOS	R_{ONDLN}	I_{SINK} = 0.1A			1	6.7	Ω
On-Resistance pMOS	R_{ONDLP}	I_{SOURCE} = 0.1A			1.9	11.1	Ω
Peak Sink Current	I_{IDL_SINK}				1		A
Peak Source Current	I_{IDL_SOURCE}				0.75		A
OSCILLATOR (OSC)/SYNCHRONIZATION (SYNC)/CLOCK OUTPUT (CKO) (MAX5088 Only)							
Clock Output-High Level	V_{CKOH}	V_L = 5.2V, I_{SOURCE} = 5mA		3.54			V
Clock Output-Low Level	V_{CKOL}	V_L = 5.2V, I_{SINK} = 5mA				0.4	V
Switching Frequency	f_{SW}	V+ = V_L = 5.2V	R_{OSC} = 5.62kΩ	1900	2100	2400	kHz
			R_{OSC} = 41.2kΩ	275	312	350	
			R_{OSC} = 10kΩ	1130	1250	1380	
Minimum Controllable On-Time	t_{ON_MIN}				120		ns
Maximum Duty Cycle	D_{MAX}	f_{SW} = 2.2MHz	MAX5088	82	87.5		%
			MAX5089	82	87.5		

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

ELECTRICAL CHARACTERISTICS (continued)

(V+ = V_L = 5V or V+ = 5.5V to 23V, V_{EN} = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Circuits of Figures 5 and 6. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Frequency Range (Note 3)	f_{SYNC}		200		2200	kHz
Sync Input to SOURCE Rising-Edge Phase Delay (Note 4)	$SYNC_{PHASE}$	R_{OSC} = 10kΩ, f_{SYNC} = 1.2MHz		65		degrees
Clock Output Phase Delay With Respect to SOURCE Waveform (Note 5)	CKO_{PHASE}	R_{OSC} = 10kΩ, SYNC = GND (MAX5088 only)		115		degrees
SYNC High Threshold	V_{SYNCH}		2.0			V
SYNC Low Threshold	V_{SYNCL}				0.8	V
Minimum SYNC High Pulse Width	t_{SYNC_H}			100		ns
EN, $\overline{RESET}$ (MAX5088)/PGOOD (MAX5089)						
EN Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
EN Input Bias Current	I_{EN}				250	nA
$\overline{RESET}$ Threshold (Note 6)	V_{TH}	V_{FB} = V_{OUT}	90	92.5	95	% V_{OUT}
PGOOD Threshold (Note 6)	V_{TH}	V_{FB} = V_{OUT}	90	92.5	95	% V_{OUT}
FB to $\overline{RESET}$ or FB to PGOOD Propagation Delay	t_{FD}			3		µs
$\overline{RESET}$ Active Timeout Period	t_{RP}		140	200	254	ms
$\overline{RESET}$, PGOOD Output Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
$\overline{RESET}$, PGOOD Output Leakage Current	I_{LEAK}	V+ = V_L = 5.2V, $V_{\overline{RESET}}$ or V_{PGOOD} = 6V, V_{FB} = 0.8V			2	µA
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SHDN}	Temperature rising		+170		°C
Thermal-Shutdown Hysteresis				25		°C

Note 1: 100% tested at +125°C. Limits over temperature are guaranteed by design.

Note 2: Output current may be limited by the power dissipation of the package. See the *Power Dissipation* section in the *Applications Information* section.

Note 3: SYNC input frequency is equal to the switching frequency.

Note 4: From the SYNC rising edge to SOURCE rising edge.

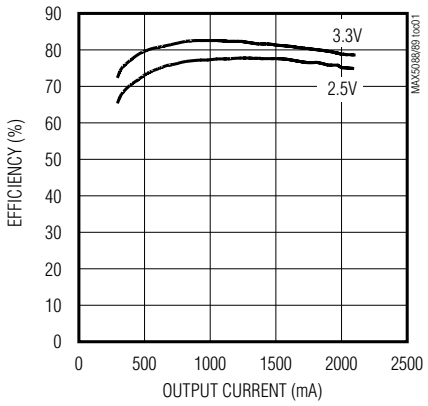
Note 5: From the rising edge of the SOURCE waveform to the rising edge of the CKO waveform.

Note 6: $\overline{RESET}$ goes high 200ms after V_{OUT} crosses this threshold, PGOOD goes high after V_{OUT} crosses this threshold.

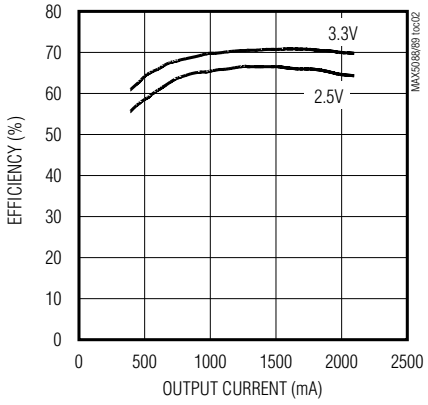
Typical Operating Characteristics

(V+ = V_L = 5.2V, T_A = +25°C, Figures 5 and 6, unless otherwise noted.)

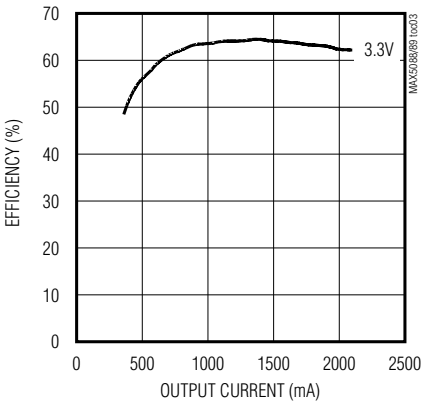
MAX5088 BUCK EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 5V, f_{SW} = 2.2MHz)



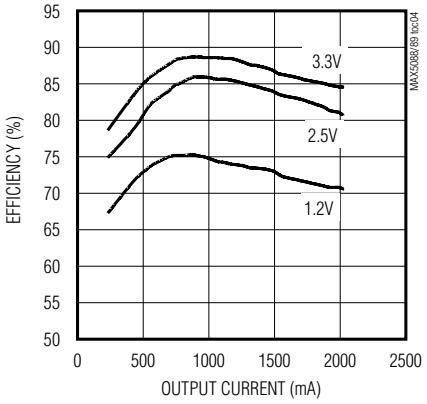
MAX5088 BUCK EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 12V, f_{SW} = 2.2MHz)



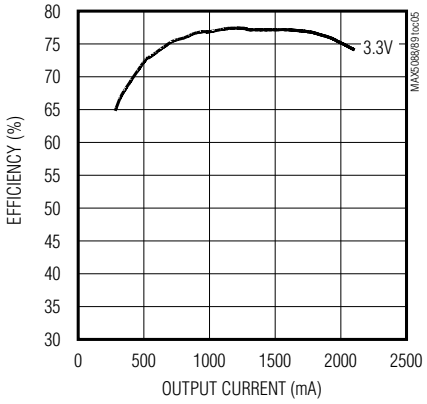
MAX5088 BUCK EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 16V, f_{SW} = 2.2MHz)



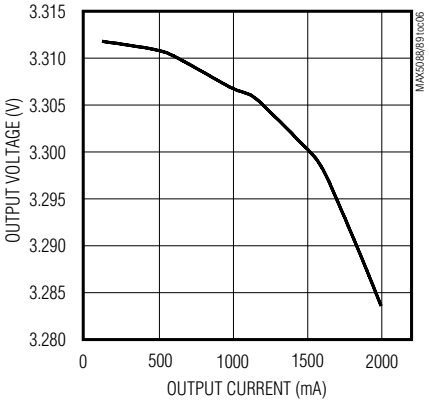
MAX5089 SYNCHRONOUS EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 12V, f_{SW} = 330kHz, L = 15µH)



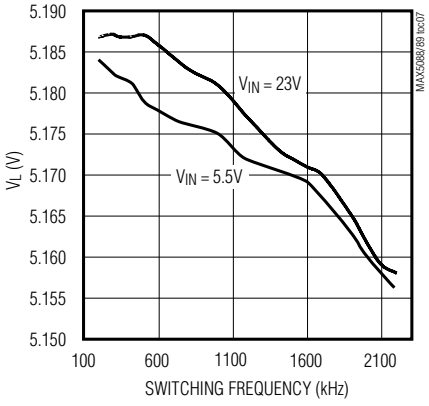
MAX5089 SYNCHRONOUS EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 12V, f_{SW} = 2.2MHz, L = 4.7µH)



MAX5089 OUTPUT VOLTAGE vs. OUTPUT CURRENT (V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 2.2MHz)



V_L OUTPUT VOLTAGE vs. SWITCHING FREQUENCY

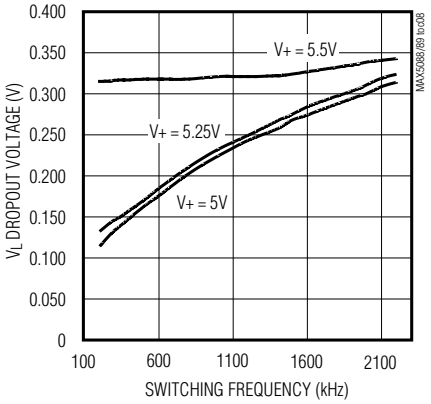


2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

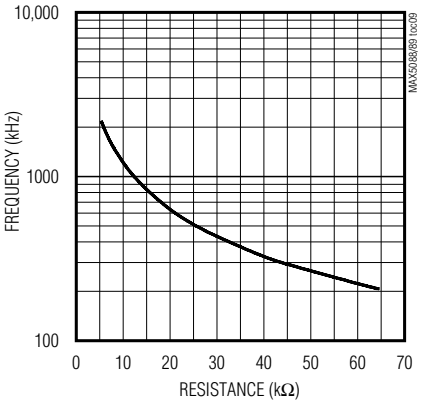
Typical Operating Characteristics (continued)

(V+ = V_L = 5.2V, T_A = +25°C, Figures 5 and 6, unless otherwise noted.)

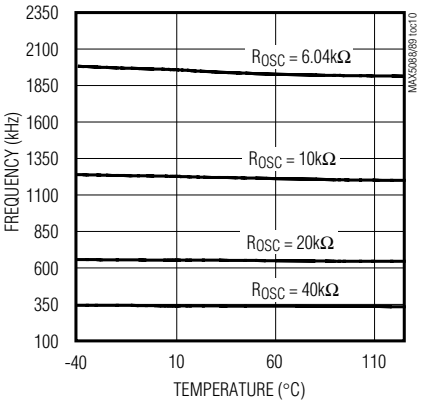
MAX5089 V_L DROPOUT VOLTAGE vs. SWITCHING FREQUENCY



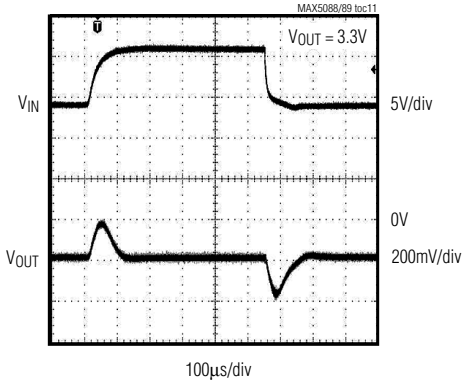
SWITCHING FREQUENCY vs. R_{OSC}



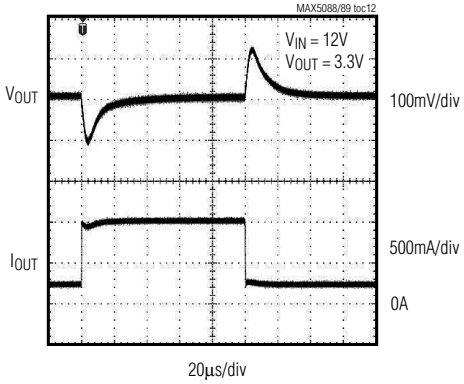
SWITCHING FREQUENCY vs. TEMPERATURE



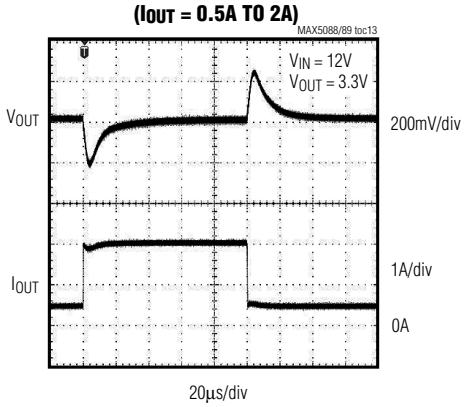
MAX5089 LINE-TRANSIENT RESPONSE (I_{OUT} = 1A, V_{IN} STEP = 14V TO 21V)



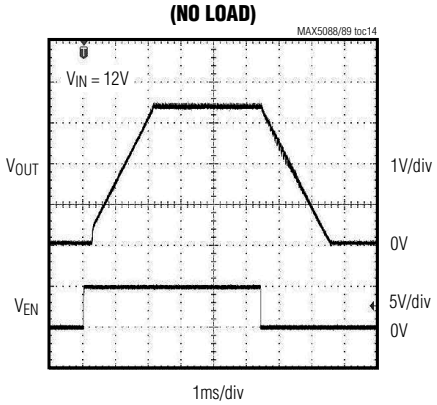
MAX5089 LOAD-TRANSIENT RESPONSE (I_{OUT} = 0.2A TO 1A)



MAX5089 LOAD-TRANSIENT RESPONSE (I_{OUT} = 0.5A TO 2A)



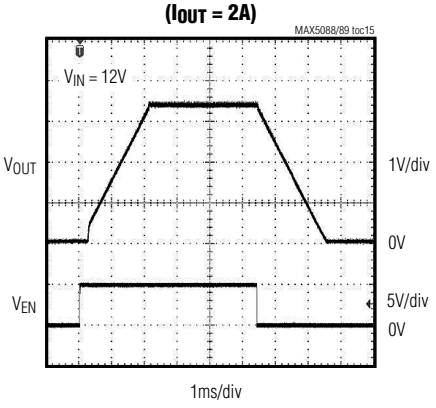
MAX5089 SOFT-START AND SHUTDOWN (NO LOAD)



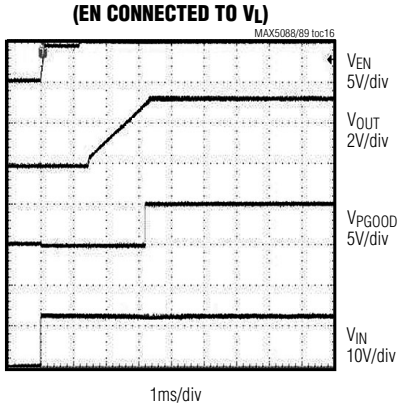
Typical Operating Characteristics (continued)

(V+ = V_L = 5.2V, T_A = +25°C, Figures 5 and 6, unless otherwise noted.)

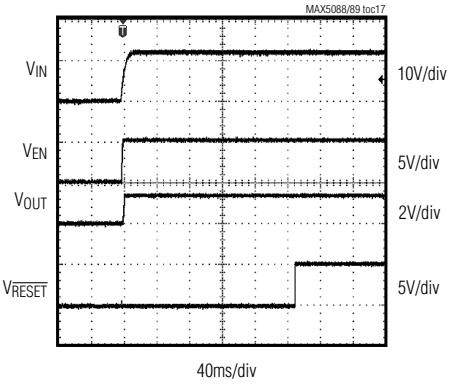
MAX5089 SOFT-START AND SHUTDOWN (I_{OUT} = 2A)



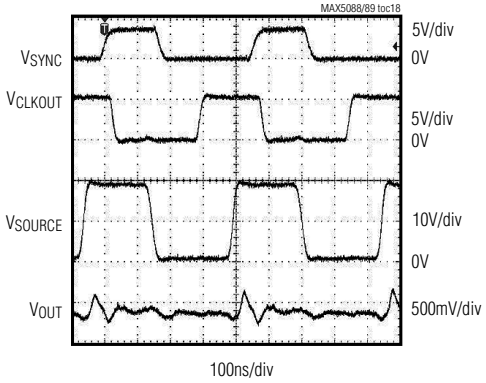
V_{IN} STARTUP WAVEFORM (EN CONNECTED TO V_L)



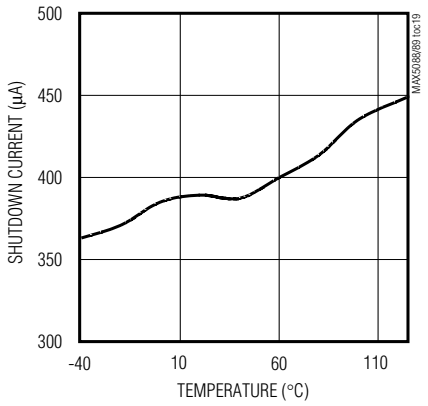
RESET TIMEOUT



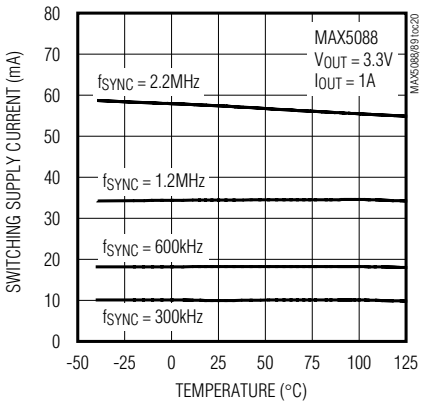
MAX5088 EXTERNALLY SYNCHRONIZED SWITCHING WAVEFORM



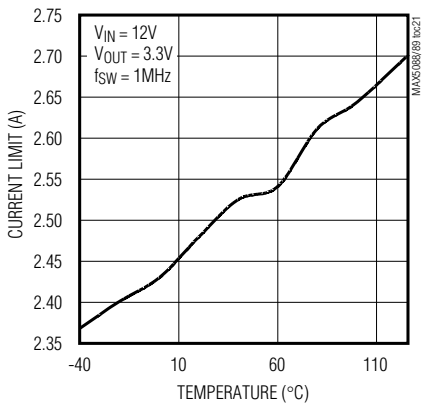
SHUTDOWN CURRENT vs. TEMPERATURE



SWITCHING SUPPLY CURRENT (I_{SW}) vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE



2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

Pin Description

PIN	NAME	FUNCTION
1, 2	DRAIN	Internal Power MOSFET Drain Connection. Use the MOSFET as a high-side switch and connect DRAIN to the input supply.
3	COMP	Transconductance Error Amplifier Output. Connect a compensation network from COMP to SGND or from COMP to FB to SGND (see the *Compensation* section).
4	FB	Feedback Input. Connect a resistive divider from the output to FB to SGND to set the output voltage.
5	OSC	Switching Frequency Set Input. Connect a resistor R_{OSC} from OSC to SGND to set the switching frequency. When using external synchronization, program R_{OSC} so that $(0.2 \times f_{SYNC}) \le f_{SW} \le (1.2 \times f_{SYNC})$. R_{OSC} is still required when external synchronization is used.
6	BYPASS	Reference Bypass Connection. Bypass to SGND with a 0.22µF or greater ceramic capacitor.
7	V+	Input Supply Voltage. V+ can range from 5.5V to 23V. Connect V+ and V_L together for 4.5V to 5.5V input operation. Bypass V+ to SGND with a minimum of 0.1µF ceramic capacitor.
8	V_L	Internal Regulator Output. Bypass V_L to SGND with a 4.7µF ceramic capacitor and to PGND with a 0.1µF ceramic capacitor. Connect V+ to V_L for 4.5V to 5.5V operation.
9	CKO	Clock Output (MAX5088 Only). CKO is an output with the same frequency as the converter's switching frequency and 115° out-of-phase. CKO is used to synchronize the MAX5088 to other MAX5088/MAX5089s.
	DL	Low-Side Synchronous Rectifier Driver (MAX5089 Only). DL sources 0.7A and sinks 1A to quickly turn on and off the external synchronous rectifier MOSFET.
10	SGND	Signal Ground
11	PGND	Power Ground. Connect the rectifier diode's anode, the input capacitor negative terminal, the output capacitor negative terminal, and V_L bypass capacitor negative terminal to PGND.
12	SOURCE	Internal Power MOSFET Source Connection. Connect SOURCE to the switched side of the inductor as shown in Figure 5.
13	SYNC	External Synchronization Input. Connect SYNC to an external logic-level clock to synchronize the MAX5088/MAX5089. Connect SYNC to SGND when not used.
14	$\overline{RESET}$	Open-Drain Active-Low Reset Output (MAX5088 Only). $\overline{RESET}$ remains low while the converter's output is below 92.5% of V_{OUT}'s nominal set point. When V_{OUT} rises above 92.5% of its nominal set point, $\overline{RESET}$ goes high after the reset timeout period of 200ms (typ).
	PGOOD	Open-Drain Power-Good Output (MAX5089 Only). PGOOD remains low while the output is below 92.5% of its nominal set point.
15	BST/VDD	Internal MOSFET Driver Supply Input. Connect BST/VDD to an external ceramic capacitor and diode (see Figure 5).
16	EN	Enable Input. A logic-low turns off the converter. A logic-high turns on the device. Connect EN to V_L for an always-on application.
—	EP	Exposed Pad. Connect to SGND. Solder EP to SGND to enhance thermal dissipation.

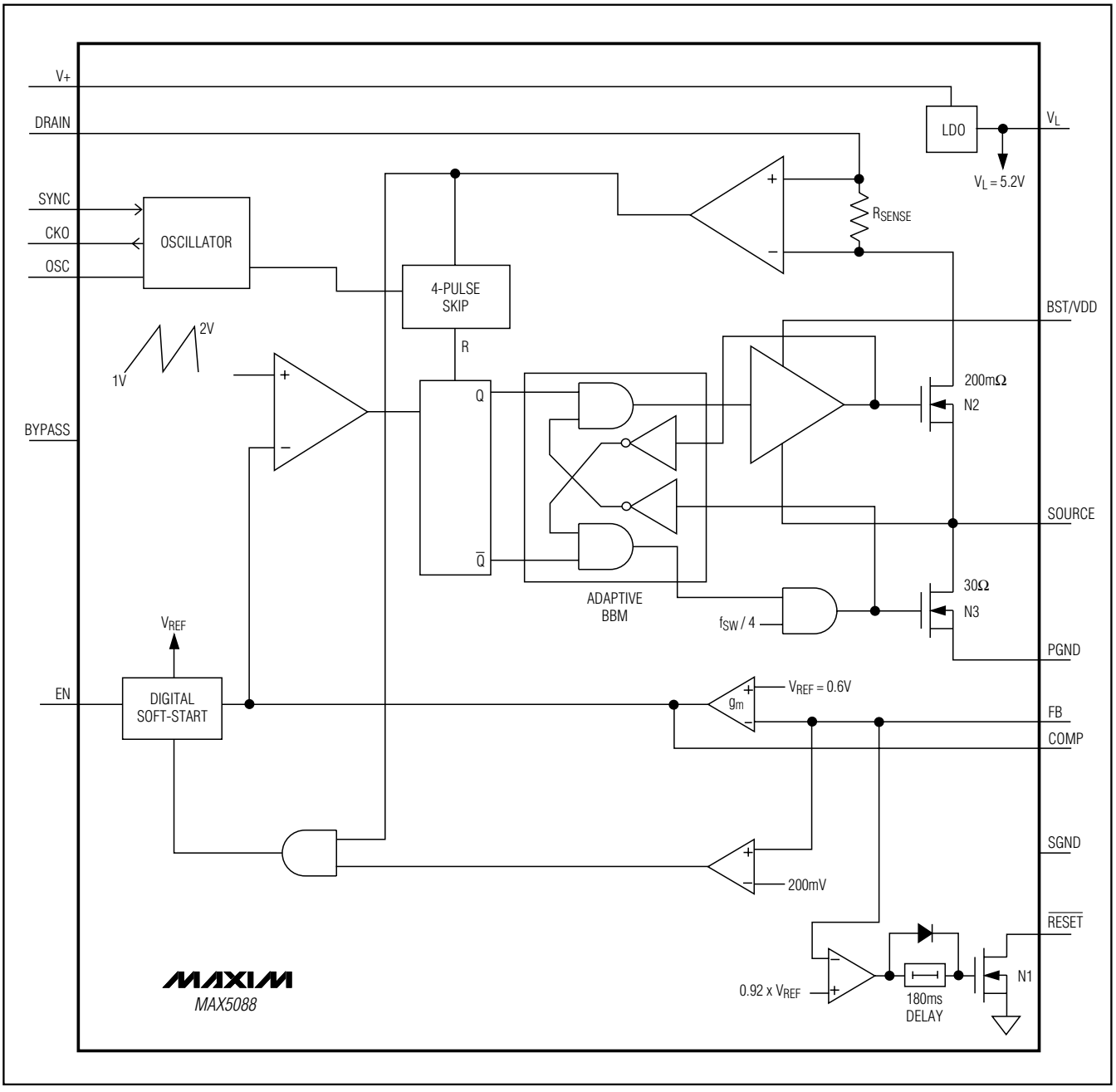


Figure 1. MAX5088 Block Diagram

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

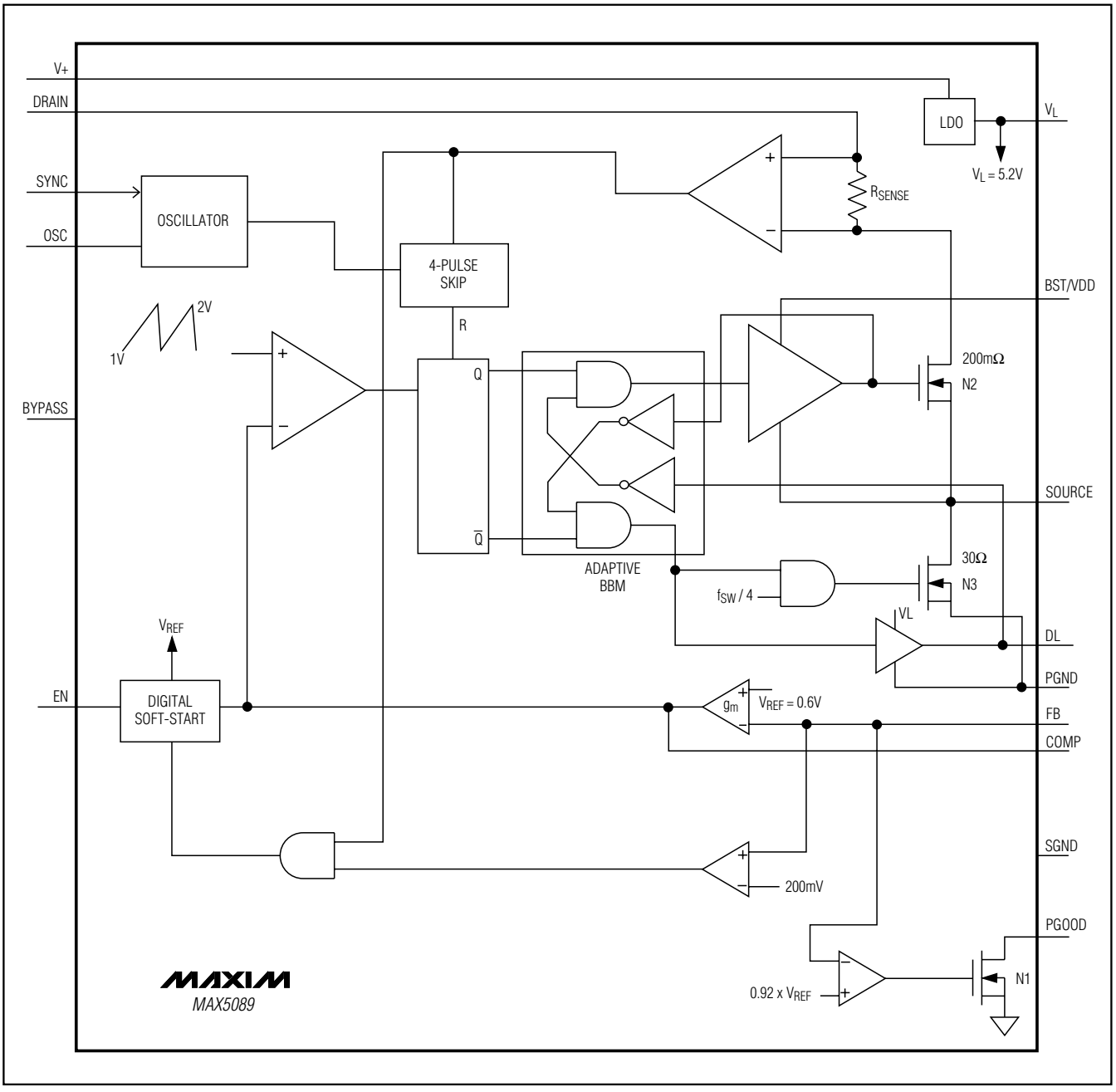


Figure 2. MAX5089 Block Diagram

Detailed Description

PWM Controller

The MAX5088/MAX5089 use a pulse-width modulation (PWM) voltage-mode control scheme. The MAX5088 is a nonsynchronous converter and uses an external low-forward-drop Schottky diode for rectification. The MAX5089 is a synchronous converter and drives a low-side, low-gate-charge MOSFET for higher efficiency. The controller generates the clock signal from an internal oscillator or the SYNC input when driven by an external clock. An internal transconductance error amplifier produces an integrated error voltage at COMP, providing high DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and an internal $1V_{P-P}$ voltage ramp. At each rising edge of the clock, the converter's high-side n-channel MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached or the maximum current limit for the switch is detected.

MAX5088

During each high-side MOSFET on-time (Figure 5), the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and forward biases the Schottky rectifier (D2 in Figure 5). During this time, the SOURCE voltage is clamped to 0.5V below ground. The inductor releases the stored energy as its current ramps down, and provides current to the output. During the MOSFET off-time, when the Schottky rectifier is conducting, the bootstrap capacitor (C10 in Figure 5) is recharged from the V_L output. At light loads, the MAX5088 goes in to discontinuous conduction mode operation when the inductor current completely discharges before the next switching cycle commences. When the MAX5088 operates in discontinuous conduction, the bootstrap capacitor can become undercharged. To prevent this, an internal low-side 30Ω switch (see N3 in Figure 1) turns on, during the off-time, once every 4 clock cycles. This ensures that the negative terminal of the bootstrap capacitor is pulled to PGND often enough to allow it to fully charge to V_L, ensuring the internal power switch properly turns on. The operation of the bootstrap capacitor wake-up switch causes a small increase in the output voltage ripple at light loads. Under overload conditions, when the inductor current exceeds the peak current limit of the internal switch, the high-side MOSFET turns off quickly and waits until the next clock cycle.

MAX5089

The MAX5089 is intended for synchronous buck operation only. During the high-side MOSFET on-time, the inductor current ramps up. When the MOSFET turns off, the inductor reverses polarity and forward biases the Schottky rectifier in parallel with the low-side synchronous MOSFET. The SOURCE voltage is clamped to 0.5V below ground until the break-before-make time (t_{BBM}) of 25ns is over. After t_{BBM}, the synchronous rectifier MOSFET turns on. The inductor releases the stored energy as its current ramps down, and continues providing current to the output. The bootstrap capacitor is also recharged from the V_L output when the MOSFET turns off. The synchronous rectifier keeps the circuit in continuous conduction mode operation even at light load. Under overload conditions, when the inductor current exceeds the peak current limit of the internal switch, the high-side MOSFET turns off and waits until the next clock cycle.

The MAX5089, with the synchronous rectifier driver output (DL), has an adaptive break-before-make circuit to avoid cross conduction between the internal power MOSFET and the external synchronous rectifier MOSFET. When the synchronous rectifier MOSFET is turning off, the internal high-side power MOSFET is kept off until V_{DL} falls below 0.97V. Similarly, DL does not go high until the internal power MOSFET gate voltage falls below 1.24V.

Input Voltage (V+)/Internal Linear Regulator (V_L)

All internal control circuitry operates from an internally regulated nominal voltage of 5.2V (V_L). At higher input voltages (V+) of 5.5V to 23V, V_L is regulated to 5.2V. At 5.5V or below, the internal linear regulator operates in dropout mode, where V_L follows V+. Depending on the load on V_L, the dropout voltage can be high enough to reduce V_L to below the undervoltage lockout (UVLO) threshold.

For input voltages of lower than 5.5V, connect V+ and V_L together. The load on V_L is proportional to the switching frequency of the converter. See the V_L Output Voltage vs. Switching Frequency graph in the *Typical Operating Characteristics*. For an input voltage higher than 5.5V, use the internal regulator.

Bypass V+ to SGND with a low-ESR 0.1µF or greater ceramic capacitor placed as close as possible to the MAX5088/MAX5089. Current spikes from V_L disturb the internal circuitry powered by V_L. Bypass V_L with a low-ESR 0.1µF ceramic capacitor to PGND and a low-ESR 4.7µF ceramic capacitor to SGND.

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

Enable

EN is an active-high input that turns the MAX5088/MAX5089 on and off. EN is a TTL logic input with 2.0V and 0.8V logic-high and low levels, respectively. When EN is asserted high, the internal digital soft-start cycle slowly ramps up the internal reference and provides a soft-start at the output. This hysteresis provides immunity to the glitches during logic turn-on of the converter. Voltage variation at EN can interrupt the soft-start sequence and can cause a latch-up. Ensure that EN remains high for at least 5ms once it is asserted. Force EN low to turn off the internal power MOSFET and cause $\overline{RESET}$ to pull low (MAX5088) or cause PGOOD to pull low (MAX5089). Connect EN to V_L when not used.

Soft-Start/Soft-Stop

The MAX5088/MAX5089 include undervoltage lockout (UVLO) with hysteresis to prevent chattering during startup. The UVLO circuit holds the MAX5088/MAX5089 off until V+ reaches 4.5V and turns the devices off when V+ falls below 4.3V. The MAX5088/MAX5089 also offer a soft-start feature, which reduces surge currents and glitches on the input during turn-on. During turn-on when the UVLO threshold is reached or EN goes from low to high, the digital soft-start ramps up the reference (V_{BYPASS}) in 64 steps. During a turn-off (by pulling EN or V+ low), the reference is reduced to zero slowly. The soft-start and soft-stop periods (t_{SS}) are 4096 cycles of the internal oscillator. To calculate the soft-start/soft-stop period use the following equation:

$$t_{SS} = \frac{4096}{f_{SW}}$$

f_{SW} is the switching frequency of the converter.

Oscillator/Synchronization (SYNC)/Clock Output (CLKOUT)

The clock frequency (or switching frequency) is generated internally and is adjustable through an external resistor connected from OSC to SGND. The relationship between R_{OSC} and f_{SW} is:

$$R_{OSC} = \frac{125 \times 10^8 \Omega/s}{f_{SW}}$$

The adjustment range for f_{SW} is from 200kHz to 2.2MHz.

Connect a logic-level clock between 200kHz to 2.2MHz at SYNC to externally synchronize the MAX5088/MAX5089's oscillator (see Figure 7). The MAX5088/MAX5089 synchronize to the rising edge of the SYNC clock. The rising edge of the SYNC clock corresponds to the turn-on edge of the internal n-channel power MOSFET with a fixed propagation delay. When operating the MAX5088/MAX5089 with an external SYNC clock, R_{OSC} must be installed. Program the internal switching frequency so that $(0.2 \times f_{SYNC}) \le f_{SW} \le (1.2 \times f_{SYNC})$. The minimum pulse width for f_{SYNC} is 100ns. Connect SYNC to SGND if synchronization is not used.

The CKO output (MAX5088 only) is a logic-level clock with the same frequency as f_{SW} and with 115° phase shift with respect to SYNC clock. Two MAX5088s can be connected in a master/slave configuration for two-phase (180°) interleaved operation. The CKO output of the master drives the SYNC input of the slave to form a dual-phase converter. To achieve the 180° out-of-phase operation, program the internal switching frequency of both converters close to each other by using the same R_{OSC} value. When synchronizing the master-slave configuration using external clock, program the internal switching frequency using R_{OSC} close to the external clock frequency (f_{SYNC}) for 180° ripple phase operation (see Figure 7). Any difference in the internal switching frequency and f_{SYNC} changes the phase delay. If both master and slave converters use the same power source, and share input bypass capacitors, the effective switching frequency at the input is twice the switching frequency of the individual converter. Higher ripple frequency at the input capacitor means a lower RMS ripple current into the capacitor.

Current Limit

The MAX5088/MAX5089 protect against output overload and short-circuit conditions when operated in a buck configuration. An internal current-sensing stage develops a voltage proportional to the instantaneous switch current. When the switch current reaches 2.8A (typ) the power MOSFET turns off and remains off until the next on cycle.

During a severe overload or short-circuit condition when the output voltage is pulled to ground the discharging slope of the inductor is V_{DS} (the voltage across the synchronous FET), or V_F (the voltage across the rectifying diode) divided by L. The short off-time does not allow the current to properly ramp down in the inductor, causing a dangerous current runaway and possibly destruction of the device. To prevent this, the MAX5088/MAX5089 include a frequency foldback feature. When the current limit is detected the frequency is reduced to 1/4th of the programmed switching frequency. When the output voltage falls below 1/3rd of its nominal set point (V_{FB} = 0.2V) the converter is turned off and soft-start cycle is initiated. This reduces the RMS current sourced by the converter during the fault condition.

At high input-to-output differential, and high switching frequency, the on-time drops to the order of 100ns. Even though the MAX5088/MAX5089 can control the on-time as low as 100ns, the internal current-limit circuit may not detect the overcurrent within this time. In that case, the output current during the fault may exceed the current limit specified in the *Electrical Characteristics* table. The MAX5088/MAX5089 may still be protected against the output short-circuit fault through the overtemperature shutdown. However, the output current may be as high as 5.5A. If the minimum on-time for a given frequency and duty cycle is less than 200ns, choose the inductor with a saturation current of greater than 5.5A.

Power-on Reset ($\overline{RESET}$) (MAX5088 Only)

$\overline{RESET}$ is an active-low open-drain output that pulls low when V_{OUT} falls below 92.5% of its nominal set point. $\overline{RESET}$ goes high impedance when V_{OUT} rises above 92.5% of its nominal set point, the soft-start period is complete, and the 200ms (typ) timeout period has elapsed. Connect a pullup resistor from $\overline{RESET}$ to a logic voltage or to V_L. The internal open-drain MOSFET at $\overline{RESET}$ can sink 3mA while providing a TTL-compatible logic-low signal. Connect $\overline{RESET}$ to SGND or leave unconnected when not used.

Power-Good (PGOOD) (MAX5089 Only)

PGOOD is an open-drain, active-high output that pulls low when V_{OUT} is below 92.5% of its nominal set point and goes high impedance when V_{OUT} goes above 92.5% its nominal set point. Connect a pullup resistor from PGOOD to a logic voltage or to V_L. PGOOD can sink up to 3mA while still providing a TTL-compatible logic-low output. Pulling EN low forces PGOOD low. Connect PGOOD to SGND or leave unconnected when not used.

Thermal-Overload Protection

During a continuous output short-circuit or overload condition, the power dissipation in the MAX5088/MAX5089 can exceed its limit. The MAX5088/MAX5089 provide an internal thermal shutdown to turn off the device when the die temperature reaches +170°C. A thermal sensor monitors the die temperature and turns the device on again when the die temperature reduces by +25°C. During thermal shutdown, the internal power MOSFET shuts off, DL pulls to SGND, V_L shuts down, $\overline{RESET}$ (MAX5088)/PGOOD (MAX5089) pulls low, and soft-start resets.

Applications Information

Setting the Switching Frequency

The controller generates the switching frequency (f_{SW}) through the internal oscillator or the signal at SYNC (f_{SYNC}), when driven by an external oscillator. The switching frequency is equal to f_{SW} or f_{SYNC}.

A resistor, R_{OSC}, from OSC to SGND sets the internal oscillator. The relationship between f_{SW} and R_{OSC} is:

$$R_{OSC} = \frac{125 \times 10^8}{f_{SW}}$$

where f_{SW} is in Hertz, and R_{OSC} is in ohms. For example, a 1.25MHz switching frequency is set with R_{OSC} = 10kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Rising clock edges on SYNC are interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by R_{OSC}. This maintains output regulation even with intermittent SYNC signals. When using an external synchronization signal, set R_{OSC} so that $(0.2 \times f_{SYNC}) \le f_{SW} \le (1.2 \times f_{SYNC})$.

Buck Converter

Use the internal n-channel power MOSFET as a high-side switch to configure the MAX5088/MAX5089 as a buck converter. In this configuration, SOURCE is connected to the inductor, DRAIN is connected to the input, and BST/VDD connects to the cathode of the bootstrap diode and capacitor. Figures 5 and 6 show the typical application circuits for MAX5088/MAX5089, respectively, in a buck configuration.

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

Effective Input Voltage Range

The MAX5088/MAX5089 can operate with input supplies ranging from 4.5V to 5.5V or 5.5V to 23V. The input voltage range (V+) can be constrained to a minimum by the duty-cycle limitations and to a maximum by the on-time limitation. The minimum input voltage is determined by:

$$V_{IN\_MIN} = \frac{V_{OUT} + V_{DROP1}}{D_{MAX}} + V_{DROP2} - V_{DROP1}$$

D_{MAX} is the maximum duty cycle of 87.5% (typ). V_{DROP1} is the total drop in the inductor discharge path that includes the diode's forward voltage drop (or the drop across the synchronous rectifier MOSFET), and the drops across the series resistance of the inductor and PC board traces. V_{DROP2} is the total drop in the inductors charging path, which includes the drop across the internal power MOSFET, and the drops across the series resistance of the inductor and PC board traces.

The maximum input voltage can be determined by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{t_{ON\_MIN} \times f_{SW}}$$

where t_{ON_MIN} = 100ns and f_{SW} is the switching frequency.

Setting the Output Voltage

For 0.6V or greater output voltages, connect a resistive divider from V_{OUT} to FB to SGND. Select the FB to SGND resistor (R2) between 1kΩ and 10kΩ and calculate the resistor from OUT to FB (R1) by the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{V_{FB}} - 1 \right]$$

where V_{FB} = 0.6V, see Figure 3.

For designs that use a Type III compensation scheme, first calculate R1 for stability requirements (see the *Compensation* section) then choose R2 so that:

$$R2 = \frac{R1 \times V_{FB}}{V_{OUT} - V_{FB}}$$

See Figure 4.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX5088/MAX5089: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value, while a lower ΔI_{P-P} requires a higher inductor value. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose ΔI_{P-P} equal to 30% of the full load current. Use the following equation to calculate the inductance:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_{P-P}}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency is set by R_{OSC} (see the *Setting the Switching Frequency* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worse at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during continuous output short-circuit. At high input-to-output differential, and high switching frequency, the on-time drops to the order of 100ns. Though the MAX5088/MAX5089 can control the on-time as low as 100ns, the internal current-limit circuit may not detect the overcurrent within this time. In that case, the output current during the fault may exceed the current limit specified in the EC table. The overtemperature shutdown protects the MAX5088/MAX5089 against the output short-circuit fault. However, the output current may reach 5.5A. Choose an inductor with a saturation current of greater than 5.5A when the minimum on-time for a given frequency and duty cycle is less than 200ns.

Input Capacitors

The discontinuous input current of the buck converter causes large input ripple current. The switching frequency, peak inductor current, and the allowable peak-to-peak input voltage ripple dictate the input capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio yielding a lower input capacitance requirement.

The input ripple comprises mainly of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume the input voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

$$ESR = \frac{\Delta V_{ESR}}{\left(I_{OUT} + \frac{\Delta I_{P-P}}{2}\right)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Output Capacitors

The allowable output voltage ripple and the maximum deviation of the output voltage during step load currents determine the output capacitance and its ESR.

The output ripple comprises of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use the ESR_{OUT} equation to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output voltage ripple.

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$V_{OUT\_RIPPLE} \cong \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above and f_{SW} is the individual converter's switching frequency.

The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step load current until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The high switching frequency of MAX5088/MAX5089 allows for a higher closed-loop bandwidth, thus reducing $t_{RESPONSE}$ and the output capacitance requirement. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output voltage deviation below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the controller. The controller response time depends on the control-loop bandwidth.

Power Dissipation

The MAX5088/MAX5089 are available in thermally enhanced 16-pin, 5mm x 5mm TQFN packages that dissipate up to 2.7W at T_A = +70°C. When the die temperature reaches +170°C, the MAX5088/MAX5089 shut down (see the *Thermal-Overload Protection* section). The power dissipated in the device is the sum of the power dissipated from supply current (P_Q), power dissipated due to switching the internal power MOSFET (P_{SW}), and the power dissipated due to the RMS cur-

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

rent through the internal power MOSFET (P_{MOSFET}). The total power dissipated in the package must be limited so the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature. Calculate the power lost in the MAX5088/MAX5089 using the following equations:

The power dissipated in the switch is:

$$P_{MOSFET} = I_{RMS\_MOSFET} \times R_{ON}$$

where:

$$I_{RMS\_MOSFET} = \sqrt{(I_{OUT}^2 \times D) + \left(\frac{\Delta I_{P-P}^2 \times D}{12}\right)}$$

ΔI_{P-P} is the peak-to-peak inductor current ripple.

The power lost due to switching the internal power MOSFET is:

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{4}$$

t_R and t_F are the rise and fall times of the internal power MOSFET measured at SOURCE.

The power lost due to the switching quiescent current of the device is:

$$P_Q = V_{IN} \times I_{SW} \quad \text{(MAX5088)}$$

The switching quiescent current (I_{SW}) of the MAX5088/MAX5089 is dependent on switching frequency. See the *Typical Operating Characteristics* section for the value of I_{SW} at a given frequency.

In the case of the MAX5089, the switching current includes the synchronous rectifier MOSFET gate-drive current (I_{SW-DL}). The I_{SW-DL} depends on the total gate charge (Q_{g-DL}) of the synchronous rectifier MOSFET and the switching frequency.

$$P_Q = V_{IN} \times (I_{SW} + I_{SW-DL}) \quad \text{(MAX5089)}$$

$$I_{SW-DL} = Q_{g-DL} \times f_{SW}$$

where the Q_{g-DL} is the total gate charge of the synchronous rectifier MOSFET at V_{GS} = 5V.

The total power dissipated in the device is:

$$P_{TOTAL} = P_{MOSFET} + P_{SW} + P_Q$$

Calculate the temperature rise of the die using the following equation:

$$T_J = T_C + (P_{TOTAL} \times \theta_{JC})$$

θ_{JC} is the junction-to-case thermal resistance equal to 1.7°C/W. T_C is the temperature of the case and T_J is the junction temperature, or die temperature. The case-to-ambient thermal resistance is dependent on how well heat can be transferred from the PC board to the air. Solder the underside exposed pad to a large copper GND plane. If the die temperature reaches +170°C the MAX5088/MAX5089 shut down and do not restart again until the die temperature cools by 25°C.

Compensation

The MAX5088/MAX5089 have an internal transconductance error amplifier with an inverting input (FB) and output (COMP) available for external frequency compensation. The flexibility of external compensation and high switching frequencies for the MAX5088/MAX5089 allow a wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use high-ESR aluminum electrolytic capacitors. For size sensitive applications, use low-ESR tantalum or ceramic capacitors at the output.

Before designing the compensation components, first choose all the passive power components that meet the output ripple, component size, and component cost requirements. Secondly, choose the compensation components to achieve the desired closed-loop bandwidth and phase margin. Use a simple 1-zero, 2-pole pair (Type II) compensation if the output capacitor ESR zero frequency (f_{ZESR}) is below the unity-gain crossover frequency (f_C). Use a 2-zero, 2-pole (Type III) compensation when the f_{ZESR} is higher than f_C.

Use procedure 1 to calculate the compensation network components when $f_{ZESR} < f_C$.

Procedure 1 (see Figure 3)

Calculate the f_{ZESR} and f_{LC} double pole:

$$f_{ZESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

Calculate the unity-gain crossover frequency as:

$$f_C = \frac{f_{SW}}{20}$$

If f_{ZESR} is lower than f_C and close to f_{LC}, use a Type II compensation network where R_FC_F provides a midband zero ($f_{mid,zero}$) and R_FC_{CF} provides a high-frequency pole.

Calculate the modulator gain (G_M) at the crossover frequency.

$$G_M = \frac{V_{IN}}{V_{OSC}} \times \frac{ESR}{ESR + (2\pi \times f_C \times L)} \times \frac{V_{FB}}{V_{OUT}}$$

where V_{OSC} is the $1V_{P-P}$ ramp amplitude and V_{FB} = 0.6V.

The transconductance error amplifier gain at f_C is:

$$G_{E/A} = g_m \times R_F$$

The total loop gain at f_C should be equal to 1:

$$G_M = G_{E/A} = 1$$

or

$$R_F = \frac{V_{OSC}\,(ESR + 2\pi \times f_C \times L)V_{OUT}}{V_{FB} \times V_{IN} \times g_m \times ESR}$$

Place a zero at or below the LC double pole:

$$C_F = \frac{1}{2\pi \times R_F \times f_{LC}}$$

Place a high-frequency pole at $f_P = 0.5 \times f_{SW}$. Therefore C_{CF} is:

$$C_{CF} = \frac{1}{\pi \times R_F \times f_{SW}}$$

Procedure 2 (see Figure 4)

When using a low-ESR ceramic-type capacitor as the output capacitor, the ESR frequency is much higher than the targeted unity-gain crossover frequency (f_C). In this case, Type III compensation is recommended. Type III compensation provides a low-frequency pole (≈DC) and two pole-zero pairs. The locations of the zero and poles should be such that the phase margin peaks at f_C.

$\frac{f_C}{f_Z} = \frac{f_P}{f_C} = 5$ The is a good number to get approximately 60° of phase margin at f_C. However, it is important to place the two zeros at or below the double pole to avoid conditional stability.

First, select the crossover frequency so that:

$$f_C \le \frac{f_{SW}}{20}$$

Calculate the LC double-pole frequency, f_{LC}:

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

$$\text{Place a zero } f_Z = \frac{1}{2\pi \times R_F \times C_F} \text{ at } 0.75 \times f_{LC}$$

where:

$$C_F = \frac{1}{2\pi \times 0.75 \times f_{LC} \times R_F}$$

with $R_F \ge 10k\Omega$.

Calculate C_A for a target unity crossover frequency, f_C:

$$C_A = \frac{2\pi \times f_C \times L \times C_{OUT} \times V_{OSC}}{V_{IN} \times R_F}$$

$$\text{Place a pole } (f_{P1} = \frac{1}{2\pi \times R_A \times C_A}) \text{ at } f_{ZESR}.$$

$$R_A = \frac{1}{2\pi \times f_{ZESR} \times C_A}$$

Place a second zero, f_{Z2}, at 0.2 x f_C or at f_{LC}, whichever is lower.

$$R_1 = \frac{1}{2\pi \times f_{Z2} \times C_A} - R_A$$

$$\text{Place a second pole } (f_{P2} = \frac{1}{2\pi \times R_F \times C_{CF}})$$

at 1/2 the switching frequency.

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F) - 1}$$

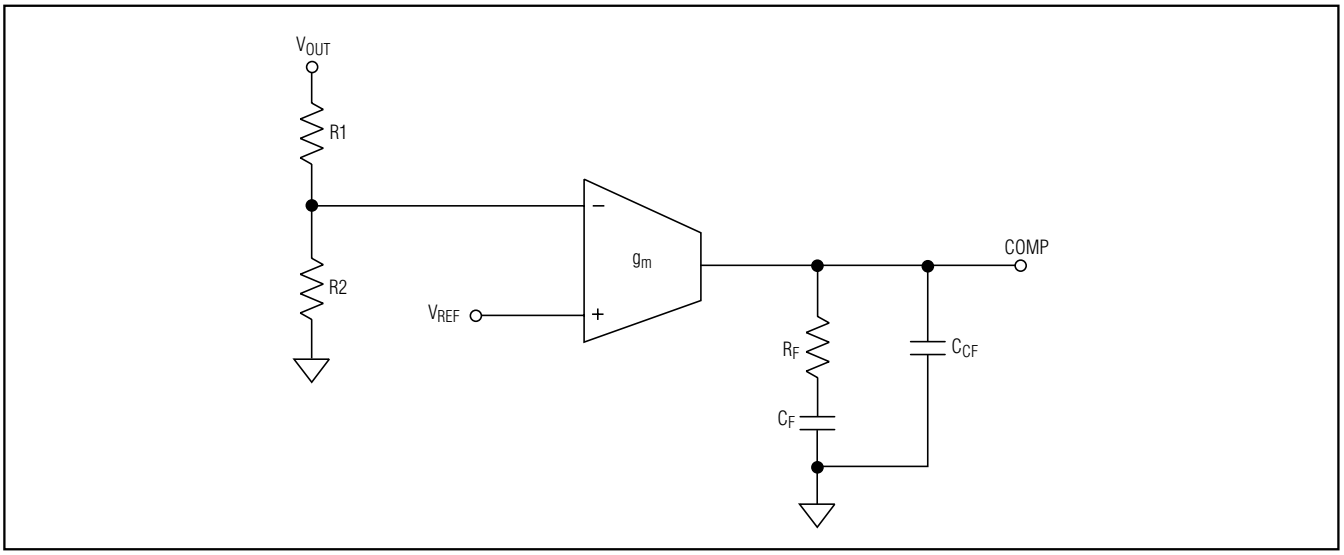


Figure 3. Type II Compensation Network

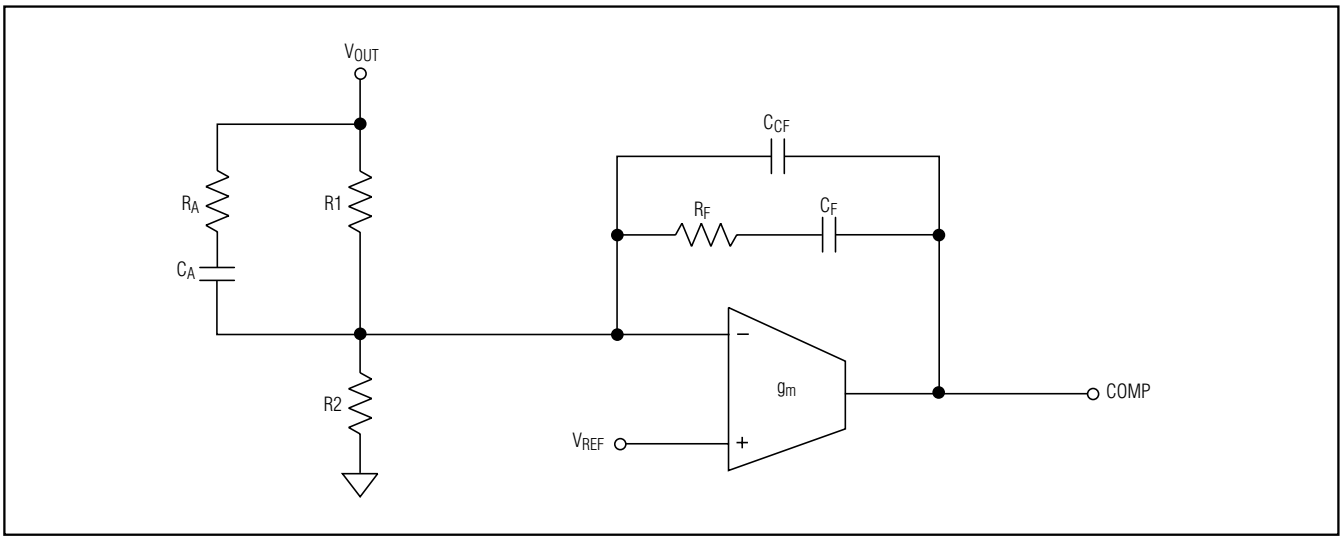


Figure 4. Type III Compensation Network

Improving Noise Immunity

When using the MAX5088/MAX5089 in noisy environments, adjust the controller's compensation to improve the system's noise immunity. In particular, high-frequency noise coupled into the feedback loop causes duty-cycle jitter. One solution is to lower the crossover frequency (see the *Compensation* section).

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low-switching power losses and clean stable operation. Use a multilayer board whenever possible for better noise immunity. Follow these guidelines for good PC board layout:

1) Solder the exposed pad to a large copper plane under the IC. To effectively use this copper area as a heat exchanger between the PC board and the ambient, expose this copper area on the top and bottom side of the PC board. Do not make a direct connection of the exposed pad copper plane to the SGND (Pin 10) underneath the IC. Connect this plane and SGND together at the return terminal of the V+ bypass capacitor
2) Isolate the power components and high-current paths from sensitive analog circuitry.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
4) Connect SGND and PGND together close to the return terminals of the V_L and V+ high-frequency bypass capacitors near the IC. Do not connect them together anywhere else.
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PC boards to enhance full-load efficiency and power dissipation capability.
6) Ensure that the feedback connection from FB to C_{OUT} is short and direct.
7) Route high-speed switching nodes (BST/VDD, SOURCE) away from the sensitive analog areas (BYPASS, COMP, FB, and OSC). Use internal PC board layers for SGND as EMI shields to keep radiated noise away from the IC, feedback dividers, and the analog bypass capacitors.

Layout Procedure

1) Place the power components (inductor, C_{IN}, and C_{OUT}) first, with ground terminals close to each other. Make all these connections on the top layer with wide, copper-filled areas (2oz copper recommended).
2) Group the gate-drive components (boost diodes and capacitors, and V_L bypass capacitor) together near the controller IC.
3) Make the ground connections as follows:
   a) Create a small-signal ground plane underneath the IC.
   b) Connect this plane to SGND and use this plane for the ground connection for BYPASS, COMP, FB, and OSC.
   c) Connect SGND and PGND together at the return terminal of V+ and V_L bypass capacitors near the IC. Make this the only connection between SGND and PGND.

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

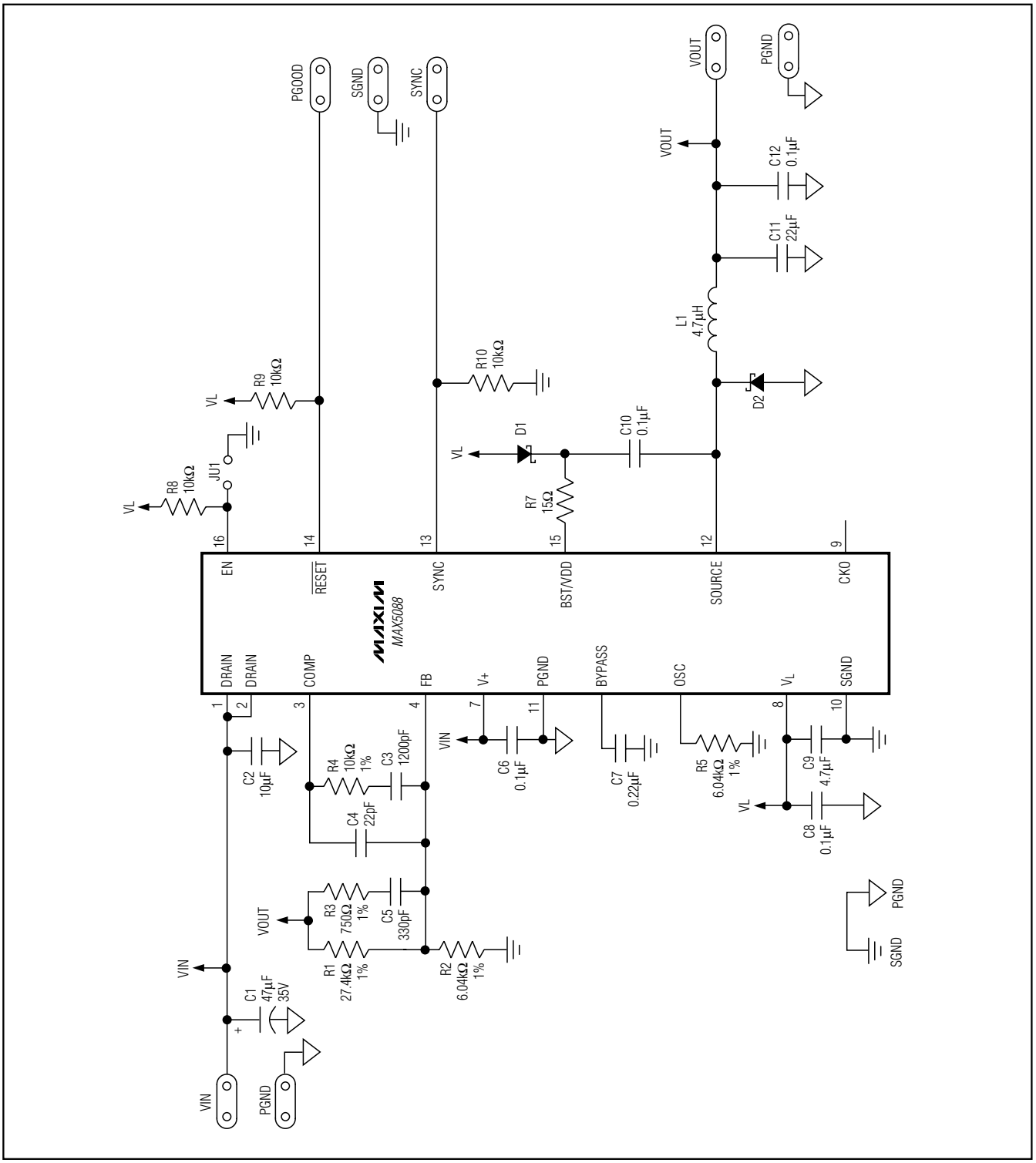


Figure 5. MAX5088 Buck Configuration

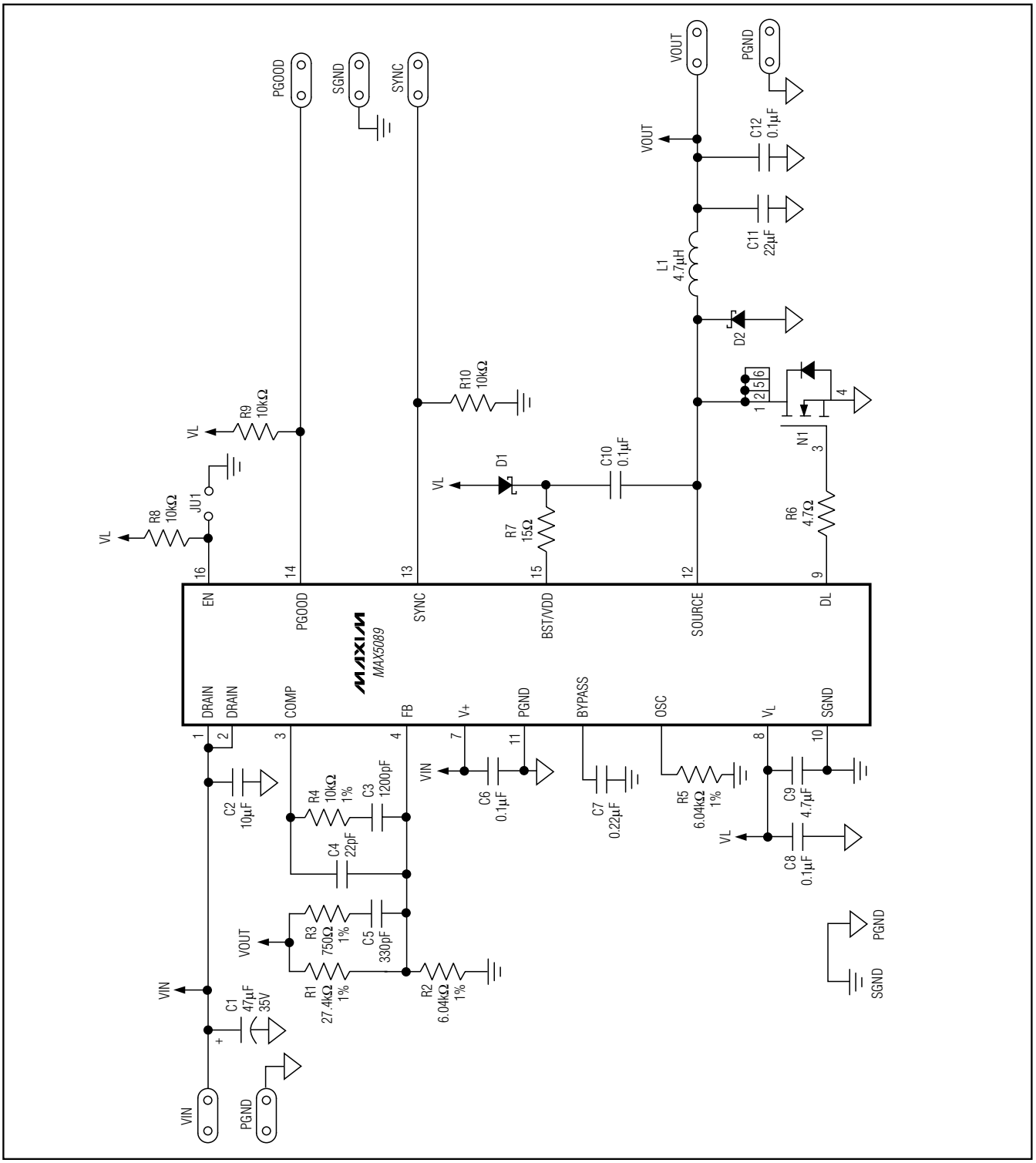


Figure 6. MAX5089 Buck Configuration

2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

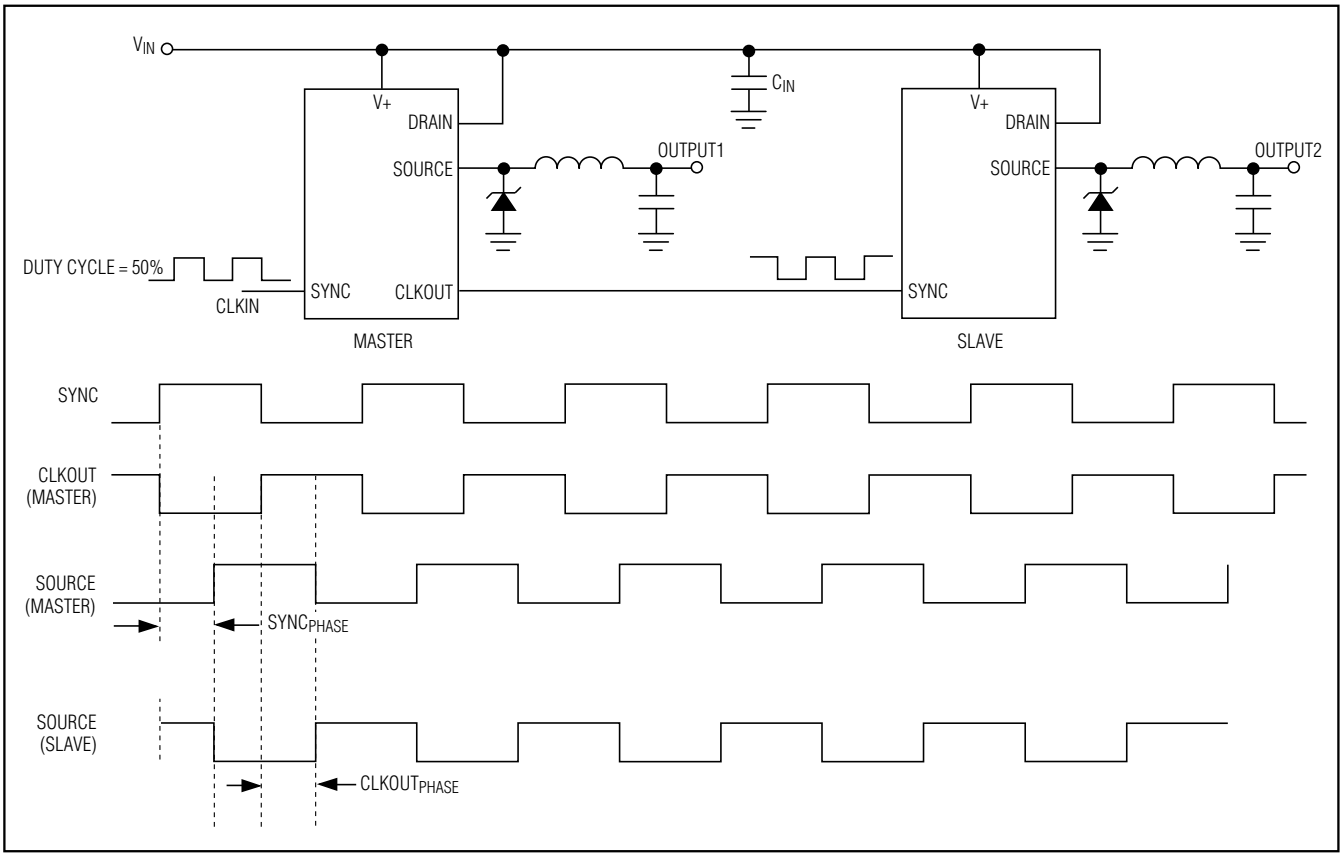
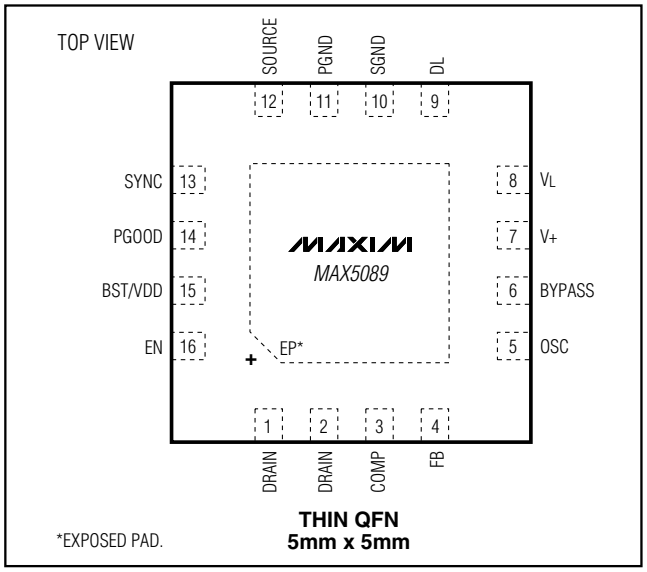


Figure 7. Synchronized Converters

Pin Configurations (continued)

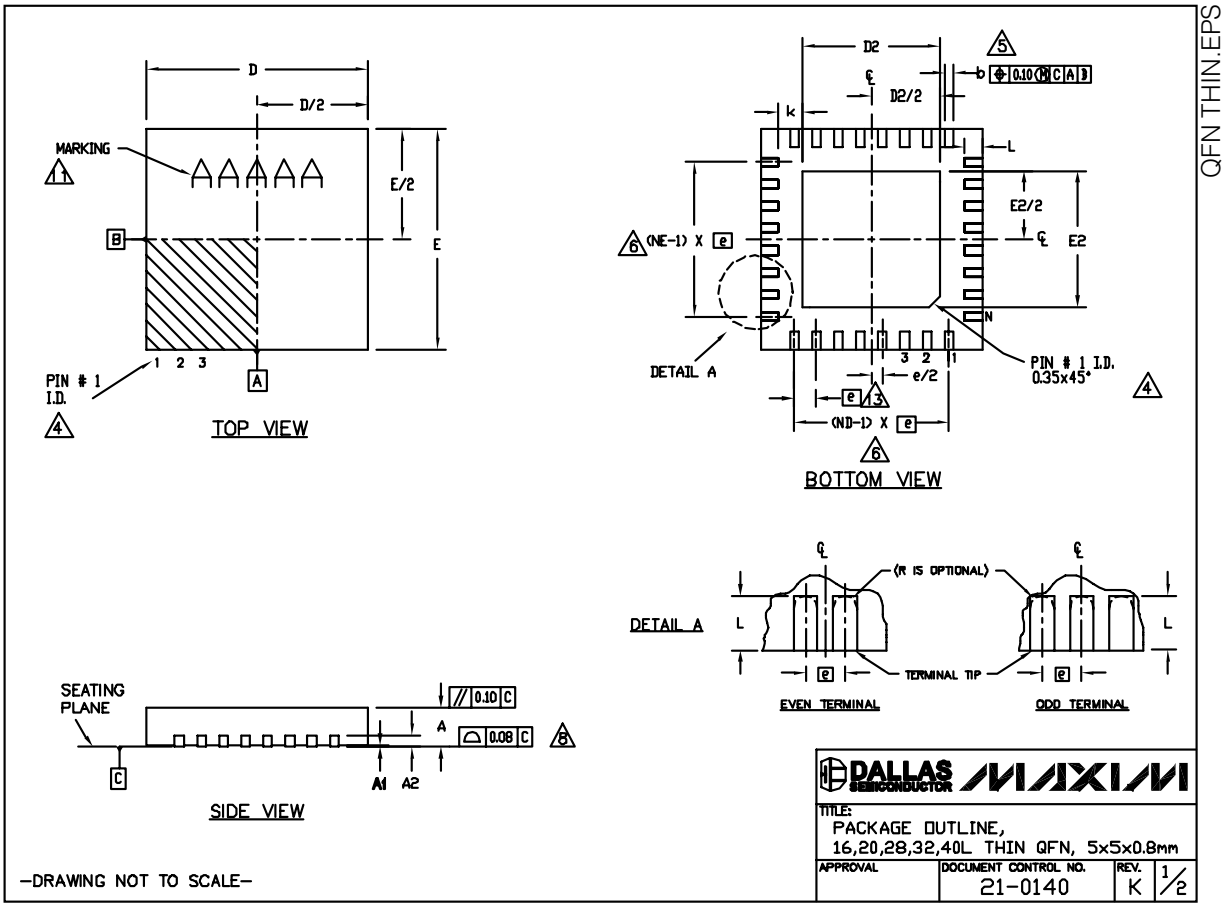


Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	K	1/2