MAXIM

315MHz/433MHz ASK Superheterodyne Receiver with AGC Lock

MAX7033

General Description

The MAX7033 fully integrated low-power CMOS superheterodyne receiver is ideal for receiving amplitude-shift-keyed (ASK) data in the 300MHz to 450MHz frequency range. The receiver has an RF input signal range of -114dBm to 0dBm. With few external components and a low-current power-down mode, it is ideal for cost-sensitive and power-sensitive applications typical in the automotive and consumer markets. The MAX7033 consists of a low-noise amplifier (LNA), a fully differential image-rejection mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO), a 10.7MHz IF limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data-recovery circuitry. The MAX7033 also has a discrete one-step automatic gain control (AGC) that reduces the LNA gain by 35dB when the RF input signal exceeds -62dBm. The AGC circuitry offers an externally controlled hold feature.

The MAX7033 is available in a 28-pin TSSOP package and is specified over the extended (-40°C to +105°C) temperature range.

Applications

Automotive Remote Keyless Entry

Security Systems

Garage Door Openers

Home Automation

Remote Controls

Local Telemetry

Wireless Sensors

Typical Application Circuit appears at end of data sheet.

Features

♦ **Optimized for 315MHz or 433MHz Band**

♦ **Operates from Single +3.3V or +5.0V Supplies**

♦ **High Dynamic Range with On-Chip AGC**

♦ **AGC Hold Circuit**

♦ **1ms AGC Release Time**

♦ **Selectable Image-Rejection Center Frequency**

♦ **Selectable x64 or x32 f_{LO}/f_{XTAL} Ratio**

♦ **Low 5.2mA Operating Supply Current**

♦ **<3.5µA Low-Current Power-Down Mode for Efficient Power Cycling**

♦ **250µs Startup Time**

♦ **Built-In 44dB RF Image Rejection**

♦ **Better than -114dBm Receive Sensitivity**
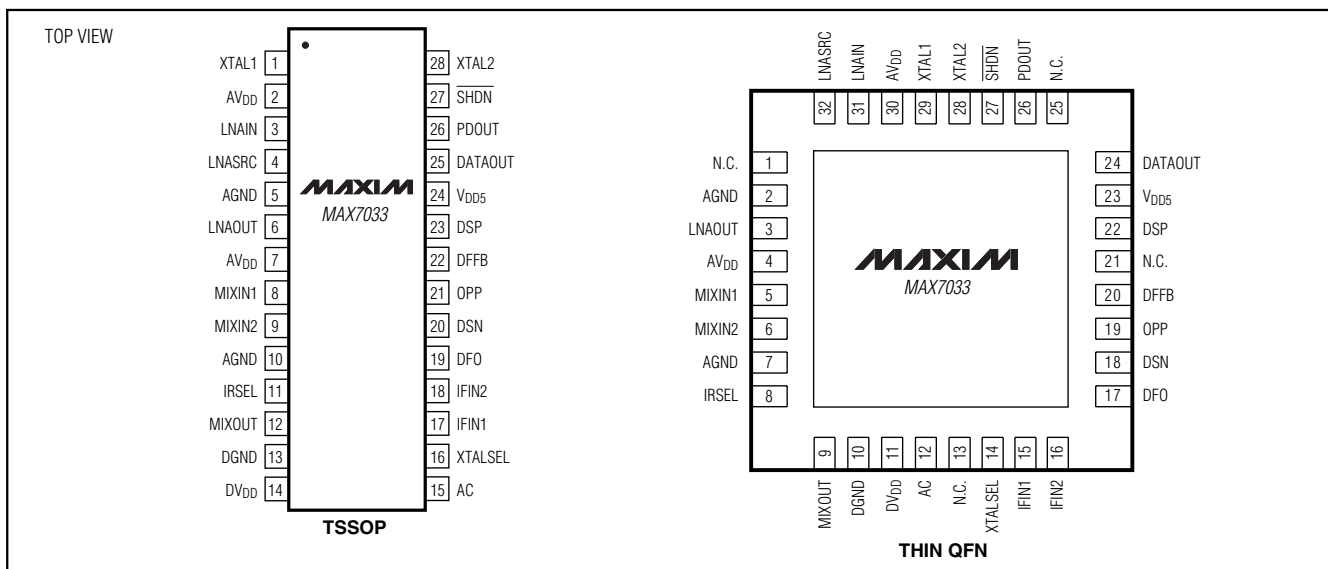
♦ **-40°C to +105°C Operation**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7033EUI	-40°C to +105°C	28 TSSOP
MAX7033ETJ*	-40°C to +105°C	32 Thin QFN-EP**

Future product—contact factory for availability.

**EP = Exposed paddle.*

Pin Configurations

TOP VIEW

TSSOP

XTAL1	1		28	XTAL2
AV_DD	2		27	SHDN
LNAIN	3		26	PDOUT
LNASRC	4		25	DATAOUT
AGND	5		24	V_DD5
LNAOUT	6		23	DSP
AV_DD	7		22	DFFB
MIXIN1	8		21	OPP
MIXIN2	9		20	DSN
AGND	10		19	DFO
IRSEL	11		18	IFIN2
MIXOUT	12		17	IFIN1
DGND	13		16	XTALSEL
DV_DD	14		15	AC

THIN QFN

MAXIM _____ **Maxim Integrated Products** 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX7033

ABSOLUTE MAXIMUM RATINGS

V_{DD5} to AGND...-0.3V to +6.0V
AV_{DD} to AGND...-0.3V to +4.0V
DV_{DD} to DGND...-0.3V to +4.0V
AGND to DGND...-0.1V to +0.1V
IRSEL, DATAOUT, XTALSEL,
   AC, $\overline{SHDN}$ to AGND ....-0.3V to (V_{DD5} + 0.3V)
All Other Pins to AGND............................-0.3V to (DV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
   28-Pin TSSOP (derate 12.8mW/°C above +70°C) ..1025.6mW
   32-Thin QFN (derate 21.3mW/°C above +70°C) 1702.1mW
Operating Temperature Range ....-40°C to +105°C
Junction Temperature...+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (+3.3V OPERATION)

(*Typical Application Circuit*, AV_{DD} = DV_{DD} = V_{DD5} = +3.0V to +3.6V, no RF signal applied, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at AV_{DD} = DV_{DD} = V_{DD5} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	AV_{DD}, DV_{DD}	+3.3V nominal supply voltage		3.0	3.3	3.6	V
Supply Current	I_{DD}	$V_{\overline{SHDN}}$ = DV_{DD}	f_{RF} = 315MHz		5.2	6.23	mA
			f_{RF} = 433MHz		5.7	6.88	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V, $V_{XTALSEL}$ = 0V	f_{RF} = 315MHz		2.6		µA
			f_{RF} = 433MHz		3.5	8.0	
Input-Voltage Low	V_{IL}					0.4	V
Input-Voltage High	V_{IH}			DV_{DD} - 0.4			V
Input Logic Current High	I_{IH}					10	µA
Image-Reject Select Voltage (Note 2)		f_{RF} = 433MHz, V_{IRSEL} = V_{DD5}		V_{DD5} - 0.4			V
		f_{RF} = 375MHz, V_{IRSEL} = V_{DD5} / 2		1.1		V_{DD5} - 1.0	
		f_{RF} = 315MHz, V_{IRSEL} = 0V				0.4	
DATAOUT Output-Voltage Low	V_{OL}	I_{SINK} = 10µA				0.125	V
DATAOUT Output-Voltage High	V_{OH}	I_{SOURCE} = 10µA		DV_{DD} - 0.125			V

DC ELECTRICAL CHARACTERISTICS (+5.0V OPERATION)

(*Typical Application Circuit*, V_{DD5} = +4.5V to +5.5V, no RF signal applied, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD5} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD5}	+5.0V nominal supply voltage		4.5	5.0	5.5	V
Supply Current	I_{DD}	$V_{\overline{SHDN}}$ = V_{DD5}	f_{RF} = 315MHz		5.2	6.4	mA
			f_{RF} = 433MHz		5.7	6.76	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V, $V_{XTALSEL}$ = 0V	f_{RF} = 315MHz		3.7		µA
			f_{RF} = 433MHz		4.2	9.0	
Input-Voltage Low	V_{IL}					0.4	V

**MAXIM**

315MHz/433MHz ASK Superheterodyne Receiver with AGC Lock

DC ELECTRICAL CHARACTERISTICS (+5.0V OPERATION) (continued)

(*Typical Application Circuit*, V_{DD5} = +4.5V to +5.5V, no RF signal applied, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DD5} = +5.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Voltage High	V_{IH}		V_{DD5} - 0.4			V
Input Logic Current High	I_{IH}			15		µA
Image-Reject Select Voltage (Note 2)		f_{RF} = 433MHz, V_{IRSEL} = V_{DD5}	V_{DD5} - 0.4			V
		f_{RF} = 375MHz, V_{IRSEL} = V_{DD5} / 2	1.1		V_{DD5} - 1.5	
		f_{RF} = 315MHz, V_{IRSEL} = 0V			0.4	
DATAOUT Output-Voltage Low	V_{OL}	I_{SINK} = 10µA		0.125		V
DATAOUT Output-Voltage High	V_{OH}	I_{SOURCE} = 10µA	V_{DD5} - 0.125			V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, AV_{DD} = DV_{DD} = V_{DD5} = +3.0V to +3.6V, all RF inputs are referenced to 50Ω, f_{RF} = 315MHz, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at AV_{DD} = DV_{DD} = V_{DD5} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Startup Time	t_{ON}	Time for valid signal detection after $V_{\overline{SHDN}}$ = DV_{DD}			250		µs
Receiver Input Frequency	f_{RF}			300		450	MHz
Maximum Receiver Input Level		Modulation depth >18dB			0		dBm
Sensitivity (Note 3)		Average carrier power level			-120		dBm
		Peak power level			-114		
AGC Hysteresis		LNA gain from low to high			8		dB
		Switching time from low to high gain			1		ms
Maximum Data Rate		Manchester coded			33		kbps
		NRZ coded			66		
LNA IN HIGH-GAIN MODE							
Input Impedance	Z_{IN_LNA}	Normalized to 50Ω	f_{RF} = 433MHz		1 - j3.4		
			f_{RF} = 375MHz		1 - j3.9		
			f_{RF} = 315MHz		1 - j4.7		
1dB Compression Point	P1dB$_{LNA}$				-22		dBm
Input-Referred 3rd-Order Intercept	IIP3$_{LNA}$				-12		dBm
LO Signal Feedthrough to Antenna					-80		dBm
Output Impedance	Z_{OUT_LNA}	Normalized to 50Ω			0.12 - j4.4		
Noise Figure	NF$_{LNA}$				3		dB

315MHz/433MHz ASK Superheterodyne Receiver with AGC Lock
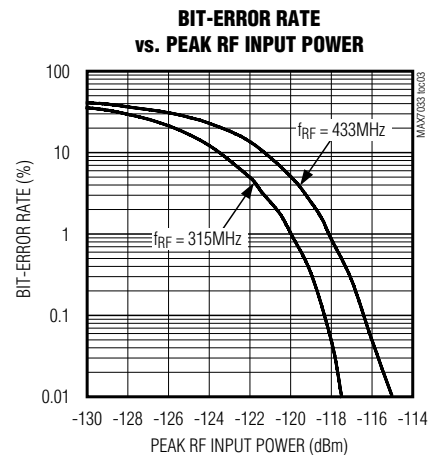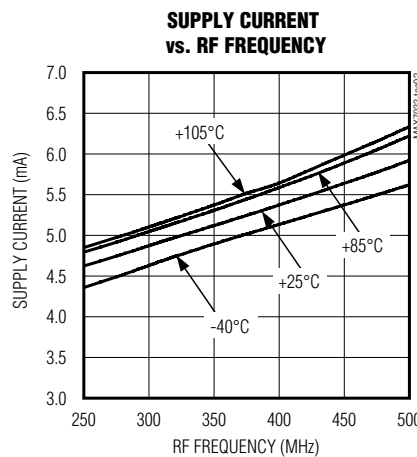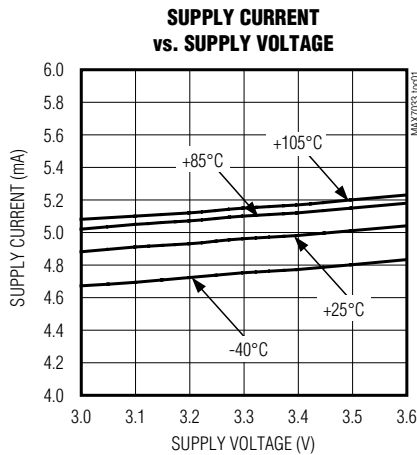
AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, AV_{DD} = DV_{DD} = V_{DD5} = +3.0V to +3.6V, all RF inputs are referenced to 50Ω, f_{RF} = 315MHz, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at AV_{DD} = DV_{DD} = V_{DD5} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LNA IN LOW-GAIN MODE							
Input Impedance	Z_{IN_LNA}	Normalized to 50Ω (Note 4)	f_{RF} = 433MHz		1 - j3.4		
			f_{RF} = 375MHz		1 - j3.9		
			f_{RF} = 315MHz		1 - j4.7		
1dB Compression Point	$P1dB_{LNA}$				-10		dBm
Input-Referred 3rd-Order Intercept	$IIP3_{LNA}$				-7		dBm
LO Signal Feedthrough to Antenna					-80		dBm
Output Impedance	Z_{OUT_LNA}	Normalized to 50Ω			0.4		
Noise Figure	NF_{LNA}				3		dB
Voltage-Gain Reduction		AGC enabled (depends on tank Q)			35		dB
MIXER							
Input Impedance	Z_{IN_MIX}	Normalized to 50Ω			0.25 - j2.4		
Input-Referred 3rd-Order Intercept	$IIP3_{MIX}$				-18		dBm
Output Impedance	Z_{OUT_MIX}				330		Ω
Noise Figure	NF_{MIX}				16		dB
Image Rejection (Not Including LNA Tank)		f_{RF} = 433MHz, V_{IRSEL} = DV_{DD}			42		dB
		f_{RF} = 375MHz, V_{IRSEL} = DV_{DD} / 2			44		
		f_{RF} = 315MHz, V_{IRSEL} = 0V			44		
LNA/Mixer Voltage Gain		330Ω IF filter load	LNA in high-gain mode		48		dB
			LNA in low-gain mode		13		
INTERMEDIATE FREQUENCY (IF)							
Input Impedance	Z_{IN_IF}				330		Ω
Operating Frequency	f_{IF}	Bandpass response			10.7		MHz
3dB Bandwidth					10		MHz
RSSI Linearity					±0.5		dB
RSSI Dynamic Range					80		dB
RSSI Level		P_{RFIN} < -120dBm			1.15		V
		P_{RFIN} > 0dBm, AGC enabled			2.2		
AGC Threshold		LNA gain from low to high			1.39		V
		LNA gain from high to low			1.98		
DATA FILTER							
Maximum Bandwidth					50		kHz
DATA SLICER							
Comparator Bandwidth					100		kHz

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AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, $AV_{DD} = DV_{DD} = V_{DD5}$ = +3.0V to +3.6V, all RF inputs are referenced to 50Ω, f_{RF} = 315MHz, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $AV_{DD} = DV_{DD} = V_{DD5}$ = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Load Capacitance	C_{LOAD}				10		pF
Output High Voltage					V_{DD5}		V
Output Low Voltage					0		V
CRYSTAL OSCILLATOR							
Crystal Frequency (Note 5)	f_{XTAL}	f_{RF} = 433MHz	$V_{XTALSEL}$ = 0V		6.6128		MHz
			$V_{XTALSEL} = V_{DD5}$		13.2256		
		f_{RF} = 315MHz	$V_{XTALSEL}$ = 0V		4.7547		
			$V_{XTALSEL} = V_{DD5}$		9.5094		
Crystal Tolerance					50		ppm
Input Capacitance		From each pin to ground			6.2		pF

Note 1: 100% tested at T_A = +25°C. Guaranteed by design and characterization over temperature.

Note 2: IRSEL is internally set to 375MHz IR mode. It can be left open when the 375MHz image-rejection setting is desired. Bypass to AGND with a 1nF capacitor in a noisy environment.

Note 3: BER = 2 x 10-3, Manchester encoded, data rate = 4kbps, IF bandwidth = 280kHz.

Note 4: Input impedance is measured at the LNAIN pin. Note that the impedance includes the 15nH inductive degeneration connected from the LNA source to ground. The equivalent input circuit is 50Ω in series with 2.2pF.

Note 5: Crystal oscillator frequency for other RF carrier frequency within the 300MHz to 450MHz range is (f_{RF} - 10.7MHz) / 64 for XTALSEL = 0V, and (f_{RF} - 10.7MHz) / 32 for XTALSEL = V_{DD5}.
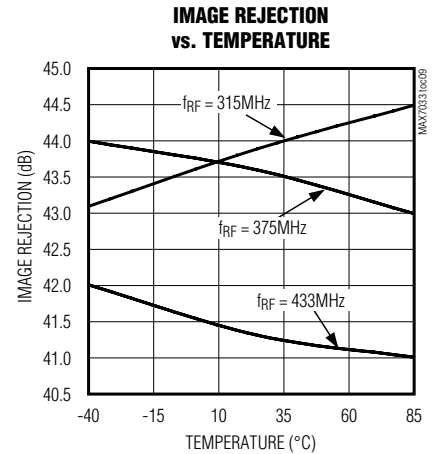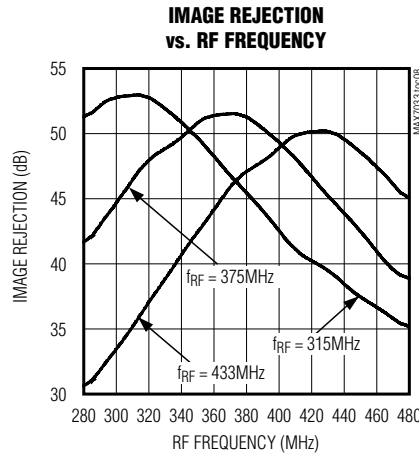
_____Typical Operating Characteristics

(*Typical Application Circuit* , $AV_{DD} = DV_{DD} = V_{DD5}$ = +3.3V, f_{RF} = 315MHz, T_A = +25°C, unless otherwise noted.)

MAX7033
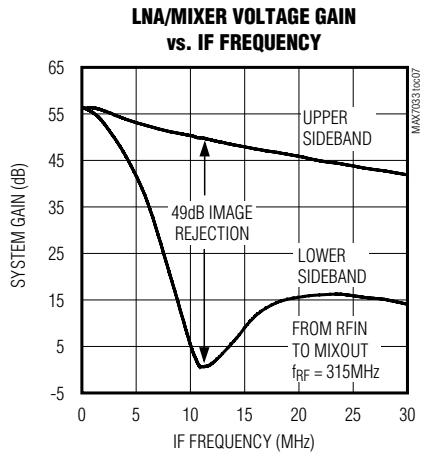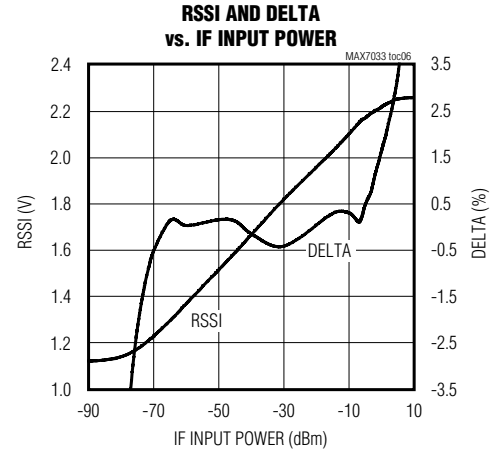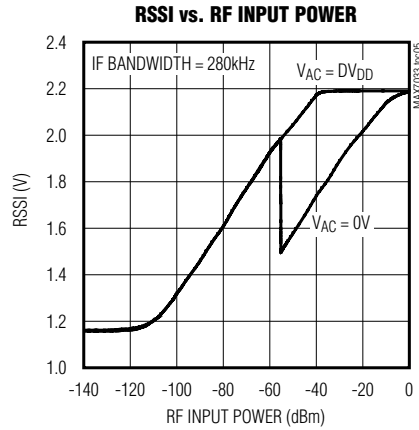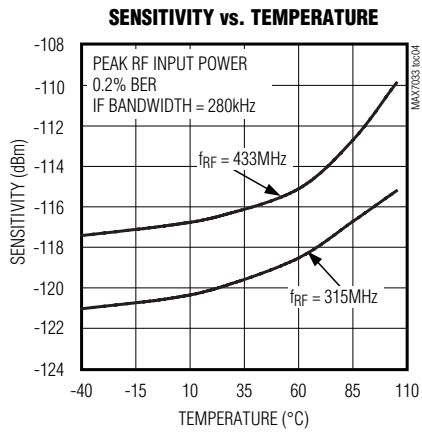
_____*Typical Operating Characteristics (continued)*

(*Typical Application Circuit* , $AV_{DD} = DV_{DD} = V_{DD5} = +3.3V$, $f_{RF} = 315MHz$, $T_A = +25°C$, unless otherwise noted.)
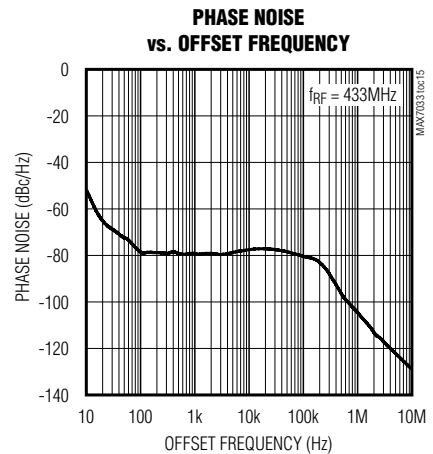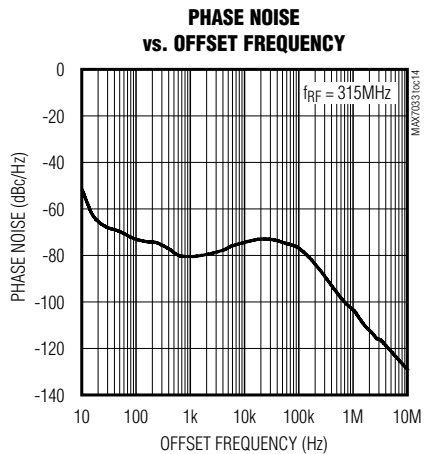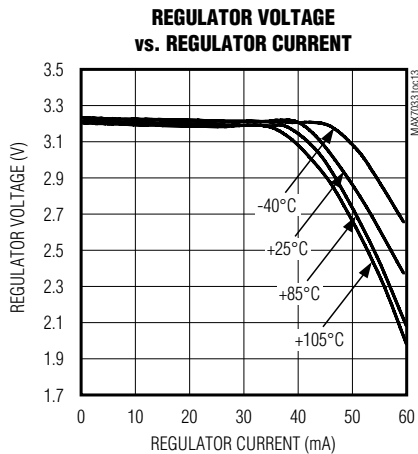
SENSITIVITY vs. TEMPERATURE

MAX7033 toc04

PEAK RF INPUT POWER
0.2% BER
IF BANDWIDTH = 280kHz

$f_{RF} = 433MHz$

$f_{RF} = 315MHz$

SENSITIVITY (dBm)

TEMPERATURE (°C)

RSSI vs. RF INPUT POWER

MAX7033 toc05

IF BANDWIDTH = 280kHz

$V_{AC} = DV_{DD}$

$V_{AC} = 0V$

RSSI (V)

RF INPUT POWER (dBm)

RSSI AND DELTA vs. IF INPUT POWER

MAX7033 toc06

DELTA

RSSI

RSSI (V)

DELTA (%)

IF INPUT POWER (dBm)

LNA/MIXER VOLTAGE GAIN vs. IF FREQUENCY

MAX7033 toc07

UPPER SIDEBAND

49dB IMAGE REJECTION

LOWER SIDEBAND

FROM RFIN TO MIXOUT
$f_{RF} = 315MHz$

SYSTEM GAIN (dB)

IF FREQUENCY (MHz)

IMAGE REJECTION vs. RF FREQUENCY

MAX7033 toc08

$f_{RF} = 375MHz$

$f_{RF} = 433MHz$

$f_{RF} = 315MHz$

IMAGE REJECTION (dB)

RF FREQUENCY (MHz)

IMAGE REJECTION vs. TEMPERATURE

MAX7033 toc09

$f_{RF} = 315MHz$

$f_{RF} = 375MHz$

$f_{RF} = 433MHz$

IMAGE REJECTION (dB)

TEMPERATURE (°C)

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MAX7033

_____Typical Operating Characteristics (continued)

(_Typical Application Circuit_ , $AV_{DD} = DV_{DD} = V_{DD5} = +3.3V$, $f_{RF} = 315MHz$, $T_A = +25°C$, unless otherwise noted.)

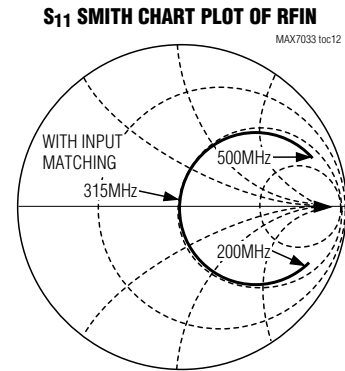**NORMALIZED IF GAIN
vs. IF FREQUENCY**

MAX7033 toc10

S_{11} LOG MAGNITUDE PLOT OF RFIN

MAX7033 toc11

S_{11} SMITH CHART PLOT OF RFIN

MAX7033 toc12

**REGULATOR VOLTAGE
vs. REGULATOR CURRENT**

MAX7033 toc13

**PHASE NOISE
vs. OFFSET FREQUENCY**

MAX7033 toc14

**PHASE NOISE
vs. OFFSET FREQUENCY**

MAX7033 toc15

MAX7033

Pin Description

| PIN		NAME	FUNCTION
TSSOP	THIN QFN		
1	29	XTAL1	Crystal Input 1 (See the *Phase-Locked Loop* section)
2, 7	4, 30	AV$_{DD}$	Positive Analog Supply Voltage. For +5V operation, AV$_{DD}$ is connected to an on-chip +3.2V low-dropout regulator. Both AV$_{DD}$ pins must be externally connected to each other. Bypass each pin to AGND with a 0.01µF capacitor as close to the pin as possible (see the *Typical Application Circuit*).
3	31	LNAIN	Low-Noise Amplifier Input (See the *Low-Noise Amplifier* section)
4	32	LNASRC	Low-Noise Amplifier Source for External Inductive Degeneration. Connect inductor to ground to set the LNA input impedance (see the *Low-Noise Amplifier* section).
5, 10	2, 7	AGND	Analog Ground
6	3	LNAOUT	Low-Noise Amplifier Output. Connect to mixer input through an LC tank filter (see the *Low-Noise Amplifier* section).
8	5	MIXIN1	1st Differential Mixer Input. Connect to LC tank filter from LNAOUT.
9	6	MIXIN2	2nd Differential Mixer Input. Connect through a 100pF capacitor to AV$_{DD}$ side of the LC tank.
11	8	IRSEL	Image-Rejection Select. Set V$_{IRSEL}$ = 0V to center image rejection at 315MHz. Leave IRSEL unconnected to center image rejection at 375MHz. Set V$_{IRSEL}$ = V$_{DD5}$ to center image rejection at 433MHz.
12	9	MIXOUT	330Ω Mixer Output. Connect to the input of the 10.7MHz bandpass filter.
13	10	DGND	Digital Ground
14	11	DV$_{DD}$	Positive Digital Supply Voltage. Connect to AV$_{DD}$. Bypass to DGND with a 0.01µF capacitor as close to the pin as possible.
15	12	AC	Automatic Gain Control. See Figure 1. Internally pulled down to AGND with a 100kΩ resistor.
16	14	XTALSEL	Crystal Divider Ratio Select. Drive XTALSEL low to select divider ratio of 64, or drive XTALSEL high to select divider ratio of 32.
17	15	IFIN1	1st Differential Intermediate-Frequency Limiter Amplifier Input. Bypass to AGND with a 1500pF capacitor as close to the pin as possible.
18	16	IFIN2	2nd Differential Intermediate-Frequency Limiter Amplifier Input. Connect to the output of a 10.7MHz bandpass filter.
19	17	DFO	Data Filter Output
20	18	DSN	Negative Data Slicer Input
21	19	OPP	Noninverting Op-Amp Input for the Sallen-Key Data Filter
22	20	DFFB	Data-Filter Feedback Node. Input for the feedback of the Sallen-Key data filter.
23	22	DSP	Positive Data Slicer Input
24	23	V$_{DD5}$	+5V Supply Voltage. For +5V operation, V$_{DD5}$ is the input to an on-chip voltage regulator whose +3.2V output drives AV$_{DD}$.
25	24	DATAOUT	Digital Baseband Data Output
26	26	PDOUT	Peak-Detector Output

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Pin Description (continued)

PIN		NAME	FUNCTION
TSSOP	**THIN QFN**		
27	27	$\overline{SHDN}$	Power-Down Select Input. Drive high to power up the IC. Internally pulled down to AGND with a 100kΩ resistor.
28	28	XTAL2	Crystal Input 2. Can also be driven with an external reference oscillator. (See the *Crystal Oscillator* section.)
—	1, 13, 21, 25	N.C	No Connection

Functional Diagram
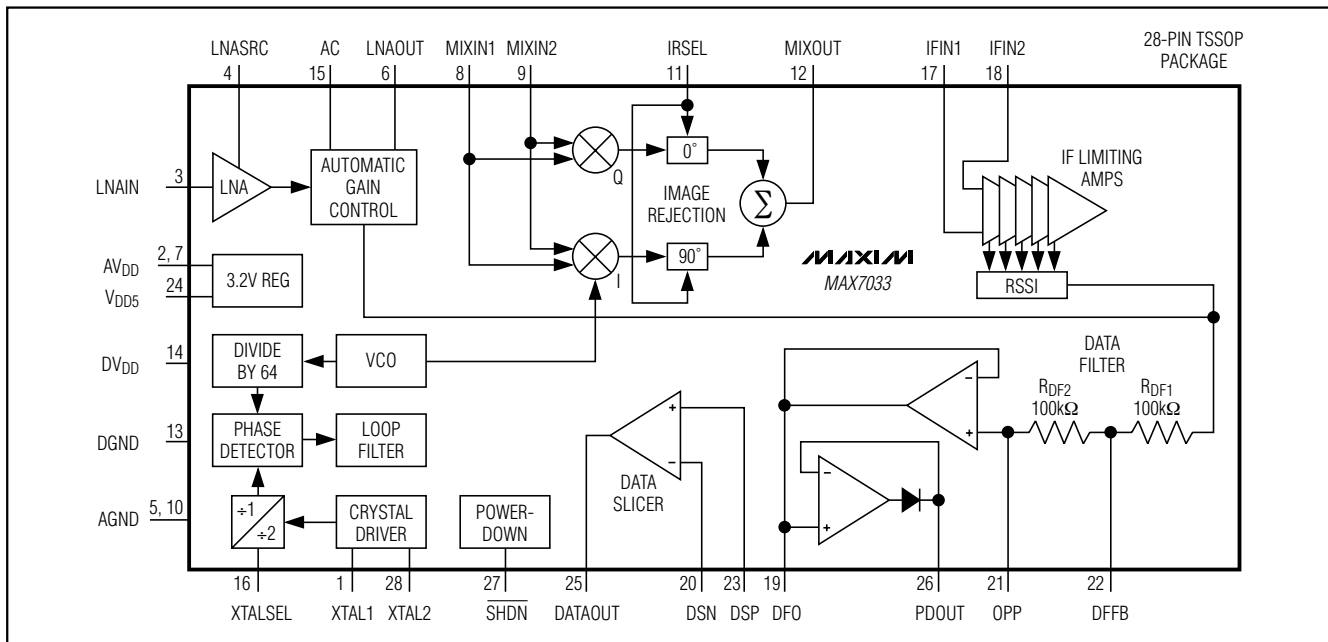
Detailed Description

The MAX7033 CMOS superheterodyne receiver and a few external components provide the complete receive chain from the antenna to the digital output data. Depending on signal power and component selection, data rates as high as 33kbps Manchester (66kbps NRZ) can be achieved.

The MAX7033 is designed to receive binary ASK data modulated in the 300MHz to 450MHz frequency range. ASK modulation uses a difference in amplitude of the carrier to represent logic 0 and logic 1 data.

Voltage Regulator

For operation with a single +3.0V to +3.6V supply voltage, connect AV$_{DD}$, DV$_{DD}$, and V$_{DD5}$ to the supply voltage.

For operation with a single +4.5V to +5.5V supply voltage, connect V$_{DD5}$ to the supply voltage. An on-chip voltage regulator drives one of the AV$_{DD}$ pins to approximately +3.2V. For proper operation, DV$_{DD}$ and both AV$_{DD}$ pins must be connected together. Bypass DV$_{DD}$ and both AV$_{DD}$ pins to AGND with 0.01µF capacitors placed as close to the pins as possible.

Low-Noise Amplifier

The LNA is an nMOS cascode amplifier with off-chip inductive degeneration, with a 3.0dB noise figure and an IIP3 of -12dBm. The gain and noise figures are dependent on both the antenna matching network at the LNA input and the LC tank network between the LNA output and the mixer inputs.

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The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedance at LNAIN, allowing for a more flexible input impedance match, such as a typical PC board trace antenna. A nominal value for this inductor with a 50Ω input impedance is 15nH, but is affected by PC board trace.

The LC tank filter connected to LNAOUT comprises L3 and C2 (see the *Typical Application Circuit*). Select L3 and C2 to resonate at the desired RF input frequency. The resonant frequency is given by:

$$f_{RF} = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where:

L_{TOTAL} = L3 + $L_{PARASITICS}$.

C_{TOTAL} = C2 + $C_{PARASITICS}$.

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PC board traces, package pins, mixer input impedance, LNA output impedance, etc. These parasitics at high frequencies cannot be ignored, and can have a dramatic effect on the tank filter center frequency. Lab experimentation should be done to optimize the center frequency of the tank.

Automatic Gain Control

When the AC pin is low, the automatic gain-control (AGC) circuit monitors the RSSI output. As the RSSI output reaches 1.98V, which corresponds to RF input level of -62dBm, the AGC switches on the LNA gain

reduction resistor. The resistor reduces the LNA gain by 35dB, thereby reducing the RSSI output by about 500mV. The LNA resumes high-gain mode when the RSSI level drops back below 1.39V (approximately -70dBm at RF input) for 1ms. The AGC has a hysteresis of 8dB. With the AGC function, the MAX7033 can reliably produce an ASK output for RF input levels up to 0dBm with modulation depth of 18dB.

When the AC pin is high and $\overline{SHDN}$ goes high, the AGC circuit is disabled and the LNA is always in high-gain mode. The AGC function can be resumed by bringing the AC pin low when $\overline{SHDN}$ is high.

The MAX7033 features an AGC lock function that is asserted when the level at the AC pin transitions from low to high while $\overline{SHDN}$ is high. Locking the AGC locks the LNA in the current gain state. As shown in Figure 1, the AGC lock function can be enabled or disabled as long as the $\overline{SHDN}$ pin is high. Changing the state of AC when $\overline{SHDN}$ is low has no effect.

Mixer

A unique feature of the MAX7033 is the integrated image rejection of the mixer. This device eliminates the need for a costly front-end SAW filter for most applications. Advantages of not using a SAW filter are increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double balanced mixers that perform an IQ downconversion of the RF input to the 10.7MHz IF from a low-side injected LO (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image-rejection circuit then combines these signals to achieve 44dB of image rejection. Low-side
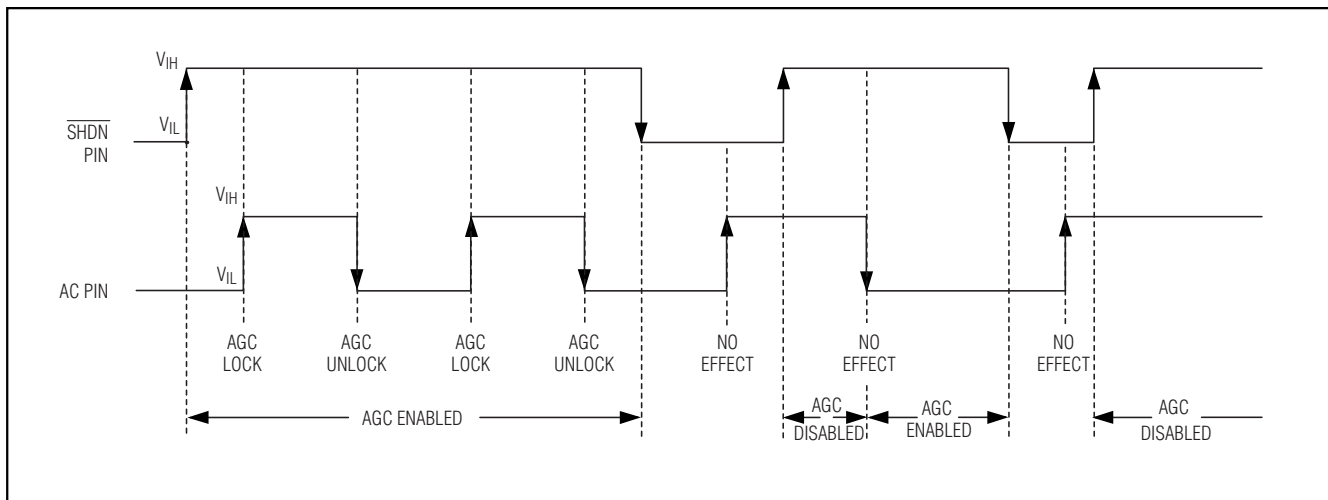

Figure 1. AGC Lock Activation Cycles

MAXIM

injection is required due to the on-chip image-rejection architecture. The IF output is driven by a source follower biased to create a driving-point impedance of 330Ω; this provides a good match to the off-chip 330Ω ceramic IF filter.

The IRSEL pin is a logic input that selects one of the three possible image-rejection frequencies. When V_{IRSEL} = 0V, the image rejection is tuned to 315MHz. V_{IRSEL} = V_{DD5} / 2 tunes the image rejection to 375MHz, and V_{IRSEL} = V_{DD5} tunes the image rejection to 433MHz. The IRSEL pin is internally set to V_{DD5} / 2 (image rejection at 375MHz) when it is left unconnected, thereby eliminating the need for an external V_{DD5} / 2 voltage.

Phase-Locked Loop

The PLL block contains a phase detector, charge pump, integrated loop filter, VCO, asynchronous 64x clock divider, and crystal oscillator driver. Besides the crystal, this PLL does not require any external components. The VCO generates a low-side LO. The relationship between the RF, IF, and reference frequencies is given by:

$$f_{REF} = \frac{f_{RF} - f_{IF}}{32 \times M}$$

where:

$$M = 1\ (V_{XTALSEL} = V_{DD5})\ \text{or}\ 2\ (V_{XTALSEL} = 0V)$$

To allow the smallest possible IF bandwidth (for best sensitivity), minimize the tolerance of the reference crystal.

Intermediate Frequency and RSSI

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. The six internal AC-coupled limiting amplifiers produce an overall gain of approximately 65dB, with a bandpass-filter-type response centered near the 10.7MHz IF frequency with a 3dB bandwidth of approximately 10MHz. The RSSI circuit demodulates the IF by producing a DC output proportional to the log of the IF signal level, with a slope of approximately 14.2mV/dB (see the *Typical Operating Characteristics*).

Applications Information

Crystal Oscillator

The crystal oscillator in the MAX7033 is designed to present a capacitance of approximately 3pF between the XTAL1 and XTAL2. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. Crystals

Table 1. Component Values for Typical Application Circuit

COMPONENT	VALUE FOR f_{RF} = 433MHz	VALUE FOR f_{RF} = 315MHz	DESCRIPTION
L1	56nH	120nH	TOKO LL1608-FH
L2	15nH	15nH	Murata LQP11A
L3	15nH	27nH	Murata LQP11A
C1	100pF	100pF	5%
C2	2pF	4pF	± 0.1pF
C3	100pF	100pF	5%
C4	100pF	100pF	5%
C5	1500pF	1500pF	10%
C6	220pF	220pF	5%
C7	470pF	470pF	5%
C8	0.47µF	0.47µF	20%
C9	220pF	220pF	10%
C10	0.01µF	0.01µF	20%
C11	0.01µF	0.01µF	20%
C12	15pF	15pF	Depends on XTAL
C13	15pF	15pF	Depends on XTAL
R1	5.1kΩ	5.1kΩ	5%
X1	6.5984MHz	4.7547MHz	—
X2	10.7MHz ceramic filter	10.7MHz ceramic filter	Murata SFECV10.7 series

315MHz/433MHz ASK Superheterodyne Receiver with AGC Lock

designed to operate with higher differential load capacitance always pull the reference frequency higher. For example, a 4.7547MHz crystal designed to operate with a 10pF load capacitance oscillates at 4.7563MHz with the MAX7033, causing the receiver to be tuned to 315.1MHz rather than 315.0MHz, an error of about 100kHz, or 320ppm.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance. Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE}+C_{LOAD}} - \frac{1}{C_{CASE}+C_{SPEC}}\right) \times 10^6$$

where:

f_P is the amount the crystal frequency pulled in ppm.

C_M is the motional capacitance of the crystal.

C_{CASE} is the case capacitance.

C_{SPEC} is the specified load capacitance.

C_{LOAD} is the actual load capacitance.

When the crystal is loaded as specified, i.e., $C_{LOAD} = C_{SPEC}$, the frequency pulling equals zero.

It is possible to use an external reference oscillator in place of a crystal to drive the VCO. AC-couple the external oscillator to XTAL2 with a 1000pF capacitor. Drive XTAL2 with a signal level of approximately -10dBm. AC-couple XTAL1 to ground with a 1000pF capacitor.

Data Filter

The data filter is implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency should be set to approximately 1.5 times the fastest expected data rate from the transmitter. Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 2 can create a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a rolloff rate of 40dB/decade for the two-pole filter.

The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of C5 and C6, use the following equations, along with the coefficients in Table 2:

$$C5 = \frac{b}{a(100k)(\pi)(f_C)}$$

$$C6 = \frac{a}{4(100k)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency.

For example, to choose a Butterworth filter response with a corner frequency of 5kHz:

$$C5 = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C6 = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Choosing standard capacitor values changes C5 to 470pF and C6 to 220pF, as shown in the *Typical Application Circuit*.

Data Slicer

The data slicer takes the analog output of the data filter and converts it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. One input is supplied by the data

Table 2. Coefficents to Calculate C5 and C6

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618
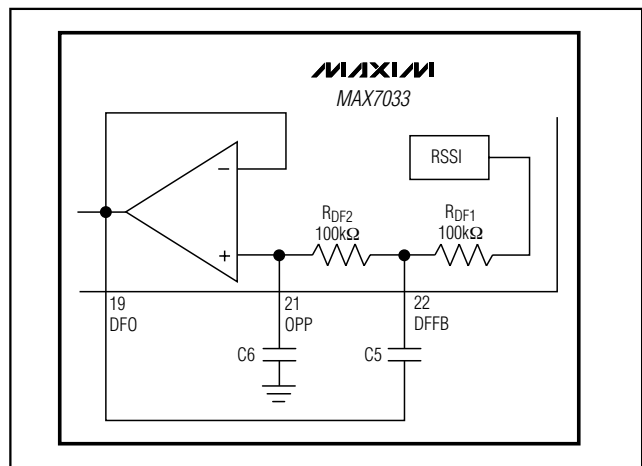
Figure 2. Sallen-Key Lowpass Data Filter

MAXIM

filter output. Both comparator inputs are accessible off-chip to allow for different methods of generating the slicing threshold, which is applied to the second comparator input.

The suggested data slicer configuration uses a resistor (R1) connected between DSN and DSP with a capacitor (C4) from DSN to DGND (Figure 3). This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The values of R1 and C4 affect how fast the threshold tracks to the analog amplitude. Be sure to keep the corner frequency of the RC circuit much lower than the lowest expected data rate.

Note that a long string of zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester coding, which has an equal number of zeros and ones, is used.

To prevent continuous toggling of DATAOUT in the absence of an RF signal due to noise, add hysteresis to the data slicer as shown in Figure 4.

Peak Detector
The peak-detector output (PDOUT), in conjunction with an external RC filter, creates a DC output voltage equal to the peak value of the data signal. The resistor provides a path for the capacitor to discharge, allowing the peak detector to dynamically follow peak changes of the data-filter output voltage. For faster data slicer response, use the circuit shown in Figure 5.

Layout Considerations
A properly designed PC board is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ/10 or longer act as antennas.

Keeping the traces short also reduces parasitic inductance. Generally, 1in of a PC board trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all V_{DD} connections.
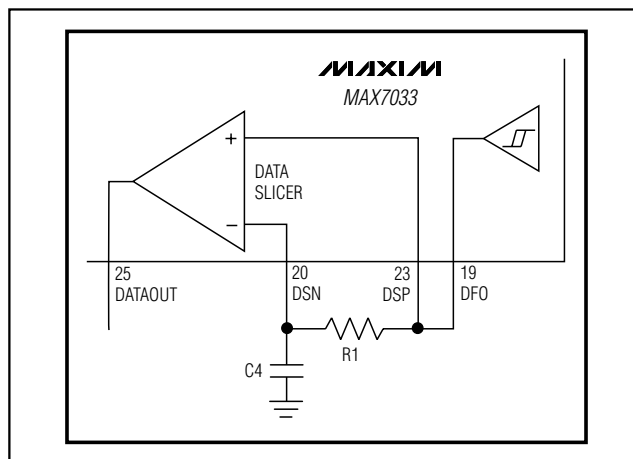

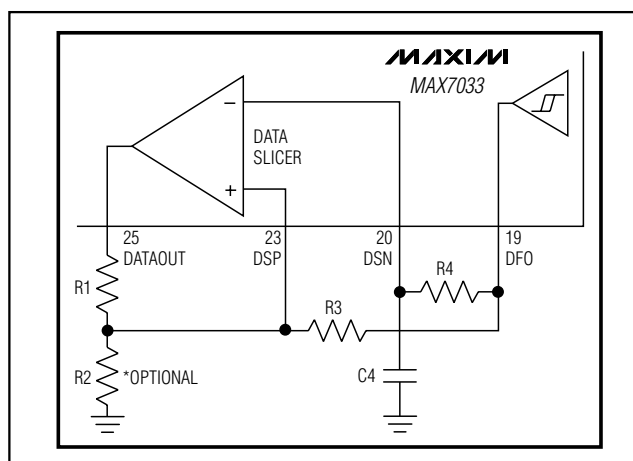Figure 3. Generating Data Slicer Threshold
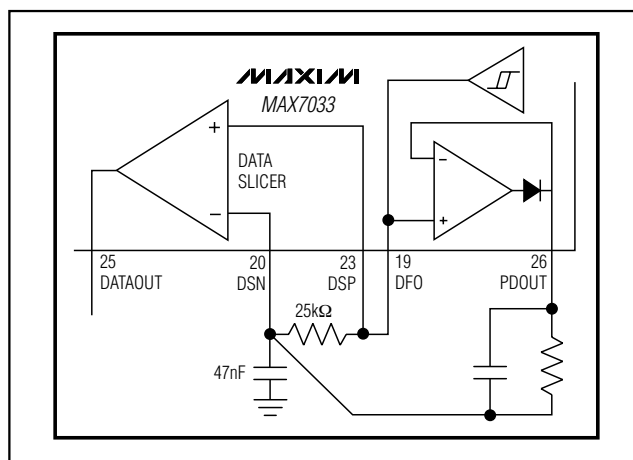

Figure 4. Generating Data Slicer Hysteresis

Figure 5. Using PDOUT for Faster Startup

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Typical Application Circuit
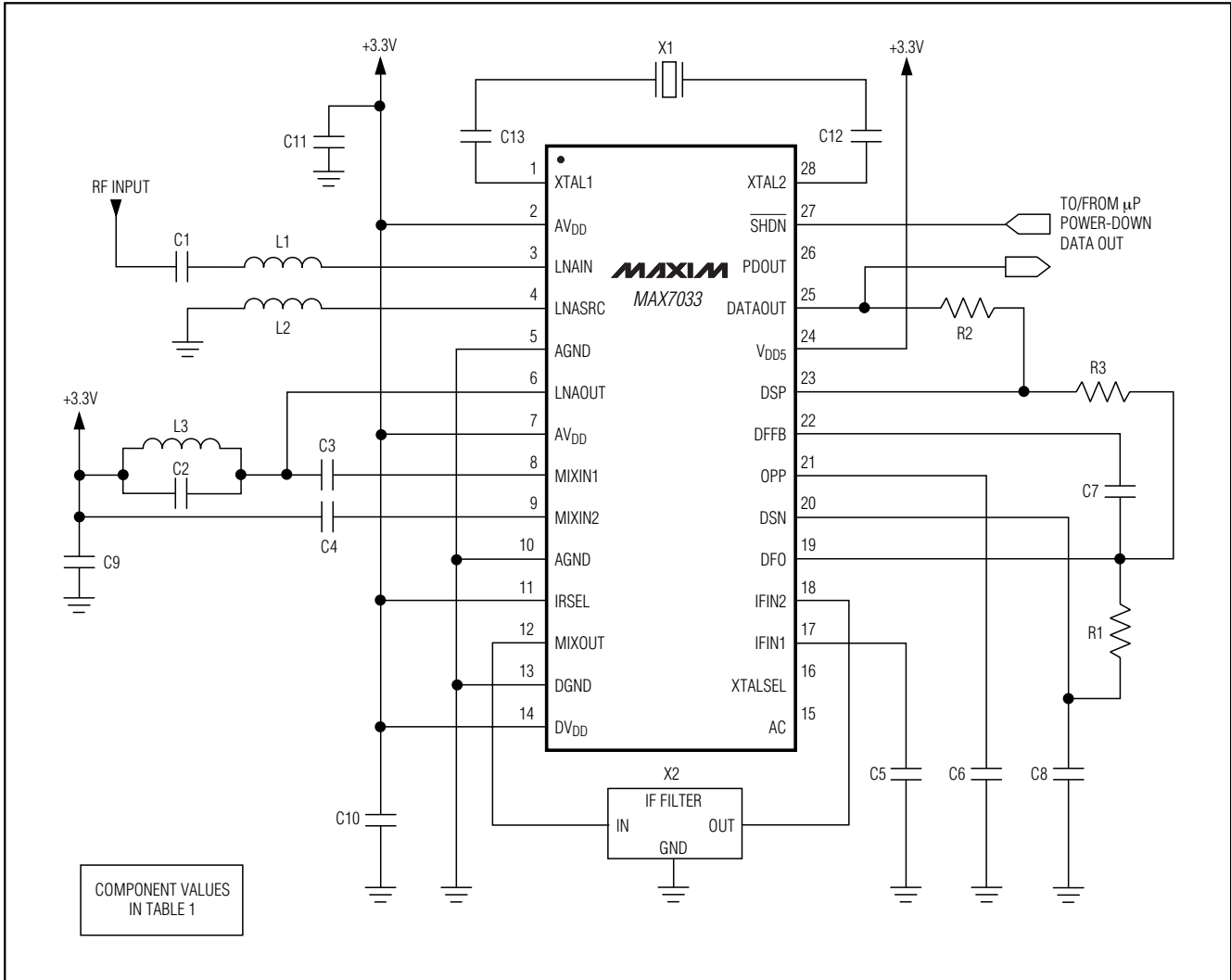
Chip Information

TRANSISTOR COUNT: 3208
PROCESS: CMOS

MAXIM

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

MAX7033

TSSOP4.40mm.EPS

COMMON DIMENSIONS

SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A₁	0.05	0.15	.002	.006
A₂	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b₁	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c₁	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

TOP VIEW

BOTTOM VIEW

SEE DETAIL A

SIDE VIEW

END VIEW

0.25 BSC

PARTING LINE

WITH PLATING

BASE METAL

DETAIL A

LEAD TIP DETAIL

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR ***MAXIM***

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0066	F	

315MHz/433MHz ASK Superheterodyne Receiver with AGC Lock

MAX7033

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)
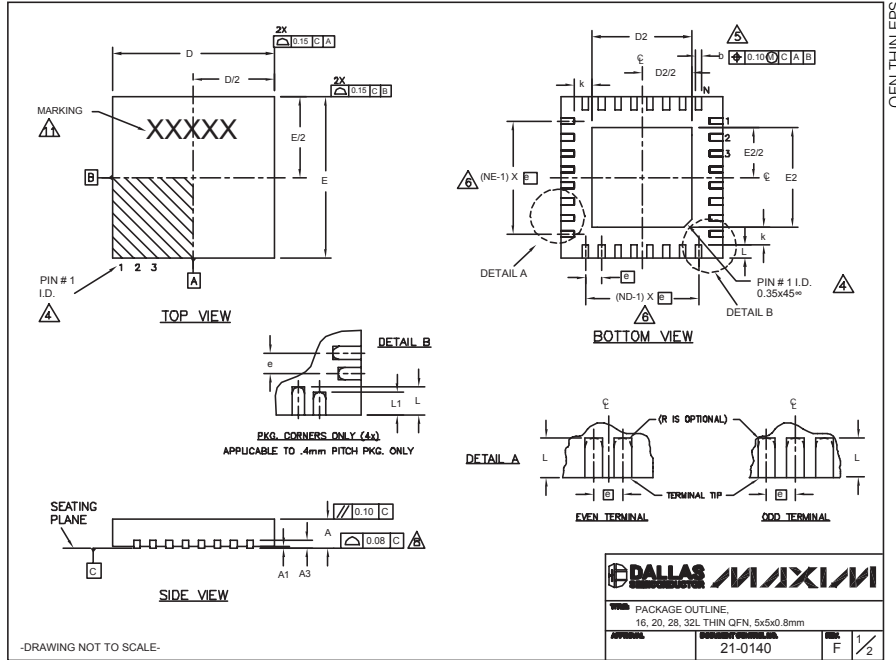

PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm
21-0140 F 1/2

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
L1	-	-	-	-	-	-	-	-	-	-	-	-
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	N
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO

**SEE COMMON DIMENSIONS TABLE

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm
21-0140 F 2/2

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