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# MAXIM

## TFT, LCD, DC-DC Converter with Operational Amplifiers

MAX8739

### General Description

The MAX8739 includes a high-performance, step-up regulator and two high-current operational amplifiers for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs). The input supply voltage range of the MAX8739 is from 1.8V to 5.5V. The device also includes a logic-controlled, high-voltage switch with adjustable delay.

The step-up DC-DC converter provides the regulated supply voltage for the panel source driver ICs. The converter is a high-frequency (600kHz/1.2MHz) current-mode regulator with an integrated 14V n-channel MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads while achieving efficiencies over 85%.

The two high-performance operational amplifiers are designed to drive the LCD backplane (VCOM) and/or the gamma-correction-divider string. The devices feature high output current ( $\pm 150\text{mA}$ ), fast slew rate ( $7.5\text{V}/\mu\text{s}$ ), wide bandwidth (12MHz), and rail-to-rail inputs and outputs.

The MAX8739 is available in a 20-pin, 5mm  $\times$  5mm thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels.

### Applications

Notebook Computer Displays  
LCD Monitor Panels  
Automotive Displays

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8739ETP+	-40°C to +85°C	20 Thin QFN-EP* (5mm $\times$ 5mm)	T2055-2

+ Denotes lead-free package.

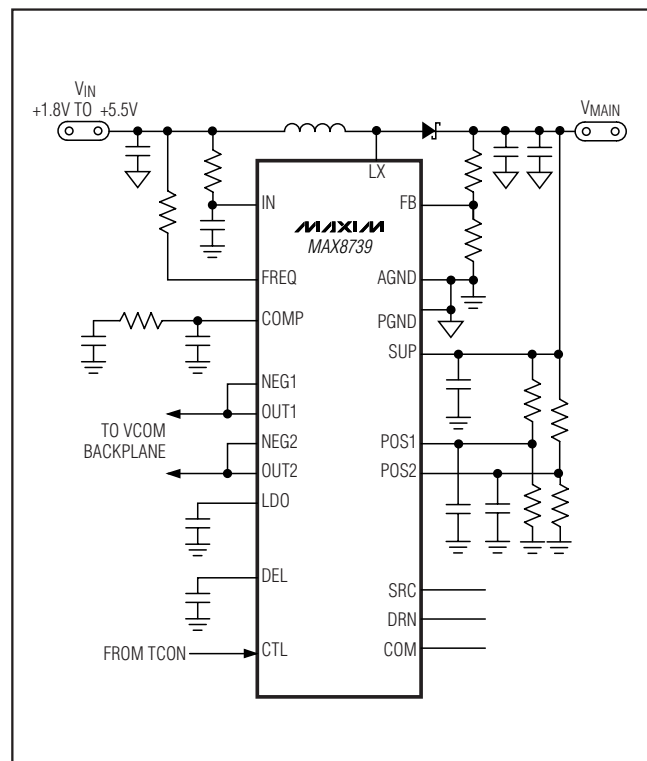
\* EP = Exposed pads.

Pin Configuration appears at end of data sheet.

### Features

- ◆ 1.8V to 5.5V Input Supply Range
- ◆ 600kHz/1.2MHz Current-Mode Step-Up Regulator
  - Fast Transient Response to Pulsed Load
  - High-Accuracy Output Voltage (1.5%)
  - Built-In 14V, 1.9A, 0.2 $\Omega$  n-Channel MOSFET
  - High Efficiency (> 85%)
  - Digital Soft-Start
- ◆ Two High-Performance Operational Amplifiers
  - $\pm 150\text{mA}$  Output Short-Circuit Current
  - 7.5V/ $\mu\text{s}$  Slew Rate
  - 12MHz, -3dB Bandwidth
  - Rail-to-Rail Inputs/Outputs
- ◆ Logic-Controlled, High-Voltage Switch with Adjustable Delay
- ◆ Built-In Power-Up Sequence
- ◆ Input Supply Undervoltage Lockout
- ◆ Timer Delay Fault Latch for All Regulator Outputs
- ◆ Thermal-Overload Protection

### Simplified Operating Circuit



MAXIM

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

# TFT, LCD, DC-DC Converter with Operational Amplifiers

## ABSOLUTE MAXIMUM RATINGS

IN, CTL, FREQ, LDO to AGND .....-0.3V to +6V  
 COMP, FB, DEL to AGND .....-0.3V to (VLDO + 0.3V)  
 PGND to AGND .....±0.3V  
 LX to PGND .....-0.3V to +14V  
 SUP to AGND .....-0.3V to +14V  
 POS1, POS2, NEG1, NEG2, OUT1,  
 OUT2 to AGND .....-0.3V to (VSUP + 0.3V)  
 SRC to AGND .....-0.3V to +30V  
 COM, DRN to AGND .....-0.3V to (VSRC + 0.3V)  
 COM RMS Output Current.....±50mA

OUT1, OUT2 Maximum Continuous Output Current .....±75mA  
 LX Switch Maximum Continuous RMS Output Current .....1.6A  
 Continuous Power Dissipation (TA = +70°C)  
 20-Pin, 5mm × 5mm, Thin QFN (derate 20.8mW/°C  
 above +70°C).....1667mW  
 Operating Temperature Range .....-40°C to +85°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(VIN = 2.5V, VSUP = 10V, VSRC = 28V, FREQ = CTL = IN, PGND = AGND = 0, TA = 0°C to +85°C. Typical values are at TA = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range			1.8		5.5	V
IN Quiescent Current	VIN = 2.5V, VFB = 1.5V			15	30	µA
IN Undervoltage Lockout Threshold	IN rising, 200mV hysteresis			1.30	1.75	V
LDO Output Voltage	6V ≤ VSUP ≤ 13V, ILDO = 12.5mA		4.6	5	5.4	V
LDO Undervoltage Lockout Threshold	LDO rising, 200mV hysteresis		2.4	2.7	3.0	V
LDO Output Current			15			mA
SUP Supply Voltage Range			4.5		13.0	V
SUP Undervoltage Fault Threshold					1.4	V
SUP Supply Current	VPOS_ = 4V, no load	LX not switching		1.8	3.0	mA
		LX switching		16	30	
Thermal Shutdown	Rising edge, 15°C hysteresis			+160		°C
<b>STEP-UP REGULATOR</b>						
Operating Frequency	FREQ = AGND		512	600	768	kHz
	FREQ = IN		1020	1200	1380	
Maximum Duty Cycle	FREQ = AGND		91	95	99	%
	FREQ = IN		88	92	96	
FREQ Input Low Voltage	VIN = 1.8V to 5.5V				0.6	V
FREQ Input High Voltage	VIN = 1.8V to 2.4V		1.4			V
	VIN = 2.4V to 5.5V		2.0			
FREQ Pulldown Current	VFREQ = 1.0V		3.5	5.0	6.0	µA
FB Regulation Voltage	ISWITCH = 200mA		1.225	1.240	1.255	V
FB Fault Trip Level	Falling edge		0.96	1.00	1.04	V
Duration to Trigger Fault Condition	FREQ = AGND		43	51	64	ms
	FREQ = IN		47	55	65	

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 2.5V$ ,  $V_{SUP} = 10V$ ,  $V_{SRC} = 28V$ ,  $FREQ = CTL = IN$ ,  $PGND = AGND = 0$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FB Load Regulation	$0 < I_{LOAD} < 200mA$ , transient only		-1		%
FB Line Regulation	$V_{IN} = 1.8V$ to $5.5V$	-0.15	-0.08	+0.15	%/V
FB Input Bias Current	$V_{FB} = 1.3V$		125	200	nA
FB Transconductance	$\Delta I_{COMP} = 5\mu A$	75	160	280	$\mu S$
FB Voltage Gain	FB to COMP		700		V/V
LX On-Resistance	$I_{LX} = 200mA$		200	400	$m\Omega$
LX Leakage Current	$V_{LX} = V_{SUP} = 13V$		0.01	20	$\mu A$
LX Current Limit	$V_{FB} = 1.1V$ , duty cycle = 65%	1.5	1.9	2.3	A
Current-Sense Transresistance		0.22	0.36	0.50	V/A
Soft-Start Period	FREQ = AGND		13		ms
	FREQ = IN		14		
Soft-Start Step Size			0.24		A
<b>OPERATIONAL AMPLIFIERS</b>					
Input Offset Voltage	$V_{CM} = V_{SUP}/2$ , $T_A = +25^{\circ}C$		0	12	mV
Input Bias Current	NEG1, POS1, NEG2, POS2	-50	+1	+50	nA
Input Common-Mode Voltage Range	NEG1, POS1, NEG2, POS2	0		$V_{SUP}$	V
Common-Mode Rejection Ratio	$0 \leq V_{NEG\_} , V_{POS\_} \leq V_{SUP}$	50	90		dB
Open-Loop Gain			125		dB
Output Voltage Swing High	$I_{OUT\_} = 100\mu A$	$V_{SUP} - 15$	$V_{SUP} - 2$		mV
	$I_{OUT\_} = 5mA$	$V_{SUP} - 150$	$V_{SUP} - 80$		
Output Voltage Swing Low	$I_{OUT\_} = -100\mu A$		2	15	mV
	$I_{OUT\_} = -5mA$		80	150	
Short-Circuit Current	To $V_{SUP}/2$	Source	50	150	mA
		Sink	50	140	
Output Source-and-Sink Current	Buffer configuration, $V_{POS\_} = 4V$ , $  \Delta V_{OS}   < 10mV$	40			mA
Power-Supply Rejection Ratio	DC, $6V \leq V_{SUP} \leq 13V$ , $V_{POS\_} , V_{NEG\_} = V_{SUP}/2$	60	100		dB
Slew Rate			7.5		V/ $\mu s$
-3dB Bandwidth	$R_L = 10k\Omega$ , $C_L = 10pF$ , buffer configuration		12		MHz
Gain-Bandwidth Product	Buffer configuration		8		MHz
<b>POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES</b>					
DEL Capacitor Charge Current	During startup, $V_{DEL} = 1V$	4	5	6	$\mu A$
DEL Turn-On Threshold		1.178	1.24	1.302	V
DEL Pin Discharge Switch On-Resistance	During UVLO, $V_{IN} = 1.3V$		20		$\Omega$
CTL Input-Low Voltage	$V_{IN} = 1.8V$ to $5.5V$			0.6	V

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 2.5V$ ,  $V_{SUP} = 10V$ ,  $V_{SRC} = 28V$ ,  $FREQ = CTL = IN$ ,  $PGND = AGND = 0$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CTL Input-High Voltage	$V_{IN} = 1.8V$ to $2.4V$	1.4			V
	$V_{IN} = 2.4V$ to $5.5V$	2.0			
CTL Input-Leakage Current	CTL = AGND or IN	-1		+1	$\mu A$
CTL-to-SRC Propagation Delay	COM falling, no load on COM		100		ns
	COM rising, no load on COM		100		
SRC Input-Voltage Range				28	V
SRC Input Current	$V_{DRN} = 8V$ , CTL = AGND, $V_{DEL} = 1.5V$		15	30	$\mu A$
	$V_{DRN} = 8V$ , CTL = IN, $V_{DEL} = 1.5V$		100	180	
DRN Input Current	$V_{DRN} = 8V$ , CTL = AGND, $V_{DEL} = 1.5V$		90	150	$\mu A$
SRC-to-COM Switch On-Resistance	$V_{DEL} = 1.5V$ , CTL = IN		15	30	$\Omega$
DRN-to-COM Switch On-Resistance	$V_{DEL} = 1.5V$ , CTL = AGND		30	60	$\Omega$

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = 2.5V$ ,  $V_{SUP} = 10V$ ,  $V_{SRC} = 28V$ ,  $FREQ = CTL = IN$ ,  $PGND = AGND = 0$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Supply Range		1.8		5.5	V
IN Quiescent Current	$V_{IN} = 2.5V$ , $V_{FB} = 1.5V$			30	$\mu A$
IN Undervoltage Lockout Threshold	IN rising, 200mV hysteresis			1.75	V
LDO Output Voltage	$6V \leq V_{SUP} \leq 13V$ , $I_{LDO} = 12.5mA$	4.6		5.4	V
LDO Undervoltage Lockout Threshold	LDO rising, 200mV hysteresis	2.4		3.0	V
LDO Output Current		15			mA
SUP Supply Voltage Range		4.5		13.0	V
SUP Undervoltage Fault Threshold				1.4	V
SUP Supply Current	$V_{POS\_} = 4V$ , no load	LX not switching		3.0	mA
		LX switching		30	
<b>STEP-UP REGULATOR</b>					
Operating Frequency	FREQ = AGND	512		768	kHz
	FREQ = IN	1020		1380	
Maximum Duty Cycle	FREQ = AGND	91		99	%
	FREQ = IN	88		96	
FREQ Input Low Voltage	$V_{IN} = 1.8V$ to $5.5V$			0.6	V

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 2.5V$ ,  $V_{SUP} = 10V$ ,  $V_{SRC} = 28V$ ,  $FREQ = CTL = IN$ ,  $PGND = AGND = 0$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FREQ Input-High Voltage	$V_{IN} = 1.8V$ to $2.4V$		1.4			V
	$V_{IN} = 2.4V$ to $5.5V$		2.0			
FREQ Pulldown Current	$V_{FREQ} = 1.0V$		3.5		6.0	$\mu A$
FB Regulation Voltage	$I_{SWITCH} = 200mA$		1.220		1.260	V
FB Fault-Trip Level	Falling edge		0.96		1.04	V
Duration to Trigger-Fault Condition	$FREQ = AGND$		41		64	ms
	$FREQ = IN$		47		65	
FB Line Regulation	$V_{IN} = 1.8V$ to $5.5V$		-0.15		+0.15	%/V
FB Input Bias Current	$V_{FB} = 1.3V$				200	nA
FB Transconductance	$\Delta I_{COMP} = 5\mu A$		75		280	$\mu S$
LX On-Resistance	$I_{LX} = 200mA$				400	$m\Omega$
LX Current Limit	$V_{FB} = IV$ , duty cycle = 65%		1.5		2.3	A
Current-Sense Transresistance			0.22		0.50	V/A
<b>OPERATIONAL AMPLIFIERS</b>						
Input Offset Voltage	$V_{CM} = V_{SUP}/2$ , $T_A = +25^{\circ}C$				12	mV
Input Common-Mode Voltage Range	NEG1, POS1, NEG2, POS2		0		$V_{SUP}$	V
Common-Mode Rejection Ratio	$0 \leq V_{NEG\_} , V_{POS\_} \leq V_{SUP}$		50			dB
Output Voltage Swing High	$I_{OUT\_} = 100\mu A$		$V_{SUP} - 15$			mV
	$I_{OUT\_} = 5mA$		$V_{SUP} - 150$			
Output Voltage Swing Low	$I_{OUT\_} = -100\mu A$		15			mV
	$I_{OUT\_} = -5mA$		150			
Short-Circuit Current	$T_o V_{SUP}/2$	Source	50			mA
		Sink	50			
Output Source-and-Sink Current	Buffer configuration, $V_{POS\_} = 4V$ , $  \Delta V_{OS}   < 10mV$		40			mA
Power-Supply Rejection Ratio	DC, $6V \leq V_{SUP} \leq 13V$ , $V_{POS\_} , V_{NEG\_} = V_{SUP}/2$		60			dB

# TFT, LCD, DC-DC Converter with Operational Amplifiers

## ELECTRICAL CHARACTERISTICS (continued)

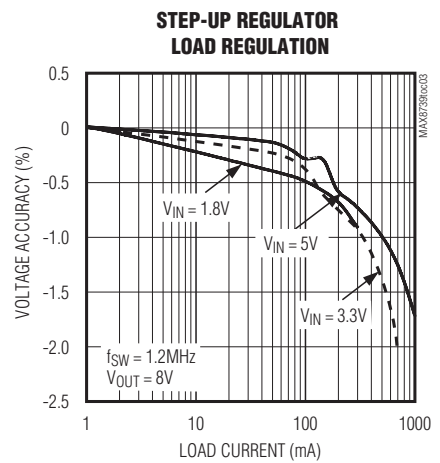
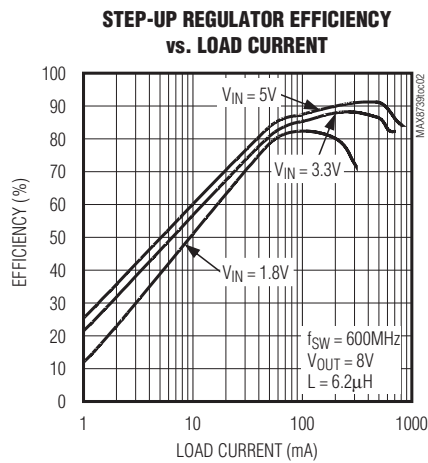
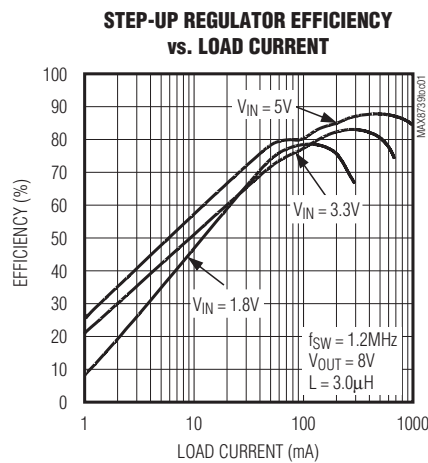
( $V_{IN} = 2.5V$ ,  $V_{SUP} = 10V$ ,  $V_{SRC} = 28V$ ,  $FREQ = CTL = IN$ ,  $PGND = AGND = 0$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES</b>					
DEL Capacitor Charge Current	During startup, $V_{DEL} = 1V$	4		6	$\mu A$
DEL Turn-On Threshold		1.178		1.302	V
CTL Input-Low Voltage	$V_{IN} = 1.8V$ to $5.5V$			0.6	V
CTL Input-High Voltage	$V_{IN} = 1.8V$ to $2.4V$	1.4			V
	$V_{IN} = 2.4V$ to $5.5V$	2.0			
SRC Input-Voltage Range				28	V
SRC Input Current	$V_{DRN} = 8V$ , $CTL = AGND$ , $V_{DEL} = 1.5V$			30	$\mu A$
	$V_{DRN} = 8V$ , $CTL = IN$ , $V_{DEL} = 1.5V$			180	
DRN Input Current	$V_{DRN} = 8V$ , $CTL = AGND$ , $V_{DEL} = 1.5V$			150	$\mu A$
SRC-to-COM Switch On-Resistance	$V_{DEL} = 1.5V$ , $CTL = IN$			30	$\Omega$
DRN-to-COM Switch On-Resistance	$V_{DEL} = 1.5V$ , $CTL = AGND$			60	$\Omega$

**Note 1:** Specifications to  $-40^{\circ}C$  are guaranteed by design, not production tested.

## Typical Operating Characteristics

(Circuit of Figure 1,  $V_{IN} = 2.5V$ ,  $V_{MAIN} = 8V$ ,  $FREQ = IN$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)

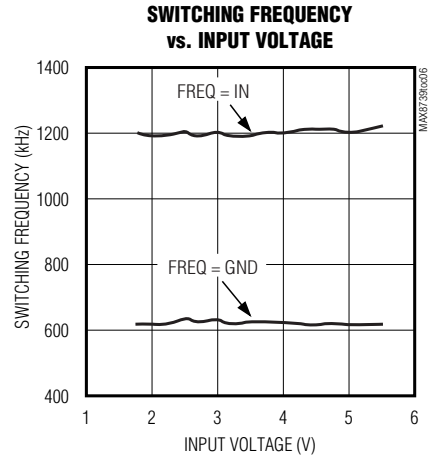
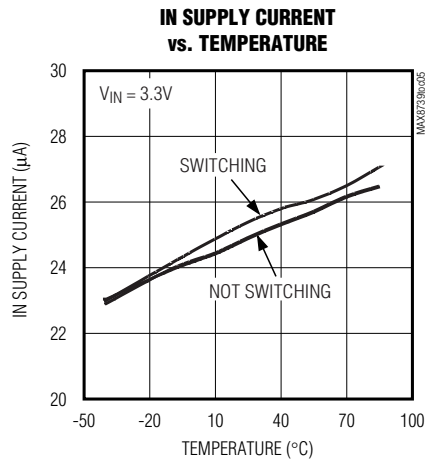
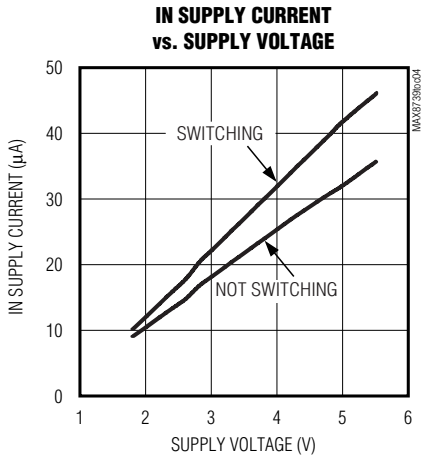


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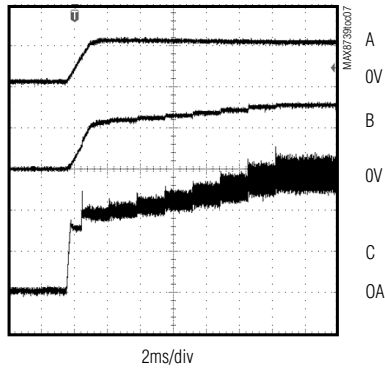
## Typical Operating Characteristics

(Circuit of Figure 1,  $V_{IN} = 2.5V$ ,  $V_{MAIN} = 8V$ ,  $FREQ = IN$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

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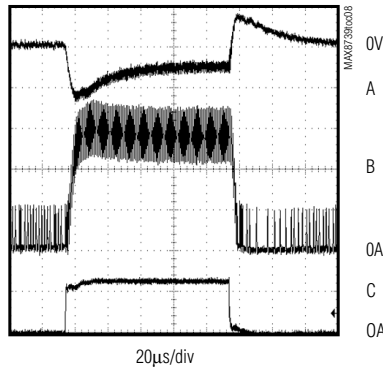


**STEP-UP REGULATOR SOFT-START (HEAVY LOAD)**



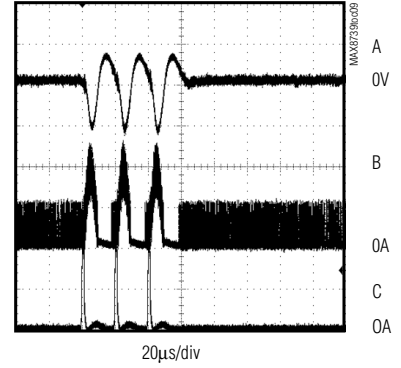
A:  $V_{IN}$ , 2V/div  
 B:  $V_{MAIN}$ , 5V/div  
 C: INDUCTOR CURRENT, 1A/div

**STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE**



A:  $V_{MAIN}$ , AC-COUPLED, 200mV/div  
 B: INDUCTOR CURRENT, 500mA/div  
 C: LOAD CURRENT, 500mA/div

**STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE**



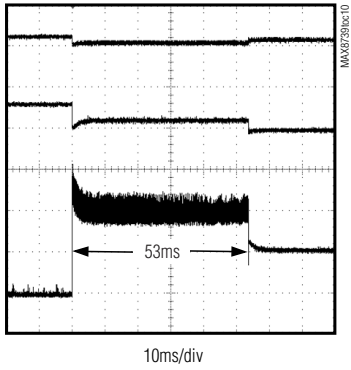
A:  $V_{MAIN}$ , AC-COUPLED, 200mV/div  
 B: INDUCTOR CURRENT, 500mA/div  
 C: LOAD CURRENT, 500mA/div

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## Typical Operating Characteristics (continued)

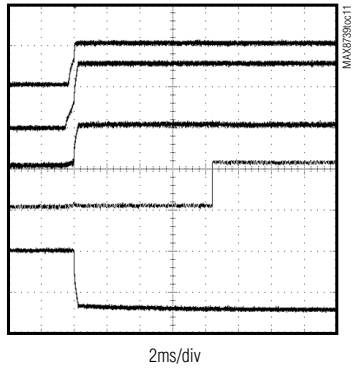
(Circuit of Figure 1,  $V_{IN} = 2.5V$ ,  $V_{MAIN} = 8V$ ,  $FREQ = 1N$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)

**TIMER DELAY LATCH RESPONSE TO OVERLOAD**



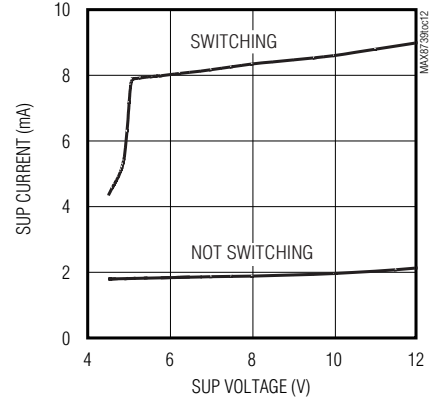
A:  $V_{IN}$ , 2V/div  
B:  $V_{MAIN}$ , 5V/div  
C: INDUCTOR CURRENT, 2A/div

**POWER-UP SEQUENCE**

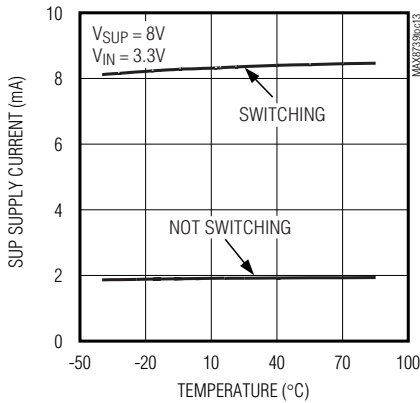


A:  $V_{LDO}$ , 5V/div  
B:  $V_{MAIN}$ , 5V/div  
C:  $V_{SRC}$ , 20V/div  
D:  $V_{GON}$ , 20V/div  
E:  $V_{GOFF}$ , 5V/div

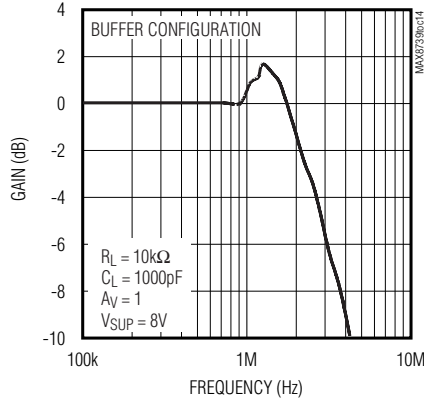
**SUP SUPPLY CURRENT vs. SUP VOLTAGE**



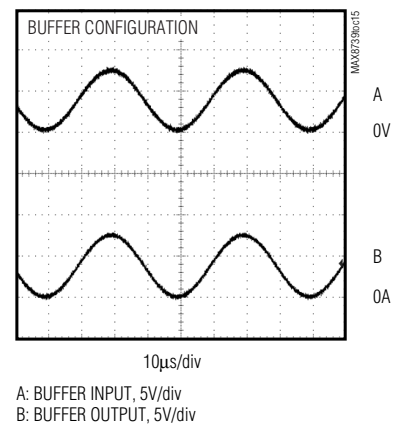
**SUP SUPPLY CURRENT vs. TEMPERATURE**



**OPERATIONAL-AMPLIFIER FREQUENCY RESPONSE**



**OPERATIONAL-AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT**





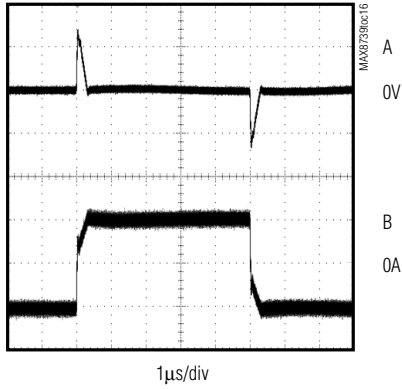
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## Typical Operating Characteristics (continued)

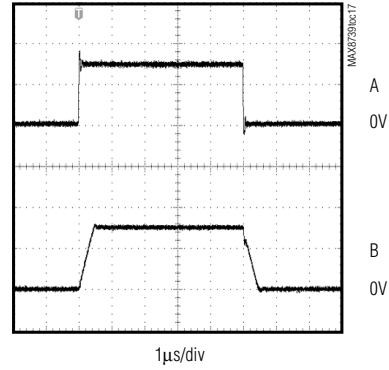
(Circuit of Figure 1,  $V_{IN} = 2.5V$ ,  $V_{MAIN} = 8V$ ,  $FREQ = 1N$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)

**OPERATIONAL-AMPLIFIER  
LOAD TRANSIENT RESPONSE**



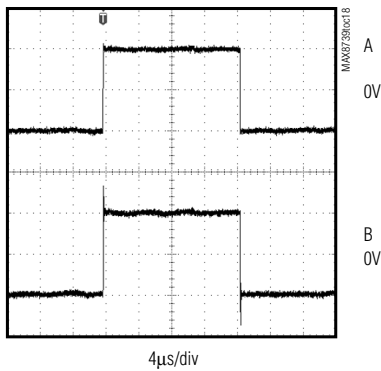
A: OUTPUT VOLTAGE, AC-COUPLED, 2V/div  
B: OUTPUT CURRENT, 50mA/div

**OPERATIONAL-AMPLIFIER  
LARGE-SIGNAL STEP RESPONSE**



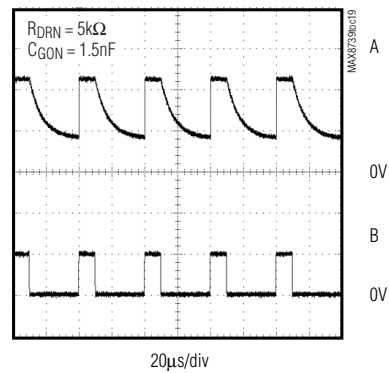
A: INPUT VOLTAGE, 5V/div  
B: OUTPUT VOLTAGE, 5V/div

**OPERATIONAL-AMPLIFIER  
SMALL-SIGNAL STEP RESPONSE**



A: INPUT VOLTAGE, AC-COUPLED 50mV/div  
B: OUTPUT VOLTAGE, AC-COUPLED 50mV/div

**SWITCH CONTROL FUNCTION**



A:  $V_{GON}$ , 10V/div  
B:  $V_{CTL}$ , 2V/div

# TFT, LCD, DC-DC Converter with Operational Amplifiers

## Pin Description

PIN	NAME	FUNCTION
1	COM	Internal High-Voltage MOSFET Switch Common Terminal
2	SRC	Switch Input. Source of the internal high-voltage, p-channel MOSFET. Bypass SRC to PGND with a minimum of 0.1 $\mu$ F close to the pins.
3	LDO	Internal 5V Linear Regulator Output. This regulator powers all internal circuitry except OUT1 and OUT2 operational amplifiers. Bypass LDO to AGND with a 0.22 $\mu$ F or greater ceramic capacitor.
4	PGND	Power Ground. PGND is the source of the step-up regulator's n-channel power MOSFET. Connect PGND to the input capacitor ground terminals through a short, wide PC board trace. Connect PGND to analog ground (AGND) underneath the IC.
5	AGND	Analog Ground. Connect AGND to power ground (PGND) underneath the IC.
6	POS1	Operational Amplifier 1 Noninverting Input
7	NEG1	Operational Amplifier 1 Inverting Input
8	OUT1	Operational Amplifier 1 Output
9	OUT2	Operational Amplifier 2 Output
10	NEG2	Operational Amplifier 2 Inverting Input
11	POS2	Operational Amplifier 2 Noninverting Input
12	SUP	Operational-Amplifier Supply Input. SUP is the positive supply rail for the OUT1 and OUT2 amplifiers. SUP is also the supply input of the internal 5V linear regulator. Connect SUP to the main step-up regulator output and bypass SUP to AGND with a 0.1 $\mu$ F capacitor.
13	LX	n-Channel Power MOSFET Drain and Switching Node. Connect the inductor and the catch diode to LX and minimize the trace area for lowest EMI.
14	IN	Supply Voltage. IN can range from 1.8V to 5.5V.
15	FREQ	Oscillator Frequency-Select Input. Pull FREQ low or leave it unconnected for 600kHz operation. Connect FREQ to IN for 1.2MHz operation. This input has a 5 $\mu$ A pulldown.
16	FB	Step-Up Regulator Feedback Input. Regulates to 1.24V (nominal). Connect a resistive voltage-divider from the output ( $V_{MAIN}$ ) to FB to analog ground (AGND). Place the divider within 5mm of FB.
17	COMP	Step-Up Regulator Error-Amplifier Compensation Point. Connect a series resistor and capacitor from COMP to AGND. See the <i>Loop Compensation</i> section for component selection guidelines.
18	DEL	High-Voltage Switch-Delay Input. Connect a capacitor from DEL to AGND to set the high-voltage switch startup delay. A 5 $\mu$ A current source charges $C_{DEL}$ . The switches between SRC, COM, and DRN are disabled during the delay period.
19	CTL	High-Voltage Switch-Control Input. When CTL is high, the high-voltage switch between COM and SRC is on and the high-voltage switches between COM and DRN are off. When CTL is low, the high-voltage switch between COM and SRC is off and the high-voltage switches between COM and DRN are on. CTL is inhibited by the undervoltage lockout and when $V_{DEL}$ is less than 1.24V.
20	DRN	Switch Input. Drain of the internal, high-voltage, back-to-back p-channel MOSFETs connected to COM.
—	EP	Exposed Pad

# TFT, LCD, DC-DC Converter with Operational Amplifiers

MAX8739

## Typical Application Circuit

The MAX8739 typical application circuit (Figure 1) generates a +8V source-driver supply and approximately +22V and -7V gate-driver supplies for TFT displays. The input-voltage range for the IC is from +1.8V to

+5.5V but the Figure 1 circuit is designed to run from 1.8V to 2.7V. Table 1 lists the key recommended components and Table 2 lists the contact information of the component suppliers.

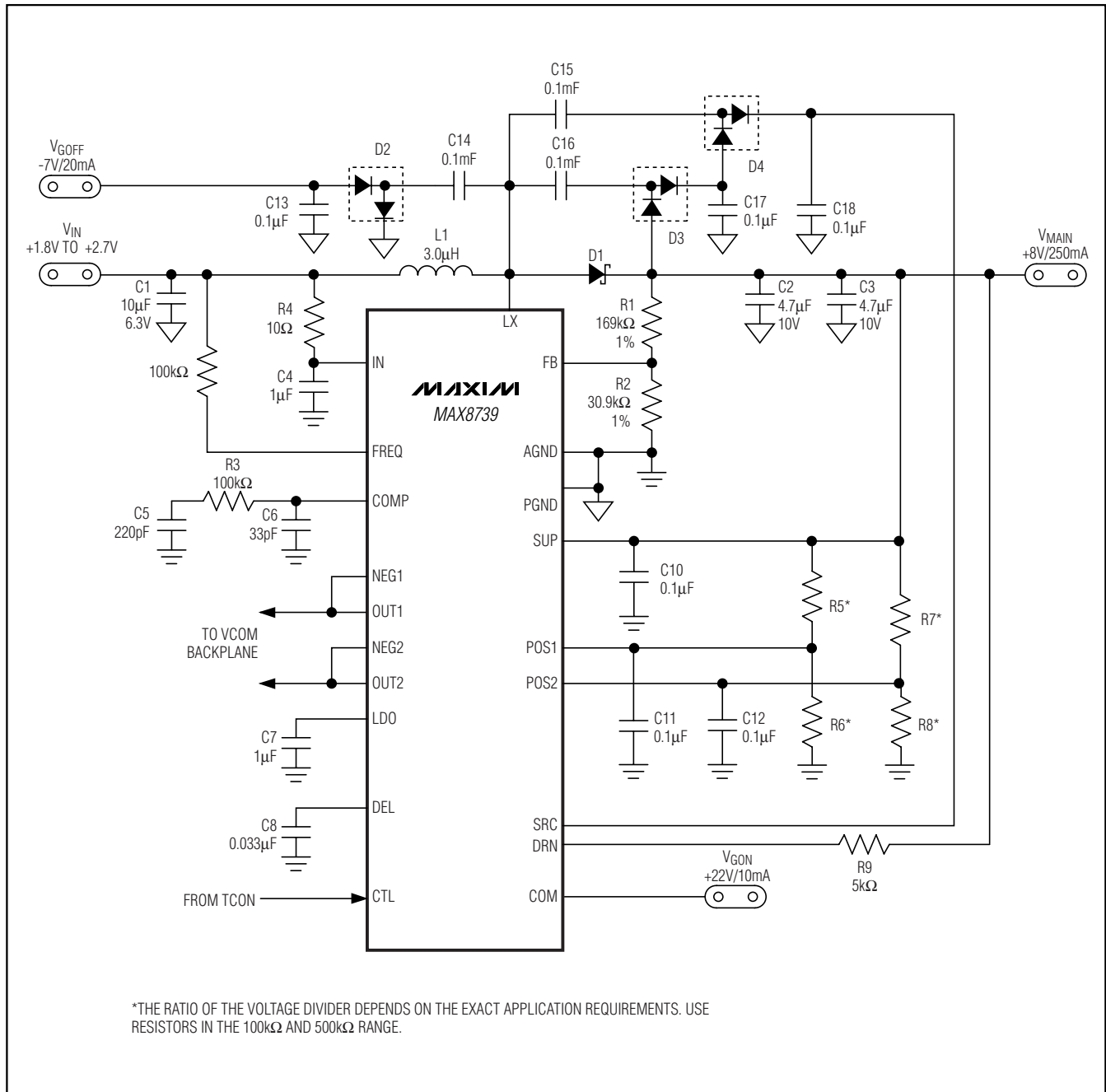


Figure 1. Typical Application Circuit

# TFT, LCD, DC-DC Converter with Operational Amplifiers

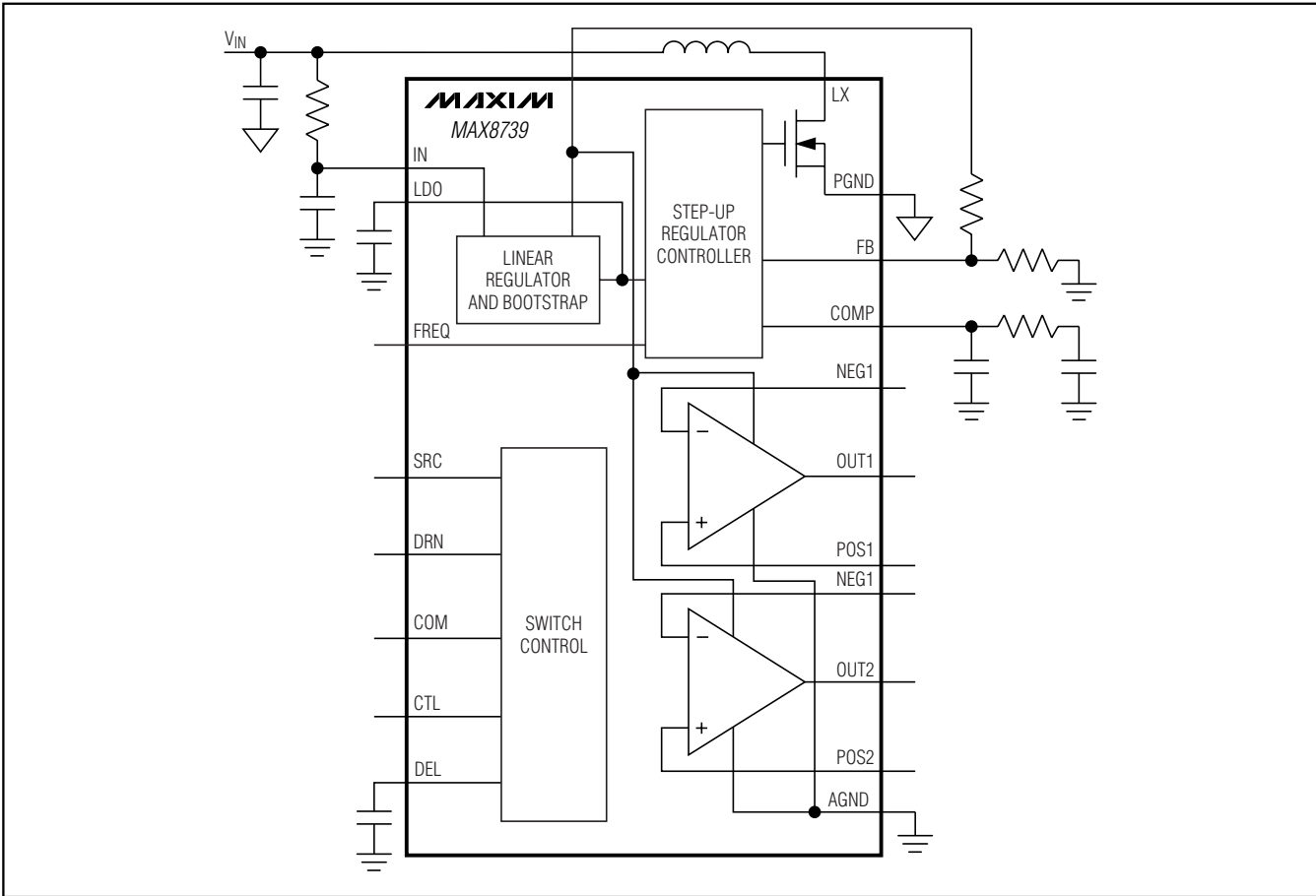


Figure 2. Functional Diagram

Table 1. Key Components List

DESIGNATION	DESCRIPTION
C1	10 $\mu$ F, 6.3V X5R ceramic capacitor (1206) TDK C3216X5ROJ106M
C2, C3	4.7 $\mu$ F, 10V X5R ceramic capacitors (1206) TDK C3216X5R1A475M
D1	3A, 30V Schottky diode (M-flat) Toshiba CMS02
D2, D3, D4	200mA, 100V, dual, ultra-fast diodes (SOT23) Fairchild MMBD4148SE
L1	3.0 $\mu$ H, 2.3A inductor Sumida CDRH6D12-3R0

## Detailed Description

The MAX8739 contains a high-performance, step-up switching regulator, two high-current operational amplifiers, and startup timing and level-shifting functionality useful for active-matrix TFT LCDs. Figure 2 shows the MAX8739 functional diagram.

### Main Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads found in source drivers of TFT LCD panels. The high-switching frequency (600kHz/1.2MHz) allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated, high-efficiency MOSFET and the IC's built-in digital soft-start functions reduce the number of external components required while controlling



# TFT, LCD, DC-DC Converter with Operational Amplifiers

uted series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A  $5\Omega$  to  $50\Omega$  resistor placed between  $OUT_+$  and the capacitive load reduces peaking but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between  $100\Omega$  and  $200\Omega$  and the typical value of the capacitor is  $10\text{pF}$ .

## Switch Control and Delay

A capacitor  $C_{DEL}$  (C8 in Figure 1), from DEL to AGND selects the switch-control block supply startup delay. After the LDO voltage exceeds its undervoltage lockout threshold ( $2.7\text{V}$  typ) and the soft-start routine for each

regulator is complete, a  $5\mu\text{A}$  current source charges  $C_{DEL}$ . Once the capacitor voltage exceeds  $V_{REF}$  ( $1.25\text{V}$  typ), COM can be connected to SRC or DRN through the internal p-channel switches, depending upon the state of CTL. Before startup and when  $IN$  is less than  $V_{UVLO}$ , DEL is internally connected to AGND to discharge  $C_{DEL}$ . Select  $C_{DEL}$  to set the delay time using the following equation:

$$C_{DEL} = \text{DELAY\_TIME} \times \frac{5\mu\text{A}}{1.25\text{V}}$$

The switch-control input (CTL) is not activated until all three of the following conditions are satisfied: the LDO voltage exceeds its undervoltage lockout voltage, the soft-start routine of all the regulators is complete, and  $V_{DEL}$  exceeds its turn-on threshold. Once activated and if CTL is high, the  $15\Omega$  internal p-channel switch between COM and SRC (Q1) turns on and the  $30\Omega$  p-channel switch between DRN and COM (Q2) turns off. If CTL is low, Q1 turns off and Q2 turns on.

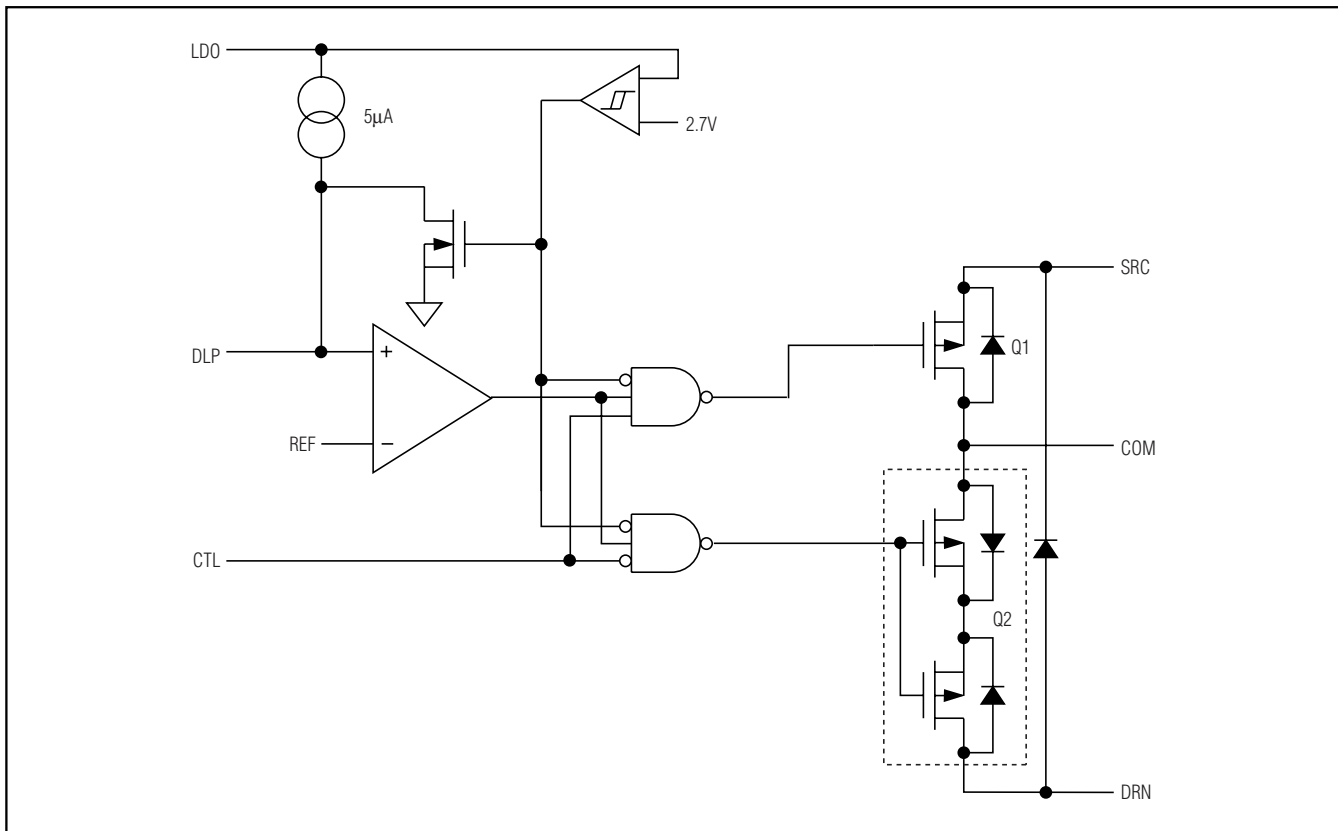


Figure 4. Switch Control

# TFT, LCD, DC-DC Converter with Operational Amplifiers

## Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit compares the input voltage at IN with the UVLO threshold (1.26V rising and 1.1V falling) to ensure that the input voltage is high enough for reliable operation. The 200mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator and the linear regulator outputs, disables the switch-control block, and the operational amplifier outputs are high impedance.

## Linear Regulator (LDO)

The MAX8739 includes an internal 5V linear regulator. SUP is the input of the linear regulator. The input voltage range is between 4.5V and 13V. The output of the linear regulator (LDO) is set to 5V (typ). The regulator powers all the internal circuitry including the gate driver. Bypass the LDO pin to AGND with a 0.22 $\mu$ F or greater ceramic capacitor. SUP should be directly connected to the output of the step-up regulator. This feature significantly improves the efficiency at low-input voltages.

## Bootstrapping and Soft-Start

The MAX8739 features bootstrapping operation. In normal operation, the internal linear regulator supplies power to the internal circuitry. The input of the linear regulator (IN) should be directly connected to the output of the step-up regulator. The MAX8739 is enabled when the input voltage at SUP is above 1.3V (typ) and the fault latch is not set. After being enabled, the regulator starts open-loop switching to generate the supply voltage for the linear regulator. The internal reference block turns on when the LDO voltage exceeds 2.7V (typ). When the reference voltage reaches regulation, the PWM controller and the current-limit circuit are enabled, and the step-up regulator enters soft-start. During soft-start, the main step-up regulator directly limits the peak-inductor current, allowing from zero up to the full current-limit value in eight equal current steps (ILIM/8). The maximum load current is available after the output voltage reaches regulation (which terminates soft-start), or after the soft-start timer expires in approximately 13ms. The soft-start routine minimizes the inrush current and voltage overshoot and ensures a well-defined startup behavior.

## Fault Protection

During steady-state operation, the MAX8739 monitors the FB voltage. If the FB voltage does not exceed 1V (typ), the MAX8739 activates an internal fault timer. If there is a continuous fault for the fault-timer duration, the MAX8739 sets the fault latch, shutting down all the

outputs. Once the fault condition is removed, cycle the input voltage to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time.

The MAX8739 monitors the SUP voltage for undervoltage and overvoltage conditions. If the SUP voltage is below 1.4V (max) or above 13.7V (typ), the MAX8739 disables the gate driver of the step-up regulator and prevents the internal MOSFET from switching. The SUP undervoltage and overvoltage conditions do not set the fault latch.

## Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds  $T_J = +160^\circ\text{C}$ , a thermal sensor immediately activates the fault protection, which shuts down the step-up regulator and the internal linear regulator, allowing the device to cool down. Once the device cools down by approximately  $15^\circ\text{C}$ , cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of  $T_J = +150^\circ\text{C}$ .

## Design Procedure

### Main Step-Up Regulator

#### Inductor Selection

The minimum inductance value, peak-current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very-high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and  $I^2R$  losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase  $I^2R$  losses in the inductor. Low-inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

## TFT, LCD, DC-DC Converter with Operational Amplifiers

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin, high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage ( $V_{IN}$ ), the maximum output current ( $I_{MAIN(MAX)}$ ), the expected efficiency ( $\eta_{TYP}$ ) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left( \frac{V_{IN}}{V_{MAIN}} \right)^2 \times \left( \frac{V_{MAIN} - V_{IN}}{I_{MAIN(MAX)} \times f_{OSC}} \right) \times \left( \frac{\eta_{TYP}}{LIR} \right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage  $V_{IN(MIN)}$  using conservation of energy and the expected efficiency at that operating point ( $\eta_{MIN}$ ) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{MAIN} - V_{IN(MIN)})}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX8739's LX current limit ( $I_{LIM}$ ) should exceed  $I_{PEAK}$  and the inductor's DC current rating should exceed

$I_{IN(DC,MAX)}$ . For good efficiency, choose an inductor with less than  $0.1\Omega$  series resistance.

Considering the *Typical Operating Circuit*, the maximum load current ( $I_{MAIN(MAX)}$ ) is 300mA, with an 8V output and a typical input voltage of 2.5V. Choosing an LIR of 0.4 and estimating efficiency of 85% at this operating point:

$$L = \left( \frac{2.5V}{8V} \right)^2 \times \left( \frac{8V - 2.5V}{0.3A \times 1.2MHz} \right) \times \left( \frac{0.85}{0.4} \right) \approx 3.0\mu H$$

Using the circuit's minimum input voltage (2.2V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.3A \times 8V}{2.2V \times 0.8} \approx 1.36A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{2.2V \times (8V - 2.2V)}{3.0\mu H \times 8V \times 1.2MHz} \approx 0.44A$$

$$I_{PEAK} = 1.36A + \frac{0.44A}{2} \approx 1.58A$$

### Output-Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}} \times \left( \frac{V_{MAIN} - V_{IN}}{V_{MAIN} \times f_{SW}} \right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} \times RESR$$

where  $I_{PEAK}$  is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by  $V_{RIPPLE(C)}$ . The voltage rating and temperature characteristics of the output capacitor must also be considered.

### Input-Capacitor Selection

The input capacitor ( $C_{IN}$ ) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10 $\mu$ F ceramic capacitor is used in the *Typical Application Circuit* (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source



# TFT, LCD, DC-DC Converter with Operational Amplifiers

impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically,  $C_{IN}$  can be reduced below the values used in the *Typical Application Circuit*. Ensure a low noise supply at IN by using adequate  $C_{IN}$ . Alternatively, greater voltage variation can be tolerated on  $C_{IN}$  if IN is decoupled from  $C_{IN}$  using an RC lowpass filter (see Figure 1).

## Rectifier Diode

The MAX8739's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode complements the internal MOSFET well.

## Output-Voltage Selection

The output voltage of the main step-up regulator can be adjusted by connecting a resistive voltage-divider from the output ( $V_{MAIN}$ ) to AGND with the center tap connected to FB (see Figure 1). Select R2 in the 10k $\Omega$  to 50k $\Omega$  range. Calculate R1 with the following equation:

$$R1 = R2 \times \left( \frac{V_{MAIN}}{V_{FB}} - 1 \right)$$

where  $V_{FB}$ , the step-up regulator's feedback set point, is 1.236V. Place R1 and R2 close to the IC.

## Loop Compensation

Choose  $R_{COMP}$  to set the high-frequency integrator gain for fast transient response. Choose  $C_{COMP}$  to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{315 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary  $R_{COMP}$  in 20% steps and  $C_{COMP}$  in 50% steps while observing transient response waveforms.

## Applications Information

### Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PC board copper area, other thermal mass, and airflow.

The MAX8739, with its exposed backside pad soldered to 1in<sup>2</sup> of PC board copper, can dissipate about 1.7W into +70°C still air. More PC board copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and the power dissipated by the operational amplifiers.

### Step-Up Regulator

The largest portions of power dissipation in the step-up regulator are the internal MOSFET, inductor, and the output diode. If the step-up regulator has 90% efficiency, about 3% to 5% of the power is lost in the internal MOSFET, about 3% to 4% in the inductor, and about 1% in the output diode. The remaining 1% to 3% is distributed among the input and output capacitors and the PC board traces. If the input power is about 5W, the power lost in the internal MOSFET is about 150mW to 250mW.

### Operational Amplifier

The power dissipated in the operational amplifiers depends on their output current, the output voltage, and the supply voltage:

$$P_{DSOURCE} = I_{OUT\_SOURCE} \times (V_{SUP} - V_{OUT\_})$$

$$P_{DSINK} = I_{OUT\_SINK} \times V_{OUT\_}$$

where  $I_{OUT\_SOURCE}$  is the output current sourced by the operational amplifier, and  $I_{OUT\_SINK}$  is the output current that the operational amplifier sinks.

In a typical case where the supply voltage is 10V and the output voltage is 5V with an output source current of 30mA, the power dissipated is 150mW.

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## PC Board Layout and Grounding

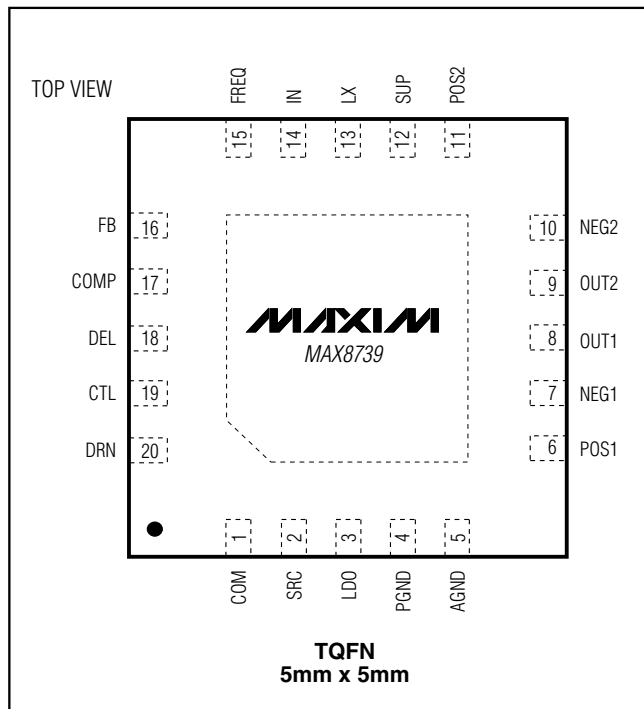
Careful PC board layout is important for proper operation. Use the following guidelines for good PC board layout:

- 1) Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- 2) Create a power-ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power-ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier-divider ground connections, the COMP and DEL capacitor ground connections, the SUP and LDO bypass capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
- 3) Place the feedback-voltage-divider resistors as close to the feedback pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX or the switching nodes in the charge pumps.

- 4) Place IN pin and LDO pin bypass capacitors as close to the device as possible. The ground connections of the IN and LDO bypass capacitors should be connected directly to the AGND pin with a wide trace.
- 5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- 6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as shield if necessary.

Refer to the MAX8739 evaluation kit for an example of proper board layout.

## Pin Configuration



## Chip Information

TRANSISTOR COUNT: 4396

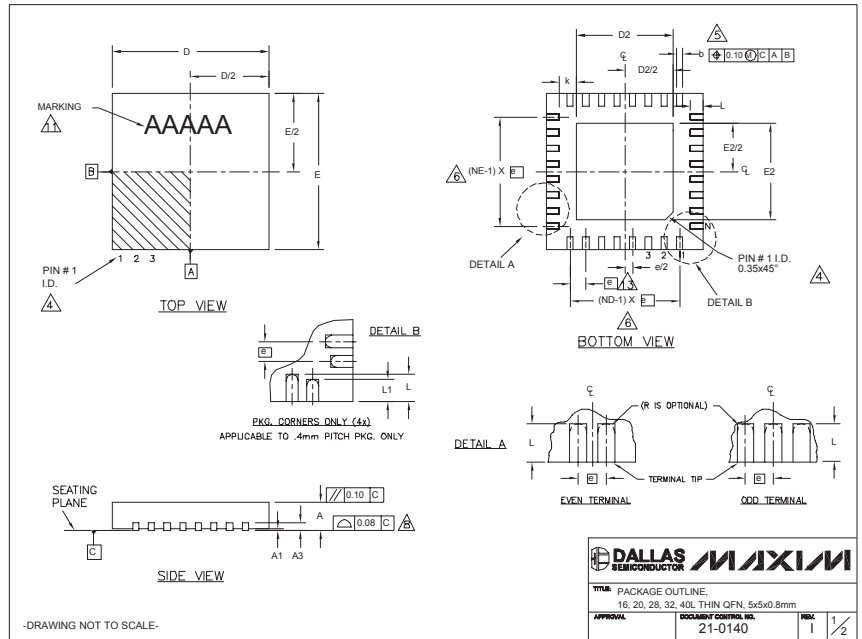
PROCESS: BICMOS

# TFT, LCD, DC-DC Converter with Operational Amplifiers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX8739



COMMON DIMENSIONS															
PKG. SYMBOL	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16	-	-	20	-	-	28	-	-	32	-	-	40	-	-
ND	4	-	-	5	-	-	7	-	-	8	-	-	10	-	-
NE	4	-	-	5	-	-	7	-	-	8	-	-	10	-	-
JEDEC	WHHB	-	-	WHHC	-	-	WHHD-1	-	-	WHHD-2	-	-	----	-	-

EXPOSED PAD VARIATIONS												
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			±0.15			
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES*				
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO				
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO				
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES				
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO				
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES				
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES				
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES				
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO				
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO				
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES				
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES				
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO				
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES				
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO				
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES				
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO				
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES				

NOTES:  
 1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.  
 2. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.  
 3. N IS THE TOTAL NUMBER OF TERMINALS.  
 \* THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SFP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.  
 Δ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.  
 Δ ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.  
 7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.  
 Δ COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.  
 9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.  
 Δ WARPAGE SHALL NOT EXCEED 0.10 mm.  
 11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.  
 12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.  
 Δ LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

**DALLAS SEMICONDUCTOR MAXIM**  
 PACKAGE OUTLINE  
 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm  
 APPROVAL: 21-0140

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