

ASSP

1 CHANNEL 8-BIT A/D CONVERTER

MB40528

■ DESCRIPTION

The MB40528 is a full parallel comparison (flash) type 8-bit resolution analog-to-digital converter, designed for various video and image processing applications.

The MB40528 has 8-bit resolution 1 channel A/D converter. Input analog data are converted into digital data by the A/D converter in minimum 60 Mega samples per seconds (MSPS).

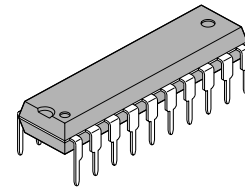
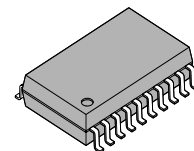
The analog data is provided in a range of DC +3V to +5V (2Vp-p level) and the output digital data in TTL level.

The MB40528 is fabricated by the Fujitsu's advanced bipolar process and housed in a 20-pin plastic DIP/SOP.

The MB40528 is suitable for various video and image applications.

■ FEATURES

- Conversion method : Full parallel comparison type
- 8-bit x 1 channel A/D converter :
- Max. 60 MHz input clock frequency providing 60 MSPS data conversion rate
- Linearity error : Typical +/-0.15%
- Analog input voltage range : 3V to 5V (2Vp-p level)
- Digital input/output voltage level : TTL level
- On-chip reference voltage generator
- Low power consumption : Typical 400mW
- Single +5V power supply
- Operating temperature range : -20°C to +70°C
- Fujitsu's advanced bipolar process
- Package options :
 - 20-pin plastic DIP (Suffix : -P)
 - 20-pin plastic SOP (Suffix : -PF)

MB40528P**PLASTIC PACKAGE
(DIP-20P-M01)****MB40528PF****PLASTIC PACKAGE
(FPT-20P-M05)**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Figure 1. Pin Assignment

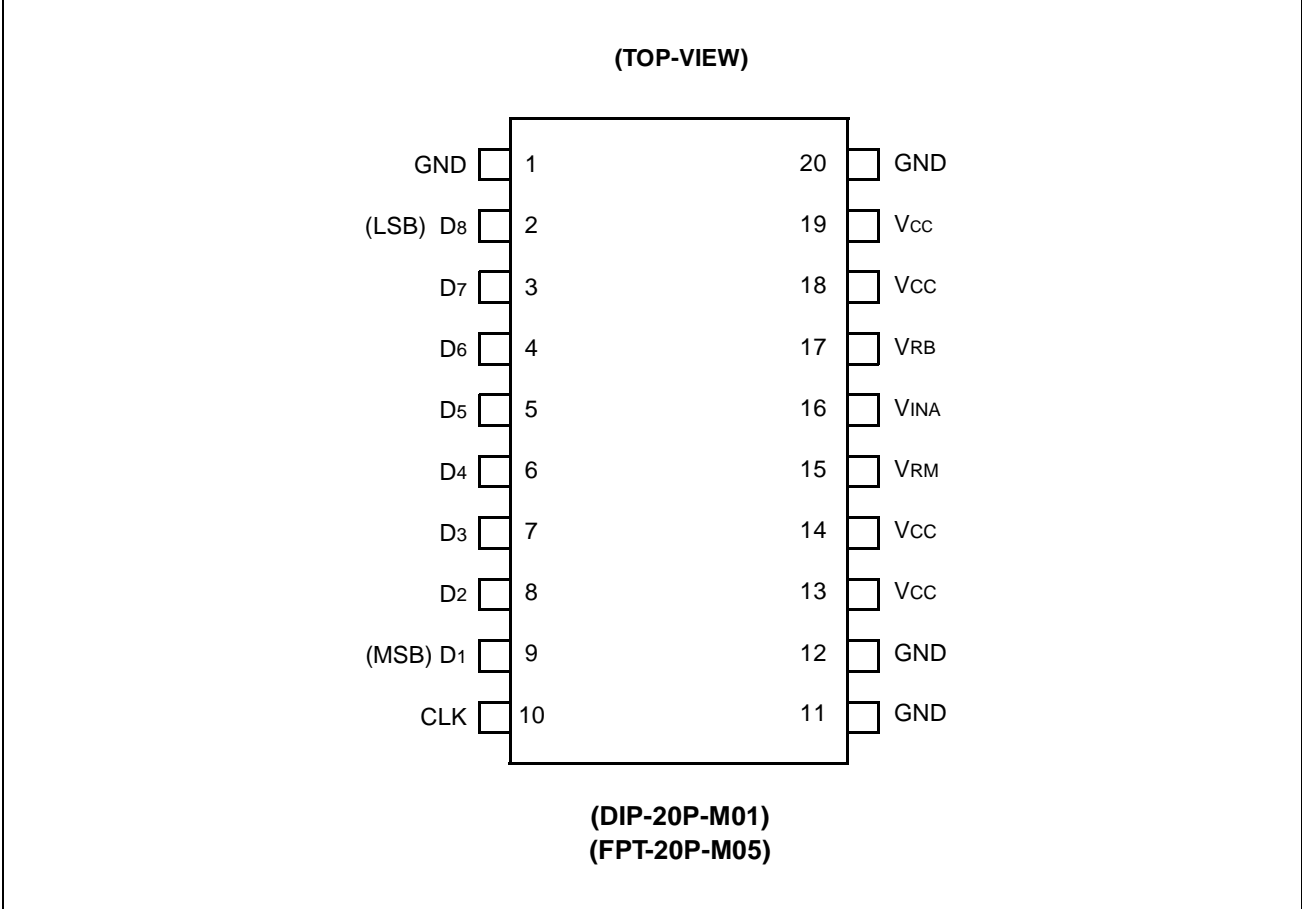
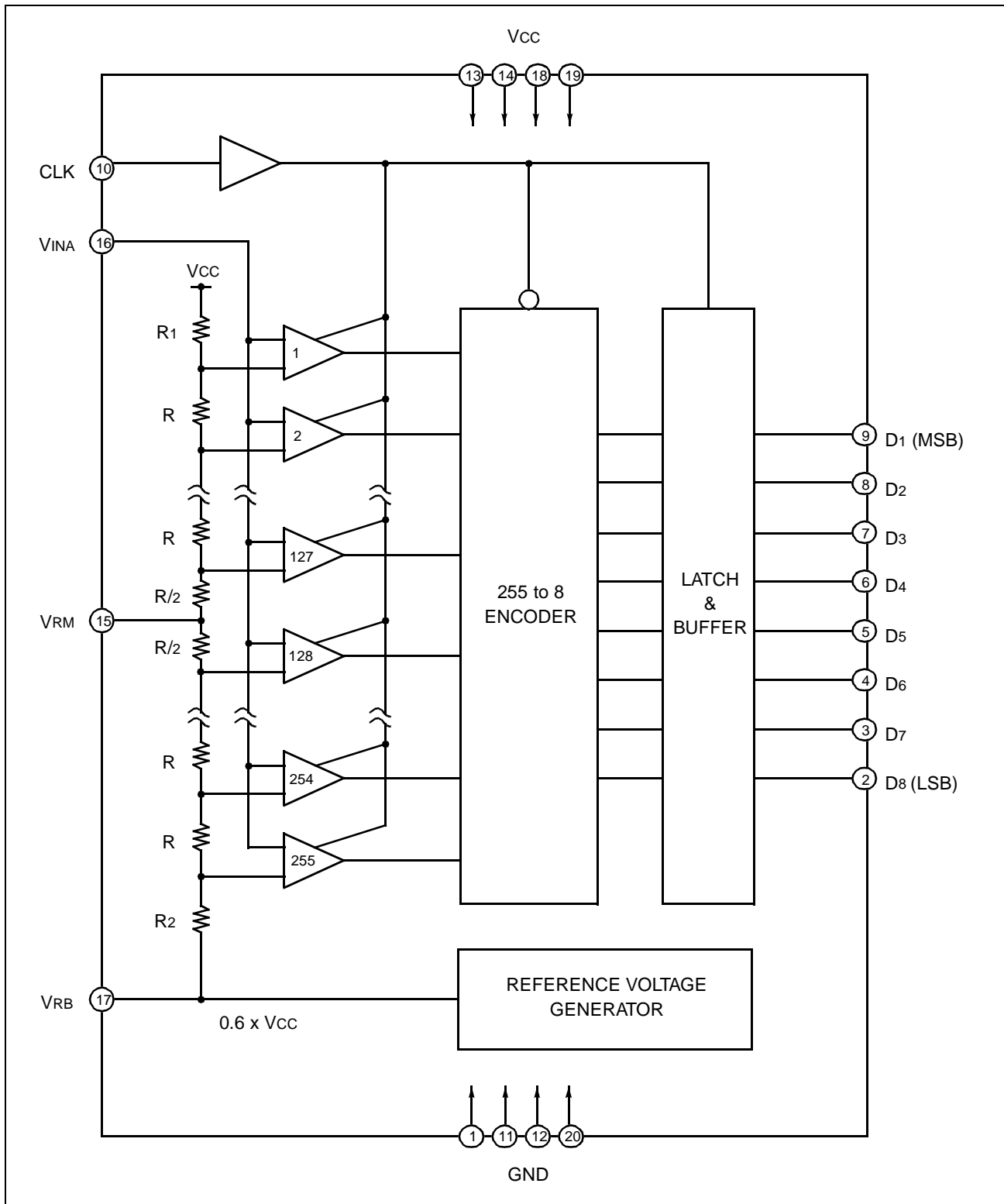


Figure 2. Block Diagram



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■ PIN DESCRIPTION

Table 1 lists the pin description of the MB40528.

Table.1 Pin Description

Symbol	Pin No.	Type	Name & Function
Power Supply			
VCC	13, 14, 18, 19	-	+5 V DC power supply pins.
GND	1, 11, 12, 20	-	Ground pins.
Clock			
CLK	10	I	Clock input pin. The input voltage is a TTL level.
Analog Input			
VINA	16	I	Analog signal input pin. The analog data to be converted is input to this pin. The input voltage range is 3V to 5V (VRB to VCC).
Digital Output			
D1	2	O	8-bit resolution A/D converter outputs. The output voltage is a TTL level. Also, D1 pin is an MSB and D8 pin is a LSB.
D2	3		
D3	4		
D4	5		
D5	6		
D6	7		
D7	8		
D8	9		
Reference Voltage Output			
VRB	17	O	Reference voltage output pin. This pin outputs $0.6 \times VCC$ [V] (Typ. 3V). An $1\mu\text{F}$ or more capacitor having superior frequency characteristic should be connected to this pin. The capacitor must be connected near the device.
Others			
VRM	15	O	An intermediate voltage output pin. An intermediate voltage between VCC and VRB (Typ. 4V) is output from this pin. Normally this pin is left open.

■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

(GND = 0V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	VCC	–	-0.5 ~ +7.0	v
Analog Input Voltage	VINA	–	-0.5 ~ VCC +0.5	v
Digital Input Voltage	VIND	–	-0.5 ~ +7.0	v
Storage Temperature	Tstg	–	-55 ~ +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

(GND = 0V)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	VCC	–	4.75	5.00	5.25	V
Analog Input Voltage	VINA	–	VRB	–	VCC	V
Digital “H” Level Input Voltage	VIHD	–	2.0	–	–	V
Digital “L” Level Input Voltage	VILD	–	–	–	0.8	V
Digital “H” Level Output Current	IOH	–	-400	–	–	μA
Digital “L” Level Output Current	IOL	–	–	–	1.6	mA
Clock Frequency	fCLK	–	–	–	60	MHz
Minimum Clock “H” Level Pulse Width	twH	–	7.0	–	–	ns
Minimum Clock “L” Level Pulse Width	twL	–	8.0	–	–	ns
Operating Ambient Temperature	Top	–	-20	–	70	°C

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■ ELECTRICAL CHARACTERISTICS

(RECOMMENDED OPERATING CONDITIONS OTHERWISE NOTED)

1. DC CHARACTERISTICS

(1) Analog Block

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Resolution	–	–	–	8	–	bit
Linearity Error	LE	DC Accuracy	–	±0.15	±0.3	%
Differential Linearity Error	DLE	DC Accuracy	–	0.12	–	%
Analog Input Equivalent Resister	RINA	–	0.2	1.5	–	MΩ
Analog Input Capacitance	CINA	–	–	40	–	pF
Analog "H" Level Input Current	I _{IHA}	V _{INA} = V _{CC}	–	–	210	μA
Analog "L" Level Input Current	I _{I_{LA}}	V _{INA} = V _{REF}	–	–	200	μA
Reference Voltage	VRB	–	0.6V _{CC} -0.1	0.6V _{CC}	0.6V _{CC} +0.1	V
Supply Current	I _{CC}	–	–	80*	150	mA

* : V_{CC} = 5.0V, T_a = +25°C

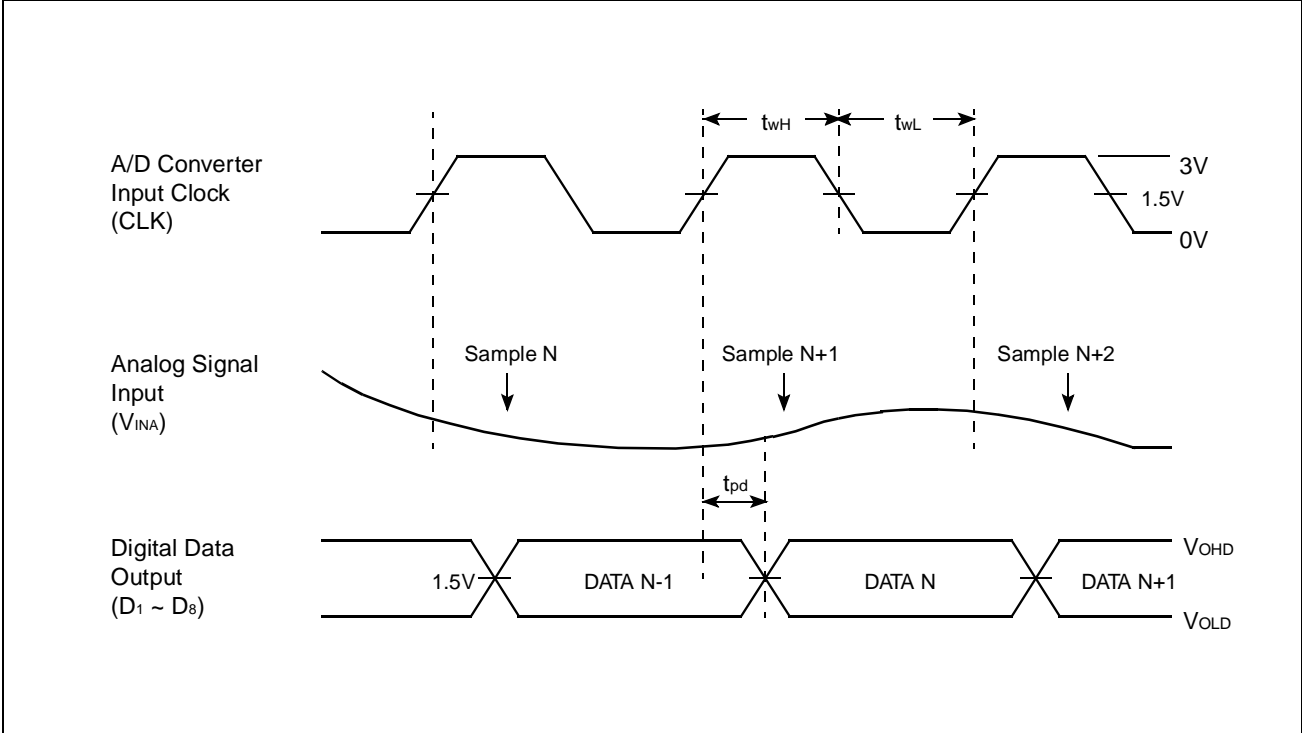
(1) Digital Block

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Digital "H" Level Output Voltage	V _{OHD}	I _{OH} = -400μA	2.7	–	–	V
Digital "L" Level Output Voltage	V _{OLD}	I _{OL} = 1.6mA	–	–	0.4	V
Digital "H" Level Input Voltage	V _{IHD}	–	2.0	–	–	V
Digital "L" Level Input Voltage	V _{ILD}	–	–	–	0.8	V
Digital "H" Level Input Current	I _{IHD}	–	–	–	20	μA
Digital "L" Level Input Current	I _{ILD}	–	-100	–	–	μA

2. AC CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Maximum Conversion Rate	f _s	–	60	–	–	MSPS
Digital Output Delay Time	t _{pd}	–	5.0	8.5	15	ns

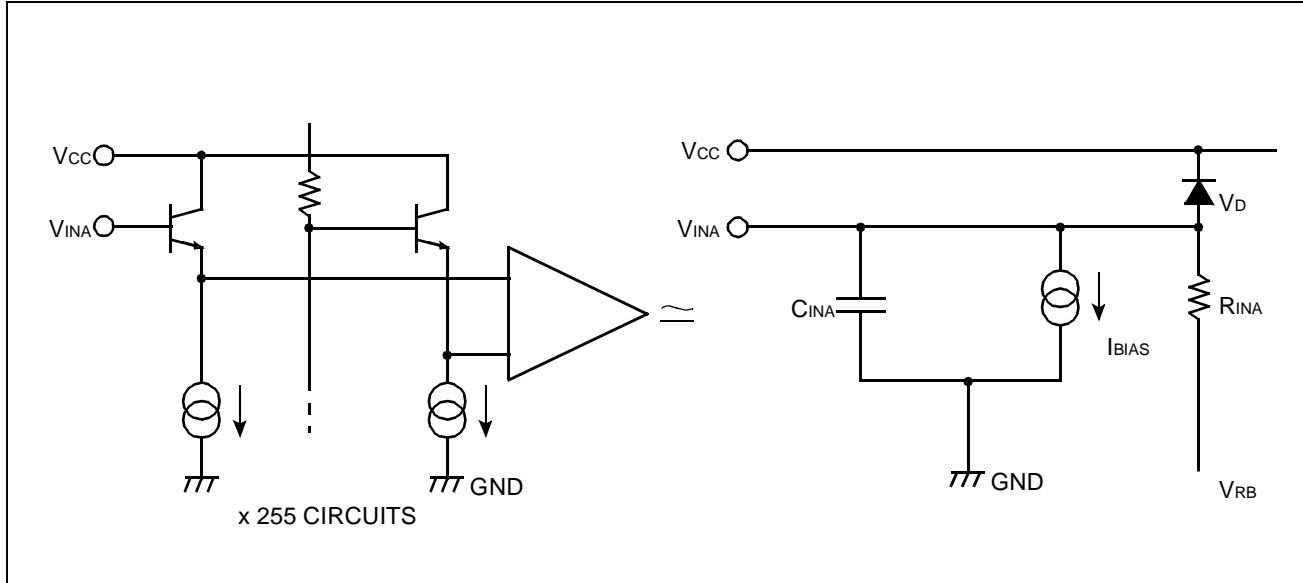
Figure 3. AC Timing Chart



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■ EQUIVALENT CIRCUITS

Figure 4. Analog Input Equivalent Circuit



CINA: Non-linear Emitter-follower Junction Capacitance

RINA: Linear Resistance Model for Input Current Transition by Comparator Switching:
finite value for $V_{INA} < V_{RB}$ or when CLK=High

VRB: Voltage at VRB pin (Not the VRB pin itself)

IBIAS: Constant Input Bias Current

VD: The base-collector junction diode of emitter-follower transistor.

Figure 5. Reference Voltage Circuit

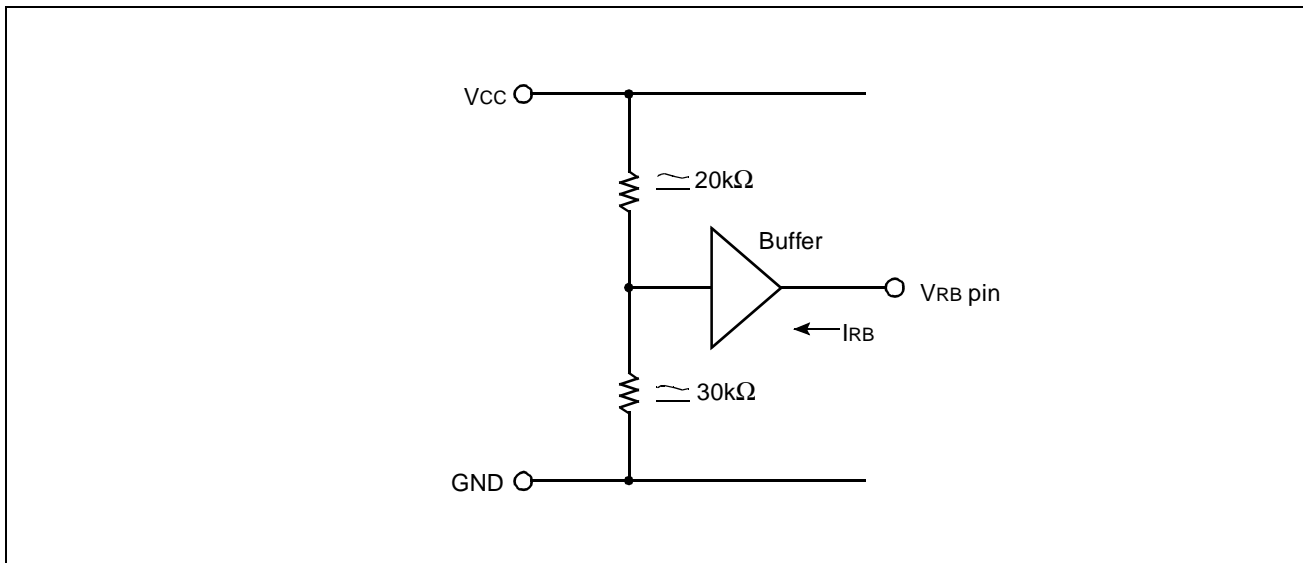


Figure 6. Digital Input Equivalent Circuit

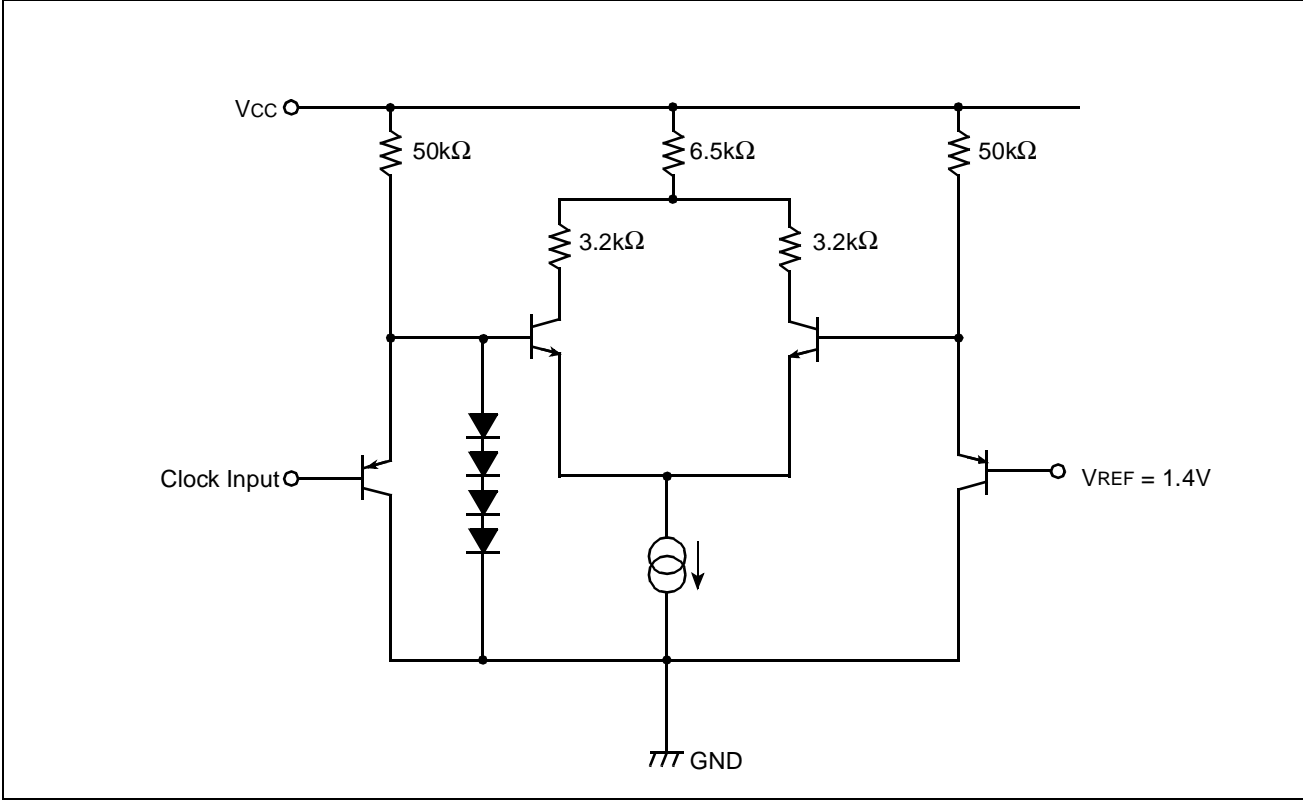
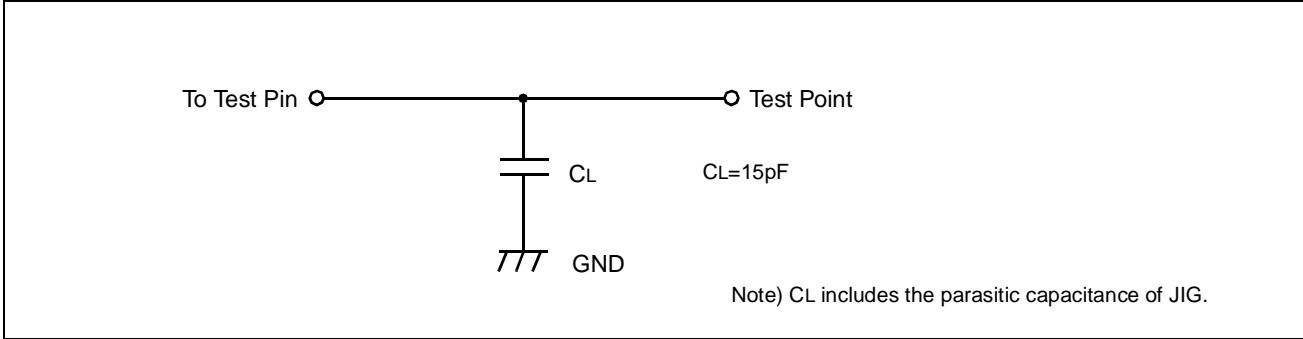


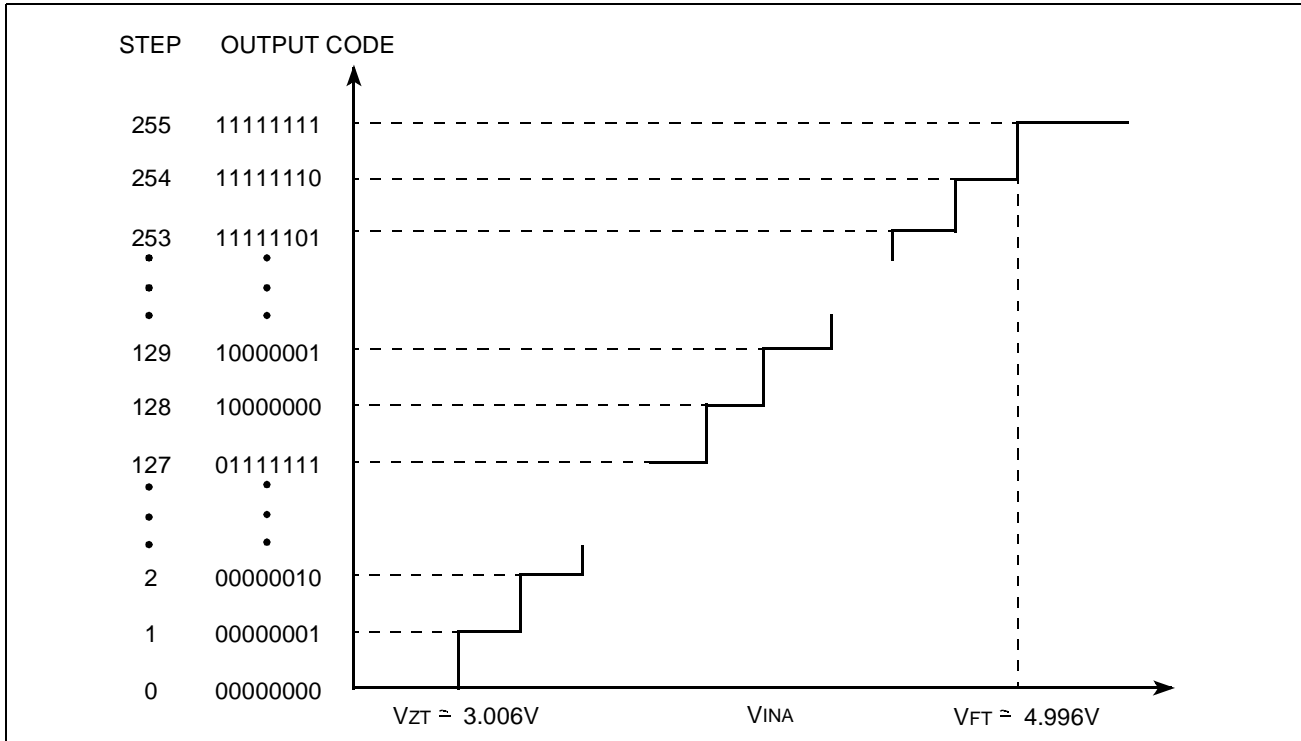
Figure 7. Output Buffer Load Circuit



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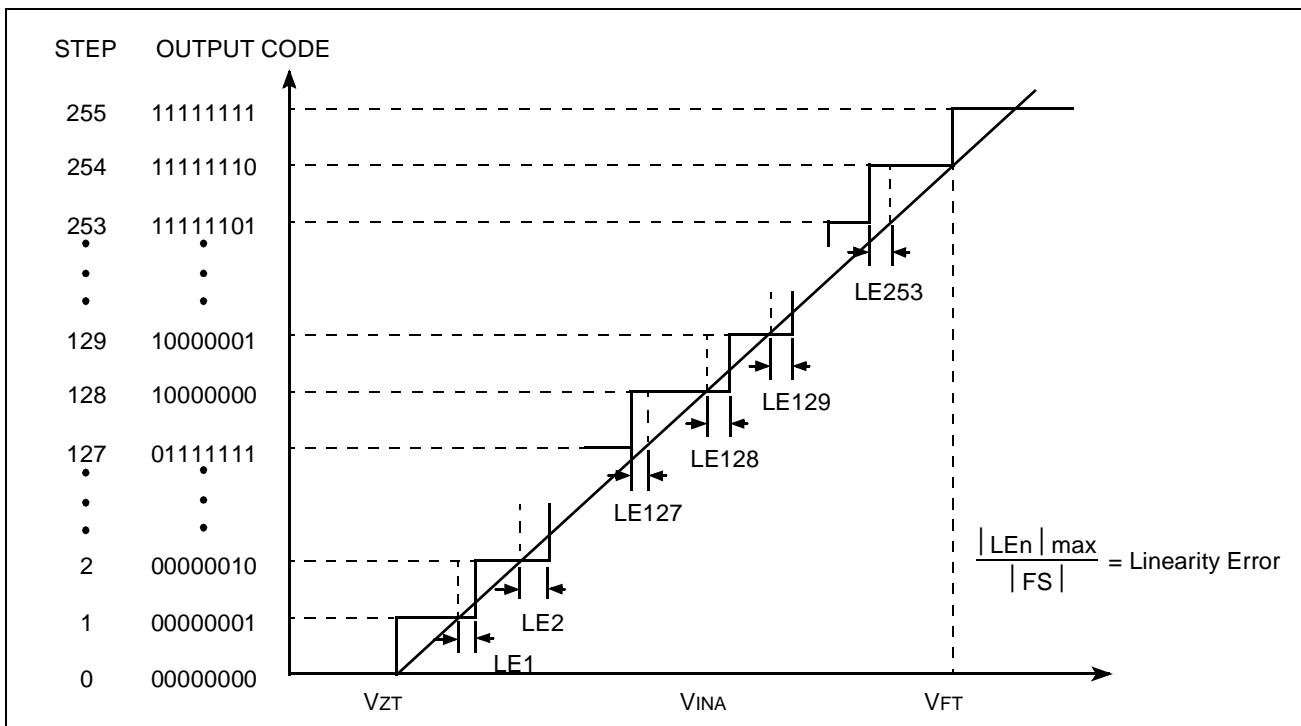
■ LINEARITY ERROR

1. Ideal Conversion Characteristic



VZT and VFT are the typical values when VCC = 5V and VRB = 3V.

2. Actual Conversion Characteristic



(NOTE) Refer to RECOMMENDED OPERATING CONDITIONS for a range of VINA inputs.

■ NOTES ON USE

1. Power Supply Patterns of the PCB

The power supply wire patterns (V_{CC} and GND patterns) of the PCB should be designed as wide as possible in order to reduce parasitic impedance.

Also, the V_{CC} and GND patterns which are connected to the V_{CC} and GND pins of the device must be handled and designed as analog system pattern and so, their circuit patterns must be separate from digital system patterns of other peripheral devices.

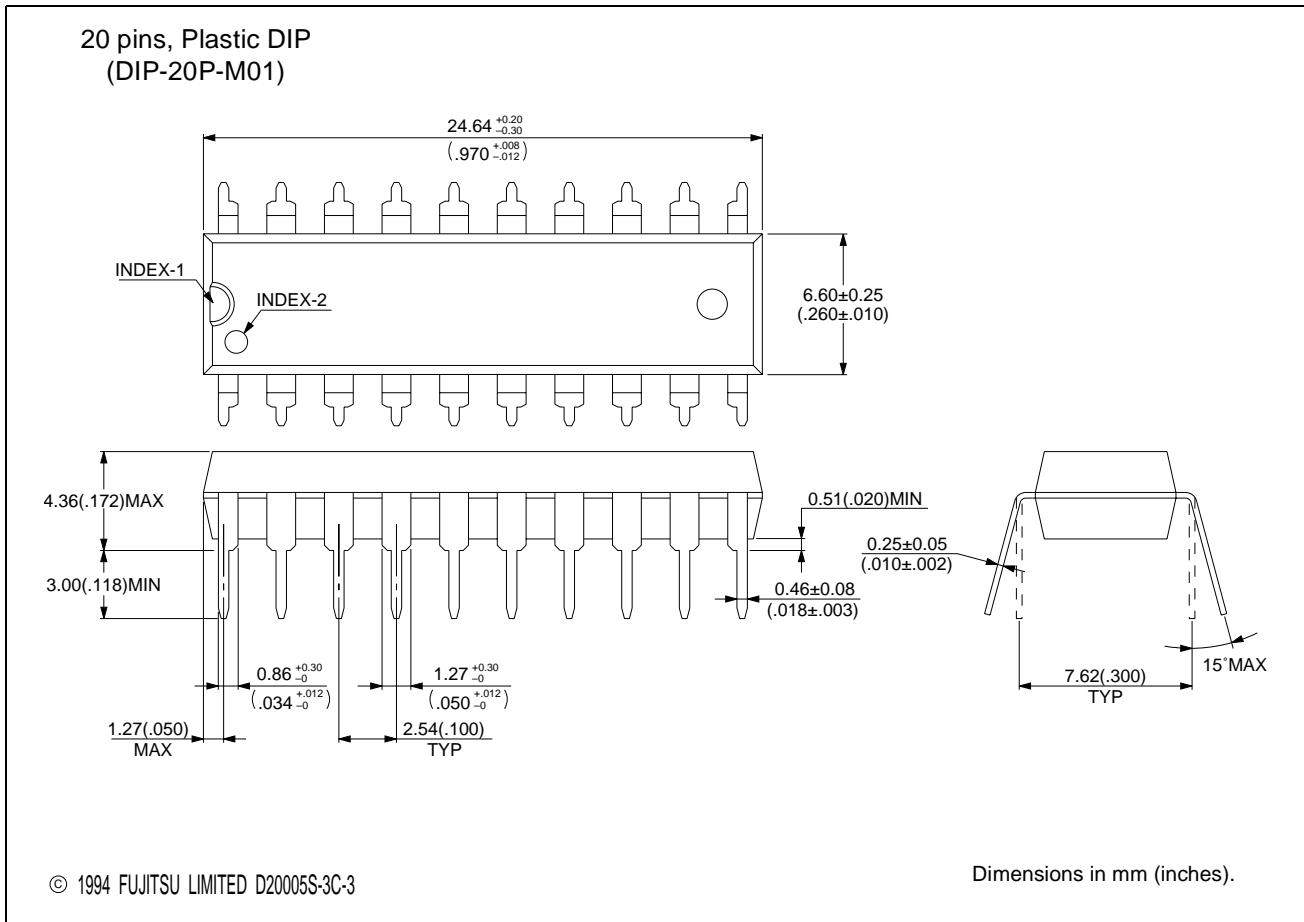
2. Switching Noise

In order to reduce switching noise as much as possible, high-frequency bypass capacitor must be connected between V_{CC} and GND pins and V_{RB} and GND pins.

In this case, the capacitor should be connected to the pins as near as possible.

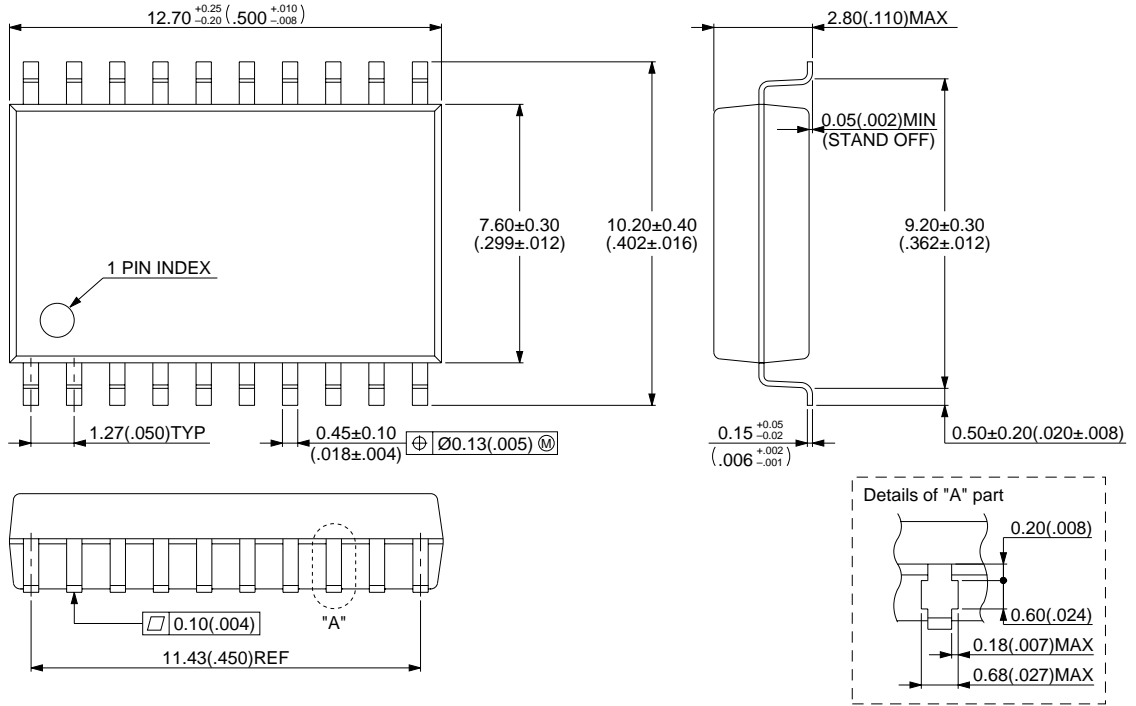
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■ PACKAGE DIMENSIONS



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20 pins, Plastic SOP
(FPT-20P-M05)



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Dimensions in mm (inches).

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