

ASSP For Video Applications

CMOS

8-bit 100 MSPS A/D Converter

MB40C328

■ DESCRIPTION

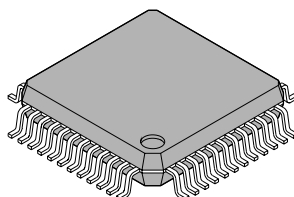
MB40C328 is a high-speed A/D converter using a fast CMOS technology.

■ FEATURES

- Resolution : 8 bit
- Linearity error : $\pm 0.40\%$ (standard)
- Maximum conversion rate : 100 MSPS (minimum)
- Power supply voltage : 3.3 V single (standard)
- Digital input/output voltage range : CMOS level compatible
- Analog input voltage range : 0 to 3.0 V (2 Vp-p)
- Analog input capacitance : 22 pF (standard)
- Power dissipation : 210 mW (standard)
- Additional features : Reference voltage generator circuit: $V_{\text{REFT}} = 3.0 \text{ V}$, $V_{\text{REFB}} = 1.0 \text{ V}$
High impedance output, power down function
1:2 demultiplex output enable (RESET action enable)
1/2 deviding clock output
Cross sampling at 50 MHz (two-phase CLK) enable (CLKA, CLKB)
- Package : LQFP48 (7 mm \times 7 mm, lead pitch 0.5 mm)

■ PACKAGE

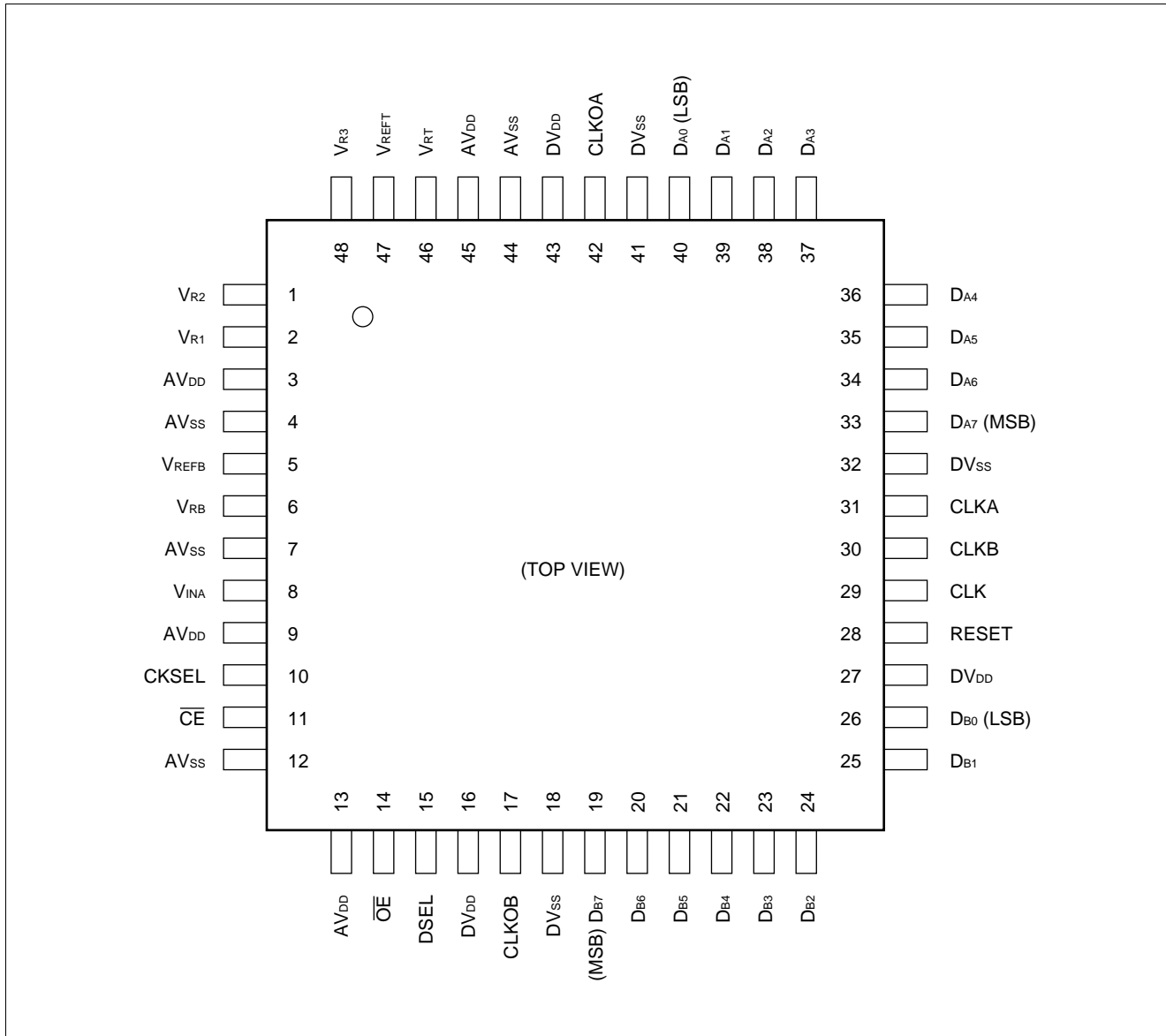
48-pin plastic LQFP



(FPT-48P-M05)

MB40C328

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

| Pin No. | Symbol | Description |
|--------------|------------------------------------|---|
| 3, 9, 13, 45 | AV _{DD} | Analog power supply (+3.3 V) |
| 16, 27, 43 | DV _{DD} | Digital power supply (+3.3 V) |
| 4, 7, 12, 44 | AV _{SS} | Analog power supply ground pin (0 V) |
| 18, 32, 41 | DV _{SS} | Digital power supply ground pin (0 V) |
| 33 to 40 | DA ₇ to DA ₀ | Digital output pin (Port A) DA ₇ : MSB, DA ₀ : LSB |
| 19 to 26 | DB ₇ to DB ₀ | Digital output pin (Port B) DB ₇ : MSB, DB ₀ : LSB |
| 11 | $\overline{\text{CE}}$ | Power down at $\overline{\text{CE}}$ input "H" (internal pull-up resistor) |
| 14 | $\overline{\text{OE}}$ | Digital output (Both Port A, B) and clock output (CLKOA, CLKOB) are high impedance at $\overline{\text{OE}}$ input "H". |
| 10 | CKSEL | Mode of operation setting input pin (Refer to ■ MODE SETTING) |
| 15 | DSEL | |
| 28 | RESET | Dividing circuit reset input pin (See ■ TIMING CHART 2, 3) |
| 29 | CLK | Clock input pin (max 100 MHz) |
| 31 | CLKA | A ch clock input pin (max 50 MHz) |
| 30 | CLKB | B ch clock input pin (max 50 MHz) |
| 42 | CLKOA | Clock output pin (See ■ TIMING CHART 1 to 4) |
| 17 | CLKOB | Clock output pin (See ■ TIMING CHART 1 to 4) |
| 8 | V _{INA} | Analog input pin Input range is V _{RT} to V _{RB} (0 V to 3.0 V: 2 Vp-p) |
| 2 | V _{R1} | Reference 1/4 voltage output pin (Add 0.1 μF for AV _{SS}) Reference 1/2 voltage output pin (Add 0.1 μF for AV _{SS}) Reference 3/4 voltage output pin (Add 0.1 μF for AV _{SS}) |
| 1 | V _{R2} | |
| 48 | V _{R3} | |
| 46 | V _{RT} | Reference voltage input pin on top side |
| 47 | V _{REFT} | Reference voltage output pin By connecting to V _{RT} , 0.9 × AV _{DD} (≒ 3 V) is generated. |
| 6 | V _{RB} | Reference voltage input pin on bottom side |
| 5 | V _{REFB} | Reference voltage output pin By connecting to V _{RB} , 0.3 × AV _{DD} (≒ 1 V) is generated. |

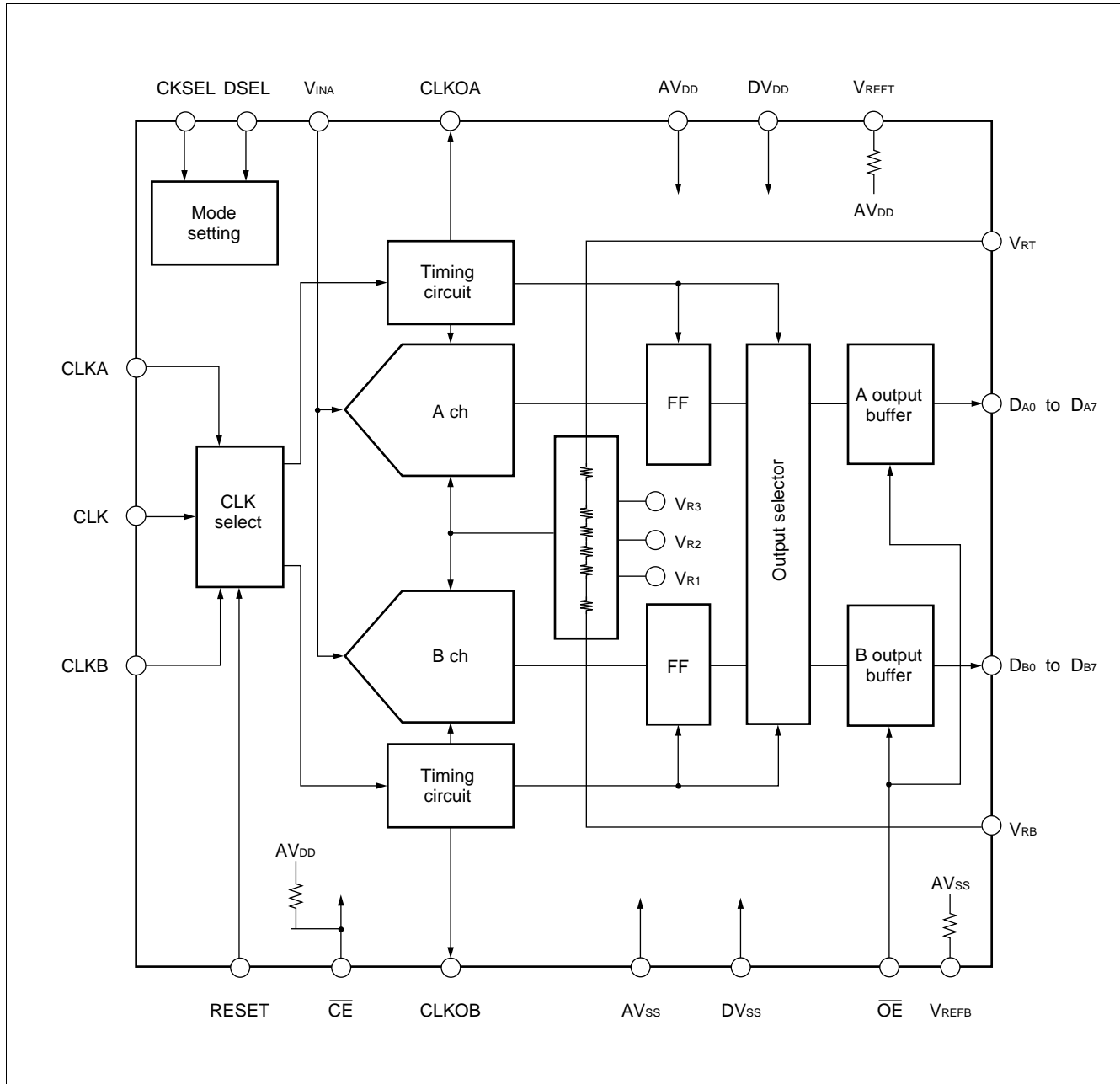
The values in parentheses are standard.

■ PRECAUTIONS ON USE

- Be sure to ground the pins of AV_{DD}, DV_{DD}, V_{RT}, V_{RB}, V_{R1}, V_{R2}, and V_{R3} via high-frequency capacitor. Place the high-frequency capacitor as close as possible to the pin.
- To avoid generation of undesired current owing to indetermination of internal logic, set $\overline{\text{CE}}$ to "H" at powering on and input more than five clock pulses just after operation ($\overline{\text{CE}}$: "H" → "L").

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■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|----------------------|---|--------|-----------------|------|
| | | Min. | Max. | |
| Power supply voltage | AV_{DD}, DV_{DD} | -0.3 | +4.0 | V |
| Input/output voltage | $V_{INA}, V_{RT}, V_{RB}, V_{REFT}, V_{REFB}, V_{R1}, V_{R2}, V_{R3}, \overline{CE}, CKSEL$ | -0.3 | $AV_{DD}+0.3^*$ | V |
| | DA_0 to DA_7, DB_0 to $DB_7, CLKOA, CLKOB, CLKA, CLKB, CLK, DSEL, \overline{OE}, RESET$ | -0.3 | $DV_{DD}+0.3^*$ | V |
| Storage temperature | T_{STG} | -55 | +125 | °C |

* : Do not exceed +4.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|--|---|-----------------|------|----------|-------------|
| | | Min. | Typ. | Max. | |
| Power supply voltage | AV_{DD}, DV_{DD} | 3.00 | 3.30 | 3.60 | V |
| Analog input voltage | V_{INA} | V_{RB} | — | V_{RT} | V |
| Analog reference voltage: T | V_{RT} | — | — | 3.00 | V |
| Analog reference voltage: B | V_{RB} | 0.00 | — | — | V |
| Analog reference voltage range | $V_{RT} - V_{RB}$ | 1.90 | 2.00 | 2.10 | V |
| Digital "H" level input voltage | $\overline{OE}, DSEL, RESET, CLK, CLKA, CLKB$ | $DV_{DD} - 0.5$ | — | — | V |
| | $CKSEL, \overline{CE}$ | $AV_{DD} - 0.5$ | — | — | V |
| Digital "L" level input voltage | $\overline{OE}, DSEL, RESET, CLK, CLKA, CLKB$ | — | — | 0.5 | V |
| | $CKSEL, \overline{CE}$ | — | — | 0.5 | V |
| Digital input current | I_{ID} | -20 | — | 5 | μA |
| Single-phase clock frequency | f_{CLK} | 0.1 | — | 100 | MHz |
| Two-phase clock frequency | f_{CLKA}, f_{CLKB} | 0.1 | — | 50 | MHz |
| Minimum clock pulse width (single-phase) | t_{WS}^+, t_{WS}^- | 4.0 | 5.0 | — | ns |
| Minimum clock pulse width (two-phase) | t_{WD}^+, t_{WD}^- | 8.0 | 10.0 | — | ns |
| Clock pulse rising/falling time | t_r, t_f | — | 2.0 | — | ns |
| RESET signal setup time | t_s | 3.0 | — | — | ns |
| RESET signal hold time | t_h | 3.0 | — | — | ns |
| Operating temperature range | T_a | -20 | — | 70 | $^{\circ}C$ |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics in Analog Section

($A_{V_{DD}} = D_{V_{DD}} = 3.00\text{ V to }3.60\text{ V}$, $T_a = -20^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit |
|------------------------------|------------|-----------------------|-----------------------|-----------------------|------|
| | | Min. | Typ. | Max. | |
| Resolution | — | — | 8 | — | bit |
| Linearity error | LE | — | ± 0.40 | ± 0.6 | % |
| Differential linearity error | DLE | — | ± 0.20 | ± 0.36 | % |
| Analog input capacity | C_{INA} | — | 22 | — | pF |
| Reference voltage: T | V_{REFT} | $0.88 \times AV_{DD}$ | $0.91 \times AV_{DD}$ | $0.94 \times AV_{DD}$ | V |
| Reference voltage: B | V_{REFB} | $0.27 \times AV_{DD}$ | $0.3 \times AV_{DD}$ | $0.33 \times AV_{DD}$ | V |
| Reference current | I_{RB} | -15 | -10 | — | mA |
| Analog supply current | A_{DD} | — | 42.0 | 85.0 | mA |
| Digital supply current | D_{DD} | — | 20.0 | 40.0 | mA |
| Standby current | I_{SB} | — | 100 | — | mA |

• DC Characteristics in Digital Section

($A_{V_{DD}} = D_{V_{DD}} = 3.00\text{ V to }3.60\text{ V}$, $T_a = -20^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit |
|----------------------------------|-----------|--------------------|------|--------------|---------------|
| | | Min. | Typ. | Max. | |
| Digital "H" level output voltage | V_{OHD} | $D_{V_{DD}} - 0.4$ | — | $D_{V_{DD}}$ | V |
| Digital "L" level output voltage | V_{OLD} | — | — | 0.4 | V |
| Digital "H" level output current | I_{OHD} | -400 | — | — | μA |
| Digital "L" level output current | I_{OLD} | — | — | 1.6 | mA |

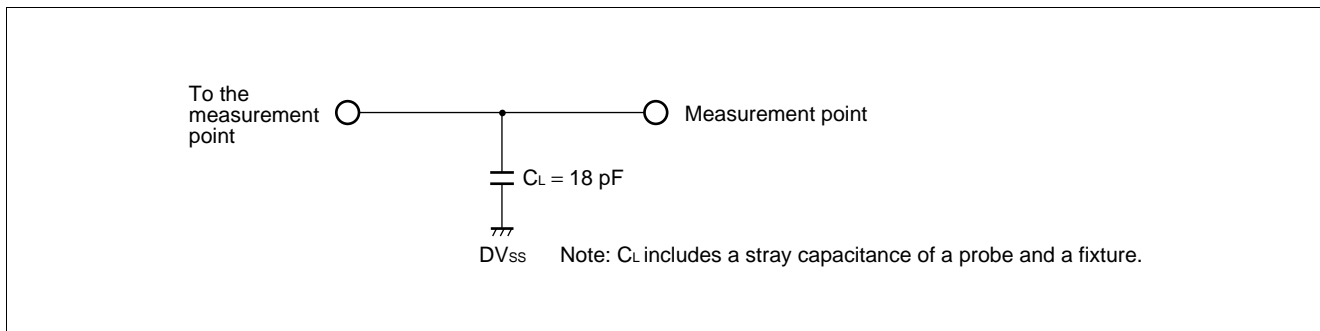
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• Switching Characteristics

($A_{V_{DD}} = DV_{DD} = 3.00\text{ V to }3.60\text{ V}$, $T_a = -20^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | | Symbol | Value | | | Unit |
|---------------------------|----------------|-------------|------------------|------------------|-----------------|------|
| | | | Min. | Typ. | Max. | |
| Maximum conversion rate | | f_s | 100 | — | — | MSPS |
| Aperture time | | t_{AD} | — | 1.7 | — | ns |
| Digital output delay time | Timing chart 1 | t_{pdS} | 2.5 | 6.0 | 9.0 | ns |
| | | t_{pdSO} | $t_{ws}^+ + 2.5$ | $t_{ws}^+ + 6.0$ | $t_{ws}^+ + 10$ | ns |
| | Timing chart 2 | t_{pdM1} | 2.5 | 5.5 | 10 | ns |
| | | t_{pdM1O} | $T + 2.5$ | $T + 5.5$ | $T + 10$ | ns |
| | Timing chart 3 | t_{pdM2} | 2.5 | 5.5 | 10 | ns |
| | | t_{pdM2O} | $T + 2.5$ | $T + 5.5$ | $T + 10$ | ns |
| | Timing chart 4 | t_{pdD} | 2.5 | 6.5 | 11 | ns |
| | | t_{pdDO} | $t_{wD}^+ + 2.5$ | $t_{wD}^+ + 6.5$ | $t_{wD}^+ + 11$ | ns |

■ DIGITAL OUTPUT BUFFER LOAD CIRCUIT



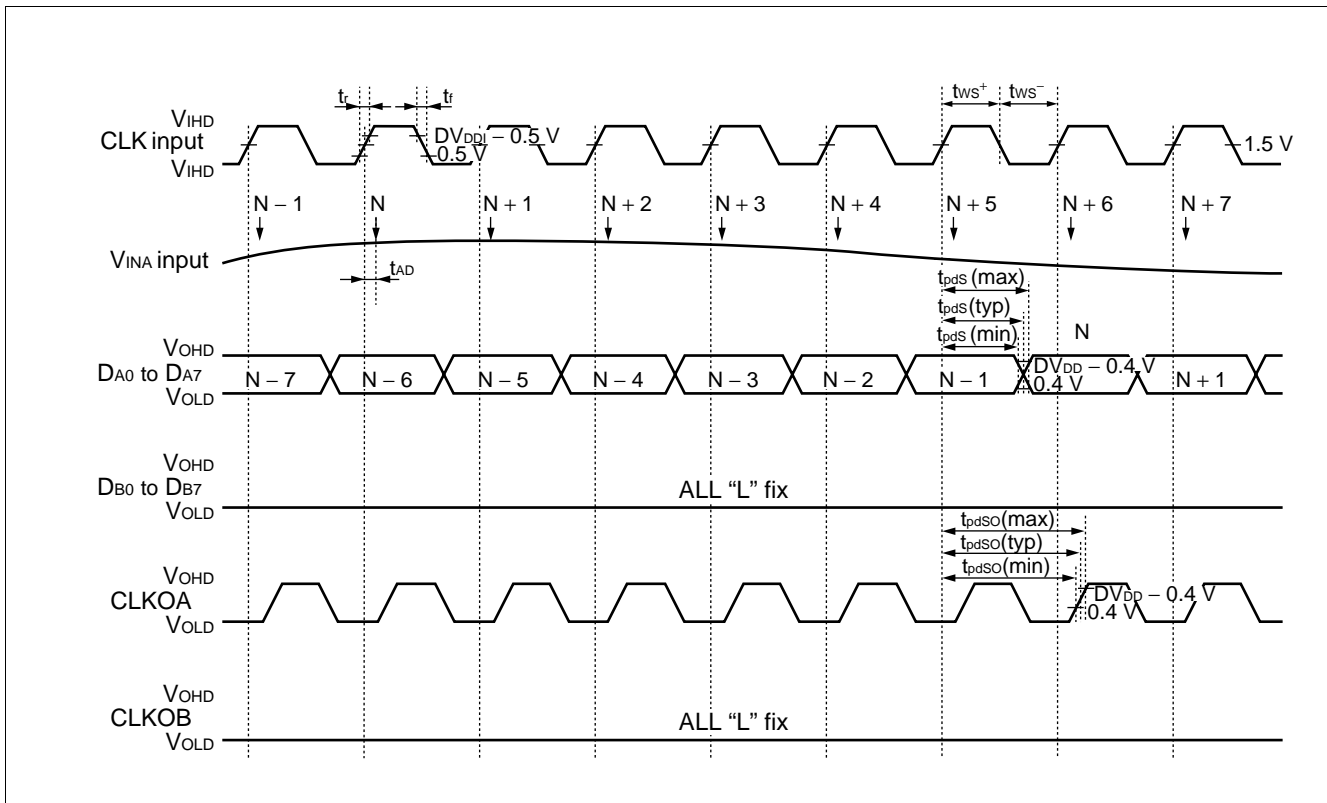
■ MODE SETTING

| CKCEL | DCEL | Mode | Timing Chart |
|-------|------|---|----------------|
| H | H | CLK input-straight output mode | Timing chart 1 |
| H | L | CLK input-demultiplex output (in-phase) mode | Timing chart 2 |
| L | H | CLK input-demultiplex output (two-phase) mode | Timing chart 3 |
| L | L | Two-phase CLK input mode (CLKA, CLKB) | Timing chart 4 |

■ TIMING CHART 1

CLK input-straight output mode

- CLK = 100 MHz (max)
- CLKA = CLKB = "L" (DV_{SS})
- CKSEL = "H" (AV_{DD})
- DSEL = "H" (DV_{DD})
- RESET = "H" (DV_{DD})
- $\overline{\text{CE}}$ = "L" (AV_{SS})
- $\overline{\text{OE}}$ = "L" (DV_{SS})



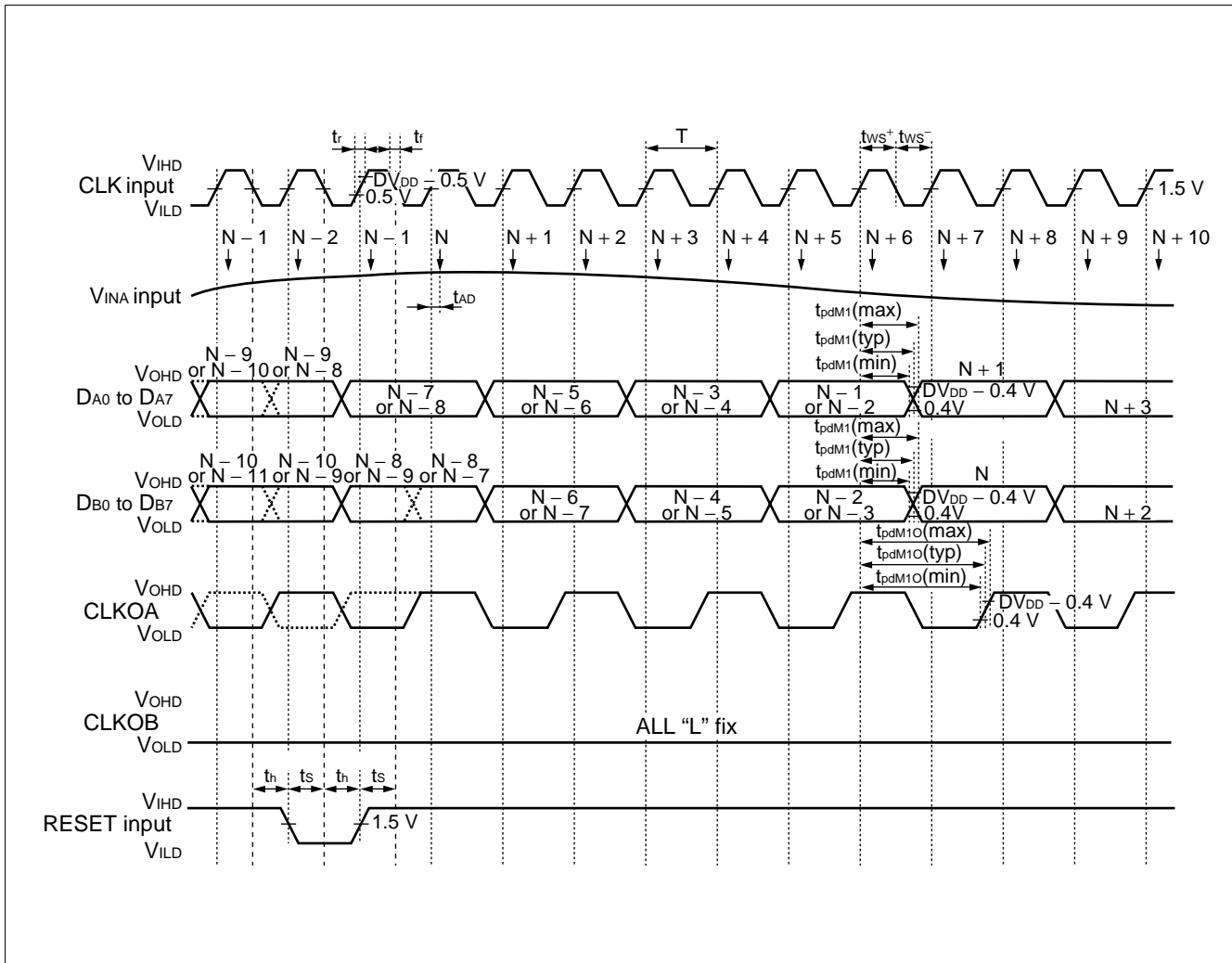
- V_{INA} input — Sampling at CLK rising
- DA₀ to DA₇ — Output (after 5 CLK + t_{pds} from Sampling) at CLK rising

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■ TIMING CHART 2

CLK input-demultiplex output (in-phase) mode

- CLK = 100 MHz (max)
- CLKA = CLKB = "L" (DV_{SS})
- CKSEL = "H" (AV_{DD})
- DSEL = "L" (DV_{SS})
- \overline{CE} = "L" (AV_{SS})
- \overline{OE} = "L" (DV_{SS})

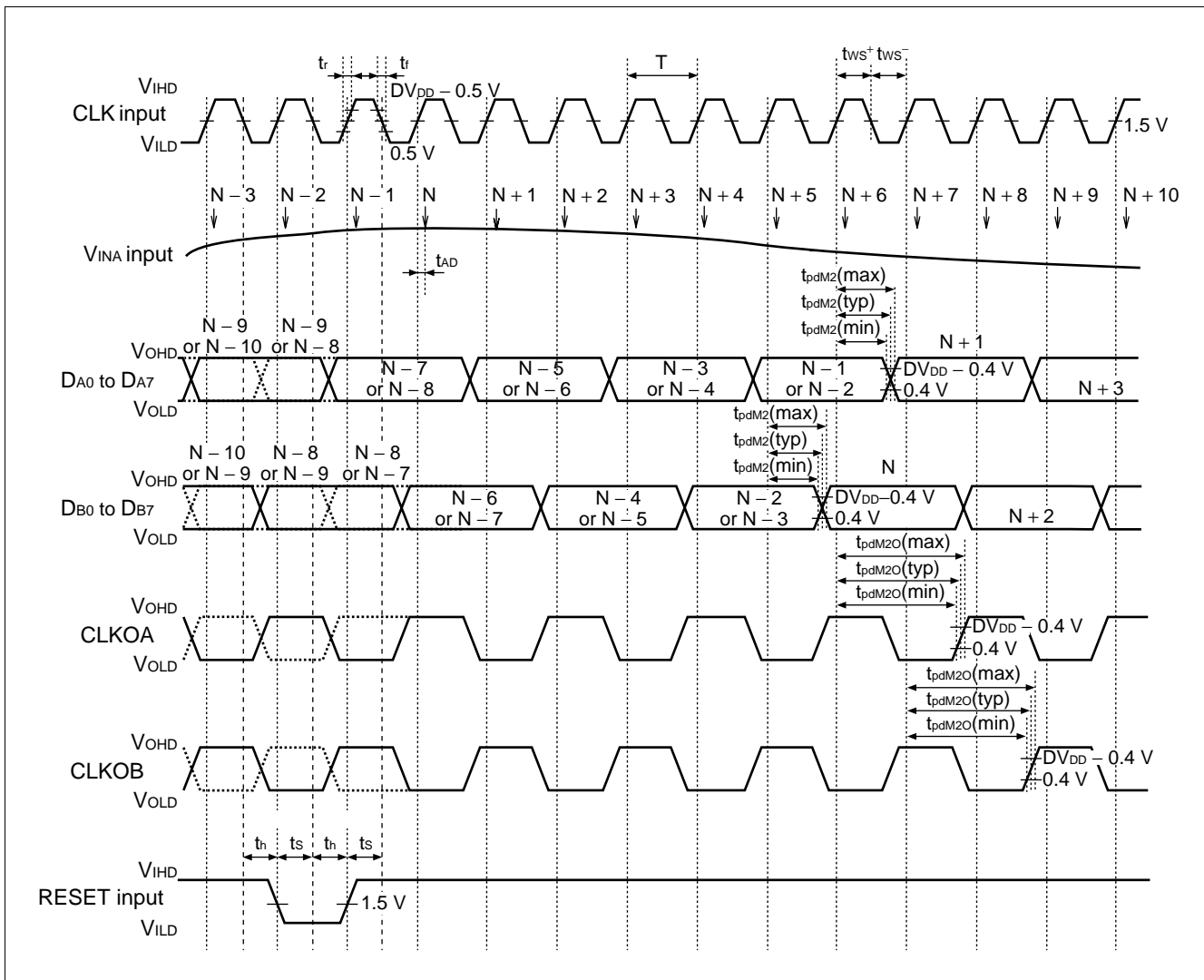


- V_{INA} input — Sampling at CLK rising
- DA₀ to DA₇ — Output (after 5 CLK + t_{pdM1} from Sampling) at CLK rising
- DB₀ to DB₇ — Output (after 6 CLK + t_{pdM1} from Sampling) at CLK rising

■ TIMING CHART 3

CLK input-demultiplex output (two-phase) mode

- CLK = 100 MHz (max)
- CLKA = CLKB = "L" (DV_{SS})
- CKSEL = "L" (AV_{SS})
- DSEL = "H" (DV_{DD})
- \overline{CE} = "L" (AV_{SS})
- \overline{OE} = "L" (DV_{SS})



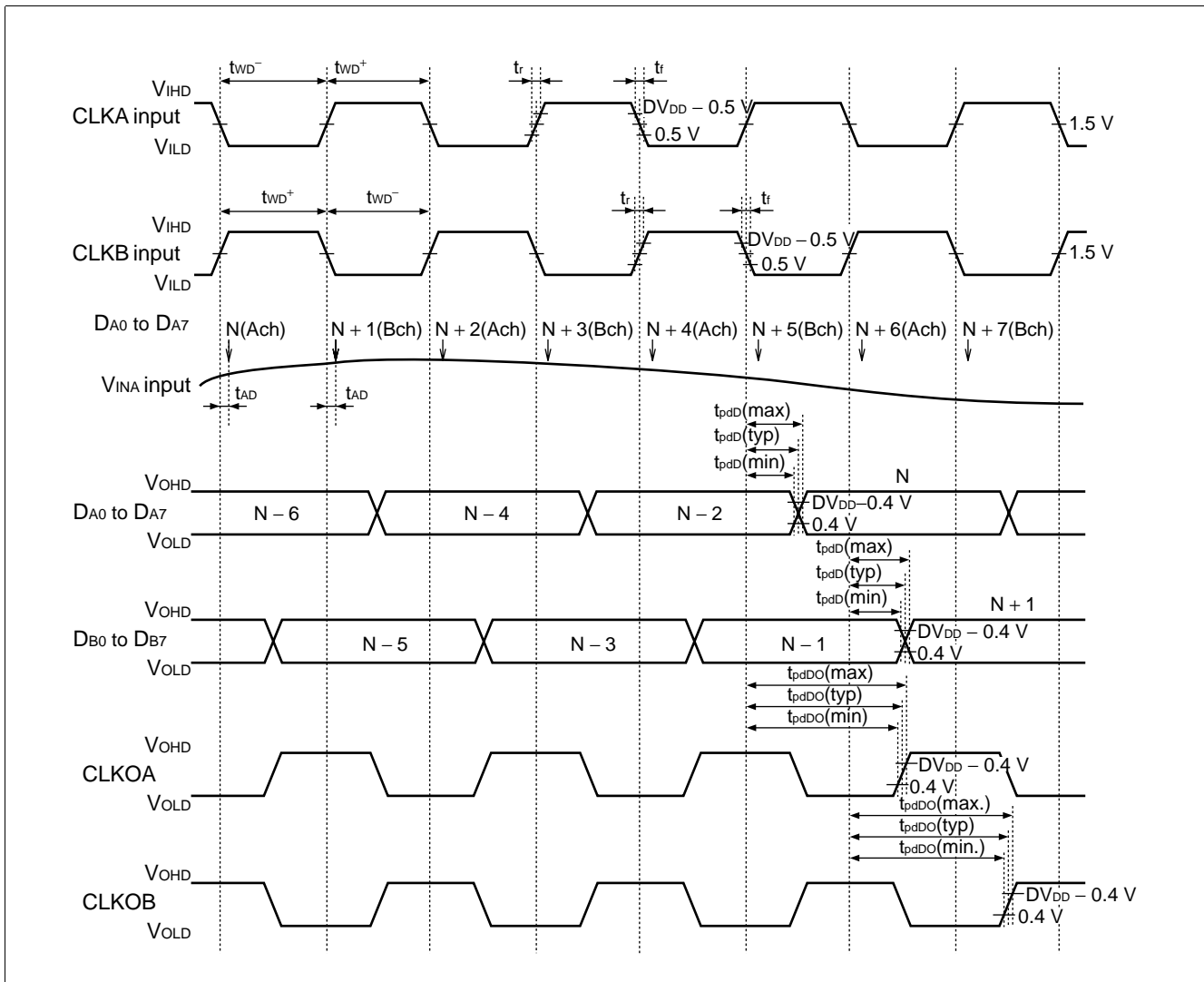
- V_{INA} input — Sampling at CLK rising
- DA₀ to DA₇ — Output (after 5 CLK + t_{pdM2} from Sampling) at CLK rising
- DB₀ to DB₇ — Output (after 5 CLK + t_{pdM2} from Sampling) at CLK rising

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■ TIMING CHART 4

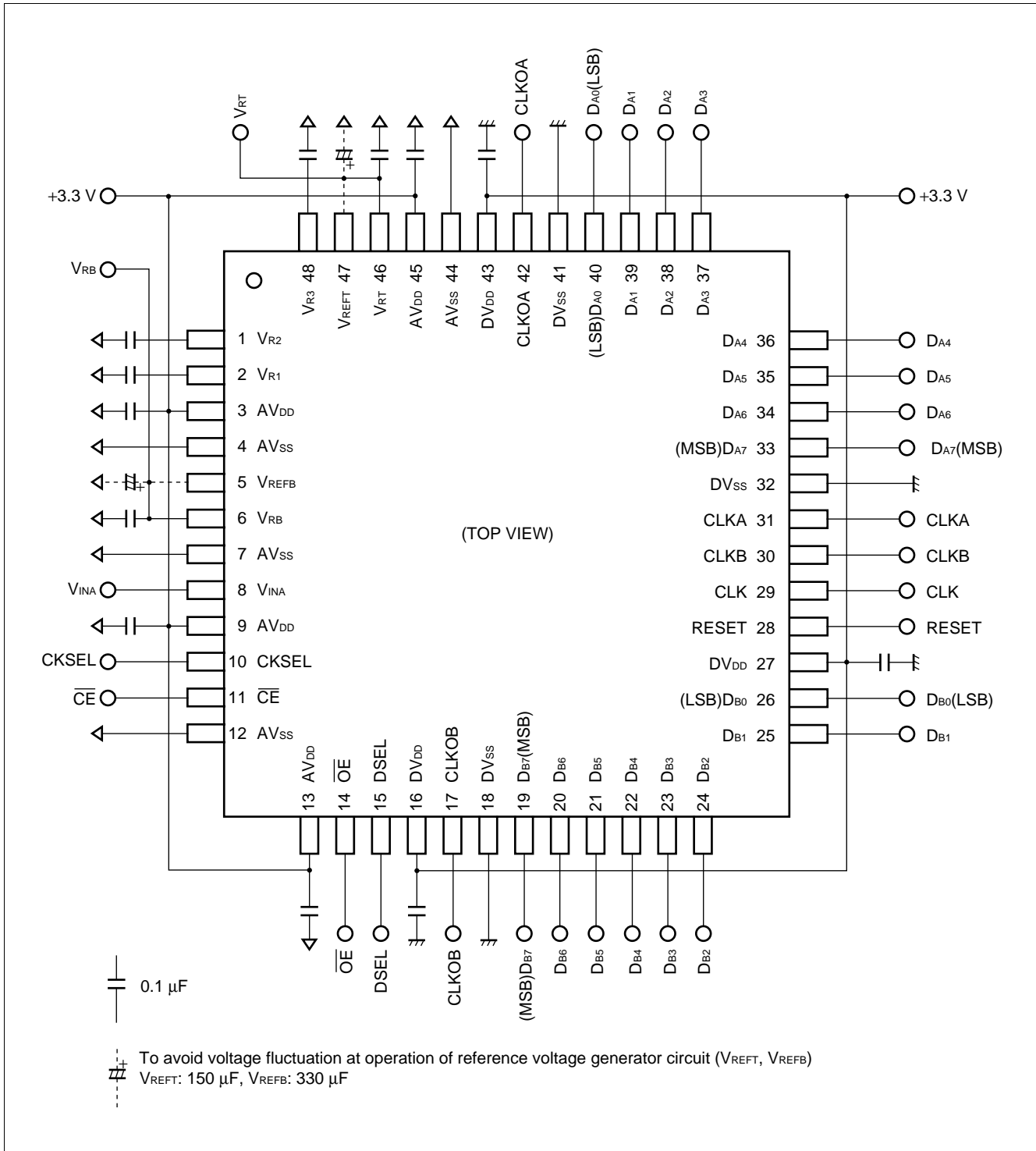
Two-phase CLK input mode (CLKA, CLKB)

- CLK = "L" (DV_{SS}) or "H" (DV_{DD})
- CLKA = CLKB = 50 MHz (max)
- CKSEL = "L" (AV_{SS})
- DSEL = "L" (DV_{SS})
- RESET = "H" (DV_{DD}) or "L" (DV_{SS})
- \overline{CE} = "L" (AV_{SS})
- \overline{OE} = "L" (DV_{SS})



- V_{INA} input — Sampling (A ch) at CLKA falling
Sampling (B ch) at CLKB falling
- DA₀ to DA₇ — Output (after 2.5 CLK + t_{pD} from Sampling) at CLKA rising
- DB₀ to DB₇ — Output (after 2.5 CLK + t_{pD} from Sampling) at CLKB rising

TYPICAL CONNECTION EXAMPLE



MB40C328

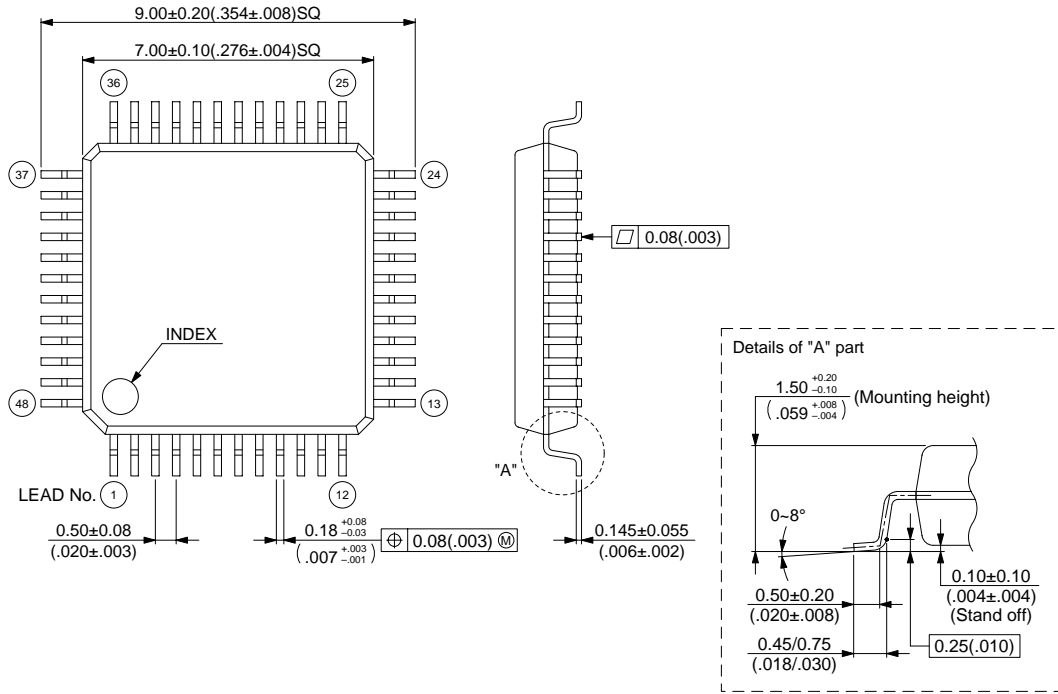
■ ORDERING INFORMATION

| Part number | Package | Remark |
|-------------|--------------------------------------|--------|
| MB40C328PFV | 48-pin Plastic LQFP (FPT-48P-M05) | |

■ PACKAGE DIMENSION

48-pin Plastic LQFP
(FPT-48P-M05)

Note) Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches).

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