

Preliminary

MOS Memories

FUJITSU

■ MB8464A-10-W, MB8464A-15-W CMOS 65,536-Bit Static Random Access Memory with Data Retention Mode

Description

The Fujitsu MB8464A-W is a 8,192-word by 8-bit static random access memory fabricated with a CMOS silicon gate process.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volt power supply is required.

The MB8464A-W is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

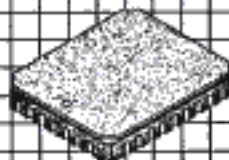
Features

- Organization: 8,192 words x 8-bits
- Fast access time:
 TAVQV = TELQV = 100 ns max. (MB8464A-10-W)
 TAVQV = TELQV = 150 ns max. (MB8464A-15-W)
- Completely static operation:
 No clock required
- TTL compatible input/output
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby:
 11 mW max.
- Data retention: 2.0V min.
- 28-pin ceramic package (300 mil width)
 (600 mil width)
- 32-pad leadless chip carrier
- Pin compatible with MB8464-W



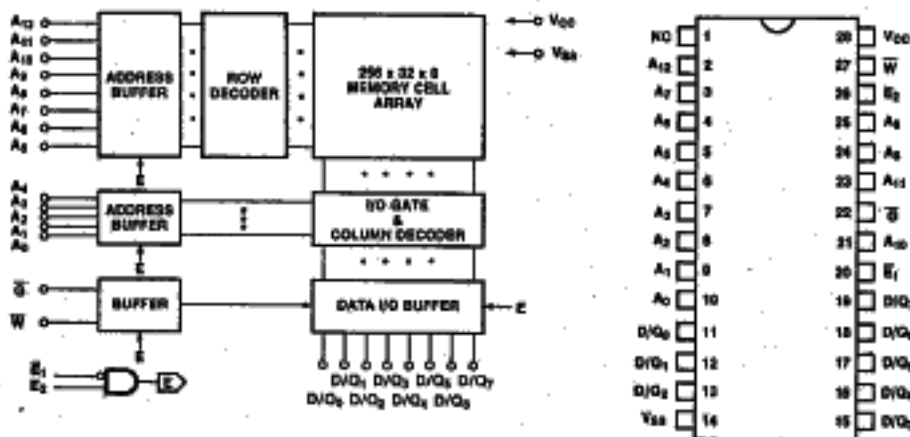
DIP-28C-A07

DIP-28C-A08

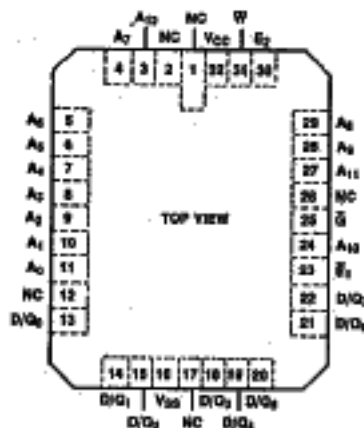


LCC-32C-A02

MB8464A-10-W
 MB8464A-16-W

MB8464A-W Block Diagram and Pin Assignment

TRUTH TABLE

E_1	E_2	G	W	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{BB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{BB}	HIGH-Z
L	H	H	H	OUT DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	Q_{OUT}
L	H	X	L	WRITE	I_{CC}	W


Absolute Maximum Ratings
 (See note)

Rating	Symbol	Value	Unit
Storage temperature range	T_{STG}	-85 to +150	$^{\circ}C$
Temperature under bias	T_{BUS}	-55 to +125	$^{\circ}C$
Supply voltage	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB8464A-10-W
MB8464A-15-W

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input high voltage	V_{IH}	2.4		$V_{CC} + 0.3$	V
Ambient temperature	T_A	-55		+125	°C

Capacitance
($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit
I/O capacitance ($V_{IO} = 0\text{V}$)	C_{IO}			8	pF
Input capacitance ($V_{IN} = 0\text{V}$)	C_{IN}			8	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8464A-10-W MB8464A-15-W		Unit	Test Condition
		Min	Max		
Standby supply current	I_{BS1}	2		mA	$E_2 \leq 0.2\text{V}$, $E_1 \geq V_{CC} - 0.2\text{V}$ ($E_2 \leq 0.2\text{V}$ or $E_2 \geq V_{CC} - 0.2\text{V}$)
	I_{BS2}	5		mA	$E_1 = V_{IH}$ or $E_2 = V_{IL}$
Active supply current	I_{CC1}	70		mA	$E_1 = V_{IL}$, $E_2 = V_{IH}$ $V_{IH} = V_{IH}$ or V_{IL} , $I_{OUT} = 0\text{ mA}$
Operating supply current	I_{CC2}	90		mA	Cycle = min., duty = 100%, $I_{OUT} = 0\text{ mA}$
Input leakage current	I_{LI}	-10	10	μA	$V_{IN} = 0\text{V}$ to V_{CC}
Output leakage current	I_{LIO}	-50	50	μA	$V_{IO} = 0\text{V}$ to V_{CC} $E_1 = V_{IH}$ or $E_2 = V_{IL}$ or $G = V_{IH}$ or $\bar{W} = V_{IL}$
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -1.0\text{ mA}$
Output low voltage	V_{OL}		0.4	V	$I_{OL} = 2.1\text{ mA}$

Note: All voltages are referenced to V_{SS} .

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Read Cycle

Parameter	Symbol	MB8464A-10-W		MB8464A-15-W		Unit
		Min	Max	Min	Max	
Read cycle time	T_{RWAX}	100		150		ns
Address access time	T_{RWQV}		100		150	ns
E_1 access time	$TE1LQV$		100		150	ns
E_2 access time	$TE2HOV$		100		150	ns
Output enable to output valid	T_{GLQV}		45		60	ns
Output hold from address change	T_{AXQX}	10		10		ns
Chip enable to output low-Z*	$TE1LOX$ $TE2HOX$	10		10		ns
Output enable to output low-Z*	T_{GLQZ}		5		5	ns
Chip enable to output high-Z*	$TE1HOZ$ $TE2LOZ$		40		50	ns
Output enable to output high-Z*	T_{GHQZ}		40		50	ns

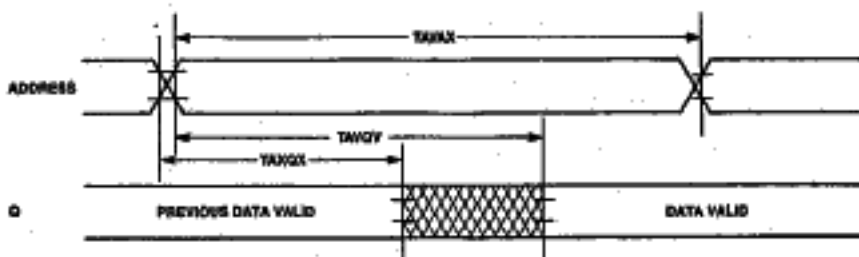
Note: * Transition is measured at the point of -500 mV from steady state voltage.

MB9464A-10-W
MB9464A-15-W

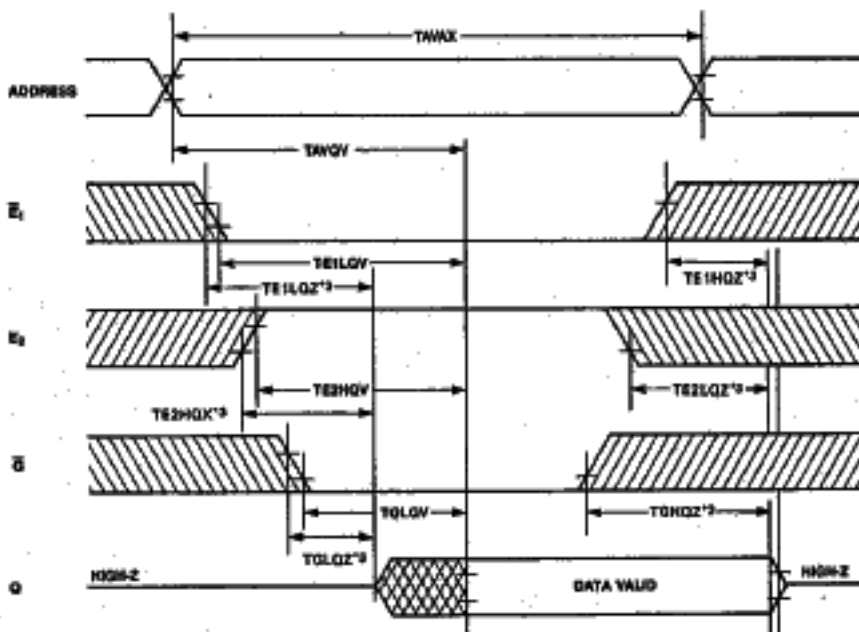
AC Characteristics
(Continued)
(Recommended operating
conditions unless otherwise
noted)

Read Cycle Timing Diagrams

Read Cycle I^{1,2}



Read Cycle II¹



NOTES: ¹ \bar{W} IS HIGH FOR READ CYCLE.
² DEVICE IS CONTINUOUSLY SELECTED, $E_1 = \bar{D} = V_{cc}$, $E_2 = V_{cc}$.
³ TRANSITION IS MEASURED AT THE POINT OF 4500-mV STEADY STATE VOLTAGE.

▨ DONT CARE
▨ UNDERPHED

MB8464A-10-W
MB8464A-15-W

AC Characteristics

(Continued)
(Recommended operating
conditions unless otherwise
noted)

Write Cycle

Parameter	Symbol	MB8464A-10-W		MB8464A-15-W		Unit
		Min	Max	Min	Max	
Write cycle time	TWAX	100		150		ns
Address valid to end of write	TAVWH, TAVE1L, TAVE2H	80		100		ns
Chip enable to end of write	TE1LE1H, TE2H2EL	80		100		ns
Data valid to end of write	TDVWH, TDVE1L, TDVE2H	40		50		ns
Data hold time	TWHDX, TE1HDX, TE2LDX	5		5		ns
Write pulse width	TWLWH	60		70		ns
Address setup time	TAVWL, TAVE1L, TAVE2H	0		10		ns
Write recovery time	TWHAX, TE1HAX, TE2LAX	10		10		ns
Write enable to output low-Z*	TWHQX	5		5		ns
Write enable to output high-Z*	TWLQZ		40		50	ns

*TRANSITION IS MEASURED AT THE POINT OF ± 500 mV STEADY STATE VOLTAGE.

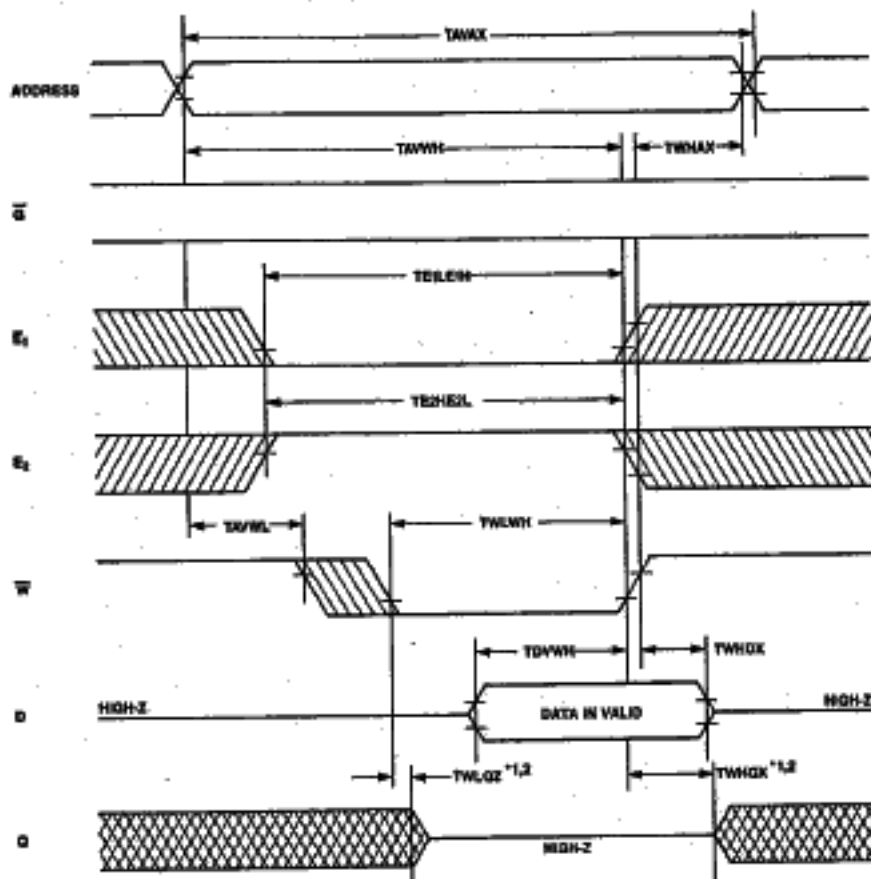
MB8464A-16-W
MB8464A-18-W

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted)

Write Cycle Timing Diagrams

Write Cycle 1 (\bar{W} Controlled)



NOTE: *1 IF \bar{CS} , \bar{E}_1 , AND \bar{E}_2 ARE IN THE READ MODE DURING THIS PERIOD, \bar{DQ} PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

*2 TRANSITION IS MEASURED AT THE POINT OF ± 500 mV FROM STEADY STATE VOLTAGE.

▨ DONT CARE

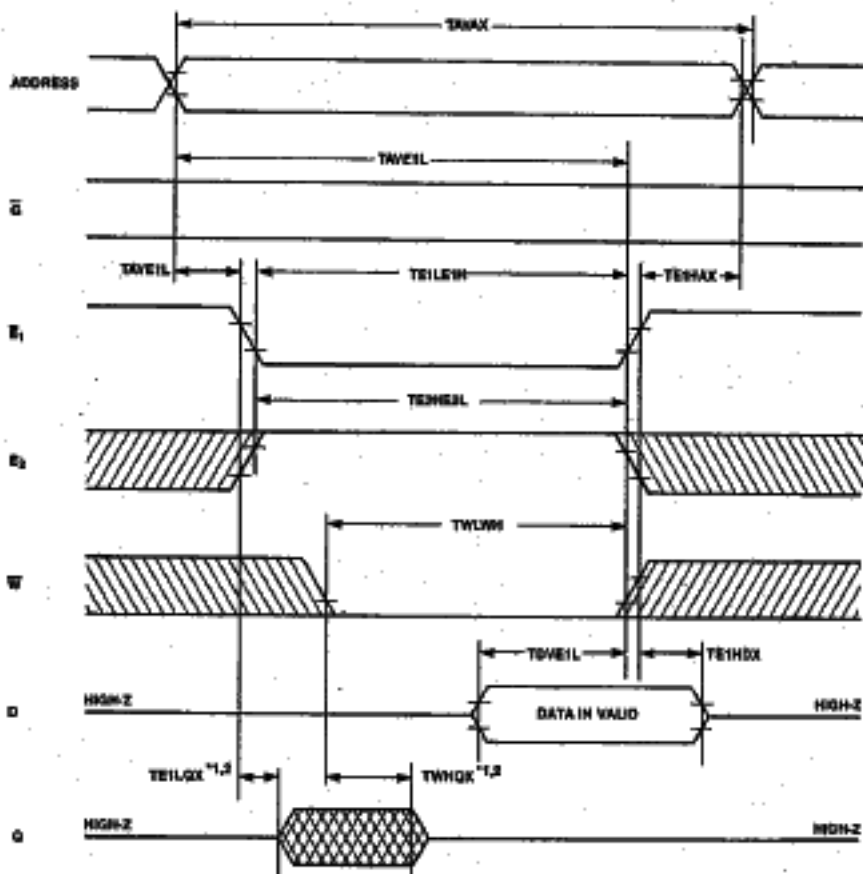
▩ UNSPINDED

MB8464A-10-W
MB8464A-15-W

AC Characteristics

(Continued)
(Recommended operating
conditions unless otherwise
noted)

Write Cycle II (\bar{E}_1 Controlled)



NOTE: *1 IF \bar{E}_2 , \bar{E}_1 AND \bar{W} ARE IN THE READ MODE DURING THIS PERIOD, D/Q PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

*2 TRANSITION IS MEASURED AT THE POINT OF ± 500 mV FROM STEADY STATE VOLTAGE.

▨ DONT CARE

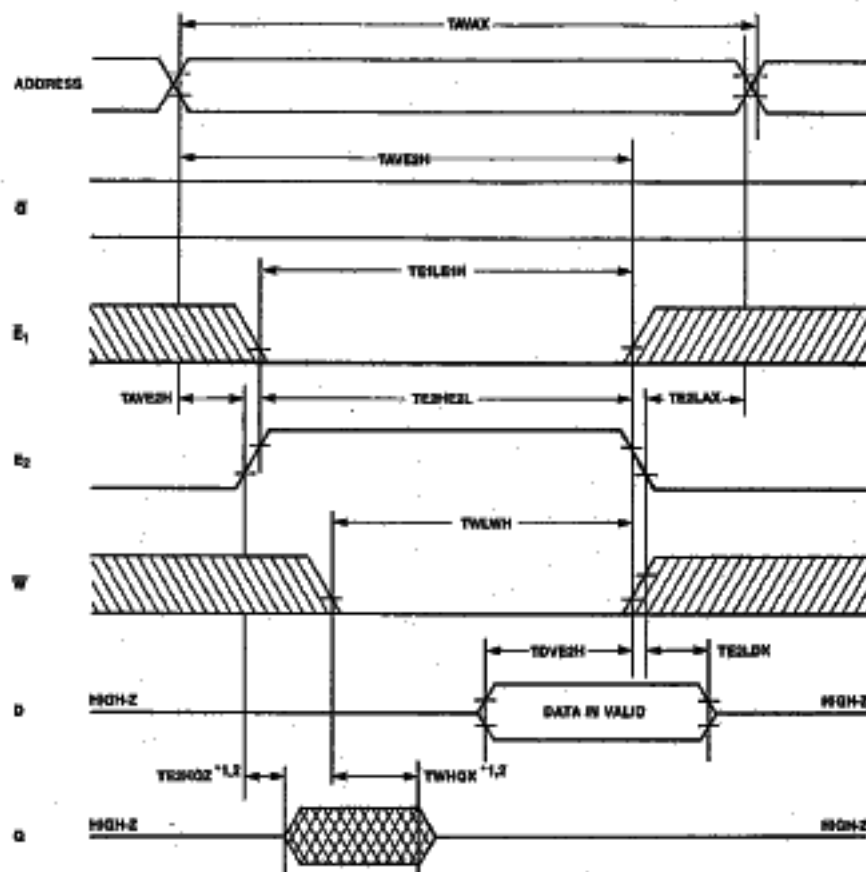
▩ UNDERPULSED

MB8464A-10-W
MB8464A-15-W

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted)

Write Cycle III (E_2 Controlled)



NOTE: *1 IF \bar{Q} , E_2 , AND \bar{W} ARE IN THE READ MODE DURING THIS PERIOD, DO PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

*2 TRANSITION IS MEASURED AT THE POINT OF ± 500 mV FROM STEADY STATE VOLTAGE.

▨ DONT CARE

▩ UNDEFINED

Data Retention Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Data retention supply voltage ^{*1}	V_{DR}	2.0	5.5	V
Data retention supply current ^{*2}	I_{DR}	Standard	0.5	mA
Data retention setup time	TE1HVL, TE2LVL	0		ns
Operation recovery time	TVHE1L, TVHE2H	TAVAX		

Notes: *1 E_2 controlled: $E_2 = 0.2V$

E_1 controlled: $E_1 = V_{DR} - 0.2V$ ($E_2 = 0.2V$ or $E_2 = V_{DR} - 0.2V$)

*2 E_2 controlled: $V_{DR} = 3.0V$, $E_2 = 0.2V$

E_1 controlled: $V_{DR} = 3.0V$, $E_1 = V_{DR} - 0.2V$ ($E_2 = 0.2V$ or $E_2 = V_{DR} - 0.2V$)

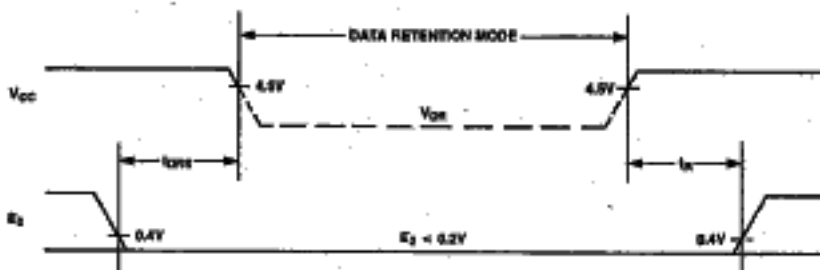
MB8464A-10-W
MB8464A-15-W

Data Retention Characteristics (Continued)

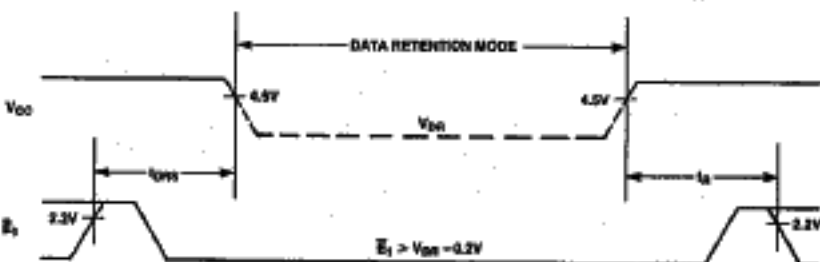
(Recommended operating conditions unless otherwise noted)

Data Retention Timing

Data Retention I (E_2 Controlled)



Data Retention II (E_1 Controlled)

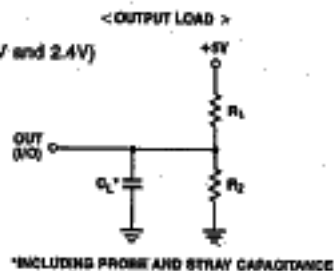


AC Test Conditions

Input Pulse Levels: 0.4V to 2.6V
Input Pulse Rise and Fall Times: 5 ns (Transition time between 0.6V and 2.4V)
Timing Reference Levels: Input: $V_{IL} = 0.6V$, $V_{IH} = 2.4V$
Output: $V_{OL} = 0.6V$, $V_{OH} = 2.0V$

Output Load:

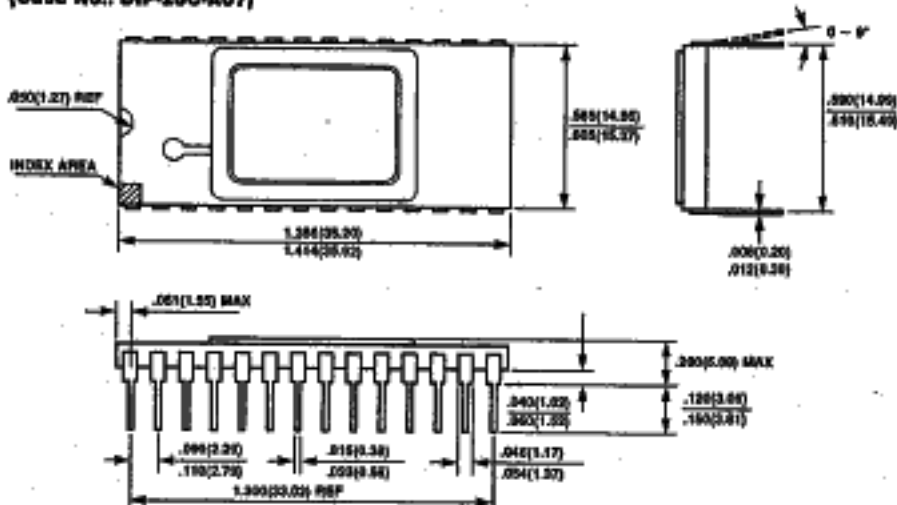
	R_1	R_2	C_L	PARAMETERS MEASURED
LOAD I	1.8 K Ω	890 Ω	100 pF	EXCEPT TEHQX, TBLGZ, TEHNGZ, TQHGZ, TWHGX AND TWLQZ
LOAD II	1.8 K Ω	890 Ω	5 pF	TEHGX, TBLGZ, TEHNGZ, TQHGZ, TWHGX AND TWLQZ



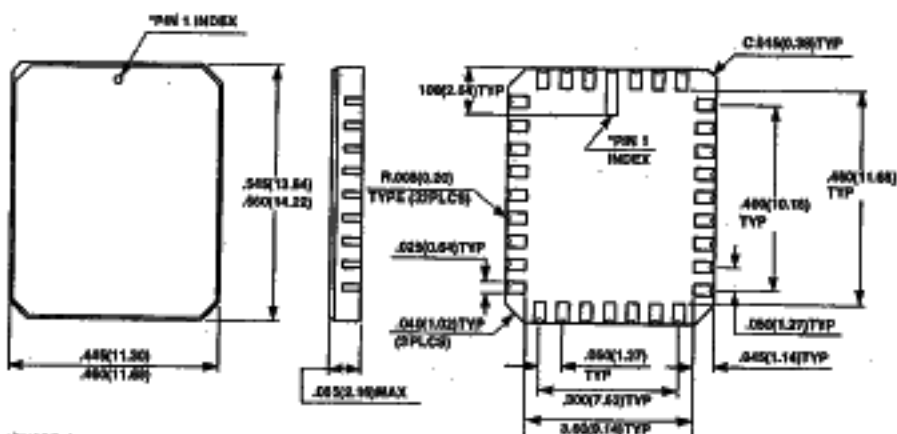
MBB464A-10-W
 MBB464A-15-W

Package Dimensions
 Dimensions in inches
 (millimeters)

28-Lead Ceramic Dual-In-Line Package
 (Case No.: DIP-28C-A07)



32-PAD Ceramic (Metal Seal) Leadless Chip Carrier
 (Case No.: LCC-32C-A02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MB6464A-10-W
 MB6464A-15-W

Package Dimensions
 (Continued)
 Dimensions in inches
 (millimeter)

28-Lead Ceramic (Metal Seal) Dual In-Line Package
 (Case No.: DIP-28C-A08)

