

MCP (Multi-Chip Package) FLASH MEMORY

CMOS

8M (× 8/× 16) FLASH MEMORY & 8M (× 8/× 16) FLASH MEMORY

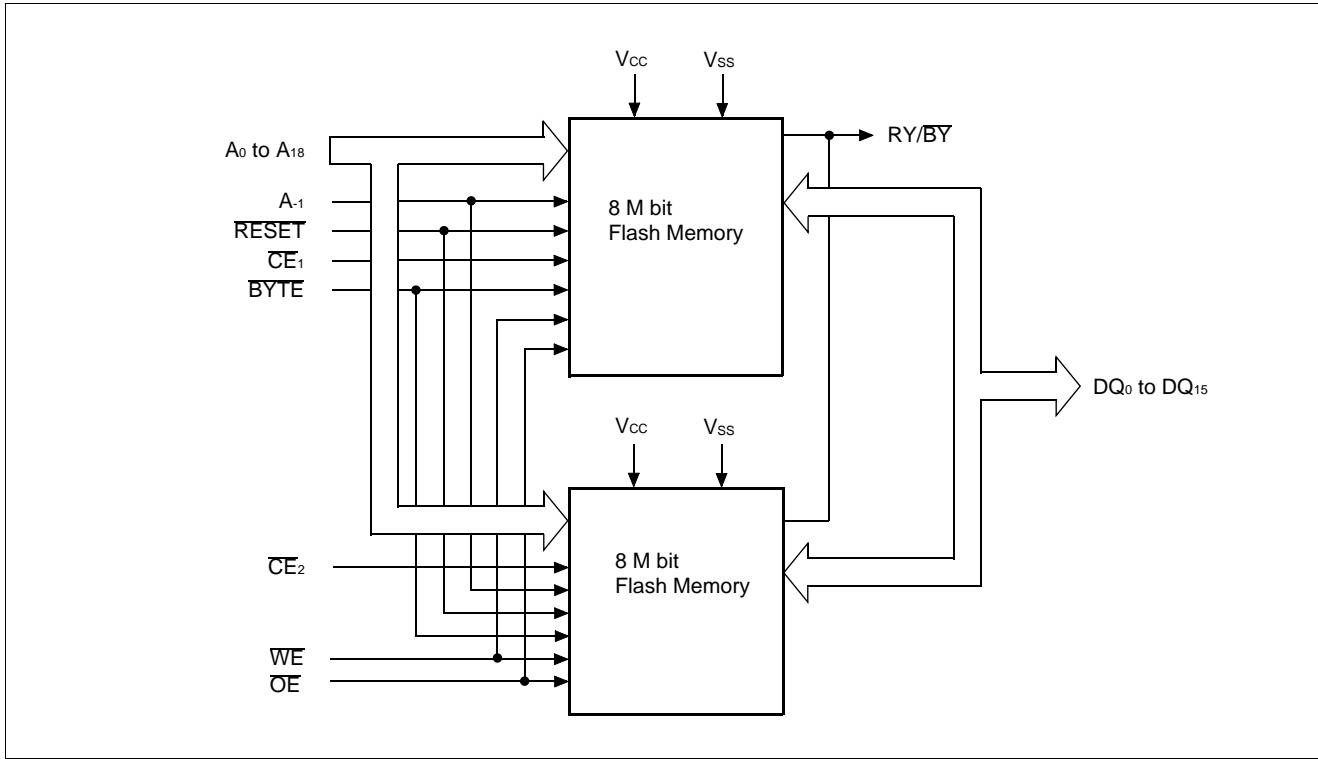
MB84VB2000-10/MB84VB2001-10

■ FEATURES

- Contain 2 chips of MBM29LV800A, and each chip have separate \overline{CE} .
- Power supply voltage of 2.7 to 3.6 V
- High performance
100 ns maximum access time
- Operating Temperature
-40 to +85°C
- Minimum 100,000 write/erase cycles
- Sector erase architecture
One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes × 2 chips
Any combination of sectors can be concurrently erased. Also supports full chip erase.
- Boot Code Sector Architecture
MB84VB2000: Top sector
MB84VB2001: Bottom sector
- Embedded Erase™ Algorithms
Automatically pre-programs and erases the chip or any sector
- Embedded Program™ Algorithms
Automatically writes and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Ready/Busy output (RY/BY)
Hardware method for detection of program or erase cycle completion
- Automatic sleep mode
When addresses remain stable, automatically switch themselves to low power mode.
- Low V_{cc} write inhibit ≤ 2.5 V
- Erase Suspend/Resume
Suspends the erase operation to allow a read data in another sector within the same device
- Please refer to "MBM29LV800TA/BA" data sheet in detailed function

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■ BLOCK DIAGRAM



■ CONNECTION DIAGRAM

(Top View)

| | A | B | C | D | E | F | G | H |
|---|-----------------|-----------------|-------------------|-------------------|------------------|------------------|------------------|-----------------------------------|
| 6 | N.C. | V _{SS} | DQ ₁ | A ₁ | A ₂ | A ₄ | N.C. | A ₉ |
| 5 | A ₁₀ | DQ ₅ | DQ ₂ | A ₀ | A ₃ | A ₇ | RY/BY | A ₁₄ |
| 4 | \overline{OE} | DQ ₇ | DQ ₄ | DQ ₀ | A ₆ | A ₁₈ | RESET | A ₁₅ |
| 3 | A ₁₁ | A ₈ | A ₅ | DQ ₈ | DQ ₃ | DQ ₁₂ | A ₁₂ | BYTE |
| 2 | A ₁₃ | A ₁₇ | \overline{CE}_2 | \overline{CE}_1 | DQ ₁₀ | V _{CC} | DQ ₆ | DQ ₁₅ /A ₋₁ |
| 1 | \overline{WE} | N.C. | A ₁₆ | V _{SS} | DQ ₉ | DQ ₁₁ | DQ ₁₃ | DQ ₁₄ |

Table 1 MB84VB2000/MB84VB2001 Pin Configuration

| Pin | Function | Input/ Output |
|---|--|------------------|
| A ₋₁ , A ₀ to A ₁₈ | Address Inputs (Common) | I |
| DQ ₀ to DQ ₁₅ | Data Inputs/Outputs (Common) | I/O |
| \overline{CE}_1 | Chip Enable 1 | I |
| \overline{CE}_2 | Chip Enable 2 | I |
| \overline{OE} | Output Enable (Common) | I |
| \overline{WE} | Write Enable (Common) | I |
| RY/BY | Ready/Busy Outputs (Common) | O |
| RESET | Hardware Reset Pin/Sector Protection Unlock (Common) | I |
| BYTE | Selects 8-bit or 16-bit mode (Common) | I |
| N.C. | No Internal Connection | — |
| V _{SS} | Device Ground (Common) | Power |
| V _{CC} | Device Power Supply (Common) | Power |


MB84VB2000-10/MB84VB2001-10

■ PRODUCT LINE UP

| Part No. | | MB84VB2000/MB84VB2001 |
|---------------------------------------|---|-----------------------|
| Ordering Part No. | $V_{CC} = 3.0\text{ V}$ ^{+0.6V} / _{-0.3V} | -10 |
| Max. Address Access Time (ns) | | 100 |
| Max. \overline{CE} Access Time (ns) | | 100 |
| Max. \overline{OE} Access Time (ns) | | 40 |


■ LOGIC SYMBOL

Table 2 MB84VB2000/MB84VB2001 User Bus Operations (BYTE = V_{IH})

| Operation (5) | \overline{CE}_1 | \overline{CE}_2 | \overline{OE} | \overline{WE} | A ₀ | A ₁ | A ₆ | A ₉ | DQ ₀ to DQ ₁₅ | RESET |
|------------------------------------|-------------------|-------------------|-----------------|---|----------------|----------------|----------------|----------------|-------------------------------------|----------|
| Auto-Select Manufacture's Code (1) | H | L | L | H | L | L | L | V_{ID} | Code | H |
| | L | H | | | | | | | | |
| Auto-Select Device Code (1) | H | L | L | H | H | L | L | V_{ID} | Code | H |
| | L | H | | | | | | | | |
| Read (3) | H | L | L | H | A ₀ | A ₁ | A ₆ | A ₉ | D _{OUT} | H |
| | L | H | | | | | | | | |
| Full Standby | H | H | X | X | X | X | X | X | HIGH-Z | H |
| Output Disable | X | X | H | H | X | X | X | X | HIGH-Z | H |
| Write (Program/Erase) | H | L | H | L | A ₀ | A ₁ | A ₆ | A ₉ | D _{IN} | H |
| | L | H | | | | | | | | |
| Enable Sector Protection (2), (4) | H | L | V_{ID} |  | L | H | L | V_{ID} | X | H |
| | L | H | | | | | | | | |
| Verify Sector Protection (2), (4) | H | L | L | H | L | H | L | V_{ID} | Code | H |
| | L | H | | | | | | | | |
| Temporary Sector Unprotection | X | X | X | X | X | X | X | X | X | V_{ID} |
| Reset (Hardware)/Standby | X | X | X | X | X | X | X | X | HIGH-Z | L |

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Table 3 MB84VB2000/MB84VB2001 User Bus Operations (BYTE = V_{IL})

| Operation (5) | \overline{CE}_1 | \overline{CE}_2 | \overline{OE} | \overline{WE} | DQ ₁₅ / A ₋₁ | A ₀ | A ₁ | A ₆ | A ₉ | DQ ₀ to DQ ₇ | RESET |
|------------------------------------|-------------------|-------------------|-----------------|---|---------------------------------------|----------------|----------------|----------------|-----------------|---------------------------------------|-----------------|
| Auto-Select Manufacture's Code (1) | H | L | L | H | L | L | L | L | V _{ID} | Code | H |
| | L | H | | | | | | | | | |
| Auto-Select Device Code (1) | H | L | L | H | L | H | L | L | V _{ID} | Code | H |
| | L | H | | | | | | | | | |
| Read (3) | H | L | L | H | A ₋₁ | A ₀ | A ₁ | A ₆ | A ₉ | D _{OUT} | H |
| | L | H | | | | | | | | | |
| Full Standby | H | H | X | X | X | X | X | X | X | HIGH-Z | H |
| Output Disable | X | X | H | H | X | X | X | X | X | HIGH-Z | H |
| Write (Program/Erase) | H | L | H | L | A ₋₁ | A ₀ | A ₁ | A ₆ | A ₉ | D _{IN} | H |
| | L | H | | | | | | | | | |
| Enable Sector Protection (2), (4) | H | L | V _{ID} |  | L | L | H | L | V _{ID} | X | H |
| | L | H | | | | | | | | | |
| Verify Sector Protection (2), (4) | H | L | L | H | L | L | H | L | V _{ID} | Code | H |
| | L | H | | | | | | | | | |
| Temporary Sector Unprotection | X | X | X | X | X | X | X | X | X | X | V _{ID} |
| Reset (Hardware)/Standby | X | X | X | X | X | X | X | X | X | HIGH-Z | L |

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH},  = Pulse input. See DC Characteristics for voltage levels.

Notes: 1.Manufacturer and device codes may also be accessed via a command register write sequence. See Table 7.

2.Refer to the section on Sector Protection.

3. \overline{WE} can be V_{IL} if \overline{OE} is V_{IL}, \overline{OE} at V_{IH} initiates the write operations.

4.V_{CC} = 3.3 V ±10%

5.Do not apply $\overline{CE}_1 = \overline{CE}_2 = V_{IL}$ at a time.

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■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes × 2.
- Individual-sector, multiple-sector, or bulk-erase capability.

| | (×8) | (×16) | | (×8) | (×16) |
|-------------------|--------|--------|-------------------|--------|--------|
| 16K byte/8K word | FFFFFH | 7FFFFH | 64K byte/32K word | FFFFFH | 7FFFFH |
| 8K byte/4K word | FC000H | 7E000H | 64K byte/32K word | F0000H | 78000H |
| 8K byte/4K word | FA000H | 7D000H | 64K byte/32K word | E0000H | 70000H |
| 32K byte/16K word | F8000H | 7C000H | 64K byte/32K word | D0000H | 68000H |
| 64K byte/32K word | F0000H | 78000H | 64K byte/32K word | C0000H | 60000H |
| 64K byte/32K word | E0000H | 70000H | 64K byte/32K word | B0000H | 58000H |
| 64K byte/32K word | D0000H | 68000H | 64K byte/32K word | A0000H | 50000H |
| 64K byte/32K word | C0000H | 60000H | 64K byte/32K word | 90000H | 48000H |
| 64K byte/32K word | B0000H | 58000H | 64K byte/32K word | 80000H | 40000H |
| 64K byte/32K word | A0000H | 50000H | 64K byte/32K word | 70000H | 38000H |
| 64K byte/32K word | 90000H | 48000H | 64K byte/32K word | 60000H | 30000H |
| 64K byte/32K word | 80000H | 40000H | 64K byte/32K word | 50000H | 28000H |
| 64K byte/32K word | 70000H | 38000H | 64K byte/32K word | 40000H | 20000H |
| 64K byte/32K word | 60000H | 30000H | 64K byte/32K word | 30000H | 18000H |
| 64K byte/32K word | 50000H | 28000H | 64K byte/32K word | 20000H | 10000H |
| 64K byte/32K word | 40000H | 20000H | 64K byte/32K word | 10000H | 08000H |
| 64K byte/32K word | 30000H | 18000H | 32K byte/16K word | 08000H | 04000H |
| 64K byte/32K word | 20000H | 10000H | 8K byte/4K word | 06000H | 03000H |
| 64K byte/32K word | 10000H | 08000H | 8K byte/4K word | 04000H | 02000H |
| 64K byte/32K word | 00000H | 00000H | 16K byte/8K word | 00000H | 00000H |

MB84VB2000 Sector Architecture

MB84VB2001 Sector Architecture

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■ FUNCTIONAL DESCRIPTION

Table 4 Sector Address Tables (MB84VB2000)

| Sector Address | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Address Range (×8) | Address Range (×16) |
|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|---------------------|
| SA0 | 0 | 0 | 0 | 0 | X | X | X | 00000H to 0FFFFH | 00000H to 07FFFH |
| SA1 | 0 | 0 | 0 | 1 | X | X | X | 10000H to 1FFFFH | 08000H to 0FFFFH |
| SA2 | 0 | 0 | 1 | 0 | X | X | X | 20000H to 2FFFFH | 10000H to 17FFFH |
| SA3 | 0 | 0 | 1 | 1 | X | X | X | 30000H to 3FFFFH | 18000H to 1FFFFH |
| SA4 | 0 | 1 | 0 | 0 | X | X | X | 40000H to 4FFFFH | 20000H to 27FFFH |
| SA5 | 0 | 1 | 0 | 1 | X | X | X | 50000H to 5FFFFH | 28000H to 2FFFFH |
| SA6 | 0 | 1 | 1 | 0 | X | X | X | 60000H to 6FFFFH | 30000H to 37FFFH |
| SA7 | 0 | 1 | 1 | 1 | X | X | X | 70000H to 7FFFFH | 38000H to 3FFFFH |
| SA8 | 1 | 0 | 0 | 0 | X | X | X | 80000H to 8FFFFH | 40000H to 47FFFH |
| SA9 | 1 | 0 | 0 | 1 | X | X | X | 90000H to 9FFFFH | 48000H to 4FFFFH |
| SA10 | 1 | 0 | 1 | 0 | X | X | X | A0000H to AFFFFH | 50000H to 57FFFH |
| SA11 | 1 | 0 | 1 | 1 | X | X | X | B0000H to BFFFFH | 58000H to 5FFFFH |
| SA12 | 1 | 1 | 0 | 0 | X | X | X | C0000H to CFFFFH | 60000H to 67FFFH |
| SA13 | 1 | 1 | 0 | 1 | X | X | X | D0000H to DFFFFH | 68000H to 6FFFFH |
| SA14 | 1 | 1 | 1 | 0 | X | X | X | E0000H to EFFFFH | 70000H to 77FFFH |
| SA15 | 1 | 1 | 1 | 1 | 0 | X | X | F0000H to F7FFFH | 78000H to 7BFFFH |
| SA16 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | F8000H to F9FFFH | 7C000H to 7CFFFH |
| SA17 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FA000H to FBFFFH | 7D000H to 7DFFFH |
| SA18 | 1 | 1 | 1 | 1 | 1 | 1 | X | FC000H to FFFFFH | 7E000H to 7FFFFH |

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Table 5 Sector Address Tables (MB84VB2001)

| Sector Address | A ₁₈ | A ₁₇ | A ₁₆ | A ₁₅ | A ₁₄ | A ₁₃ | A ₁₂ | Address Range (×8) | Address Range (×16) |
|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------|---------------------|
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | X | 00000H to 03FFFFH | 00000H to 01FFFFH |
| SA1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 04000H to 05FFFFH | 02000H to 02FFFFH |
| SA2 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 06000H to 07FFFFH | 03000H to 03FFFFH |
| SA3 | 0 | 0 | 0 | 0 | 1 | X | X | 08000H to 0FFFFH | 04000H to 07FFFFH |
| SA4 | 0 | 0 | 0 | 1 | X | X | X | 10000H to 1FFFFH | 08000H to 0FFFFH |
| SA5 | 0 | 0 | 1 | 0 | X | X | X | 20000H to 2FFFFH | 10000H to 17FFFFH |
| SA6 | 0 | 0 | 1 | 1 | X | X | X | 30000H to 3FFFFH | 18000H to 1FFFFH |
| SA7 | 0 | 1 | 0 | 0 | X | X | X | 40000H to 4FFFFH | 20000H to 27FFFFH |
| SA8 | 0 | 1 | 0 | 1 | X | X | X | 50000H to 5FFFFH | 28000H to 2FFFFH |
| SA9 | 0 | 1 | 1 | 0 | X | X | X | 60000H to 6FFFFH | 30000H to 37FFFFH |
| SA10 | 0 | 1 | 1 | 1 | X | X | X | 70000H to 7FFFFH | 38000H to 3FFFFH |
| SA11 | 1 | 0 | 0 | 0 | X | X | X | 80000H to 8FFFFH | 40000H to 47FFFFH |
| SA12 | 1 | 0 | 0 | 1 | X | X | X | 90000H to 9FFFFH | 48000H to 4FFFFH |
| SA13 | 1 | 0 | 1 | 0 | X | X | X | A0000H to AFFFFH | 50000H to 57FFFFH |
| SA14 | 1 | 0 | 1 | 1 | X | X | X | B0000H to BFFFFH | 58000H to 5FFFFH |
| SA15 | 1 | 1 | 0 | 0 | X | X | X | C0000H to CFFFFH | 60000H to 67FFFFH |
| SA16 | 1 | 1 | 0 | 1 | X | X | X | D0000H to DFFFFH | 68000H to 6FFFFH |
| SA17 | 1 | 1 | 1 | 0 | X | X | X | E0000H to EFFFFH | 70000H to 77FFFFH |
| SA18 | 1 | 1 | 1 | 1 | X | X | X | F0000H to FFFFFH | 78000H to 7FFFFH |

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Table 6.1 Flash Memory Autoselect Codes

| Type | | A ₆ | A ₁ | A ₀ | A ₋₁ ^{*1} | Code (HEX) |
|--------------------|------------|-----------------|-----------------|-----------------|-------------------------------|------------|
| Manufacture's Code | | V _{IL} | V _{IL} | V _{IL} | V _{IL} | 04H |
| Device Code | MB84VB2000 | Byte | V _{IL} | V _{IL} | V _{IL} | DAH |
| | | Word | | | X | 22DAH |
| | MB84VB2001 | Byte | V _{IL} | V _{IL} | V _{IL} | 5BH |
| | | Word | | | X | 225BH |

*1: A₋₁ is for Byte mode.

Table 6.2 Expanded Autoselect Code Table

| Type | | Code | DQ ₁₅ | DQ ₁₄ | DQ ₁₃ | DQ ₁₂ | DQ ₁₁ | DQ ₁₀ | DQ ₉ | DQ ₈ | DQ ₇ | DQ ₆ | DQ ₅ | DQ ₄ | DQ ₃ | DQ ₂ | DQ ₁ | DQ ₀ |
|--------------------|------------|------|--------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Manufacture's Code | | 04H | A ₋₁ /0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Device Code | MB84VB2000 | (B) | DAH | A ₋₁ | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| | | (W) | 22DAH | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| | MB84VB2001 | (B) | 5BH | A ₋₁ | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | HI-Z | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | (W) | 225BH | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

(B): Byte mode

(W): Word mode

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Table 7 Flash Memory Command Definitions

| Command Sequence | Bus Write Cycles Req'd | First Bus Write Cycle | | Second Bus Write Cycle | | Third Bus Write Cycle | | Fourth Bus Read/Write Cycle | | Fifth Bus Write Cycle | | Sixth Bus Write Cycle | |
|-----------------------------|--|-----------------------|------|------------------------|------|-----------------------|------|-----------------------------|------|-----------------------|------|-----------------------|------|
| | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data |
| Read/Reset | 1 | XXXH | F0H | — | — | — | — | — | — | — | — | — | — |
| Read/Reset | 3 | 555H | AAH | 2AAH | 55H | 555H | F0H | RA | RD | — | — | — | — |
| | | AAAH | | 555H | | AAAH | | | | | | | |
| Autoselect | 3 | 555H | AAH | 2AAH | 55H | 555H | 90H | — | — | — | — | — | — |
| | | AAAH | | 555H | | AAAH | | | | | | | |
| Program | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA | PD | — | — | — | — |
| | | AAAH | | 555H | | AAAH | | | | | | | |
| Chip Erase | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| | | AAAH | | 555H | | AAAH | | 555H | | AAAH | | | |
| Sector Erase | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | SA | 30H |
| | | AAAH | | 555H | | AAAH | | 555H | | | | | |
| Sector Erase Suspend | Erase can be suspended during sector erase with Addr. ("H" or "L"). Data (B0H) | | | | | | | | | | | | |
| Sector Erase Resume | Erase can be resumed after suspend with Addr. ("H" or "L"). Data (30H) | | | | | | | | | | | | |
| Set to Fast Mode | 3 | 555H | AAH | 2AAH | 55H | 555H | 20H | — | — | — | — | — | — |
| | | AAAH | | 555H | | AAAH | | | | | | | |
| Fast Program (Note) | 2 | XXXH | A0H | PA | PD | — | — | — | — | — | — | — | — |
| Reset from Fast Mode (Note) | 2 | XXXH | 90H | XXXH | F0H | — | — | — | — | — | — | — | — |
| | | XXXH | | XXXH | | | | | | | | | |
| Extended Sector Protect | 4 | XXXH | 60H | SPA | 60H | SPA | 40H | SPA | SD | — | — | — | — |

Address bits A₁₁ to A₁₇ = X = "H" or "L" for all address commands except or Program Address (PA) and Sector Address (SA).

Bus operations are defined in Tables 2 and 3.

The system should generate the following address patterns:

Word Mode: 555H or 2AAH to addresses A₀ to A₁₀

Byte Mode: AAH or 555H to addresses A₋₁ and A₀ to A₁₀

Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

RA =Address of the memory location to be read

PA =Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.

SA =Address of the sector to be erased. The combination of A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃, and A₁₂ will uniquely select any sector.

RD =Data read from location RA during read operation.

PD =Data to be programmed at location PA. Data is latched on the falling edge of write pulse.

SPA:Sector address to be protected. Set sector address (SA) and (A₆, A₁, A₀) = (0, 1, 0).

SD:Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

■ ABSOLUTE MAXIMUM RATINGS

| | |
|--|----------------------------|
| Storage Temperature | -55°C to +125°C |
| Ambient Temperature with Power Applied | -25°C to +85°C |
| Voltage with Respect to Ground All pins (Note) | -0.3 V to $V_{CC} + 0.5$ V |
| V_{CCf}/V_{CCS} Supply (Note) | -0.3 V to +4.6 V |

Note: Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are $V_{CCf} + 0.5$ V or $V_{CCS} + 0.5$ V. During voltage transitions, outputs may positive overshoot to $V_{CC} + 2.0$ V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

| | |
|-------------------------------------|------------------|
| Commercial Devices | |
| Ambient Temperature (T_A) | -40°C to +85°C |
| V_{CC} Supply Voltages | +2.7 V to +3.6 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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■ DC CHARACTERISTICS

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit | |
|------------------|---|---|-----------------------|-----------------------|------|----|
| I _{LI} | Input Leakage Current | V _{IN} = V _{SS} to V _{CC} , V _{CC} = V _{CC} Max. | -1.0 | +1.0 | μA | |
| I _{LO} | Output Leakage Current | V _{OUT} = V _{SS} to V _{CC} , V _{CC} = V _{CC} Max. | -1.0 | +1.0 | μA | |
| I _{LIT} | A ₉ , $\overline{\text{OE}}$, RESET Inputs Leakage Current | V _{CC} = V _{CC} Max. A ₉ , $\overline{\text{OE}}$, RESET = 12.5 V | — | 70 | μA | |
| I _{CC1} | V _{CC} Active Current (Note 1, 5) | $\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}} = V_{IH}$, f = 10 MHz | Byte | — | 22 | mA |
| | | | Word | — | 25 | |
| | | $\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}} = V_{IH}$, f = 5 MHz | Byte | — | 12 | mA |
| | | | Word | — | 15 | |
| I _{CC2} | V _{CC} Active Current (Note 2, 5) | $\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}} = V_{IH}$ | — | 35 | mA | |
| I _{CC3} | V _{CC} Current (Standby) (Note 5) | V _{CC} = V _{CC} Max., $\overline{\text{CE}} = V_{CC} \pm 0.3$ V, RESET = V _{CC} ± 0.3 V | — | 5 | μA | |
| I _{CC4} | V _{CC} Current (Standby, Reset) (Note 5) | V _{CC} = V _{CC} Max., RESET = V _{SS} ± 0.3 V | — | 5 | μA | |
| I _{CC5} | V _{CC} Current (Automatic Sleep Mode) (Note 3, 5) | V _{CC} = V _{CC} Max., $\overline{\text{CE}} = V_{SS} \pm 0.3$ V, RESET = V _{CC} ± 0.3 V V _{IN} = V _{CC} ± 0.3 V or V _{SS} ± 0.3 V | — | 5 | μA | |
| V _{IL} | Input Low Level | — | -0.5 | 0.6 | V | |
| V _{IH} | Input High Level | — | 2.0 | V _{CC} + 0.3 | V | |
| V _{ID} | Voltage for Autoselect and Sector Protection (A ₉ , $\overline{\text{OE}}$, RESET) (Note 4) | — | 11.5 | 12.5 | V | |
| V _{OL} | Output Low Voltage Level | I _{OL} = 4.0 mA, V _{CC} = V _{CC} Min. | — | 0.45 | V | |
| V _{OH1} | Output High Voltage Level | I _{OH} = -2.0 mA, V _{CC} = V _{CC} Min. | 2.4 | — | V | |
| V _{OH2} | | I _{OH} = -100 μA, V _{CC} = V _{CC} Min. | V _{CC} - 0.4 | — | V | |
| V _{LKO} | Low V _{CC} Lock-Out Voltage | — | 2.3 | 2.5 | V | |

- Notes:**
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 10 MHz).
 2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
 3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
 4. (V_{ID} - V_{CC}) do not exceed 9 V.
 5. Total power consumption is (condition of Flash 1) + (condition of Flash 2).

■ AC CHARACTERISTICS

• \overline{CE} Timing

| Parameter Symbols | | Description | Test Setup | | -10 | Unit |
|-------------------|------------------|------------------------------|------------|------|-----|------|
| JEDEC | Standard | | | | | |
| — | t _{CCR} | \overline{CE} Recover Time | — | Min. | 0 | ns |

• Read Only Operations Characteristics

| Parameter Symbols | | Description | Test Setup | -10 (Note) | | Unit |
|-------------------|--|--|--|------------|------|------|
| JEDEC | Standard | | | Min. | Max. | |
| t _{AVAV} | t _{RC} | Read Cycle Time | — | 100 | — | ns |
| t _{AVQV} | t _{ACC} | Address to Output Delay | $\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$ | — | 100 | ns |
| t _{ELQV} | t _{CE} | Chip Enable to Output Delay | $\overline{OE} = V_{IL}$ | — | 100 | ns |
| t _{GLQV} | t _{OE} | Output Enable to Output Delay | — | — | 40 | ns |
| t _{EHQZ} | t _{DF} | Chip Enable to Output High-Z | — | — | 30 | ns |
| t _{GHQZ} | t _{DF} | Output Enable to Output High-Z | — | — | 30 | ns |
| t _{AXQX} | t _{OH} | Output Hold Time from Addresses, \overline{CE} or \overline{OE} , Whichever Occurs First | — | 0 | — | ns |
| — | t _{READY} | RESET Pin Low to Read Mode | — | — | 20 | μs |
| — | t _{ELFL} t _{ELFH} | \overline{CE} or BYTE Switching Low or High | — | — | 5 | ns |

Note: Test Conditions—Output Load: 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V to 3.0 V
 Timing measurement reference level
 Input: 1.5 V
 Output: 1.5 V

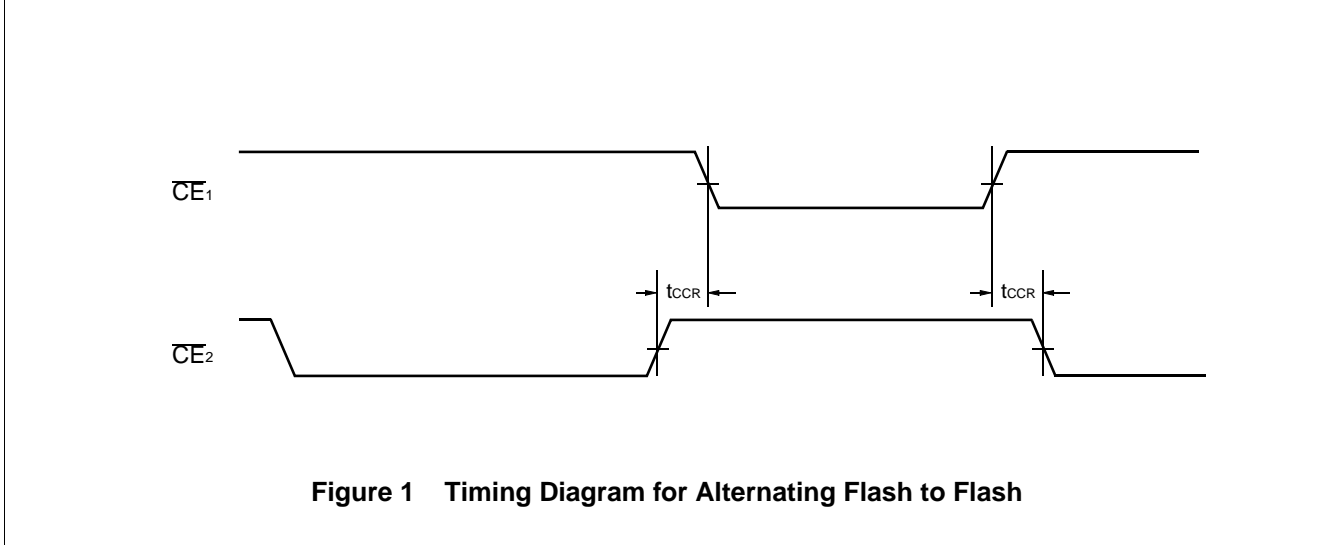
MB84VB2000-10/MB84VB2001-10

• Erase/Program Operations

| Parameter Symbols | | Description | -10 | | | Unit |
|--------------------|--------------------|---|------|------|------|------|
| JEDEC | Standard | | Min. | Typ. | Max. | |
| t _{AVAV} | t _{WC} | Write Cycle Time | 100 | — | — | ns |
| t _{AVWL} | t _{AS} | Address Setup Time (\overline{WE} to Addr.) | 0 | — | — | ns |
| t _{AVEL} | t _{AS} | Address Setup Time (\overline{CE} to Addr.) | 0 | — | — | ns |
| t _{WLAX} | t _{AH} | Address Hold Time (\overline{WE} to Addr.) | 50 | — | — | ns |
| t _{ELAX} | t _{AH} | Address Hold Time (\overline{CE} to Addr.) | 50 | — | — | ns |
| t _{DVWH} | t _{DS} | Data Setup Time | 50 | — | — | ns |
| t _{WHDX} | t _{DH} | Data Hold Time | 0 | — | — | ns |
| — | t _{OES} | Output Enable Setup Time | 0 | — | — | ns |
| — | t _{OEHL} | Output Enable Hold Time | 0 | — | — | ns |
| | | Read Toggle and Data Polling | 10 | — | — | ns |
| t _{GHEL} | t _{GHEL} | Read Recover Time Before Write (\overline{OE} to \overline{CE}) | 0 | — | — | ns |
| t _{GHWL} | t _{GHWL} | Read Recover Time Before Write (\overline{OE} to \overline{WE}) | 0 | — | — | ns |
| t _{WLEL} | t _{WS} | \overline{WE} Setup Time (\overline{CE} to \overline{WE}) | 0 | — | — | ns |
| t _{ELWL} | t _{CS} | \overline{CE} Setup Time (\overline{WE} to \overline{CE}) | 0 | — | — | ns |
| t _{EHWH} | t _{WH} | \overline{WE} Hold Time (\overline{CE} to \overline{WE}) | 0 | — | — | ns |
| t _{WHEH} | t _{CH} | \overline{CE} Hold Time (\overline{WE} to \overline{CE}) | 0 | — | — | ns |
| t _{WLWH} | t _{WP} | Write Pulse Width | 50 | — | — | ns |
| t _{ELEH} | t _{CP} | \overline{CE} Pulse Width | 50 | — | — | ns |
| t _{WHWL} | t _{WPH} | Write Pulse Width High | 30 | — | — | ns |
| t _{EHEL} | t _{CPH} | \overline{CE} Pulse Width High | 30 | — | — | ns |
| t _{WHWH1} | t _{WHWH1} | Byte Programming Operation | — | 8 | — | μs |
| t _{WHWH2} | t _{WHWH2} | Sector Erase Operation (Note 1) | — | 1 | 15 | sec |
| — | t _{VCS} | V _{CC} Setup Time | 50 | — | — | μs |
| — | t _{VIDR} | Rise Time to V _{ID} (Note 2) | 500 | — | — | ns |
| — | t _{VLHT} | Voltage Transition Time (Note 2) | 4 | — | — | μs |
| — | t _{WPP} | Write Pulse Width (Note 2) | 100 | — | — | μs |
| — | t _{OESP} | \overline{OE} Setup Time to \overline{WE} Active (Note 2) | 4 | — | — | μs |
| — | t _{CSP} | \overline{CE} Setup Time to \overline{WE} Active (Note 2) | 4 | — | — | μs |
| — | t _{RB} | Recover Time from RY/BY | 0 | — | — | ns |
| — | t _{RP} | RESET Pulse Width | 500 | — | — | ns |
| — | t _{RH} | RESET Hold Time Before Read | 200 | — | — | ns |
| — | t _{EOE} | Delay Time from Embedded Output Enable | — | — | 100 | ns |
| — | t _{BUSY} | Program/Erase Valid to RY/BY Delay | — | — | 90 | ns |
| — | t _{FLQZ} | BYTE Switching Low to Output High-Z | — | — | 30 | ns |
| — | t _{FLQV} | BYTE Switching High to Output Active | 30 | — | — | ns |

- Notes:** 1. This does not include the preprogramming time.
2. This timing is for Sector Protection operation.

■ SWITCHING WAVEFORMS



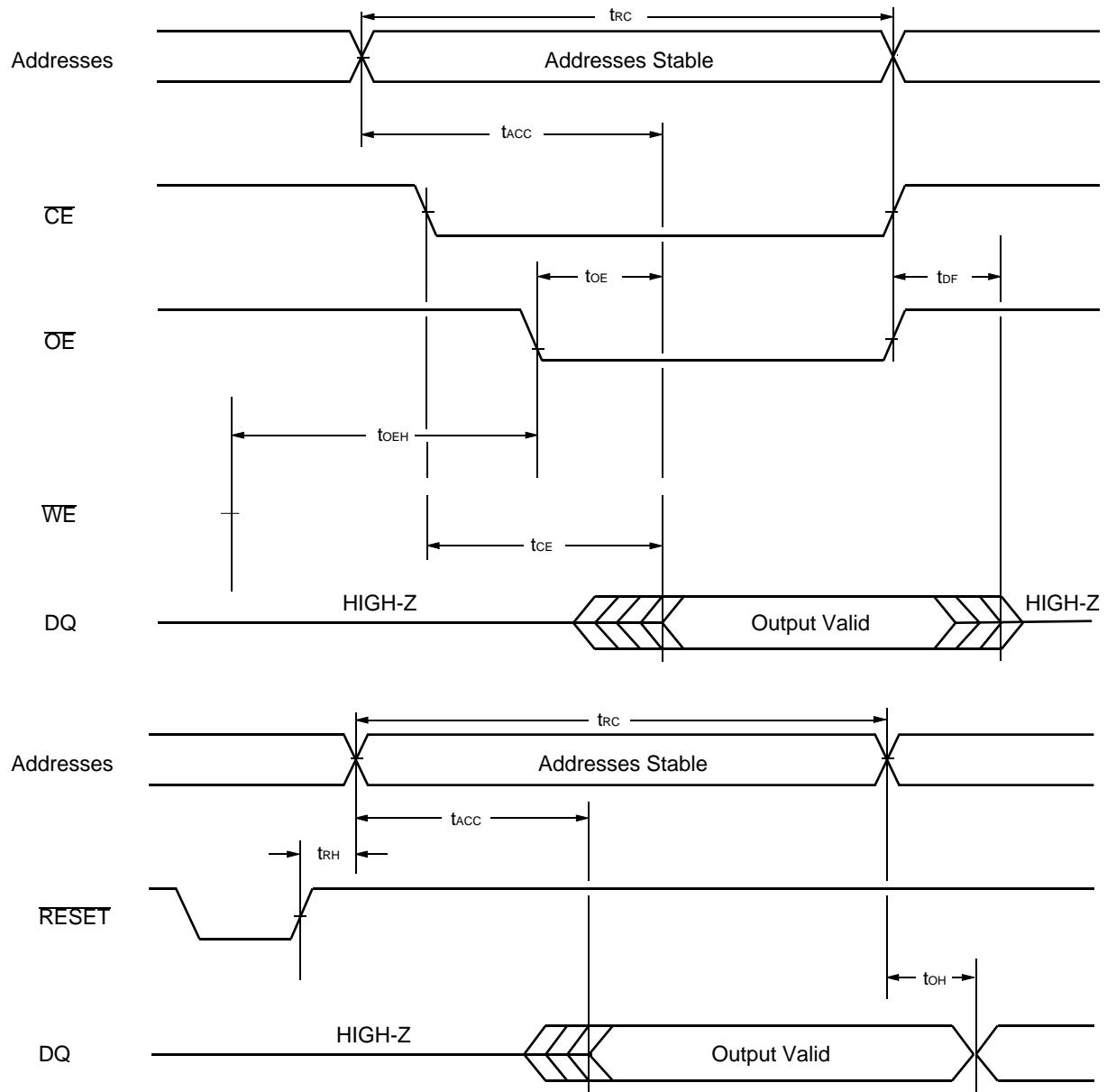
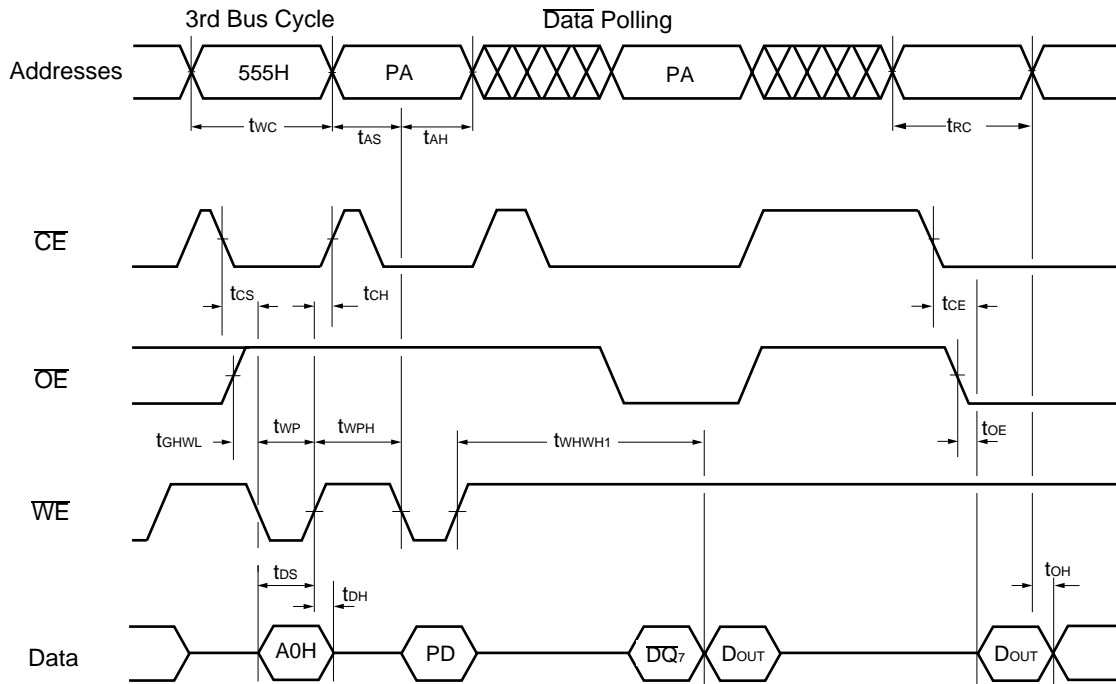
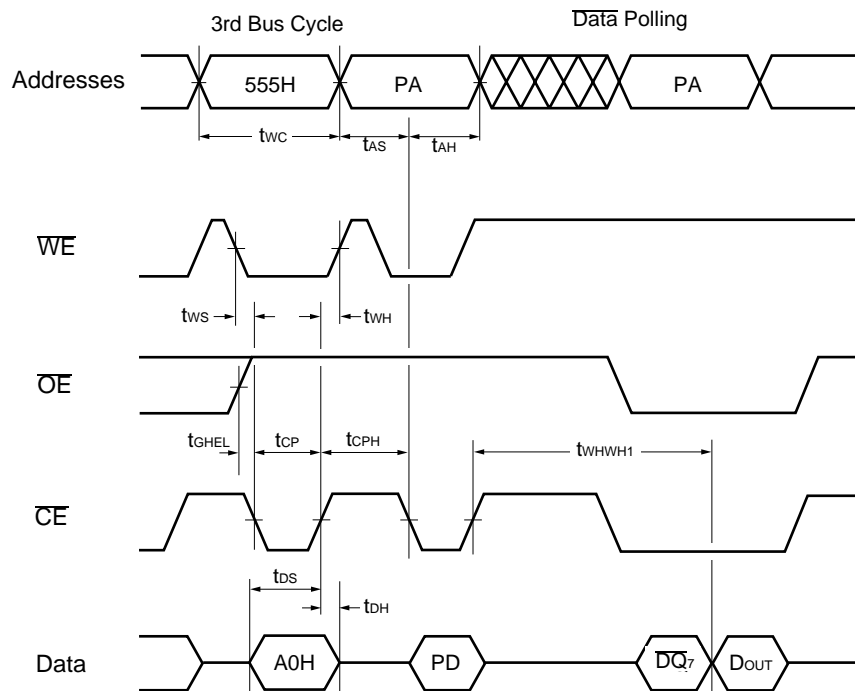


Figure 2 AC Waveforms for Read Operations



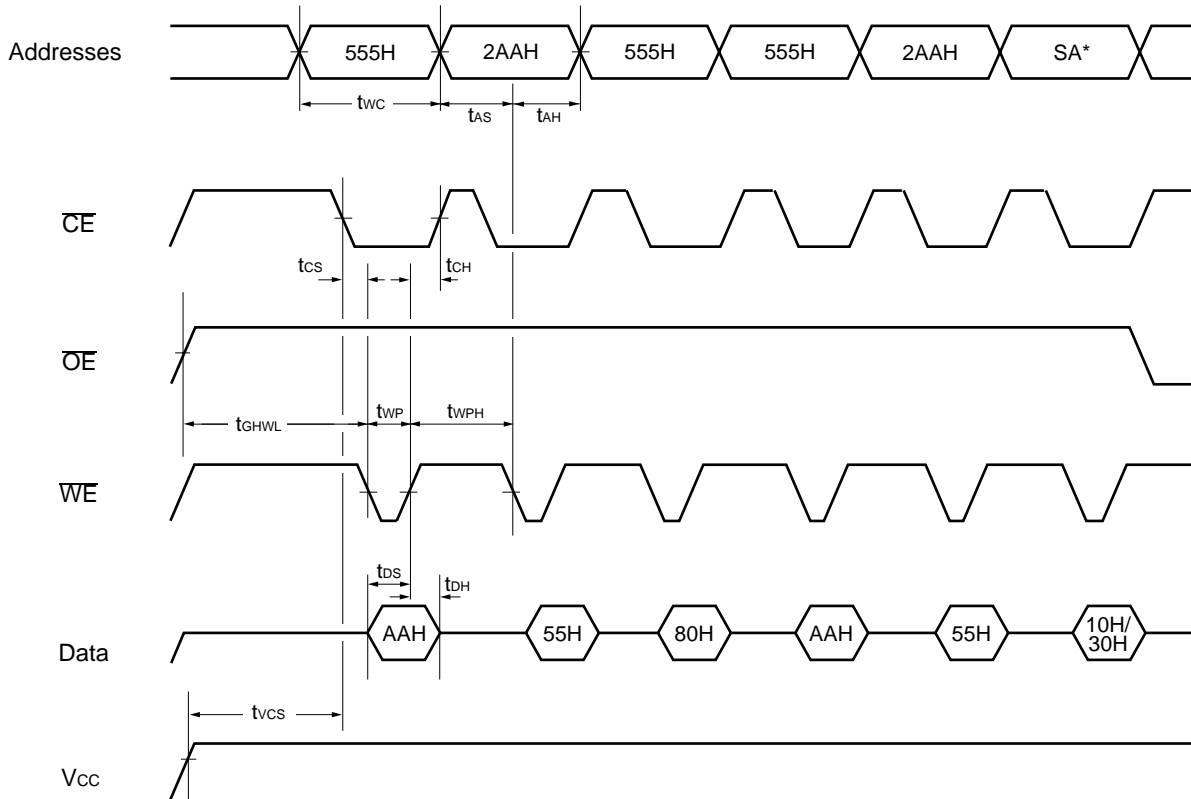
- Notes:**
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. \overline{DQ}_7 is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 3 Alternate WE Controlled Program Operation Timings



- Notes:**
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. \overline{DQ}_7 is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence.
 6. These waveforms are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

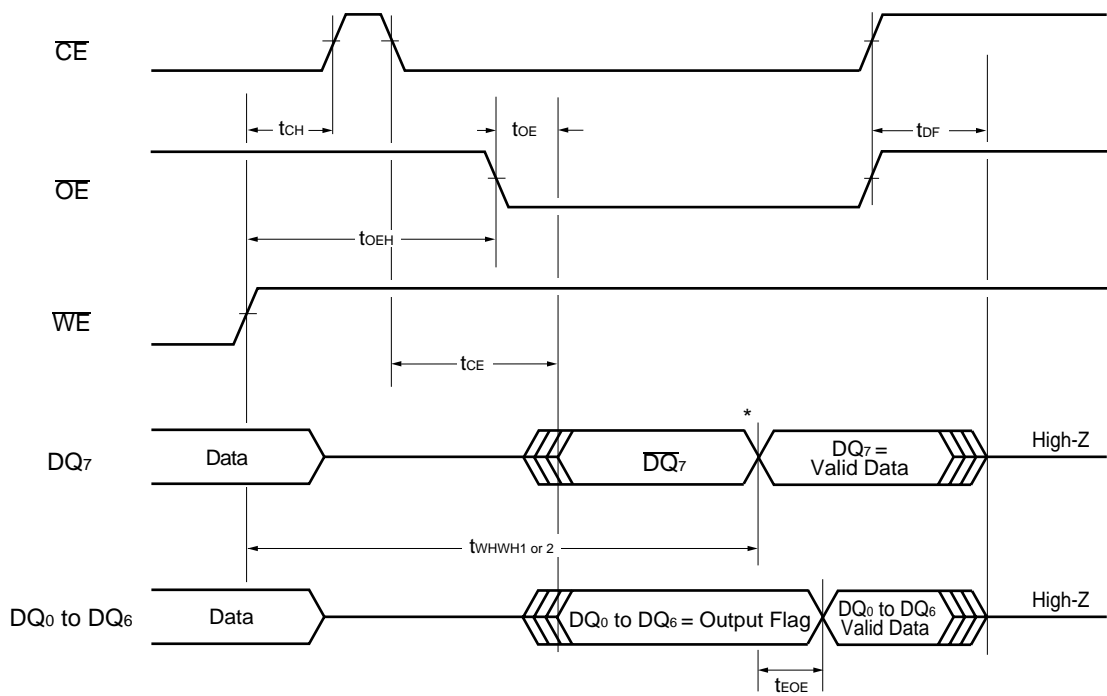
Figure 4 Alternate CE Controlled Program Operation Timings



* : SA is the sector address for Sector Erase. Addresses = 555H (Word), AAH (Byte) for Chip Erase.

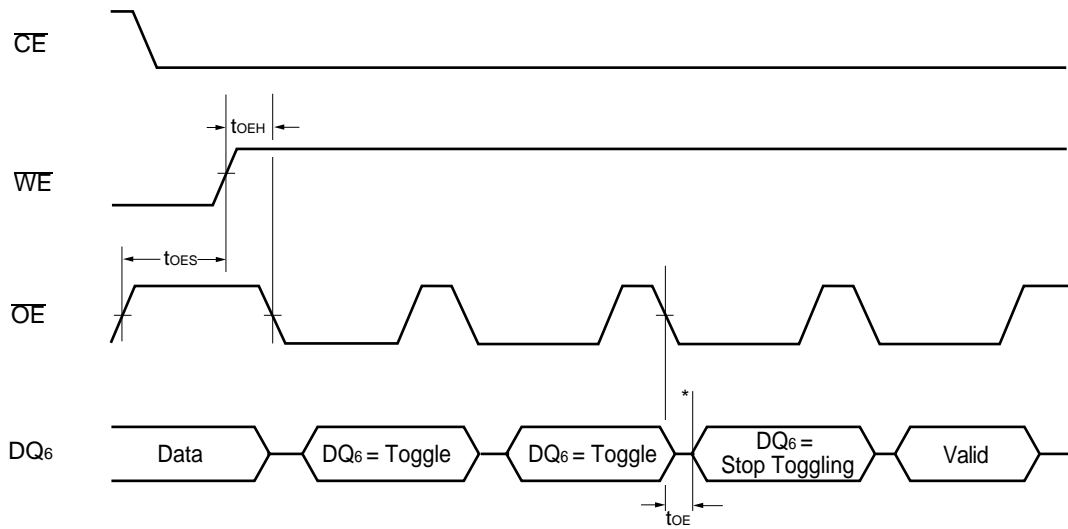
Note: These waveforms are for the $\times 16$ mode. (The addresses differ from $\times 8$ mode.)

Figure 5 AC Waveforms Chip/Sector Erase Operations



* : DQ₇ = Valid Data (The device has completed the Embedded operation.)

Figure 6 AC Waveforms for Data Polling during Embedded Algorithm Operations



* : DQ₆ stops toggling.(The device has completed the Embedded operation.)

Figure 7 AC Waveforms for Toggle Bit during Embedded Algorithm Operations

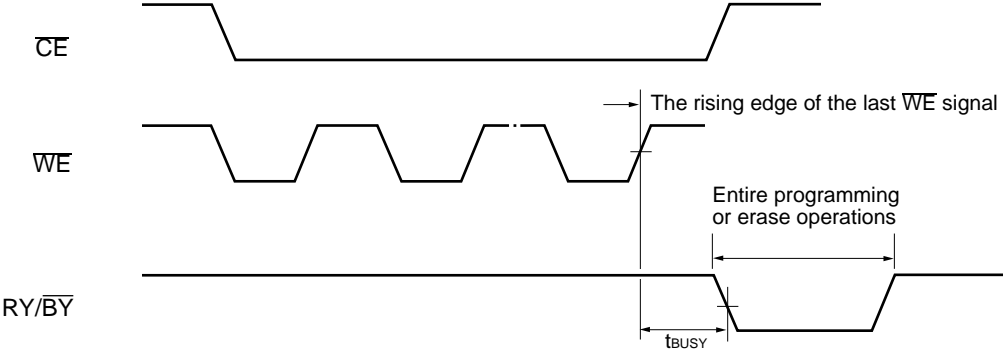


Figure 8 $\overline{RY/BY}$ Timing Diagram during Write/Erase Operations

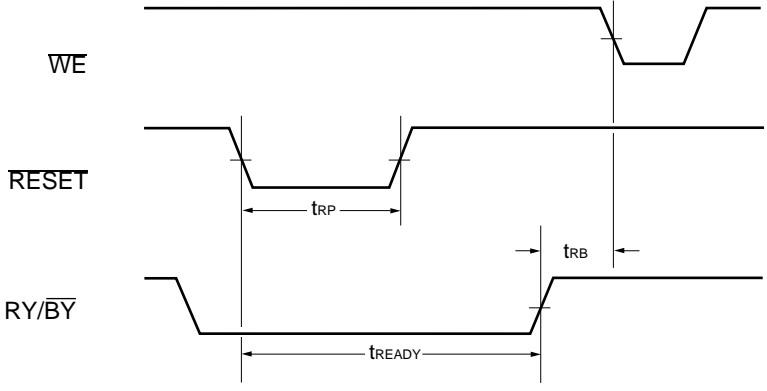
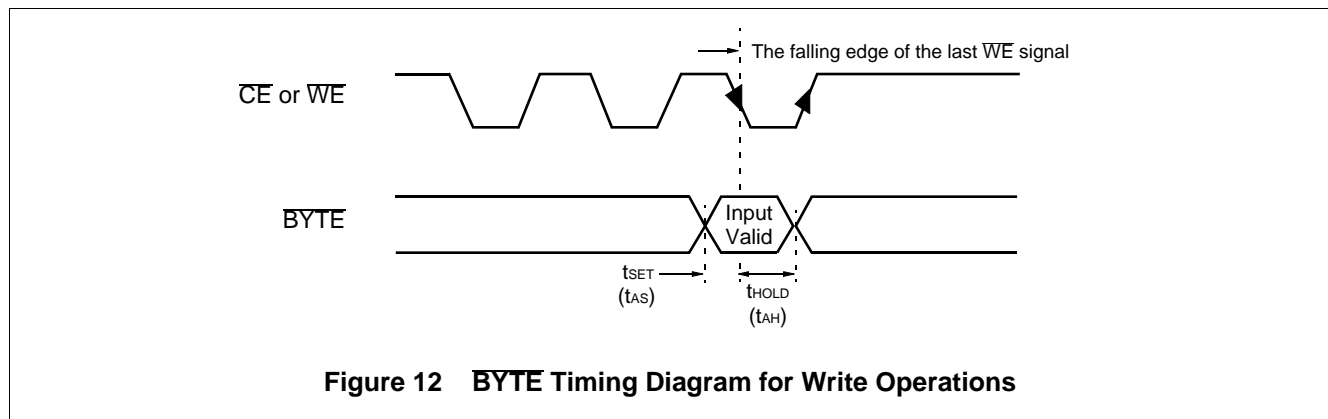
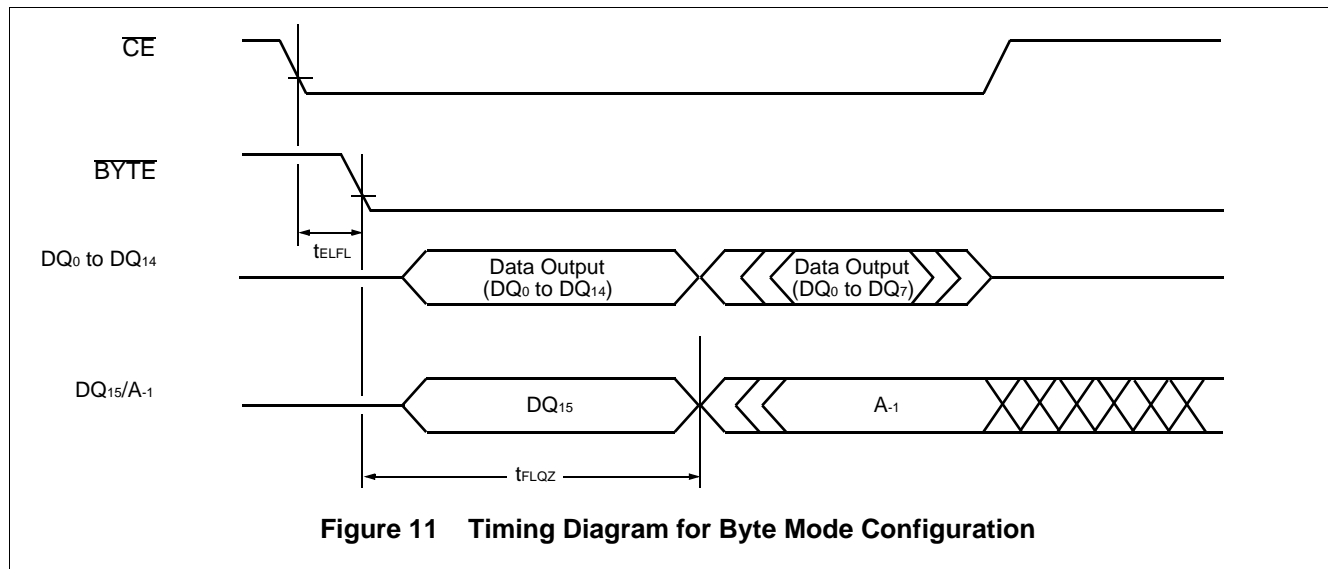
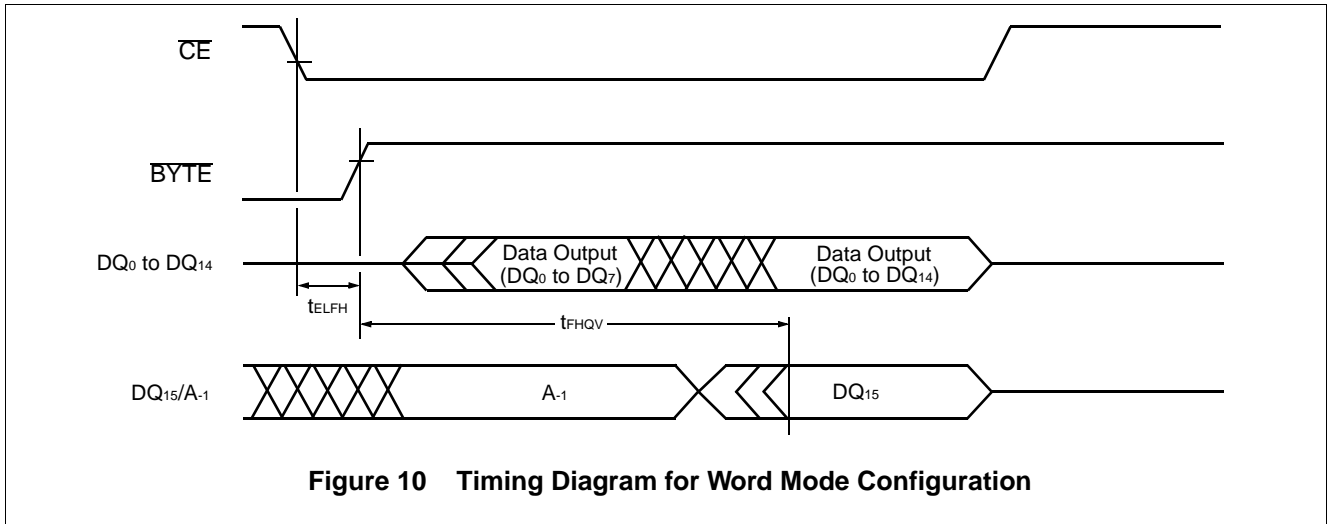
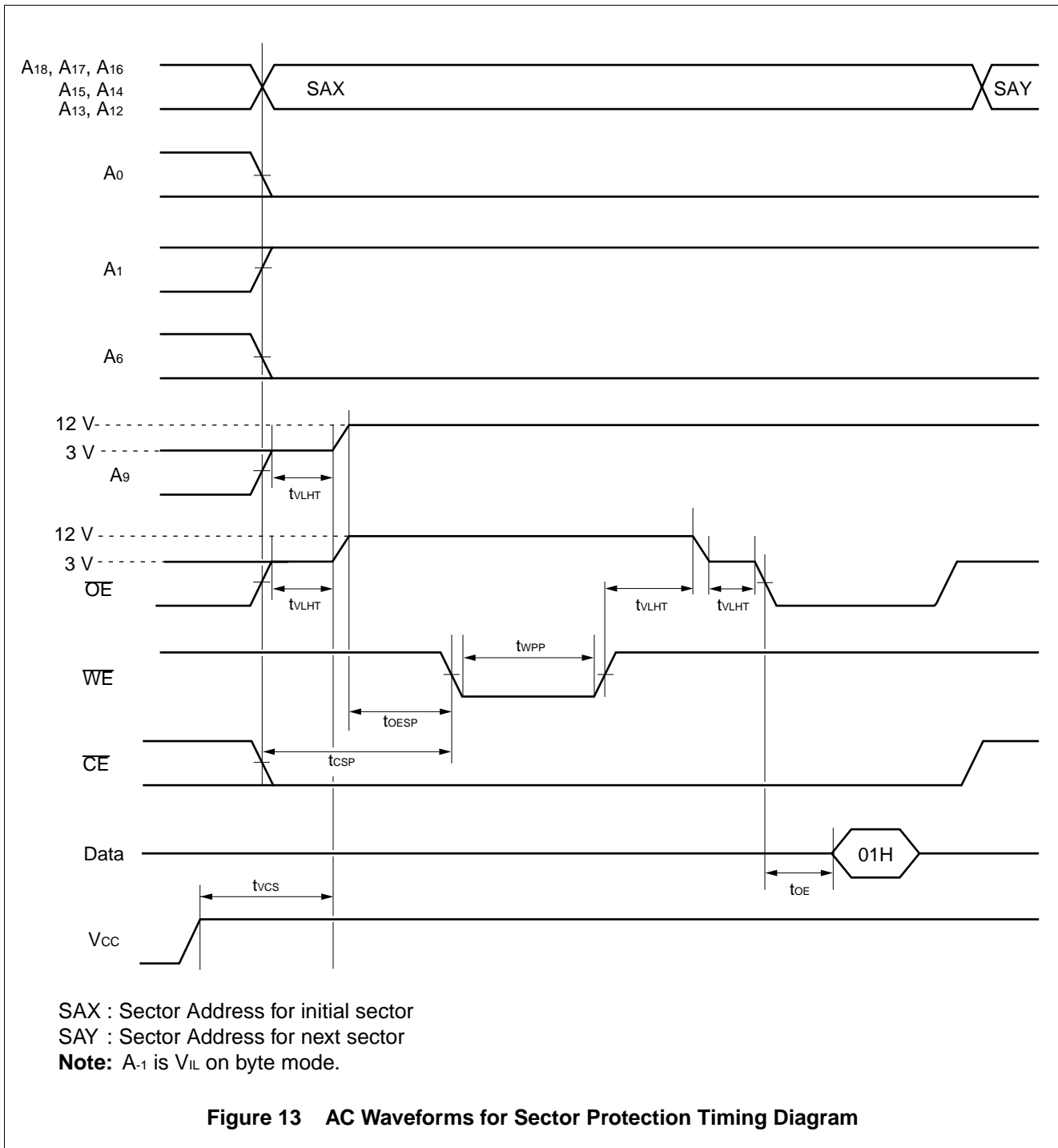


Figure 9 \overline{RESET} , $\overline{RY/BY}$ Timing Diagram





FAST MODE ALGORITHM

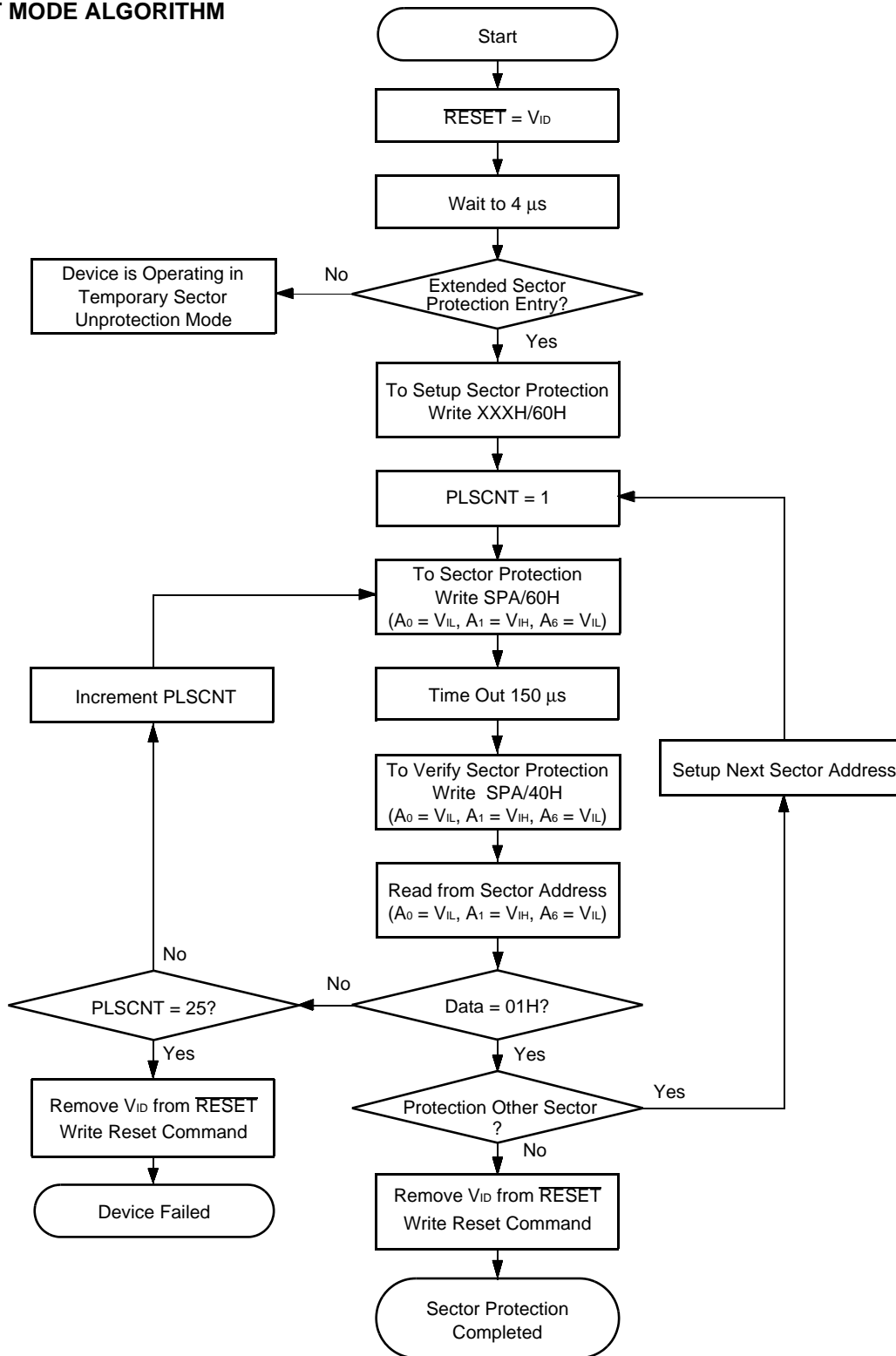
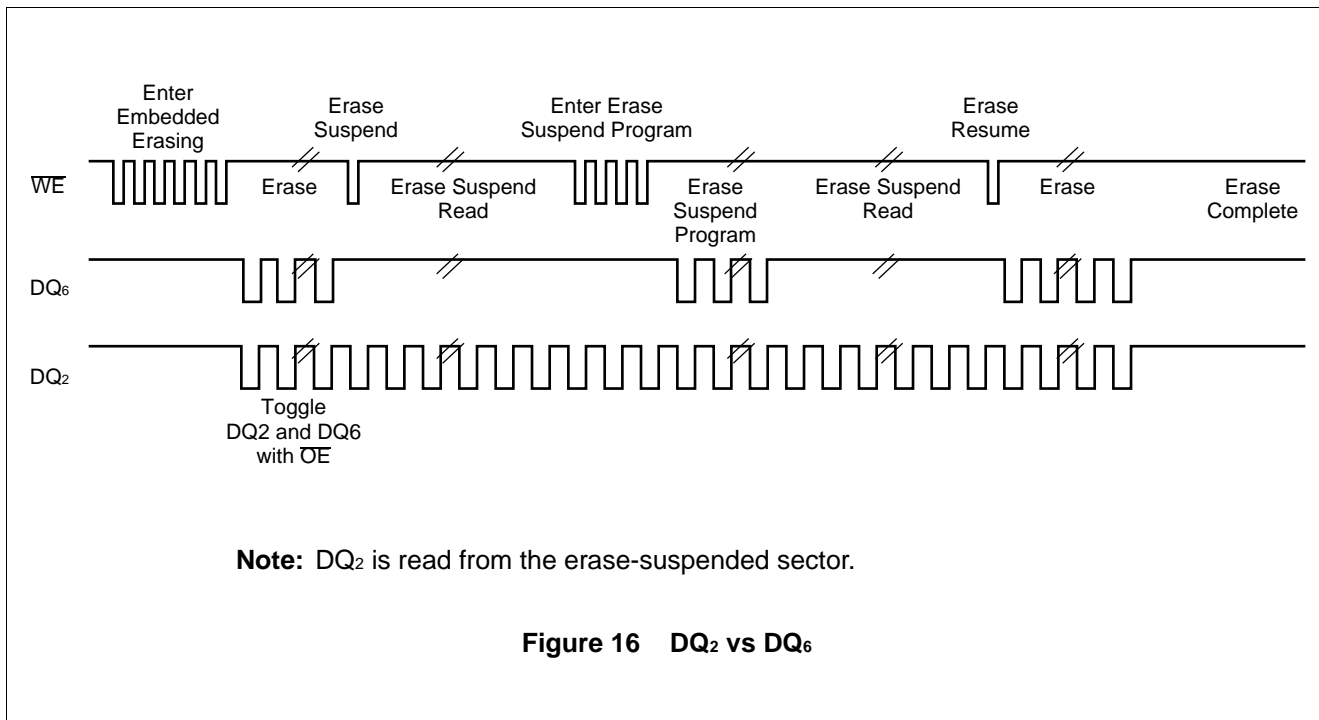
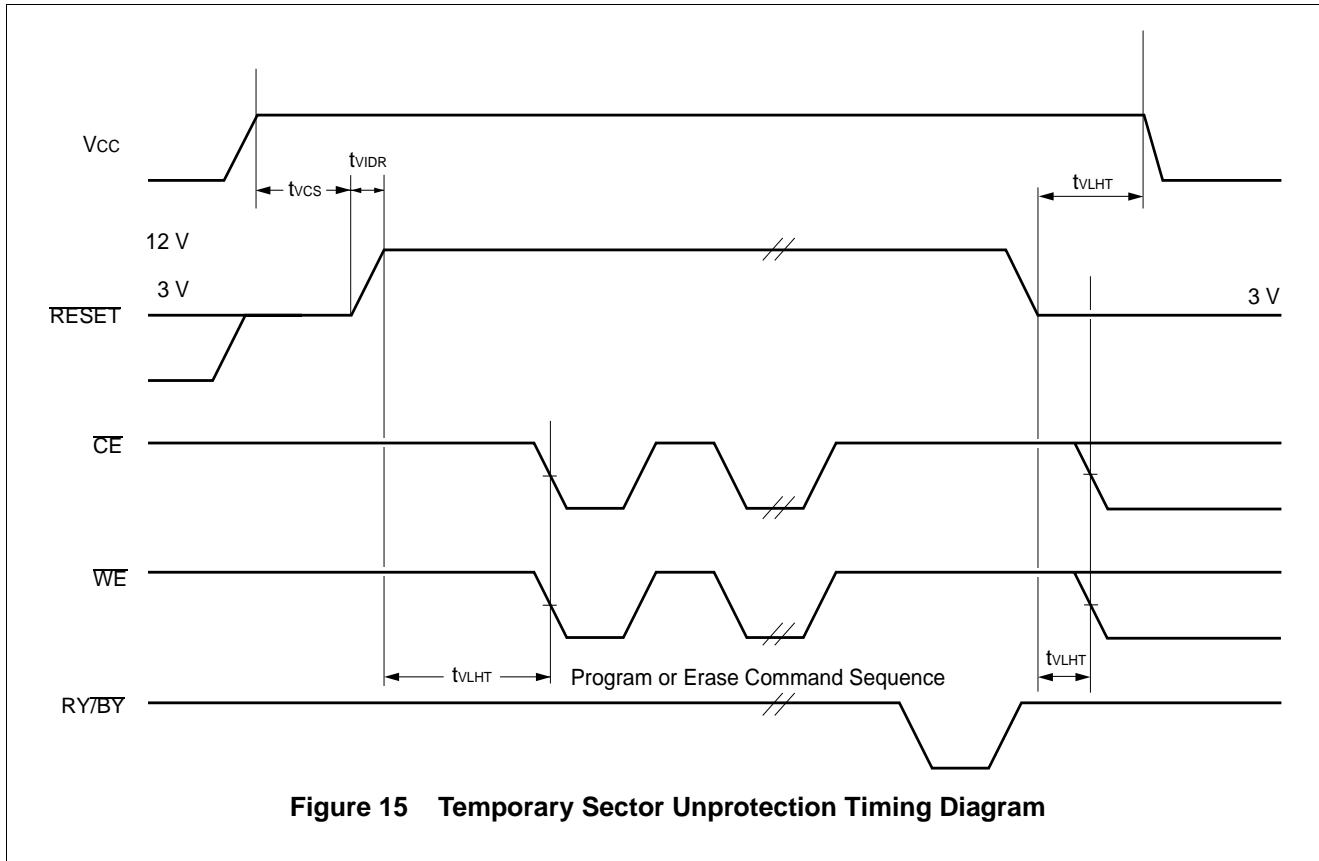


Figure 14 Extended Sector Protection Algorithm



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■ ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Limits | | | Unit | Comments |
|---------------------------------|---------|------|-------|--------|--|
| | Min. | Typ. | Max. | | |
| Sector Erase Time | — | 1 | 15 | sec | Excludes programming time prior to erasure |
| Word Programming Time | — | 16 | 5,200 | μs | Excludes system-level overhead |
| Byte Programming Time | — | 8 | 3,600 | μs | |
| Chip Programming Time (1M Byte) | — | 8.4 | 50 | sec | Excludes system-level overhead |
| Erase/Program Cycle | 100,000 | — | — | cycles | |

■ PIN CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ. | Max. | Unit |
|------------------|-------------------------|----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0 | TBD | TBD | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0 | TBD | TBD | pF |
| C _{IN2} | Control Pin Capacitance | V _{IN} = 0 | TBD | TBD | pF |

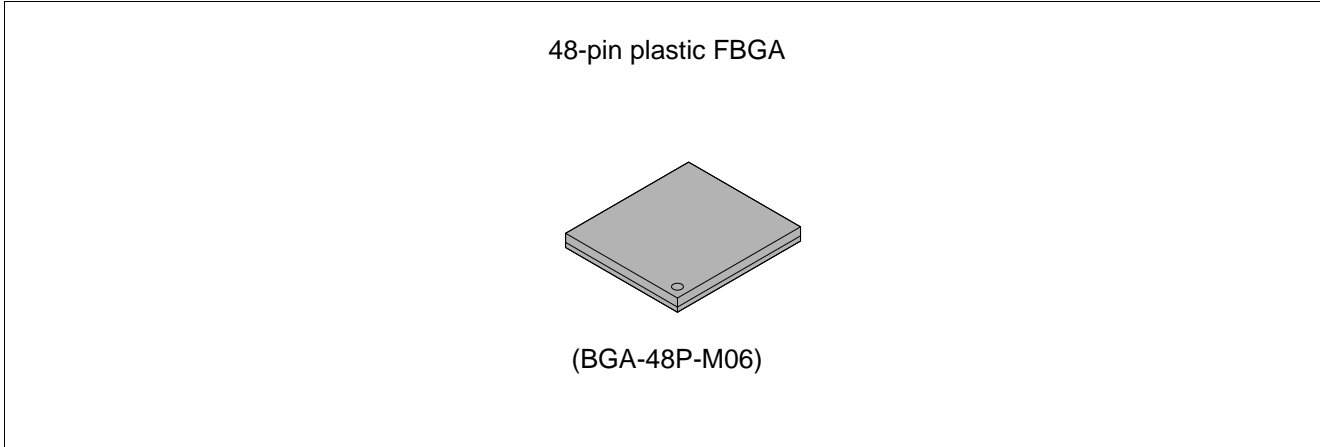
Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package are right angle.

MB84VB2000-10/MB84VB2001-10

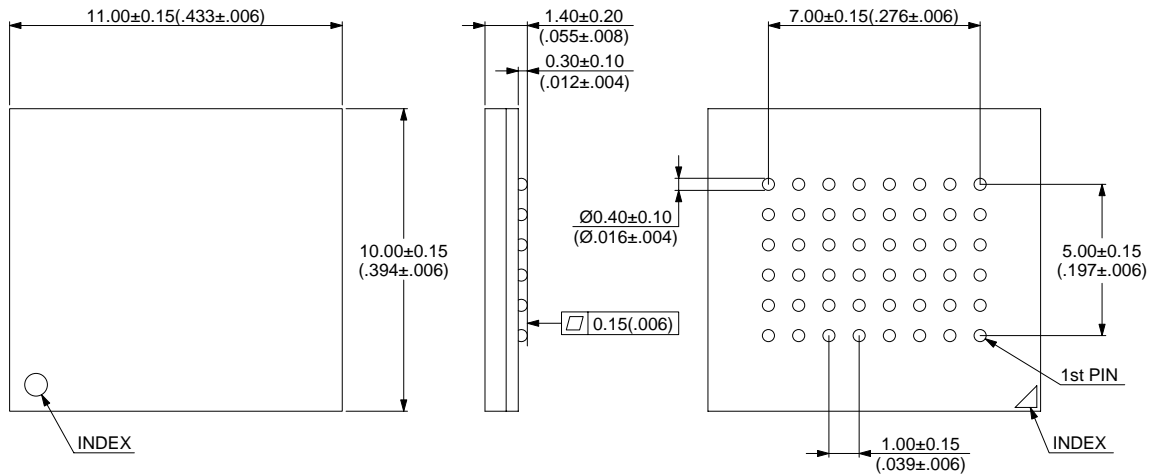
■ PACKAGE



■ PACKAGE DIMENSIONS

48-pin plastic BGA
(BGA-48P-M06)

Note: The actual shape of corners may differ from the dimension.



Dimension in mm (inches).

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