

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89490 Series

MB89497/498/F499/PV490

■ DESCRIPTION

The MB89490 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as 21-bit timebase timer, watch prescaler, PWM timer, 8/16-bit timer/counter, remote receiver control, LCD controller/driver, external interrupt 0 (edge), external interrupt 1 (level), 10-bit A/D converter, UART/SIO, SIO, I²C and watchdog timer reset.

The MB89490 series is designed suitable for compact disc/cassette tape/radio receiver controller as well as in a wide range of applications for consumer product.

*: F²MC stands for FUJITSU Flexible Microcontroller.

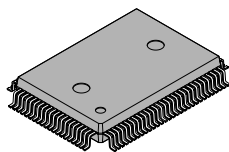
■ FEATURES

- Package used
QFP package for MB89F499, MB89497, MB89498
MQFP package for MB89PV490
- High speed operating capability at low voltage
- Minimum execution time: 0.32 μ s/12.5MHz

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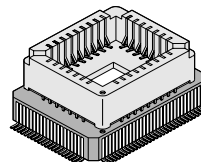
■ PACKAGE

100-pin Plastic QFP



(FTP-100P-M06)

100-pin Ceramic MQFP



(MQP-100C-P01)

MB89490 Series

(Continued)

- F²MC-8L family CPU core

Instruction set optimized for controllers {
 Multiplication and division instructions
 16-bit arithmetic operations
 Test and branch instructions
 Bit manipulation instructions, etc.

- Clock
 Embedded PLL clock multiplication circuit for sub-clock
 Operating clock (PLL for sub-clock) can be selected four times of the sub-clock oscillation
- Six timers
 PWM timer x 2
 8/16-bit timer/counter x 2
 21-bit timebase timer
 Watch prescaler
- External interrupt
 Edge detection (selectable edge) : 8 channels
 Low level interrupt (wake-up function) : 8 channels
- 10-bit A/D converter (8 channels)
 10-bit successive approximation type
- UART/SIO
 Synchronous/asynchronous data transfer capability
- SIO
 Synchronous data transfer capability
- LCD controller/driver
 Max. 32 segments output x 4 commons
- I²C interface circuit
- Remote receiver circuit
- Low-power consumption mode
 Stop mode (oscillation stops so as to minimize the current consumption.)
 Sleep mode (CPU stops so as to reduce the current consumption to approx. 1/3 of normal.)
 Watch mode (everything except the watch prescaler stops so as to reduce the power consumption to an extremely low level.)
 Sub-clock mode
- Watchdog timer reset
- I/O ports: max. 66channels

■ PRODUCT LINEUP

| Part number Parameter | MB89497 | MB89498 | MB89F499 | MB89PV490 |
|--------------------------|--|-------------------------------|------------------------------|------------------------------|
| Classification | Mass production products (mask ROM product) | | FLASH | Piggy-back |
| ROM size | 32K x 8-bit (internal ROM) | 48K x 8-bit (internal ROM) | 60K x 8-bit (internal FLASH) | 60K x 8-bit (external ROM)*1 |
| RAM size | 1K x 8-bit | 2K x 8-bit | 2K x 8-bit | 2K x 8-bit |

*1 : Use MBM27C512 as the external ROM.

MB89490 Series

| Part number Parameter | MB89497 | MB89498 | MB89F499 | MB89PV490 |
|--------------------------------------|---|---------|-------------|-------------|
| CPU functions | Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.32 μ s/12.5 MHz Minimum interrupt processing time : 2.88 μ s/12.5 MHz | | | |
| Ports | I/O ports (CMOS) : 56 pins Input ports (CMOS) : 2 pins N-channel open drain I/O ports : 8 pins Total : 66 pins | | | |
| 21-bit timebase timer | Interrupt period (0.66 ms, 2.6 ms, 21.0 ms, 335.5 ms) at 12.5 MHz | | | |
| Watchdog timer | Reset period (167.8 ms to 335.5 ms) at 12.5 MHz. | | | |
| PWM timer 0,1 | 8-bit reload timer operation (supports square wave output, operating clock period: 1, 8, 16, 64 t_{inst} .) 8-bit resolution PWM operation | | | |
| 8/16-bit timer/counter 00, 01 | Can be operated either as a 2-channel 8-bit timer/counter (timer 00 and timer 01, each with its own independent operating clock cycle), or as one 16-bit timer/counter In timer 00 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capability | | | |
| 8/16-bit timer/counter 10, 11 | Can be operated either as a 2-channel 8-bit timer/counter (timer 10 and timer 11, each with its own independent operating clock cycle), or as one 16-bit timer/counter In timer 10 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capability | | | |
| External interrupt 0 (edge) | 8 independent channels (selectable edge, interrupt vector, request flag) | | | |
| External interrupt 1 (level) | 8 channels (low level interrupt) | | | |
| A/D converter | 10-bit resolution \times 8 channels A/D conversion function (conversion time: 38 t_{inst}) Supports repeated activation by internal clock | | | |
| LCD controller/driver | Common output : 4 (max.) Segment output : 32 (max.) Bias power supply pins : 3 LCD display RAM size : 32 \times 4 bits | | | |
| UART/SIO | Synchronous/asynchronous data transfer capability (Max. baud rate: 97.656 Kbps at 12.5 MHz) (7 and 8 bits with parity bit; 8 and 9 bits without parity bit) | | | |
| SIO | 8-bit serial I/O with LSB first/MSB first selectability One clock selectable from four operation clock (one external shift clock, three internal shift clock: 0.64 μ s, 2.56 μ s, 10.24 μ s at 12.5MHz) | | | |
| I²C^{*1} | 1 channel Use a 2-wire protocol to communicate with other device | | | |
| Remote receiver | Selectable maximum noise width removal Reversible input polarity | | | |
| Standby mode | Sleep mode, stop mode, watch mode, sub-clock mode | | | |
| Process | CMOS | | | |
| Operating voltage | 2.2V ~ 3.6V | | 2.7V ~ 3.6V | 2.7V ~ 3.6V |

*1 : I²C is complied to Philips I²C specification.

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■ PACKAGE AND CORRESPONDING PRODUCTS

| Part number / Package | MB89497/498 | MB89F499 | MB89PV490 |
|-----------------------|-------------|----------|-----------|
| FPT-100P-M06 | O | O | X |
| MQP-100C-P01 | X | X | O |

O : Available
X : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following point:

- The stack area is set at the upper limit of the RAM.

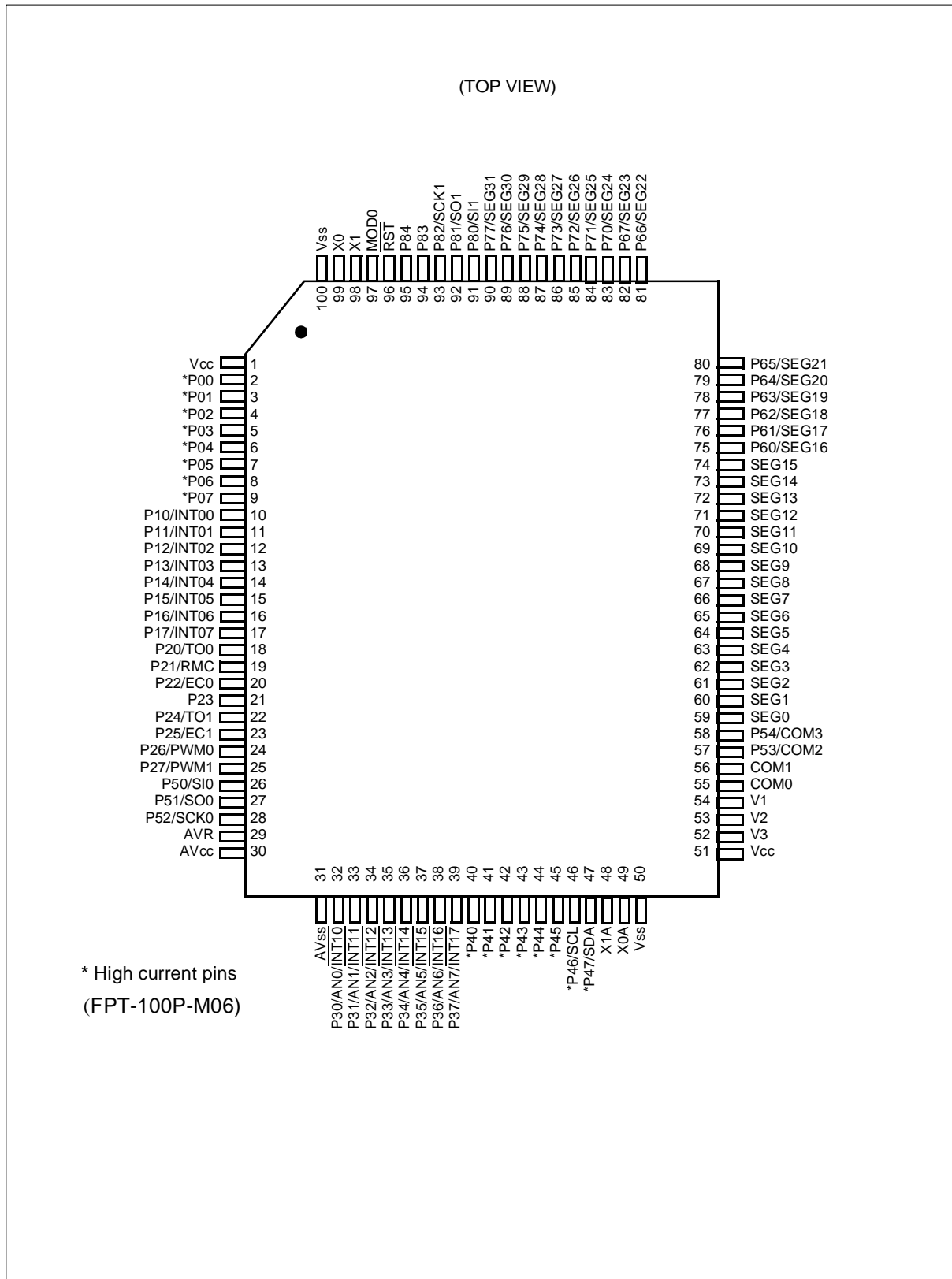
2. Current Consumption

- For the MB89PV490 the current consumed by the EPROM mounted in the piggy-back socket is needed to be included.
- When operating at low speed, the current consumed by the FLASH product is greater than that for the mask ROM product. However, the current consumption is roughly the same in sleep and stop mode.
- For more information, see “■ Electrical Characteristics.”

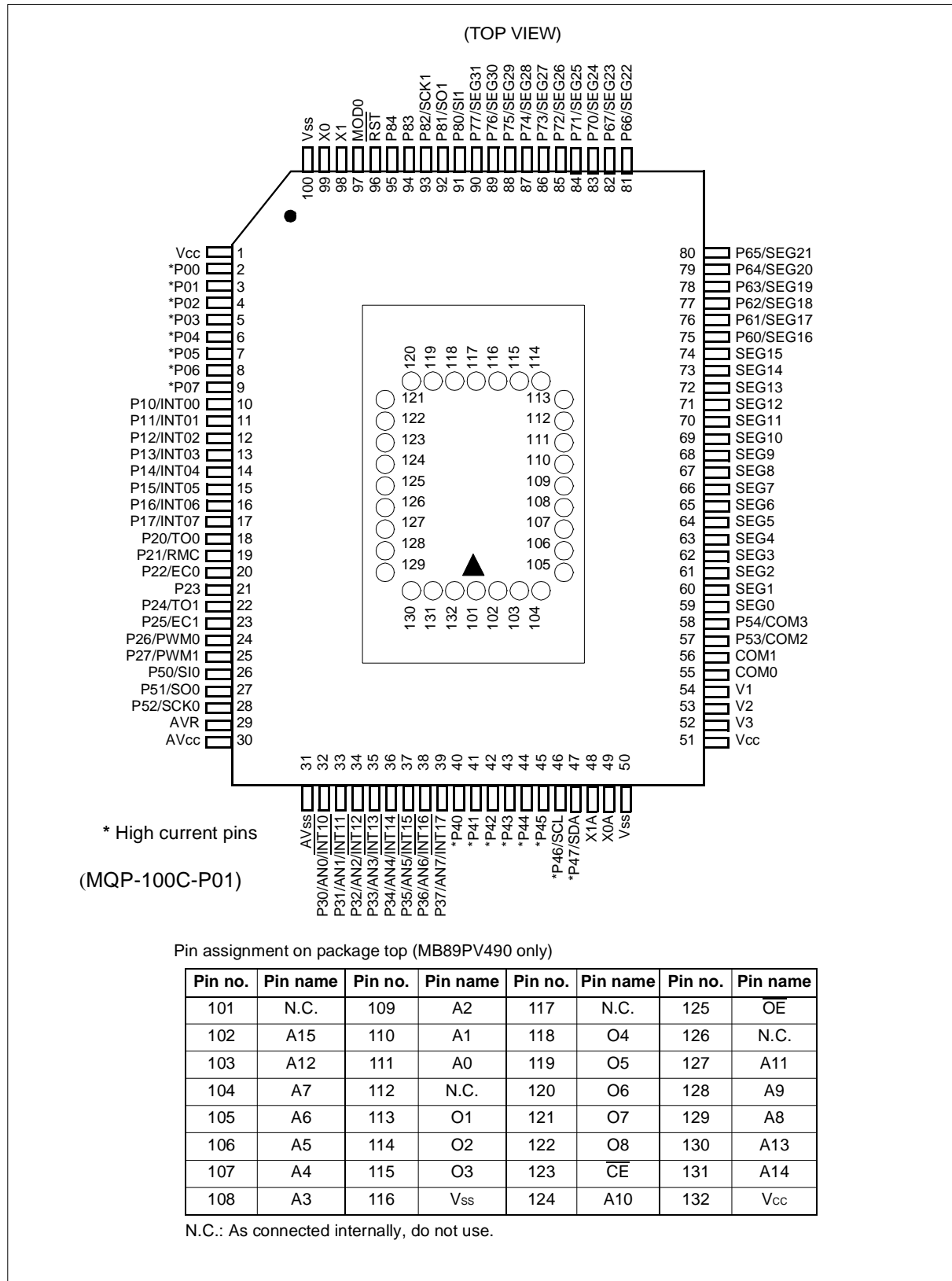
3. Oscillation Stabilization Time after Power-on Reset

- For MB89PV490 and MB89F499, the power-on stabilization time cannot be selected.
- For MB89497 and MB89498, the power-on stabilization time can be selected.
- For more information, please refer to “■ Mask Option”.

PIN ASSIGNMENT



MB89490 Series



■ PIN DESCRIPTION

| Pin number MQFP*1/QFP*2 | Pin name | I/O circuit type | Function |
|----------------------------|---|---------------------|---|
| 99 | X0 | A | Connection pins for a crystal or other oscillator. An external clock can be connected to X0. In this case, leave X1 open. |
| 98 | X1 | | |
| 49 | X0A | A | Connection pins for a crystal or other oscillator. An external clock can be connected to X0A. In this case, leave X1A open. |
| 48 | X1A | | |
| 97 | MOD0 | B | Input pin for setting the memory access mode. Connect directly to V _{SS} . |
| 95, 94 | P84,P83 | J | General-purpose CMOS Input port. |
| 96 | $\overline{\text{RST}}$ | C | Reset I/O pin. The pin is an N-ch open-drain type with pull-up resistor and a hysteresis input. The pin outputs an "L" level when an internal reset request is present. Inputting an "L" level initializes internal circuits. |
| 2~9 | P00 ~ P07 | D | General-purpose CMOS I/O port. |
| 10~17 | P10/INT00 ~ P17/INT07 | E | General-purpose CMOS I/O port. The pin is shared with external interrupt 0 input. |
| 18 | P20/TO0 | F | General-purpose CMOS I/O port. The pin is shared with 8/16-bit timer/counter 00, 01 output. |
| 19 | P21/RMC | E | General-purpose CMOS I/O port. The pin is shared with remote receiver input. |
| 20 | P22/EC0 | E | General-purpose CMOS I/O port. The pin is shared with 8/16-bit timer/counter 00, 01 input. |
| 21 | P23 | F | General-purpose CMOS I/O port. |
| 22 | P24/TO1 | F | General-purpose CMOS I/O port. The pin is shared with 8/16-bit timer/counter 10, 11 output. |
| 23 | P25/EC1 | E | General-purpose CMOS I/O port. The pin is shared with 8/16-bit timer/counter 10,11 input. |
| 24 | P26/PWM0 | F | General-purpose CMOS I/O port. The pin is shared with PWM0 output. |
| 25 | P27/PWM1 | F | General-purpose CMOS I/O port. The pin is shared with PWM1 output. |
| 32 ~ 39 | P30/AN0/ $\overline{\text{INT10}}$ ~ P37/AN7/ $\overline{\text{INT17}}$ | G | General-purpose CMOS I/O port. The pin is shared with external interrupt 1 input and A/D converter input. |
| 40 ~ 45 | P40~P45 | H | General-purpose N-ch open-drain I/O port. |
| 46 | P46/SCL | H | General-purpose N-ch open-drain I/O port. The pin is shared with I2C clock I/O. |
| 47 | P47/SDA | H | General-purpose N-ch open-drain I/O port. The pin is shared with I2C data I/O. |
| 26 | P50/SI0 | E | General-purpose CMOS I/O port. The pin is shared with SIO data input. |
| 27 | P51/SO0 | F | General-purpose CMOS I/O port. The pin is shared with SIO data output. |
| 28 | P52/SCK0 | E | General-purpose CMOS I/O port. The pin is shared with SIO clock I/O. |

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| Pin number MQFP*1/QFP*2 | Pin name | I/O circuit type | Function |
|----------------------------|-----------------------------|------------------|---|
| 57 | P53/COM2 | F / I | General-purpose CMOS I/O port. The pin is shared with the LCD common output. |
| 58 | P54/COM3 | F / I | General-purpose CMOS I/O port. The pin is shared with the LCD common output. |
| 75 ~ 82 | P60/SEG16 ~ P67/SEG23 | F / I | General-purpose CMOS I/O port. The pin is shared with LCD segment output. |
| 83 ~ 90 | P70/SEG24 ~ P77/SEG31 | F / I | General-purpose CMOS I/O port. The pin is shared with LCD segment output. |
| 91 | P80/SI1 | E | General-purpose CMOS I/O port. The pin is shared with UART/SIO data input. |
| 92 | P81/SO1 | F | General-purpose CMOS I/O port. The pin is shared with UART/SIO data output. |
| 93 | P82/SCK1 | E | General-purpose CMOS I/O port. The pin is shared with UART/SIO clock I/O. |
| 59 ~ 74 | SEG0 ~ SEG15 | I | LCD segment output-only pin. |
| 55 ~ 56 | COM0 ~ COM1 | I | LCD common output-only pin. |
| 54, 53, 52 | V1 to V3 | — | LCD driving power supply pin. |
| 1,51 | V _{CC} | — | Power supply pin. |
| 50,100 | V _{SS} | — | Power supply pin (GND). |
| 30 | AV _{CC} | — | A/D converter power supply pin. |
| 29 | AVR | — | A/D converter reference voltage input pin. |
| 31 | AV _{SS} | — | A/D converter power supply pin. Use at the same voltage level as V _{SS} . |

*1: MQP-100C-P01

*2: FPT-100P-M06

• External EPROM Socket (MB89PV490 only)

| Pin number | Pin name | I/O | Function |
|--|--|-----|---|
| MQFP*1 | | | |
| 102 131 130 103 127 124 128 129 104 105 106 107 108 109 110 111 | A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 | O | Address output pins. |
| 122 121 120 119 118 115 114 113 | O8 O7 O6 O5 O4 O3 O2 O1 | I | Data input pins. |
| 101 112 117 126 | N.C. | — | Internally connected pins. Always leave open. |
| 116 | V _{SS} | O | Power supply pin (GND). |
| 123 | \overline{CE} | O | Chip enable pin for the EPROM. Outputs "H" in standby mode. |
| 125 | \overline{OE} | O | Output enable pin for the EPROM. Always outputs "L". |
| 132 | V _{CC} | O | Power supply pin for the EPROM. |

*1: MQP-100C-P01

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■ I/O CIRCUIT TYPE

| Circuit Class | Circuit | Remarks |
|---------------|---------|---|
| A | | <ul style="list-style-type: none"> • Main/Sub-clock circuit |
| B | | <ul style="list-style-type: none"> • Hysteresis input (CMOS input in MB89F499) • The pull-down resistor (not available in MB89F499) Approx. 50kΩ |
| C | | <ul style="list-style-type: none"> • The pull-up resistor (P-channel) Approx. 50 kΩ • Hysteresis input |
| D | | <ul style="list-style-type: none"> • CMOS output • IOH=-4mA, IOL=12mA • CMOS input • Selectable pull-up resistor Approx. 50 kΩ |
| E | | <ul style="list-style-type: none"> • CMOS output • IOH=-2mA, IOL=4mA • CMOS port input • Hysteresis resource input • Selectable pull-up resistor Approx. 50 kΩ |

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| | | |
|----------|--|---|
| <p>F</p> | | <ul style="list-style-type: none"> • CMOS output • IOH=-2mA, IOL=4mA • CMOS input • Selectable pull-up resistor Approx. 50 kΩ |
| <p>G</p> | | <ul style="list-style-type: none"> • CMOS output • IOH=-2mA, IOL=4mA • CMOS port input • Automotive (VIH=0.85Vcc, VIL=0.5Vcc) resource input • Analog input • Selectable pull-up resistor Approx. 50 kΩ |
| <p>H</p> | | <ul style="list-style-type: none"> • N-ch open-drain output • IOL=15mA • CMOS port input • CMOS resource input • 5V tolerance |
| <p>I</p> | | <ul style="list-style-type: none"> • LCD segment output |
| <p>J</p> | | <ul style="list-style-type: none"> • CMOS input |

MB89490 Series

■ HANDLING DEVICES

1. Preventing Latch-up

Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS} .

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR), and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D is not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

7. Treatment of Unused dedicated LCD pins

When dedicated LCD pins are not in use, keep them open.

■ PROGRAMMING AND ERASING FLASH MEMORY ON THE MB89F499

1. Flash Memory

The flash memory is located between 1000_H and FFFF_H in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mask ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the CPU, providing an efficient method of updating program and data.

2. Flash Memory Features

- 60 K byte × 8-bit configuration (16 K + 8 K + 8 K + 28 K sectors)
- Automatic programming algorithm (Embedded algorithm* : Equivalent to MBM29LV200)
- Includes an erase pause and restart function
- Data polling and toggle bit for detection of program/erase completion
- Detection of program/erase completion via CPU interrupt
- Compatible with JEDEC-standard commands
- Sector Protection (sectors can be combined in any combination)
- No. of program/erase cycles : 10,000 (Min)

*: Embedded Algorithm is a trademark of Advanced Micro Devices.

3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

4. Flash Memory Register

- Control status register (FMCS)

| Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Initial value |
|-------------------|-------|--------|-------|-------|----------|----------|-------|----------|---------------|
| 007A _H | INTE | RDYINT | WE | RDY | Reserved | Reserved | — | Reserved | 000X00-0b |
| | R/W | R/W | R/W | R | R/W | R/W | — | R/W | |

5. Sector Configuration

The table below shows the sector configuration of flash memory and lists the addresses of each sector for both during CPU access a flash memory programming.

- Sector configuration of flash memory

| Flash Memory | CPU Address | Programmer Address* |
|--------------|--|--|
| 16 K bytes | FFFF _H to C000 _H | 1FFFF _H to 1C000 _H |
| 8 K bytes | BFFF _H to A000 _H | 1BFFF _H to 1A000 _H |
| 8 K bytes | 9FFF _H to 8000 _H | 19FFF _H to 18000 _H |
| 28 K bytes | 7FFF _H to 1000 _H | 17FFF _H to 11000 _H |

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* : Programmer address

The programmer address is the address to be used instead of the CPU address when programming data from a parallel flash memory programmer. Use the programmer address on programming or erasing using a general purpose parallel programmer.

6. ROM Programmer Adaptor and Recommended ROM Programmers

| Part number | Package | Adaptor Part No. | Recommended Programmer Manufacturer and Model |
|-------------|--------------|---------------------|--|
| | | Sun Hayato Co. Ltd. | Ando Denki Co. Ltd. |
| MB89F499PF | FPT-100P-M06 | TBD | AF9708 (ver 1.60 or later) AF9709 (ver 1.60 or later) |

* Enquiries

Sunhayato Co. Ltd. : FAX +81-3-5396-9106

Ando Denki Co. Ltd. : TEL +81-44-549-7300

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

2. Programming Socket Adapter

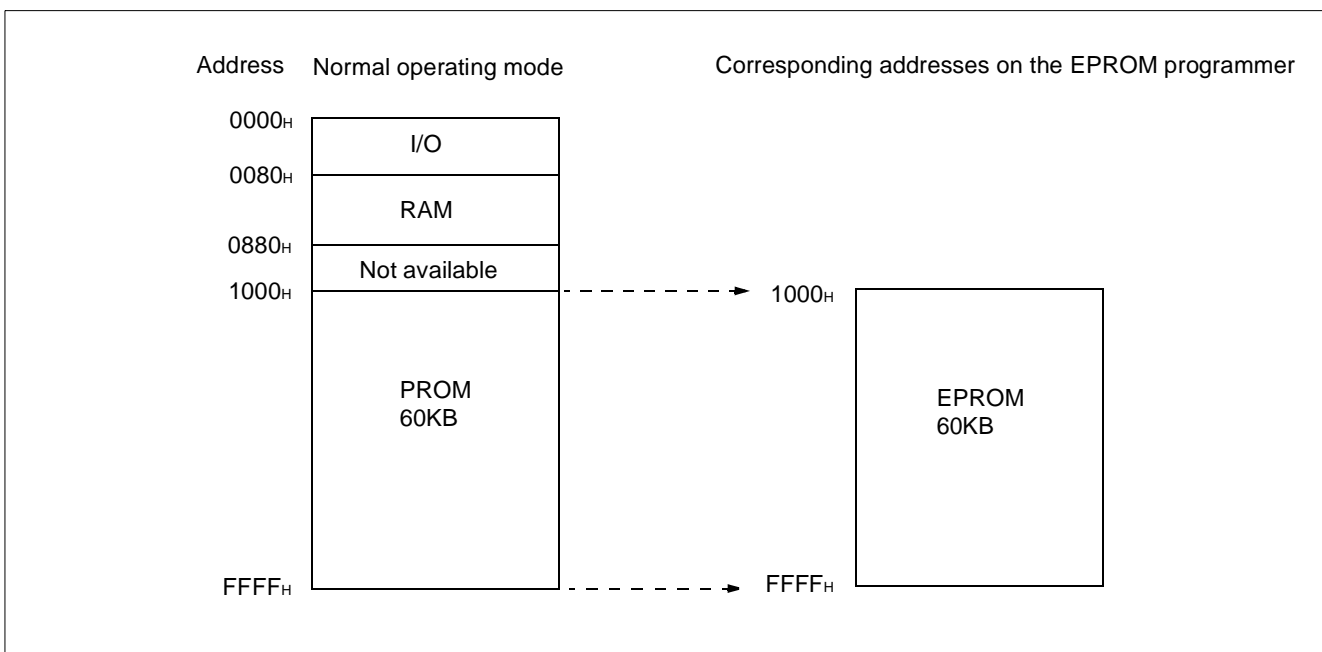
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

| Package | Adapter socket part number |
|--------------------|----------------------------|
| LCC-32 (Rectangle) | ROM-32LC-28DP-YG |

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3986-0403

3. Memory Space

Memory space in each mode is shown in the diagram below.

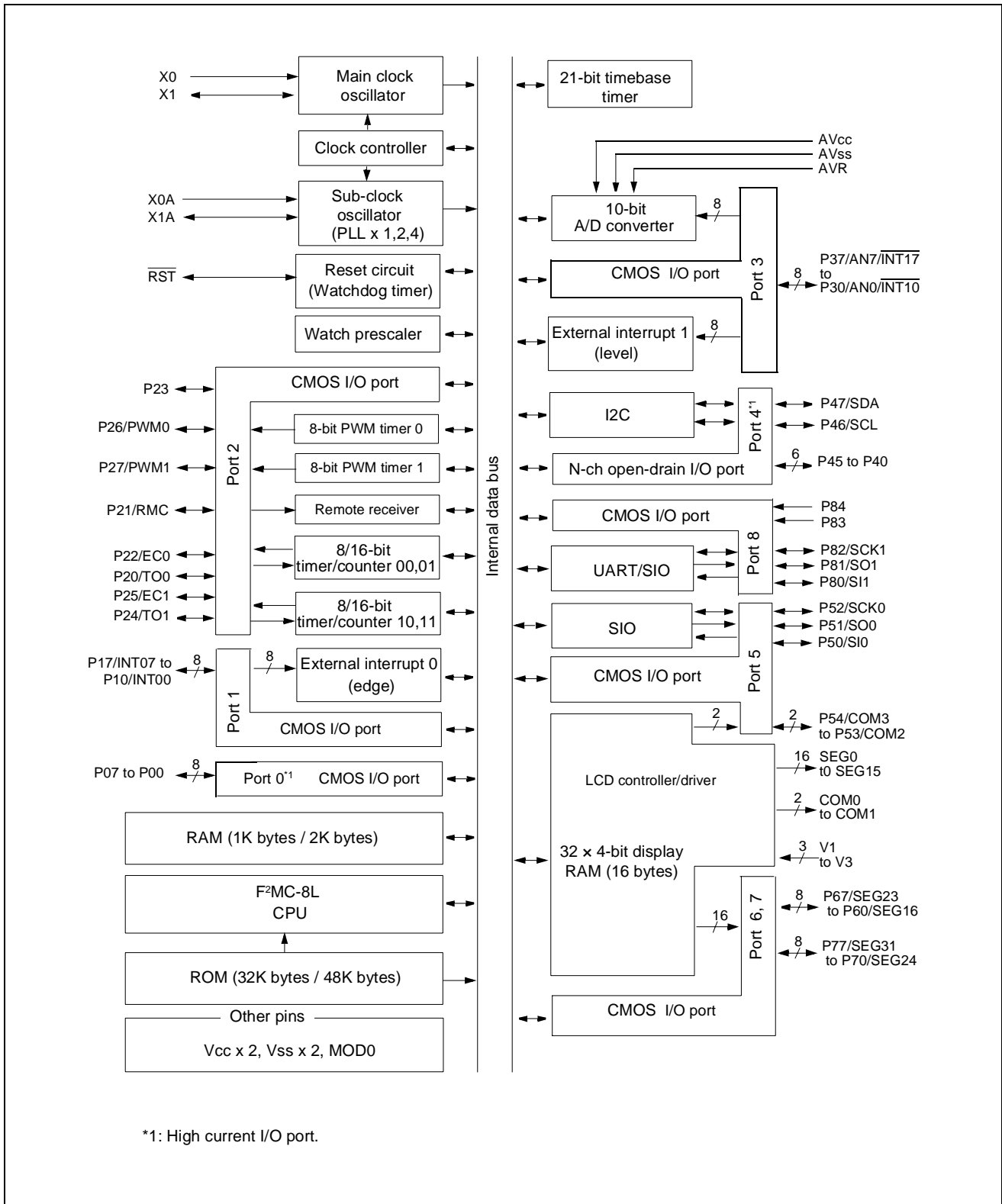


4. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C512.
- (2) Load program data into the EPROM programmer at 1000_H to FFFF_H.
- (3) Program to 1000_H to FFFF_H with the EPROM programmer.

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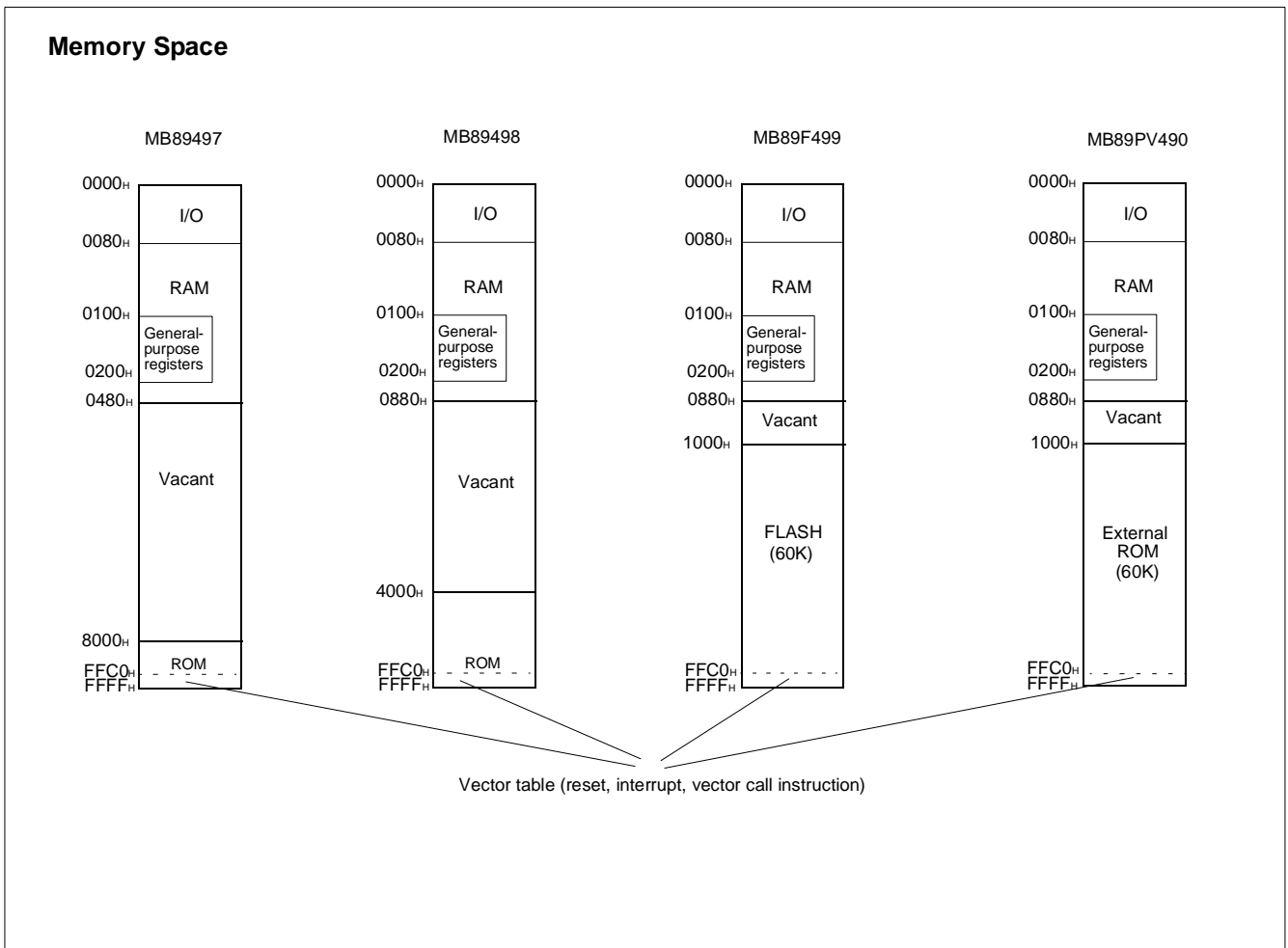
■ Block Diagram



■ CPU CORE

1. Memory Space

The microcontrollers of the MB89490 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89490 series is structured as illustrated below.

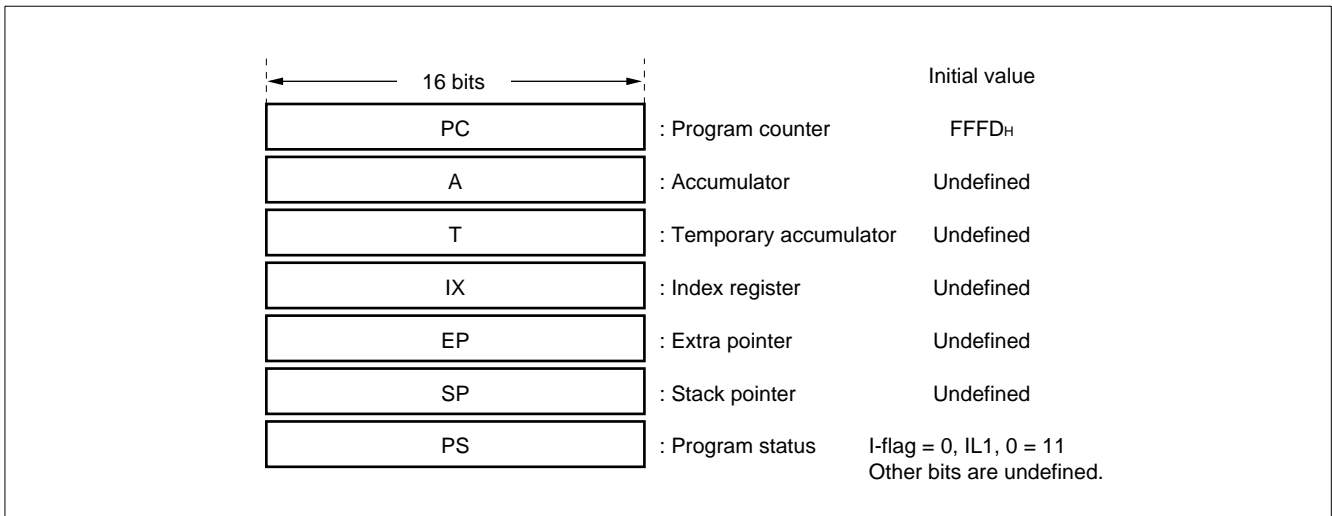


MB89490 Series

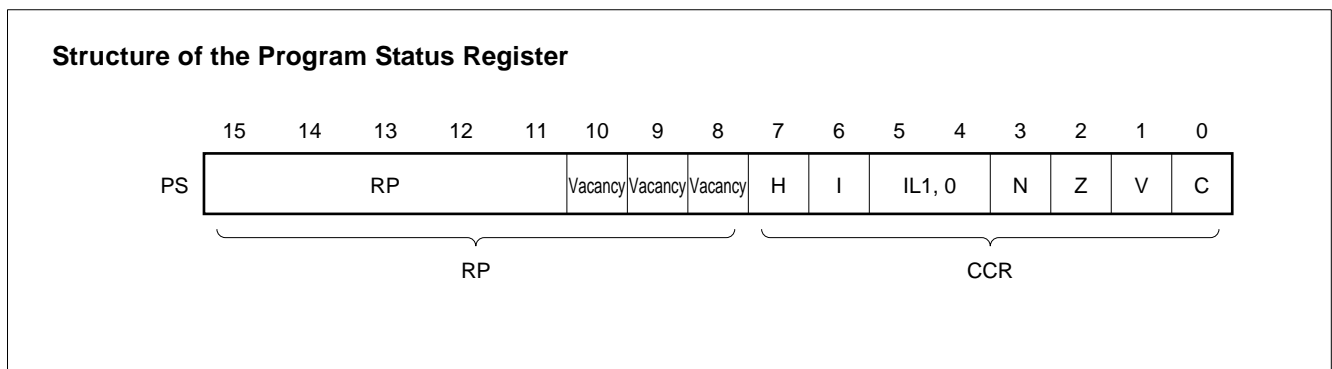
2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

- Program counter (PC): A 16-bit register for indicating instruction storage positions.
- Accumulator (A): A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T): A 16-bit register for performing arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX): A 16-bit register for index modification.
- Extra pointer (EP): A 16-bit pointer for indicating a memory address.
- Stack pointer (SP): A 16-bit register for indicating a stack area.
- Program status (PS): A 16-bit register for storing a register pointer, a condition code.

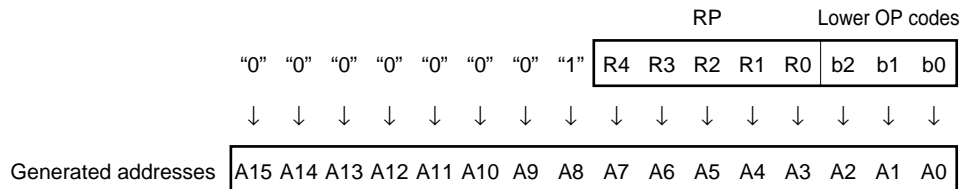


The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Clear to "0" otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to "1". Interrupt is prohibited when the flag is set to "0". Clear to "0" when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | ILO | Interrupt level | Priority |
|-----|-----|-----------------|--------------------------------------|
| 0 | 0 | 1 | High ↑ ↓ Low = no interrupt |
| 0 | 1 | | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | |

N-flag: Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Clear to "0" otherwise.

Z-flag: Set to "1" when an arithmetic operation results in "0". Clear to "0" otherwise.

V-flag: Set to "1" if a signed numeric value overflows because of an arithmetic calculation. Clear to "0" if the overflow does not occur.

C-flag: Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Clear to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

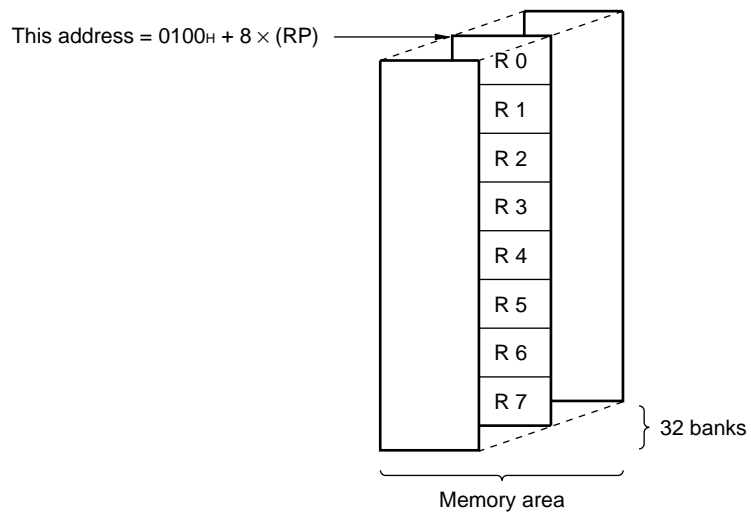
MB89490 Series

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89490 series. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



■ I/O MAP

| Address | Register name | Register description | Read/Write | Initial value |
|---------|---------------|---|------------|-----------------------|
| 00H | PDR0 | Port 0 data register | R/W | XXXXXXXX _B |
| 01H | DDR0 | Port 0 data direction register | W* | 00000000 _B |
| 02H | PDR1 | Port 1 data register | R/W | XXXXXXXX _B |
| 03H | DDR1 | Port 1 data direction register | W* | 00000000 _B |
| 04H | PDR2 | Port 2 data register | R/W | 00000000 _B |
| 05H | (Reserved) | | | |
| 06H | DDR2 | Port 2 data direction register | R/W | 00000000 _B |
| 07H | SYCC | System clock control register | R/W | X-1MM100 _B |
| 08H | STBC | Standby control register | R/W | 00010XXX _B |
| 09H | WDTC | Watchdog timer control register | W* | 0---XXXX _B |
| 0AH | TBTC | Timebase timer control register | R/W | 00---000 _B |
| 0BH | WPCR | Watch prescaler control register | R/W | 00--0000 _B |
| 0CH | PDR3 | Port 3 data register | R/W | XXXXXXXX _B |
| 0DH | DDR3 | Port 3 data direction register | R/W | 00000000 _B |
| 0EH | RSFR | Reset flag register | R | XXXX---- _B |
| 0FH | PDR4 | Port 4 data register | R/W | 11111111 _B |
| 10H | PDR5 | Port 5 data register | R/W | ---XXXX _B |
| 11H | DDR5 | Port 5 data direction register | R/W | ---0000 _B |
| 12H | PDR6 | Port 6 data register | R/W | XXXXXXXX _B |
| 13H | DDR6 | Port 6 data direction register | R/W | 00000000 _B |
| 14H | PDR7 | Port 7 data register | R/W | XXXXXXXX _B |
| 15H | DDR7 | Port 7 data direction register | R/W | 00000000 _B |
| 16H | PDR8 | Port 8 data register | R/W | ---XXXX _B |
| 17H | DDR8 | Port 8 data direction register | R/W | ---0000 _B |
| 18H | EIC0 | External interrupt 0 control register 0 | R/W | 00000000 _B |
| 19H | EIC1 | External interrupt 0 control register 1 | R/W | 00000000 _B |
| 1AH | EIC2 | External interrupt 0 control register 2 | R/W | 00000000 _B |
| 1BH | EIC3 | External interrupt 0 control register 3 | R/W | 00000000 _B |
| 1CH | EIE1 | External interrupt 1 enable register | R/W | 00000000 _B |
| 1DH | EIF1 | External interrupt 1 flag register | R/W | -----0 _B |
| 1EH | SMR | Serial mode register | R/W | 00000000 _B |
| 1FH | SDR | Serial data register | R/W | XXXXXXXX _B |
| 20H | T01CR | Timer 01 control register | R/W | 000000X0 _B |
| 21H | T00CR | Timer 00 control register | R/W | 000000X0 _B |
| 22H | T01DR | Timer 01 data register | R/W | XXXXXXXX _B |
| 23H | T00DR | Timer 00 data register | R/W | XXXXXXXX _B |
| 24H | T11CR | Timer 11 control register | R/W | 000000X0 _B |
| 25H | T10CR | Timer 10 control register | R/W | 000000X0 _B |

(Continued)

MB89490 Series

(Continued)

| Address | Register name | Register description | Read/Write | Initial value |
|------------------------------------|---------------|--|------------|-----------------------|
| 26 _H | T11DR | Timer 11 data register | R/W | XXXXXXXX _B |
| 27 _H | T10DR | Timer 10 data register | R/W | XXXXXXXX _B |
| 28 _H | ADER | A/D input enable register | R/W | 1111111 _B |
| 29 _H | ADC0 | A/D control register 0 | R/W | -0000X0 _B |
| 2A _H | ADC1 | A/D control register 1 | R/W | -0000001 _B |
| 2B _H | ADDH | A/D data register (Upper byte) | R | -----XX _B |
| 2C _H | ADDL | A/D data register (Lower byte) | R | XXXXXXXX _B |
| 2D _H | CNTR0 | PWM 0 timer control register | R/W | 0-000000 _B |
| 2E _H | COMR0 | PWM 0 timer compare register | W* | XXXXXXXX _B |
| 2F _H | SMC0 | UART/SIO serial mode control register | R/W | 00000000 _B |
| 30 _H | SMC1 | UART/SIO serial mode control register | R/W | 00000000 _B |
| 31 _H | SSD | UART/SIO serial status/data register | R/W | 00001--- _B |
| 32 _H | SIDR/SODR | UART/SIO serial data register | R/W | XXXXXXXX _B |
| 33 _H | SRC | UART/SIO serial rate control register | R/W | XXXXXXXX _B |
| 34 _H | CNTR1 | PWM 1 timer control register | R/W | 0-000000 _B |
| 35 _H | COMR1 | PWM 1 timer compare register | W* | XXXXXXXX _B |
| 36 _H | IBSR | I ² C bus status register | R | 00000000 _B |
| 37 _H | IBCR | I ² C bus control register | R/W | 00000000 _B |
| 38 _H | ICCR | I ² C clock control register | R/W | 000XXXXX _B |
| 39 _H | IADR | I ² C address register | R/W | XXXXXXXX _B |
| 3A _H | IDAR | I ² C data register | R/W | XXXXXXXX _B |
| 3B _H | PLLCR | Sub PLL control register | R/W | ----0000 _B |
| 3C _H to 3F _H | (Reserved) | | | |
| 40 _H | RMN | Remote control counter register | R | XXXXXXXX _B |
| 41 _H | RMC | Remote control control register | R/W | 00000000 _B |
| 42 _H | RMS | Remote control status register | R/W | 0X000001 _B |
| 43 _H | RMD | Remote control FIFO data register | R | X----XXX _B |
| 44 _H | RMCD0 | Remote control compare register 0 | R/W | 11111111 _B |
| 45 _H | RMCD1 | Remote control compare register 1 | R/W | 11111111 _B |
| 46 _H | RMCD2 | Remote control compare register 2 | R/W | 11111111 _B |
| 47 _H | RMCD3 | Remote control compare register 3 | R/W | 11111111 _B |
| 48 _H | RMCD4 | Remote control compare register 4 | R/W | 11111111 _B |
| 49 _H | RMCD5 | Remote control compare register 5 | R/W | 11111111 _B |
| 4A _H | RMCI | Remote interrupt register | R/W | -110-000 _B |
| 4B _H to 5D _H | (Reserved) | | | |
| 5E _H | LOCR | LCD controller output control register | R/W | -0000000 _B |
| 5F _H | LCD | LCD controller control register | R/W | 00010000 _B |
| 60 _H to 6F _H | VRAM | LCD data RAM | R/W | XXXXXXXX _B |
| 70 _H | PURC0 | Port 0 pull up resistor control register | R/W | 11111111 _B |
| 71 _H | PURC1 | Port 1 pull up resistor control register | R/W | 11111111 _B |

(Continued)

(Continued)

| Address | Register name | Register description | Read/Write | Initial value |
|------------------------------------|---------------|--|------------|-----------------------|
| 72 _H | PURC2 | Port 2 pull up resistor control register | R/W | 11111111 _B |
| 73 _H | PURC3 | Port 3 pull up resistor control register | R/W | 11111111 _B |
| 74 _H | PURC5 | Port 5 pull up resistor control register | R/W | ---1111 _B |
| 75 _H | PURC6 | Port 6 pull up resistor control register | R/W | 11111111 _B |
| 76 _H | PURC7 | Port 7 pull up resistor control register | R/W | 11111111 _B |
| 77 _H | PURC8 | Port 8 pull up resistor control register | R/W | -----111 _B |
| 78 _H to 79 _H | (Reserved) | | | |
| 7A _H | FMCS | Flash memory control status register | R/W | 000X00-0 _B |
| 7B _H | ILR1 | Interrupt level setting register 1 | W* | 11111111 _B |
| 7C _H | ILR2 | Interrupt level setting register 2 | W* | 11111111 _B |
| 7D _H | ILR3 | Interrupt level setting register 3 | W* | 11111111 _B |
| 7E _H | ILR4 | Interrupt level setting register 4 | W* | 11111111 _B |
| 7F _H | (Reserved) | | | |

* Bit manipulation instruction cannot be used.

● Read/write access symbols

R/W : Readable and writable

R : Read-only

W : Write-only

● Initial value symbols

0: The initial value of this bit is "0".

1: The initial value of this bit is "1".

X: The initial value of this bit is undefined.

- : Unused bit.

M: The initial value of this bit is determined by mask option.

MB89490 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|--|-----------------------|----------------|----------------|------|---|
| | | Min. | Max. | | |
| Power supply voltage | V_{CC} AV_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | AV_{CC} must be equal to V_{CC} |
| | AVR | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | |
| LCD power supply voltage | V1 to V3 | $V_{SS} - 0.3$ | V_{CC} | V | |
| Input voltage | V_i | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | other than P40~P47 |
| | | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | P40~P47 in MB89PV490, MB89497/498 |
| | | $V_{SS} - 0.3$ | $V_{SS} + 5.5$ | V | P40~P47 in MB89F499 |
| Output voltage | V_o | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| “L” level maximum output current | I_{OL} | — | 15 | mA | |
| “L” level average output current | I_{OLAV} | — | 4 | mA | Average value (operating current × operating rate) |
| “L” level total maximum output current | ΣI_{OL} | — | 100 | mA | |
| “L” level total average output current | ΣI_{OLAV} | — | 40 | mA | Average value (operating current × operating rate) |
| “H” level maximum output current | I_{OH} | — | -15 | mA | |
| “H” level average output current | I_{OHAV} | — | -4 | mA | Average value (operating current × operating rate) |
| “H” level total maximum output current | ΣI_{OH} | — | -50 | mA | |
| “H” level total average output current | ΣI_{OHAV} | — | -20 | mA | Average value (operating current × operating rate) |
| Power consumption | P_D | — | 300 | mW | |
| Operating temperature | T_A | -40 | +85 | °C | |
| Storage temperature | T_{stg} | -55 | +150 | °C | |

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks | |
|--------------------------|-------------------------------------|-----------------|-----------------|------|------------------------------------|------------------------|
| | | Min. | Max. | | | |
| Power supply voltage | V _{CC} AV _{CC} | 2.7* | 3.6 | V | Operation assurance range | MB89PV490, MB89F499 |
| | | 2.2* | 3.6 | V | Operation assurance range | MB89497, MB89498 |
| | | 1.5 | 3.6 | V | Retains the RAM state in stop mode | |
| | AVR | 2.7 | 3.6 | V | | |
| LCD power supply voltage | V1 to V3 | V _{SS} | V _{CC} | V | | |
| Operating temperature | T _A | -40 | +85 | °C | | |

* : These values depend on the operating conditions and the analog assurance range. See Figure 1, 2 and "5. A/D Converter Electrical Characteristics."

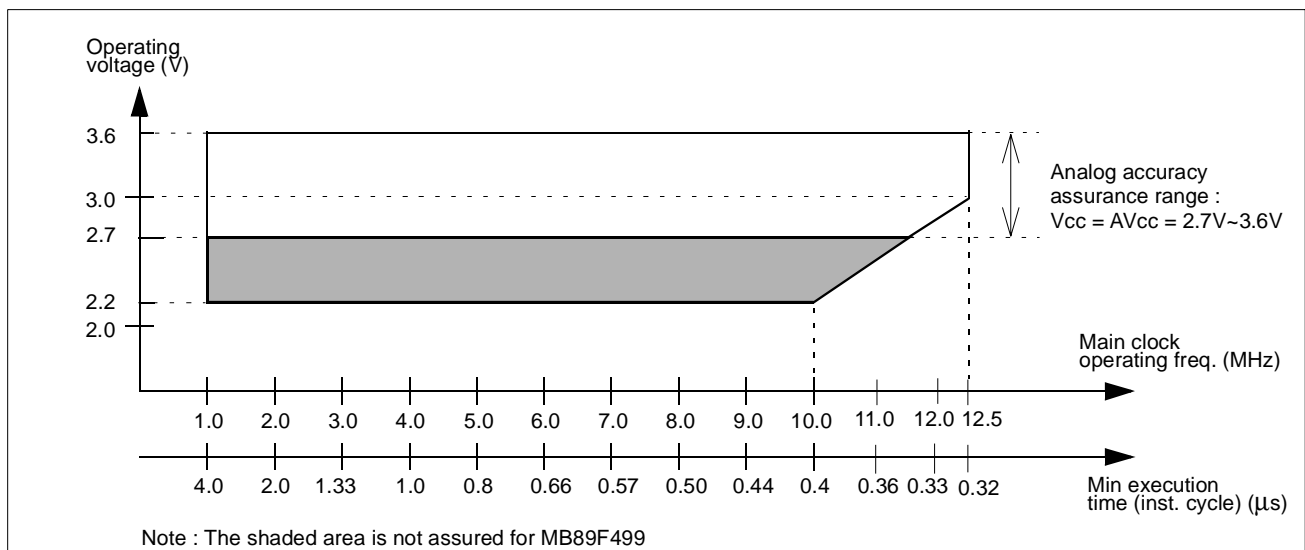


Figure 1 Operating Voltage vs. Main Clock Operating Frequency (MB89F499/497/498)

MB89490 Series

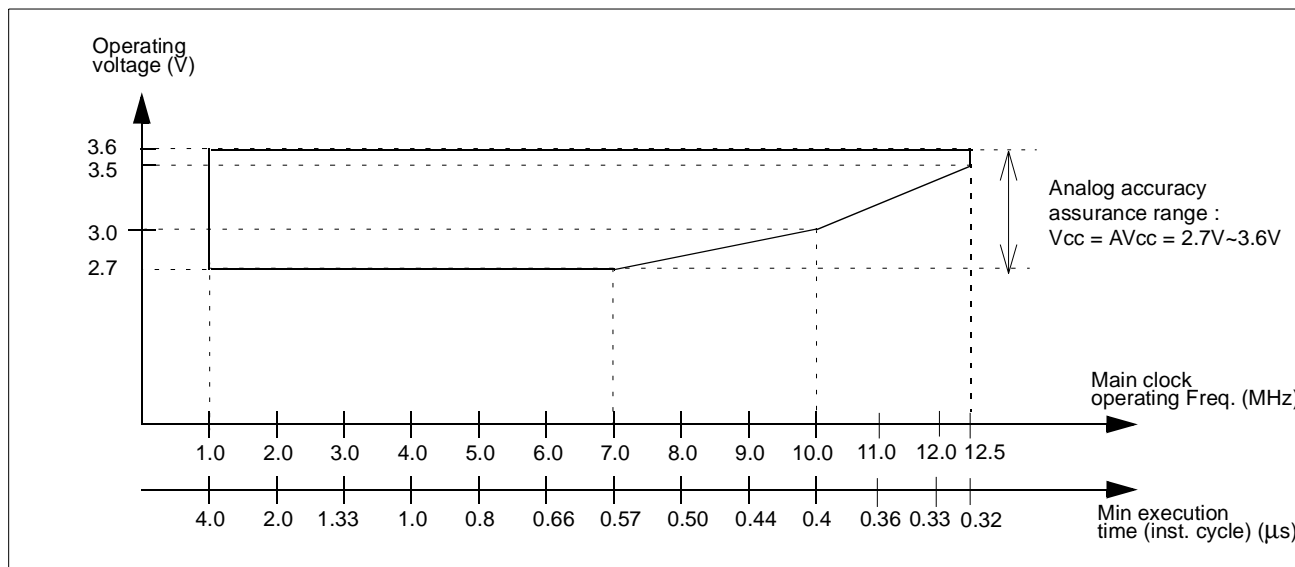


Figure 2 Operating Voltage vs. Main Clock Operating Frequency (MB89PV490)

Figure 1 and 2 indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

MB89490 Series

3. DC Characteristics

($A_{V_{CC}} = V_{CC} = 3.0\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|-----------|---|--|----------------|---------------|----------------|----------------|---------------------------|
| | | | | Min. | Typ. | Max. | | |
| “H” level input voltage | V_{IH} | P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P37, P50 ~ P54, P60 ~ P67, P70 ~ P77, P80 ~ P84, SCL, SDA, MOD1, MOD2 | — | 0.7 V_{CC} | — | $V_{CC} + 0.3$ | V | |
| | | P40 ~ P47 | — | 0.7 V_{CC} | — | $V_{SS} + 6.0$ | V | MB89PV490, MB89497/498 |
| | V_{IHS} | $\overline{\text{RST}}$, MOD0, EC0, EC1, SCK0, SI0, SCK1, SI1, RMC, INT00 ~ INT07 | — | 0.8 V_{CC} | — | $V_{CC} + 0.3$ | V | |
| | | | $\overline{\text{INT10}} \sim \overline{\text{INT17}}$ | — | 0.85 V_{CC} | — | $V_{CC} + 0.3$ | V |
| “L” level input voltage | V_{IL} | P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P37, P40 ~ P47, P50 ~ P54, P60 ~ P67, P70 ~ P77, P80 ~ P84, SCL, SDA, MOD1, MOD2 | — | $V_{SS} - 0.3$ | — | 0.3 V_{CC} | V | |
| | | $\overline{\text{RST}}$, MOD0, EC0, EC1, SCK0, SI0, SCK1, SI1, RMC, INT00 ~ INT07 | — | $V_{SS} - 0.3$ | — | 0.2 V_{CC} | V | |
| | V_{ILA} | $\overline{\text{INT10}} \sim \overline{\text{INT17}}$ | — | $V_{SS} - 0.3$ | — | 0.5 V_{CC} | V | |
| Open-drain output pin application voltage | V_D | P40 ~ P47 | — | $V_{SS} - 0.3$ | — | $V_{SS} + 6.0$ | V | MB89PV490, MB89497/498 |
| | | | — | $V_{SS} - 0.3$ | — | $V_{SS} + 5.5$ | V | MB89F499 |
| “H” level output voltage | V_{OH} | P10 ~ P17, P20 ~ P27, P30 ~ P37, P50 ~ P54, P60 ~ P67, P70 ~ P77, P80 ~ P82 | $I_{OH} = -2.0\text{ mA}$ | 2.2 | — | — | V | |
| | | P00 ~ P07 | $I_{OH} = -4.0\text{ mA}$ | 2.2 | — | — | V | |

(Continued)

MB89490 Series

(Continued)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---------------------------------------|-------------------|--|---|-------|------|------|------|--|
| | | | | Min. | Typ. | Max. | | |
| “L” level output voltage | V _{OL} | P10 ~ P17, P20 ~ P27, P30 ~ P37, P50 ~ P54, P60 ~ P67, P70 ~ P77, $\overline{\text{RST}}$ P80 ~ P82, $\overline{\text{RST}}$ | I _{OL} = 4.0 mA | — | — | 0.4 | V | |
| | | P00 ~ P07 | I _{OL} = 12.0 mA | — | — | 0.4 | V | |
| | | P40 ~ P47 | I _{OL} = 15.0 mA | — | — | 0.4 | V | |
| Input leakage current | I _{LI} | P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P37, P40 ~ P47, P50 ~ P54, P60 ~ P67, P70 ~ P77, P80 ~ P84 | 0.45 V < V _I < V _{CC} | -5 | — | +5 | μA | Without pull-up resistor |
| Open-drain output leakage current | I _{LOD} | P40 ~ P47 | 0.0 V < V _I < V _{CC} | -5 | — | +5 | μA | |
| Pull-down resistance | R _{DOWN} | MOD0 | V _I = V _{CC} | 25 | 50 | 100 | kΩ | Except MB89F499 |
| Pull-up resistance | R _{PULL} | P00 ~ P07, P10 ~ P17, P20 ~ P27, P30 ~ P37, P50 ~ P54, P60 ~ P67, P70 ~ P77, P80 ~ P82, RST | V _I = 0.0 V | 25 | 50 | 100 | kΩ | When pull-up resistor is selected (except RST) |
| Common output impedance | R _{VCOM} | COM0 to COM3 | V1 to V3 = +3.0 V | — | — | 2.5 | kΩ | |
| Segment output impedance | R _{VSEG} | SEG0 to SEG31 | V1 to V3 = +3.0 V | — | — | 15 | kΩ | |
| LCD divided resistance | R _{LCD} | — | Between V _{CC} and V _{SS} | 300 | 500 | 750 | kΩ | |
| LCD controller/driver leakage current | I _{LCDL} | V1 to V3, COM0 to COM3, SEG0 to SEG31 | — | -1 | — | +1 | μA | |

(Continued)

MB89490 Series

(Continued)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|----------------------|--|--|---|-------|----------|---------------------------|----------------|---------------------------|
| | | | | Min. | Typ. | Max. | | |
| Power supply current | I _{CC1} | V _{CC} | F _{CH} = 10 MHz t _{inst} = 0.4 μs Main clock run mode | — | 3.5 | TBD | mA | MB89PV490, MB89497/498 |
| | | | — | 6.0 | TBD | mA | MB89F499 | |
| | I _{CC2} | | F _{CH} = 10 MHz t _{inst} = 6.4 μs Main clock run mode | — | 0.4 | TBD | mA | MB89PV490, MB89497/498 |
| | | | — | 1.5 | TBD | mA | MB89F499 | |
| | I _{CCS1} | | F _{CH} = 10 MHz t _{inst} = 0.4 μs Main clock sleep mode | — | 1.2 | TBD | mA | MB89PV490, MB89497/498 |
| | | | — | 2.0 | TBD | mA | MB89F499 | |
| | I _{CCS2} | | F _{CH} = 10 MHz t _{inst} = 6.4 μs Main clock sleep mode | — | 0.4 | TBD | mA | MB89PV490, MB89497/498 |
| | | | — | 1.0 | TBD | mA | MB89F499 | |
| | I _{CCL} | | F _{CL} = 32.768 kHz Sub-clock mode T _A = +25°C | — | 22.0 | TBD | μA | MB89PV490, MB89497/498 |
| | | | — | 35.0 | TBD | μA | MB89F499 | |
| | I _{CCLPLL} | | F _{CL} = 32.768 kHz Sub-clock mode T _A = +25°C sub PLL x 4 | — | 120.0 | TBD | μA | MB89PV490, MB89497/498 |
| | | | — | 150.0 | TBD | μA | MB89F499 | |
| | I _{CCLS} | | F _{CL} = 32.768 kHz Sub-clock sleep mode T _A = +25°C | — | 7.0 | TBD | μA | MB89PV490, MB89497/498 |
| | | | — | 15.0 | TBD | μA | MB89F499 | |
| I _{CCT} | F _{CL} = 32.768 kHz Watch mode Main clock stop mode T _A = +25°C | — | 1.0 | TBD | μA | MB89PV490, MB89497/498 | | |
| | — | 5.0 | TBD | μA | MB89F499 | | | |
| I _{CCH} | T _A = +25°C Sub-clock stop mode | — | 0.8 | TBD | μA | MB89PV490, MB89497/498 | | |
| | — | 1.0 | TBD | μA | MB89F499 | | | |
| I _A | AV _{CC} | AV _{CC} = 3.0 V, T _A = +25°C | — | 1.0 | 3.0 | mA | A/D converting | |
| I _{AH} | | T _A = +25°C | — | 0.8 | 4.0 | μA | A/D stop | |
| Input capacitance | C _{IN} | Other than V _{CC} , V _{SS} , AV _{CC} , AV _{SS} , AVR | f = 1 MHz | — | 10.0 | — | pF | |

MB89490 Series

4. AC Characteristics

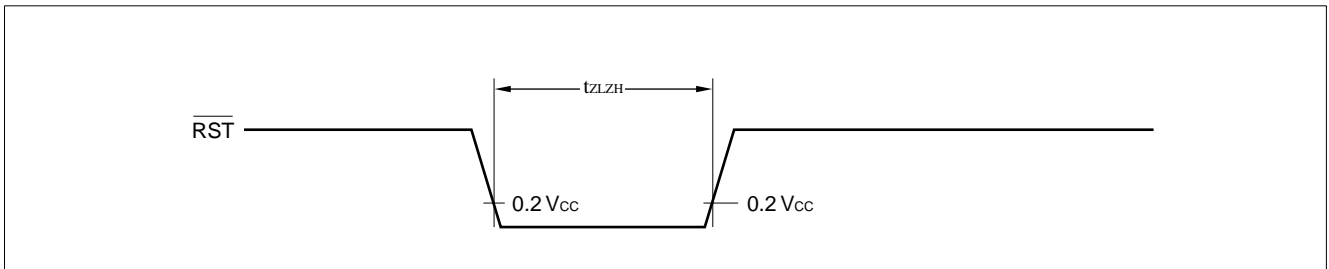
(1) Reset Timing

($A_{V_{CC}} = V_{CC} = 3.0\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|-------------------|-----------|----------------------|------|------|---------|
| | | | Min. | Max. | | |
| $\overline{\text{RST}}$ "L" pulse width | t_{ZLZH} | — | 48 t_{HCYL} | — | ns | |

Note: t_{HCYL} is the oscillation cycle ($1/F_{\text{CH}}$) to input to the X0 pin.

The MCU operation is not guaranteed when the "L" pulse width is shorter than t_{ZLZH} .



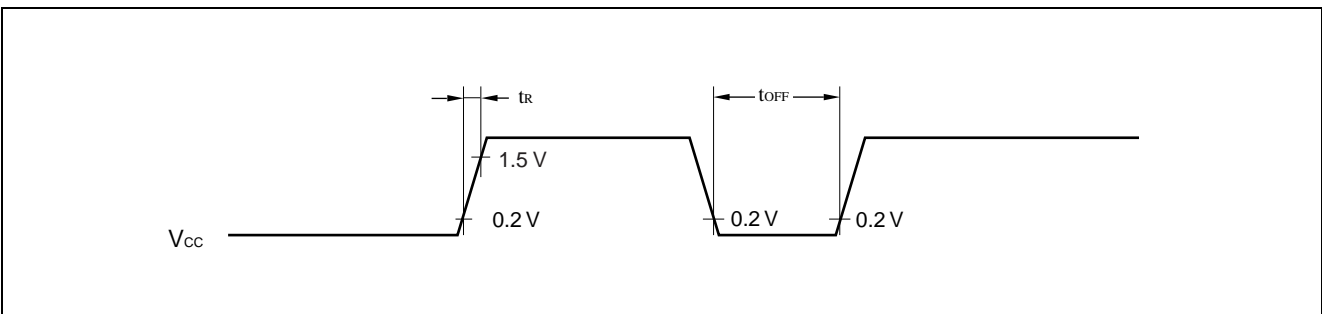
(2) Power-on Reset

($A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---------------------------|------------------|-----------|-------|------|------|----------------------------|
| | | | Min. | Max. | | |
| Power supply rising time | t_{R} | — | — | 50 | ms | |
| Power supply cut-off time | t_{OFF} | | 1 | — | ms | Due to repeated operations |

Note: Make sure that power supply rises within the selected oscillation stabilization time.

Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

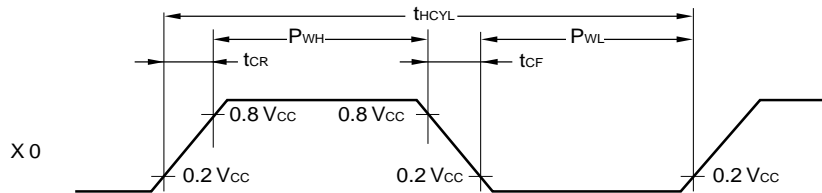


(3) Clock Timing

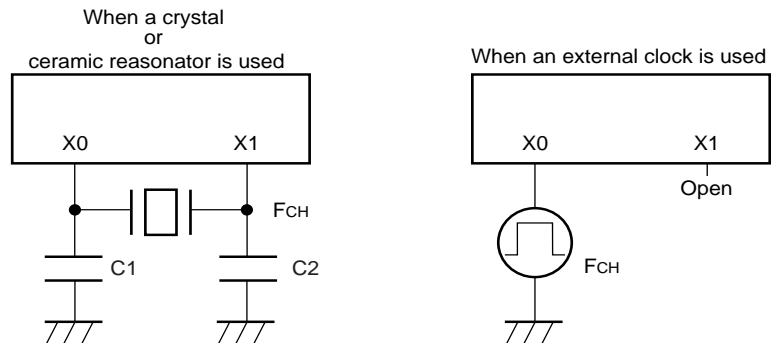
($A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---------------------------------|------------------------|----------|-------|--------|------|---------------|----------------|
| | | | Min. | Typ. | Max. | | |
| Clock frequency | F_{CH} | X0, X1 | 1 | — | 12.5 | MHz | |
| | F_{CL} | X0A, X1A | — | 32.768 | 75 | kHz | |
| Clock cycle time | t_{HCYL} | X0, X1 | 80 | — | 1000 | ns | |
| | t_{LCYL} | X0A, X1A | 13.3 | 30.5 | — | μs | |
| Input clock pulse width | P_{WH} P_{WL} | X0 | 20 | — | — | ns | External clock |
| | P_{WHL} P_{WLL} | X0A | — | 15.2 | — | μs | |
| Input clock rising/falling time | t_{CR} t_{CF} | X0, X0A | — | — | 10 | ns | |

X0 and X1 Timing and Conditions

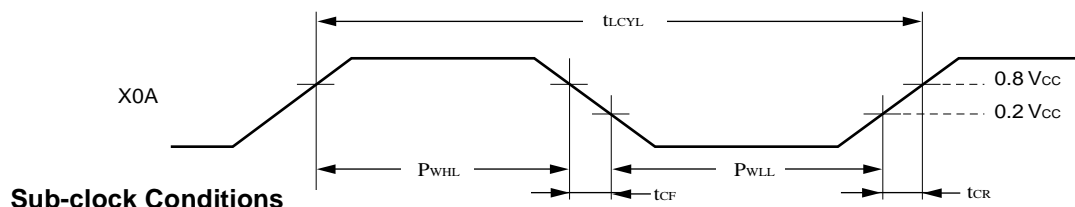


Main Clock Conditions



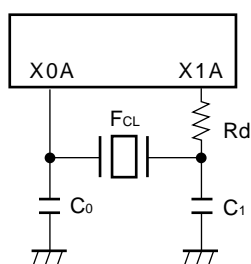
MB89490 Series

Sub-clock Timing and Conditions

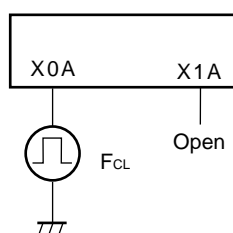


Sub-clock Conditions

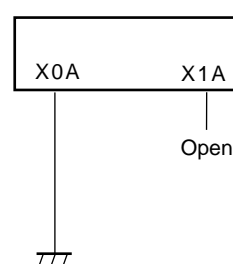
When a crystal or ceramic oscillator is used



When an external clock is used



When subclock is not used

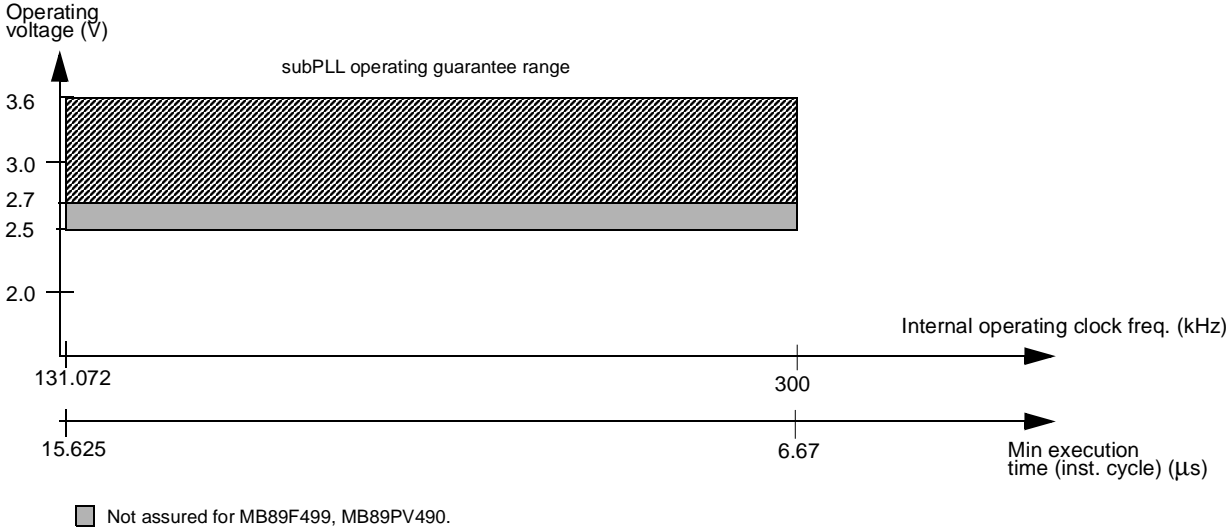


(4) Instruction Cycle

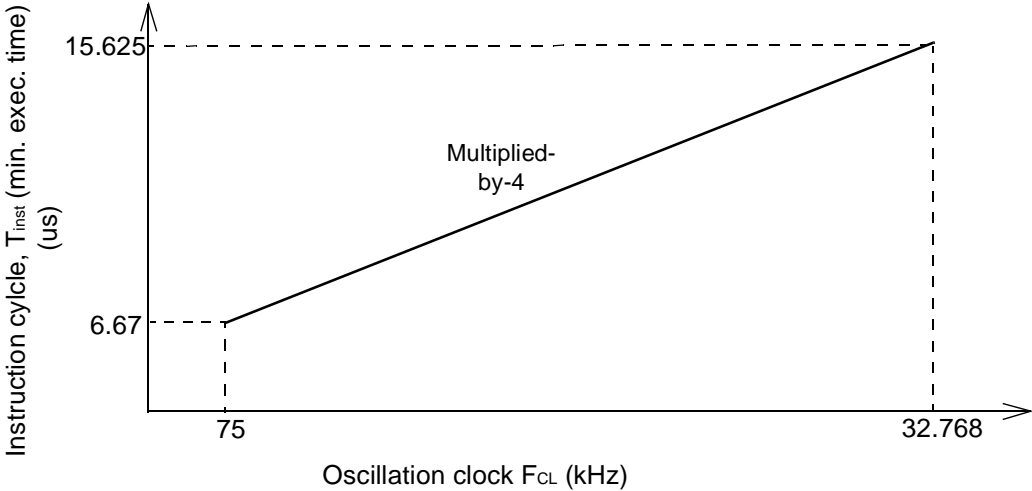
| Parameter | Symbol | Value | Unit | Remarks |
|--|------------|--|---------|---|
| Instruction cycle (minimum execution time) | t_{inst} | $4/F_{CH}, 8/F_{CH}, 16/F_{CH}, 64/F_{CH}$ | μs | $(4/F_{CH})t_{inst} = 0.32 \mu s$ when operating at $F_{CH} = 12.5 \text{ MHz}$ |
| | | $2/F_{CL}, 1/2F_{CL}$ | μs | $(2/F_{CL})t_{inst} = 61.036 \mu s$ when operating at $F_{CL} = 32.768 \text{ kHz}$ |

- PLL operation guarantee range (subPLL x 4)

Relationship between internal operating clock frequency and power supply voltage



Relationship between subclock oscillating frequency and instruction cycle when subPLL is enabled



MB89490 Series

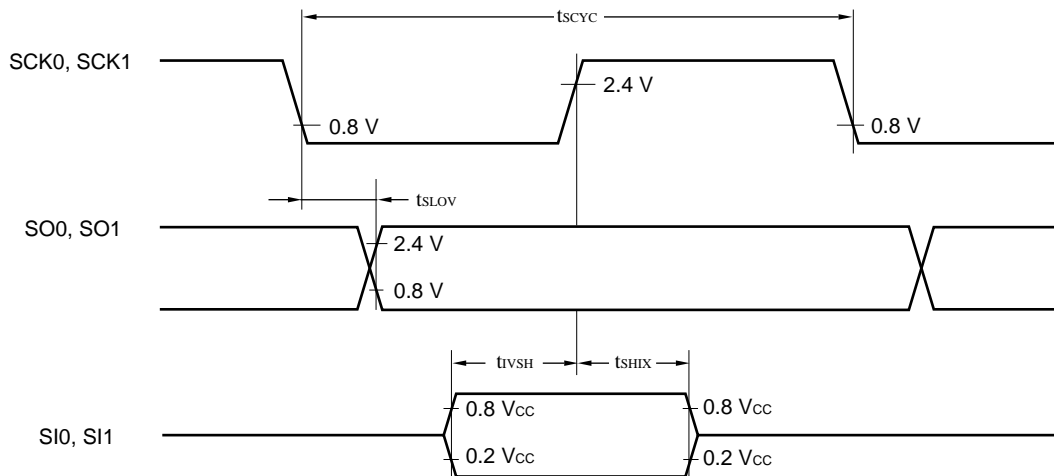
(5) Serial I/O Timing

($A_{V_{CC}} = V_{CC} = 3.0\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

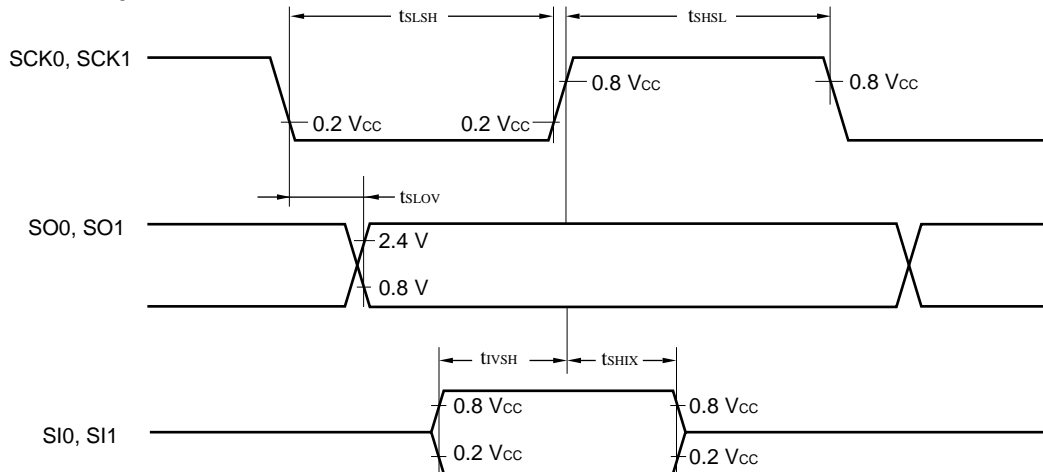
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|------------|----------------------|---------------------------|------------------|------|---------------|
| | | | | Min. | Max. | |
| Serial clock cycle time | t_{SCYC} | SCK0, SCK1 | Internal shift clock mode | $2 t_{inst}^*$ | — | μs |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK0, SCK1, SO0, SO1 | | -200 | 200 | ns |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI0, SI1, SCK0, SCK1 | | $1/2 t_{inst}^*$ | — | μs |
| SCK $\uparrow \rightarrow$ valid SI hold time | t_{SHIX} | SCK0, SCK1, SI0, SI1 | | $1/2 t_{inst}^*$ | — | μs |
| Serial clock "H" pulse width | t_{SHSL} | SCK0, SCK1 | External shift clock mode | $1 t_{inst}^*$ | — | μs |
| Serial clock "L" pulse width | t_{SLSH} | | | $1 t_{inst}^*$ | — | μs |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK0, SCK1, SO0, SO1 | | 0 | 200 | ns |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI0, SI1, SCK0, SCK1 | | $1/2 t_{inst}^*$ | — | μs |
| SCK $\uparrow \rightarrow$ valid SI hold time | t_{SHIX} | SCK0, SCK1, SI0, SI1 | | $1/2 t_{inst}^*$ | — | μs |

* : For information on t_{inst} , see "(4) Instruction Cycle."

Internal Clock Operation



External Clock Operation



(6) I²C Timing

(V_{CC} = 3.0V, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

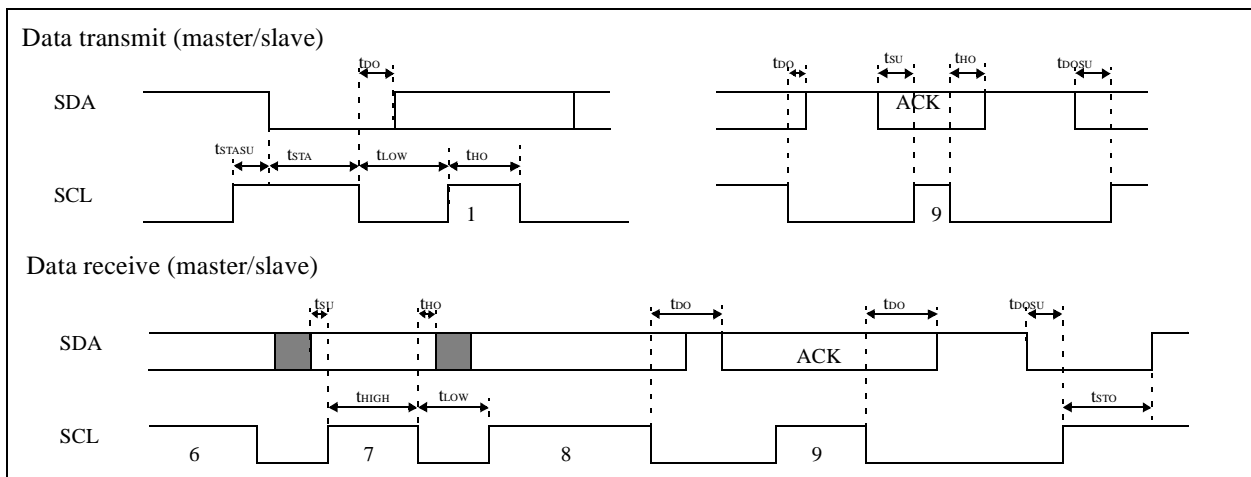
| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---------------------------------------|--------------------|------------|-----------|--|--|------|-------------|
| | | | | Min. | Max. | | |
| Start condition output | t _{STA} | SCL SDA | | $\frac{1}{4}t_{inst}^{*1} \times M \times N - 20$ | $\frac{1}{4}t_{inst} \times M \times N + 20$ | ns | master mode |
| Stop condition output | t _{STO} | SCL SDA | | $\frac{1}{4}t_{inst} \times (M \times N + 8) - 20$ | $\frac{1}{4}t_{inst} \times (M^{*2} \times N^{*3} + 8) + 20$ | ns | master mode |
| Start condition detect | t _{STA} | SCL SDA | | $\frac{1}{4}t_{inst} \times 6 + 40$ | — | ns | |
| Stop condition detect | t _{STO} | SCL SDA | | $\frac{1}{4}t_{inst} \times 6 + 40$ | — | ns | |
| Re-start condition output | t _{STASU} | SCL SDA | | $\frac{1}{4}t_{inst} \times (M \times N + 8) - 20$ | $\frac{1}{4}t_{inst} \times (M \times N + 8) + 20$ | ns | master mode |
| Re-start condition detect | t _{STASU} | SCL SDA | | $\frac{1}{4}t_{inst} \times 4 + 40$ | — | ns | |
| SCL output LOW width | t _{LOW} | SCL | | $\frac{1}{4}t_{inst} \times M \times N - 20$ | $\frac{1}{4}t_{inst} \times M \times N + 20$ | ns | master mode |
| SCL output HIGH width | t _{HIGH} | SCL | | $\frac{1}{4}t_{inst} \times (M \times N + 8) - 20$ | $\frac{1}{4}t_{inst} \times (M \times N + 8) + 20$ | ns | master mode |
| SDA output delay | t _{DO} | SDA | | $\frac{1}{4}t_{inst} \times 4 - 20$ | $\frac{1}{4}t_{inst} \times 4 + 20$ | ns | |
| SDA output setup time after interrupt | t _{DOSU} | SDA | | $\frac{1}{4}t_{inst} \times 4 - 20$ | — | ns | *4 |
| SCL input LOW pulse width | t _{LOW} | SCL | | $\frac{1}{4}t_{inst} \times 6 + 40$ | — | ns | |
| SCL input HIGH pulse width | t _{HIGH} | SCL | | $\frac{1}{4}t_{inst} \times 2 + 40$ | — | ns | |
| SDA input setup time | t _{SU} | SDA | | 40 | — | ns | |
| SDA hold time | t _{HO} | SDA | | 0 | — | ns | |

*1: For information in t_{inst}, see "(4) Instruction Cycle".

*2: M is defined in the ICCR CS4 and CS3 (bit 4 to bit 3). For details, please refer to the H/W manual register explanation.

*3: N is defined in the ICCR CS2 to CS0 (bit 2 to bit 0)

*4: When the interrupt period is greater than SCL "L" width, SDA and SCL output (Standard) value is based on hypothesis when rising time is 0 ns.



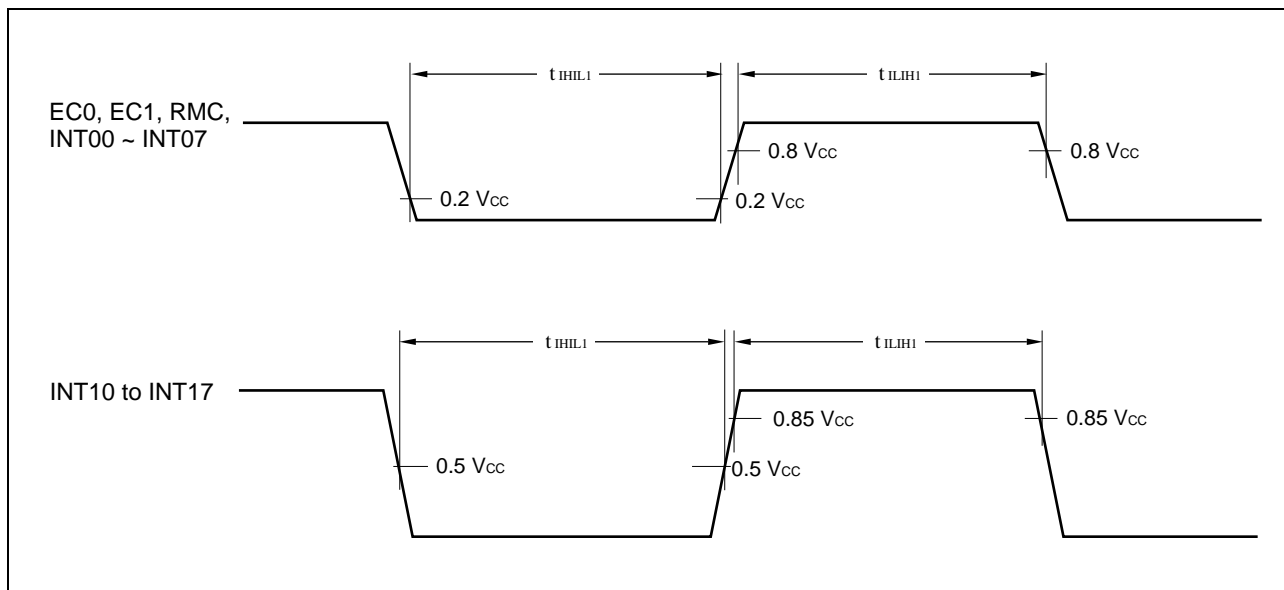
MB89490 Series

(7) Peripheral Input Timing

($V_{CC} = 3.0\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|------------------------------------|-------------|---|----------------|------|---------------|---------|
| | | | Min. | Max. | | |
| Peripheral input "H" pulse width 1 | t_{ILIH1} | EC0, EC1, RMC, INT00 ~ INT07, INT10 ~ INT17 | 2 t_{inst}^* | — | μs | |
| Peripheral input "L" pulse width 1 | t_{IHIL1} | | 2 t_{inst}^* | — | μs | |

* : For information on t_{inst} , see "(4) Instruction Cycle."



5. A/D Converter Electrical Characteristics

(1) A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 2.7\text{ V} \sim 3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

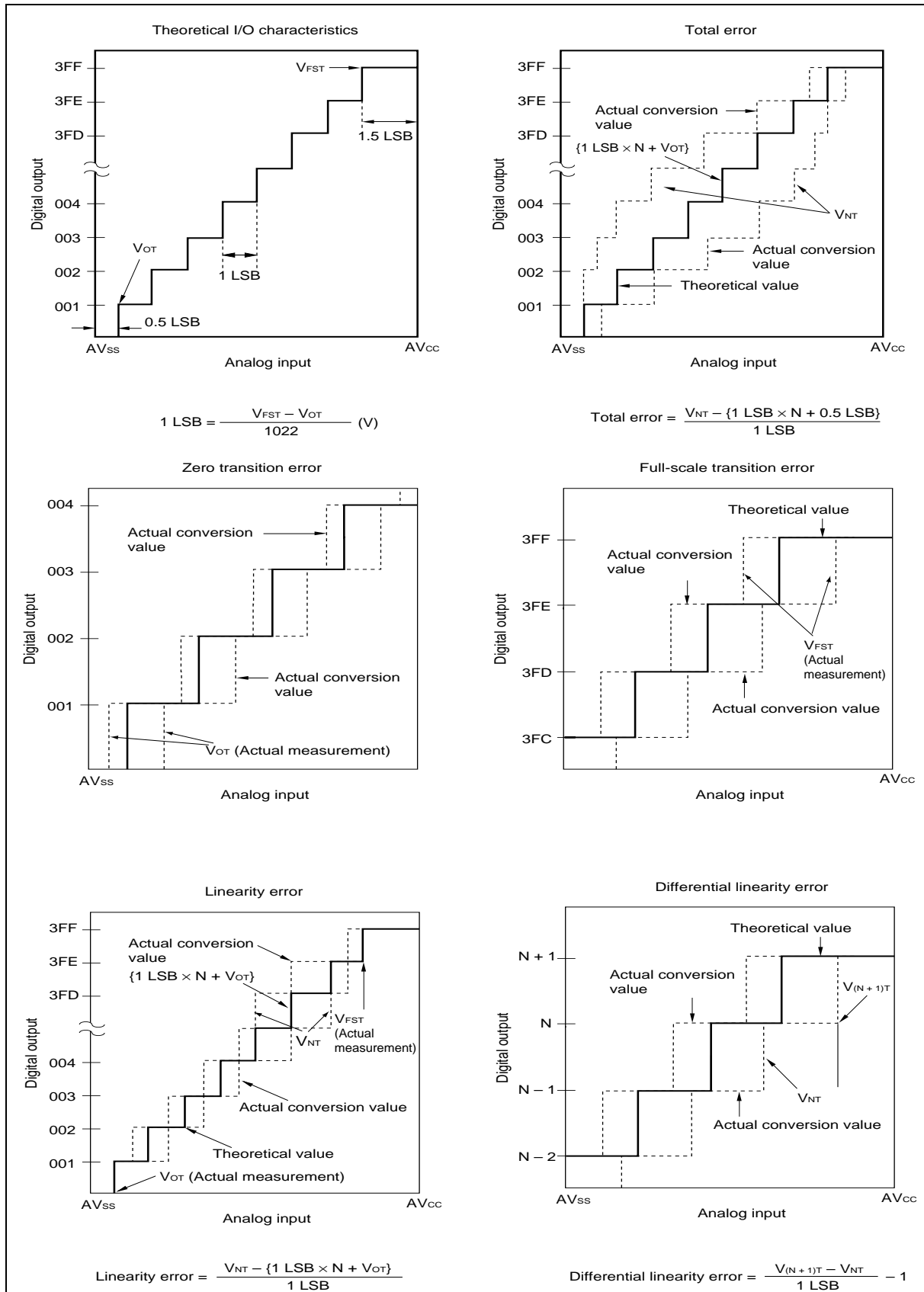
| Parameter | Symbol | Pin | Value | | | Unit | Remarks | | |
|----------------------------------|-----------|------------|-----------------|------|----------------------------|----------------------------|----------------------------|---------------|--|
| | | | Min. | Typ. | Max. | | | | |
| Resolution | — | — | — | 10 | — | bit | | | |
| Total error | | | — | — | ± 3.0 | LSB | | | |
| Linearity error | | | — | — | ± 2.5 | LSB | | | |
| Differential linearity error | | | — | — | ± 1.9 | LSB | | | |
| Zero transition voltage | | | V_{OT} | — | $AV_{SS} - 1.5\text{ LSB}$ | $AV_{SS} + 0.5\text{ LSB}$ | $AV_{SS} + 2.5\text{ LSB}$ | mV | |
| Full-scale transition voltage | | | V_{FST} | | $AV_{CC} - 3.5\text{ LSB}$ | $AV_{CC} - 1.5\text{ LSB}$ | $AV_{CC} - 0.5\text{ LSB}$ | mV | |
| A/D mode conversion time | | | — | | — | — | $38\ t_{inst}^*$ | μs | |
| Analog port input current | I_{AIN} | AN0 to AN7 | — | — | 10 | μA | | | |
| Analog input voltage | V_{AIN} | | AV_{SS} | — | AVR | V | | | |
| Reference voltage | — | AVR | $AV_{SS} + 2.7$ | — | AV_{CC} | V | | | |
| Reference voltage supply current | I_R | | — | 200 | TBD | μA | A/D is activated | | |
| | I_{RH} | | — | — | 5 | μA | A/D is stopped | | |

* : For information on t_{inst} , see "(4) Instruction Cycle" in "4. AC Characteristics".

(2) A/D Converter Glossary

- Resolution
Analog changes that are identifiable with the A/D converter.
When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit: LSB)
The deviation of the straight line connecting the zero transition point ("00 0000 0000" \leftrightarrow "00 0000 0001") with the full-scale transition point ("11 1111 1111" \leftrightarrow "11 1111 1110") from actual conversion characteristics.
- Differential linearity error (unit: LSB)
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error (unit: LSB)
The difference between theoretical and actual conversion values.

MB89490 Series



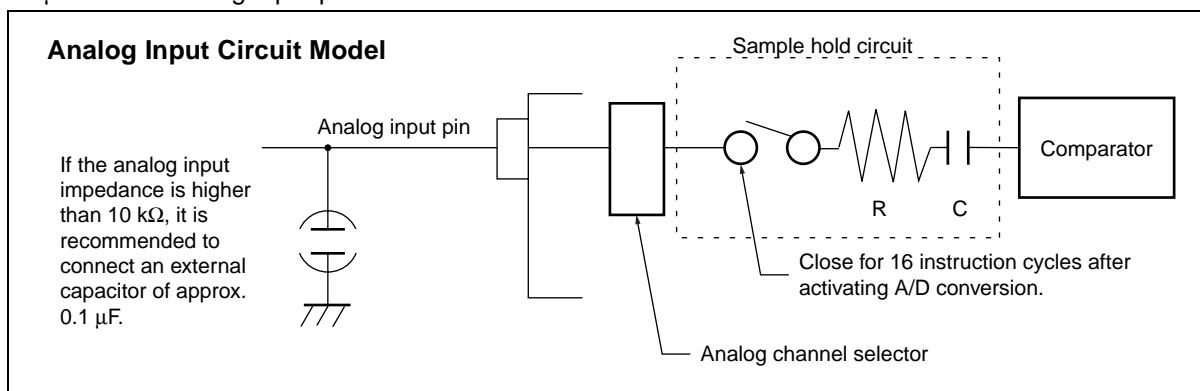
(3) Notes on Using A/D Converter

- Input impedance of the analog input pins

The A/D converter used for the MB89490 series contains a sample and hold circuit as illustrated below to fetch analog input voltage into the sample and hold capacitor for 16 instruction cycles after activation A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low.

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.



| | MB89F499 | MB89PV490/MB89497/MB89498 |
|--|----------------|---------------------------|
| R: analog input equivalent resistance | 2.4 k Ω | 2.4 k Ω |
| C: analog input equivalent capacitance | 52 pF | 53 pF |

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■ MASK OPTIONS

| No. | Part number | MB89497 | MB89498 | MB89F499 | MB89PV490 |
|-----|---|--|---------|--|-----------|
| | Specifying procedure | Specify when ordering mask | | Setting not possible | |
| 1 | Selection of oscillation stabilization time (OSC) • The initial value of the oscillation stabilization time for the main clock can be set by selecting the values of the WTM1 and WTM0 bit on the right. | Selectable OSC 1 : $2^{10}/F_{CH}$ 2 : $2^{14}/F_{CH}$ 3 : $2^{18}/F_{CH}$ | | Fixed to oscillation stabilization time of $2^{18}/F_{CH}$ | |

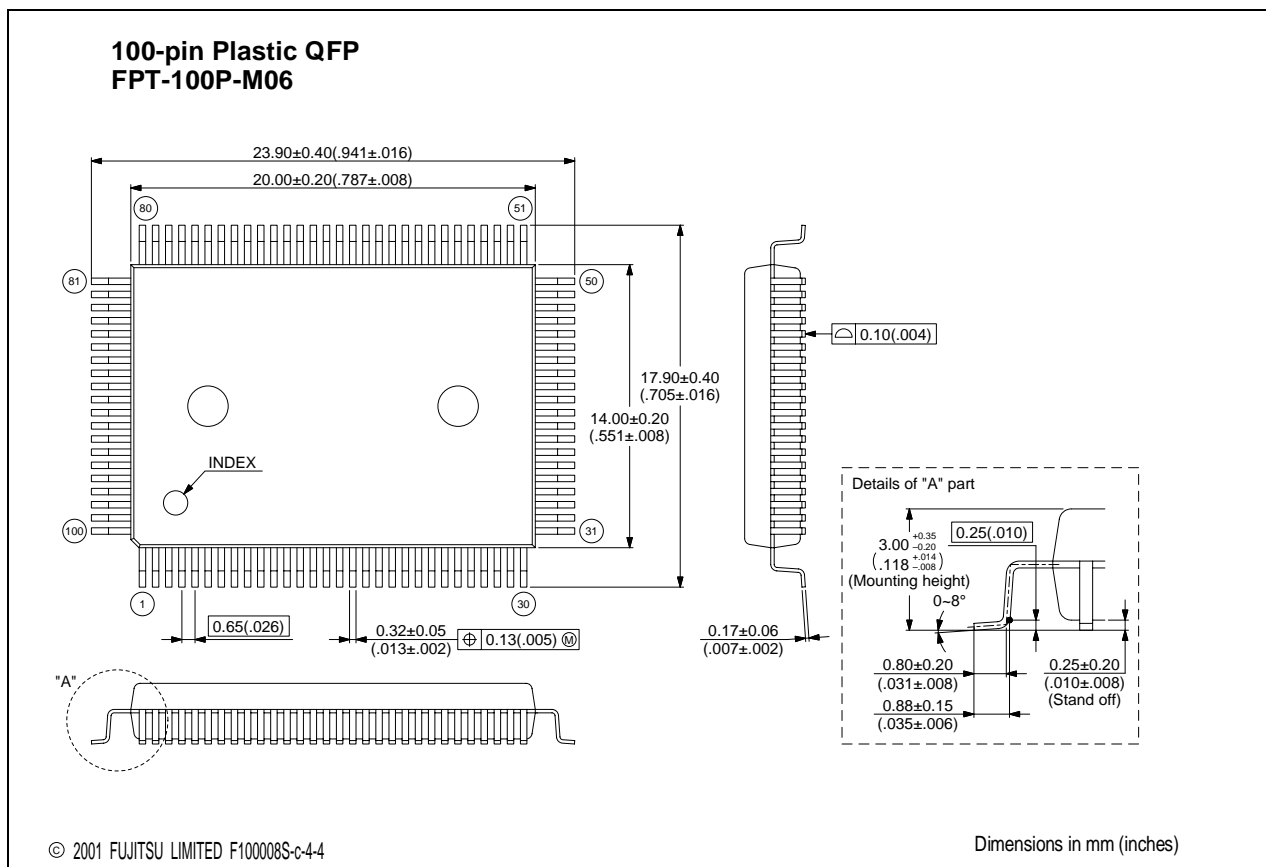
MB89490 Series

■ ORDERING INFORMATION

| Part number | Package | Remarks |
|--------------------------------------|--|---------|
| MB89497PF MB89498PF MB89F499PF | 100-pin Plastic QFP (FPT-100P-M06) | |
| MB89PV490CF | 100-pin Ceramic MQFP (MQP-100C-P01) | |

MB89490 Series

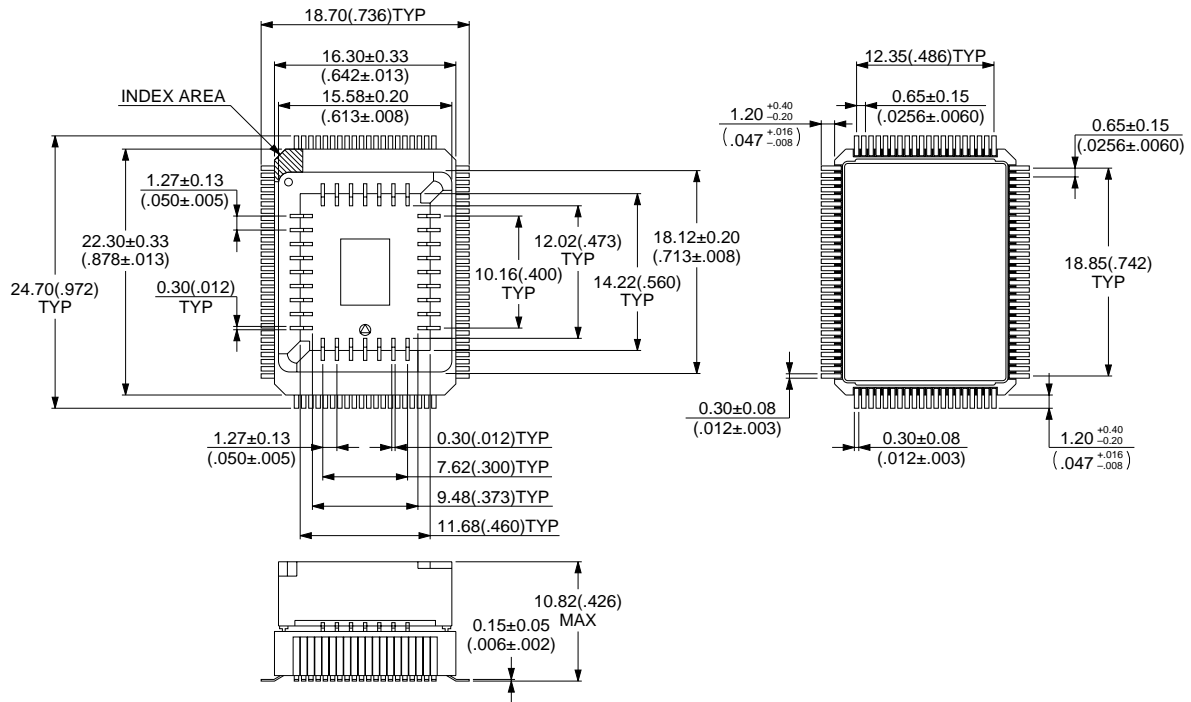
■ PACKAGE DIMENSIONS



(Continued)

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100-pin ceramic MQFP MQP-100C-P01



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