FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12550-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89550A Series

MB89557A/558A/P558A/PV550A

■ DESCRIPTION

The MB89550A series is a general-purpose, single-chip microcontroller that features a compact instruction set and contains a range of peripheral functions including a dual- clock control system, 5-level operating speed control, LCD controller driver, A/D converter, D/A converter, timer, serial interface, PWM timer, PWC timer, and external interrupts. The LCD controller driver is particularly suited for simultaneous control of LCD duty drive and static drive functions.

■ FEATURES

- **Range of package options**
  - LQFP package (0.5 mm pitch)
  - TQFP package (0.4 mm pitch)
- **High speed operation at low voltage**
  - Minimum instruction execution time 0.32 µs (for 12.5 MHz oscillation)
- **F²MCR-8L CPU core**

  Instruction set optimized for controller applications
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instructions
  - Bit manipulation instructions, etc.

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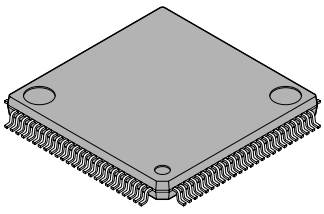
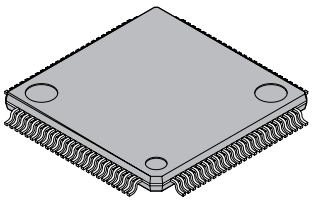
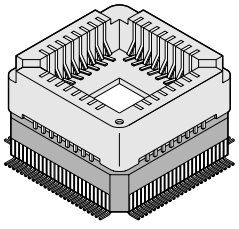
■ PACKAGE

100-pin Plastic LQFP	100-pin Plastic TQFP	100-pin Ceramic MQFP
		
(FPT-100P-M05)	(FPT-100P-M18)	(MQP-100C-P02)

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- **Dual-clock control system**
  - Main clock 12.5 MHz maximum : (Four speed settings available, oscillation halts in sub-clock mode)
  - Sub-clock 32.768 kHz : (Operation clock for sub-clock mode)
- **11 timer systems**
  - 8/16-bit timer counter 1 (square wave output, 2-channel output switching available)
  - 8/16-bit timer counter 2 (square wave output, 2-channel output switching available)
  - 16-bit timer counter (also functions as event counter)
  - 8-bit PWM timer (8-bit PWM timer × 2 channels or PPG timer × 1 channel, includes event counter function)
  - 8-bit PWC timer (8-bit PWC timer × 1 channel)
  - 6-bit PPG timer (6-bit PPG timer × 1 channel)
  - 21-bit timebase timer
  - Clock prescaler (17-bit)
- **UART/serial interface**
  - UART/SIO switching
- **UART**
  - Clock synchronous/asynchronous switching available
- **10-bit A/D converter**
  - 10-bit A/D × 8 channels
- **8-bit D/A converter**
  - 8-bit D/A × 2 channels
- **External interrupts**
  - Eight independent inputs can be used for recovery from low-power consumption modes (selection of rising, falling, or both edge detection functions).
  - Eight independent inputs can be used for recovery from low-power consumption modes (L level detection function included).
- **Clock output functions**
  - High speed clock signal multiplied by 2 available as output from HCLK pin.
  - Low speed clock pulse output available from LCLK pin.
- **LCD controller driver**
  - 32SEG × 4COM (maximum 128 pixels)
    8 dedicated to segment output only
    8 for port or segment use
    16 for port, segment, or static use
  - Built-in step-up power supply for driving LCD (optionally available)
- **Low-power consumption modes (standby modes)**
  - Stop mode (all oscillations halt in sub-clock mode, current consumption falls to almost zero)
  - Sleep mode (the CPU stops to reduce current consumption to approximately 1/3 of normal)
  - Clock mode (all operations other than the clock prescaler halt, current consumption is very low)
  - Sub clock mode (systems operate on sub-clock signals)
- **Maximum 66 I/O ports**
  - General-purpose I/O ports (N-ch open drain) : 4
  - General-purpose I/O ports (N-ch open drain) : 24
  - [also function as LCD ports, with restrictions]
  - General purpose I/O ports (CMOS) : 38

■ PRODUCT LINEUP

Parameter \ Part no.	MB89P558A-201 MB89P558A-202 MB89P558A-203	MB89557A	MB89558A	MB89PV550A*-201 MB89PV550A*-202 MB89PV550A*-203
ROM size	48 KB	32 KB	48 KB	—
RAM size	2 KB	1 KB	2 KB	1 KB
Packages	LQFP100 TQFP100	LQFP100 TQFP100	LQFP100 TQFP100	LQFP100
Classification	One-time product	Mask ROM product	Mask ROM product	Evaluation product
CPU functions	Number of instructions : 136 Instruction bit length : 8-bit Instruction length : 1 to 3bytes Data bit length : 1-, 8-, 16-bits Minimum execution time : 0.32 µs (at 12.5 MHz) Interrupt processing time : 2.88 µs (at 12.5 MHz)			
Peripheral Functions: Ports	Output-only ports (N-ch open drain) General-purpose I/O ports (N-ch open drain) General-purpose I/O ports (CMOS)			
Peripheral Functions: 8/16-bit timer counter 1	2-channel 8-bit timer/counter operation (also functions as 1-channel 16-bit timer) with square wave output function			
Peripheral Functions: 8/16-bit timer counter 2	2-channel 8-bit timer/counter operation (also functions as 1-channel 16-bit timer) with square wave output function			
Peripheral Functions: 16-bit timer counter	16-bit timer/counter operation, 16-bit event counter operation			
Peripheral Functions: PPWM timer	2-channel 8-bit PWM timer operation (also functions as 1-channel PPG timer) with event counter function			
Peripheral Functions: PWC timer	1-channel 8-bit PWC timer operation			
Peripheral Functions: 6-bit PPG timer	1-channel 6-bit PWM timer operation			
Peripheral Functions: LCD controller driver	Maximum 32SEGÅ~4COM (some ports provide selection of DUTY drive/STATIC drive/N-ch open drain I/O port functions)			
Peripheral Functions: UART / SIO	Switchable between UART (with clock synchronous/asynchronous data transfer function) and SIO (simple serial)			
Peripheral Functions: UART/SIO	Data transfer function for UART/SIO			
Peripheral Functions: A/D converter	8-channel 10-bit resolution			
Peripheral Functions: D/A converter	2-channel, 8-bit resolution			
Peripheral Functions: Clock output	High speed clock multiplied×2, and sub clock output available			
Standby modes	Sub clock mode, sleep mode, clock mode, and stop mode			

* : The MB89PV550A provides only evaluation functions (functions for use with emulation tools). This model cannot use piggyback functions (functions for use with E^2PROM).

■ OPTIONS AND CORRESPONDING PRODUCTS

		-201 Options	-202 Options	-203 Options
LCD step-up circuit		No step-up circuit	Step-up circuit included	
PORT/SEG dual-use pin selection		SEG8 to SEG31 : SEG/PORT dual use	SEG8 to SEG31 : SEG/PORT dual use	SEG8 to SEG21 : SEG/PORT dual use SEG22 to SEG31 : N-ch open drain*1
Model type	Evaluation model	MB89PV550A-201	MB89PV550A-202	MB89PV550A-203
	One-time model	MB89P558A-201	MB89P558A-202	MB89P558A-203
	Mask ROM model*2	MB89557A	MB89557A	MB89557A
		MB89558A	MB89558A	MB89558A

*1 : The SEG22-SEG31 pins (N-ch open drain) are not subject to the restriction that input voltage (V_{IN}) must be less than the voltage at the V3 pin.

*2 : Options may be specified at the time of mask ROM ordering.

■ OSCILLATOR STABILIZATION WAIT TIME SELECTION

The MB89557A/558A allow a selection of default value for oscillator stabilization wait time, to be selected at the time of mask ROM ordering.

Oscillator stabilization wait time selection	Remarks
$2^{14}/F_{CH}$	1.31 ms (at F = 12.5 MHz)
$2^{17}/F_{CH}$	10.48 ms (at F = 12.5 MHz)
$2^{18}/F_{CH}$	20.97 ms (at F = 12.5 MHz)

■ DIFFERENCES AMONG PRODUCTS AND PRECAUTIONS FOR MODEL SELECTION

• Package and Model Combinations

Models / Package	MB89PV550A	MB89P558A	MB89557A MB89558A
FPT-100P-M05 (LQFP-100 0.5 mm pitch)	×	○	○
FPT-100P-M18 (TQFP-100 0.4 mm pitch)	×	○	○
MQP-100C-P02 (MQFP-100 0.5 mm pitch)	○	×	×

Note : Compatible with all options (-201/202/203) .

• Memory Space
  • When evaluating chips using piggyback evaluators etc., please take note of the differences among products before making the evaluation.
• Current Consumption
  • When operating at low speed, one-time PROM and EPROM products will consume more current than mask ROM products. However, the current consumption in sleep/stop modes is the same.
  • For specific details about each package, see "■ PACKAGE DIMENSIONS".
  • For details about power consumption, see "■ ELECTRICAL CHARACTERISTICS" .
• Mask Options
  • The available options, and methods of using options, differ according to the model. Be sure to confirm the options from the "■ MASK OPTIONS" section.
• LCD Drive Step-up Power Circuit
  The MB89550A series is available with or without the step-up circuit option as a mask option.
• Power Supply Path
  The models in the MB89550A series have two power supply pins, V_{CC1} and V_{CC2}, with power supply paths that differ according to the model.

Models	Supply pin	Power supply path
MB89557A/ 558A	V_{CC1}	3V power supply pin for internal resource operation, including the CPU.
	V_{CC2}	5V power supply pin for input/output ports.
MB89P558A	V_{CC1}	V_{PP} pin for on-board writing.
	V_{CC2}	V power supply pin for internal resource operation, including the CPU, and for input/output pins.
MB89PV550A	V_{CC1}	Internally shut off, operates as input to V_{CC2} only.
	V_{CC2}	5V power supply pin for internal resource operation, including the CPU, and for input/output pins.

• Oscillator Startup and Power-on Reset
  On the MB89PV550A and MB89P558A, oscillator startup and power-on reset are applied at the rise of the V_{CC2} input. On the MB89558A and MB89557A, oscillator startup and power-on reset are applied at the rise of the V_{CC1} input.

- Wide Register Functions

  The space available for use of wide register functions is as follows.

MB89PV550A	2000_H to $FFFF_H$
MB89P558A	4000_H to $FFFF_H$
MB89558A	4000_H to $FFFF_H$
MB89557A	8000_H to $FFFF_H$

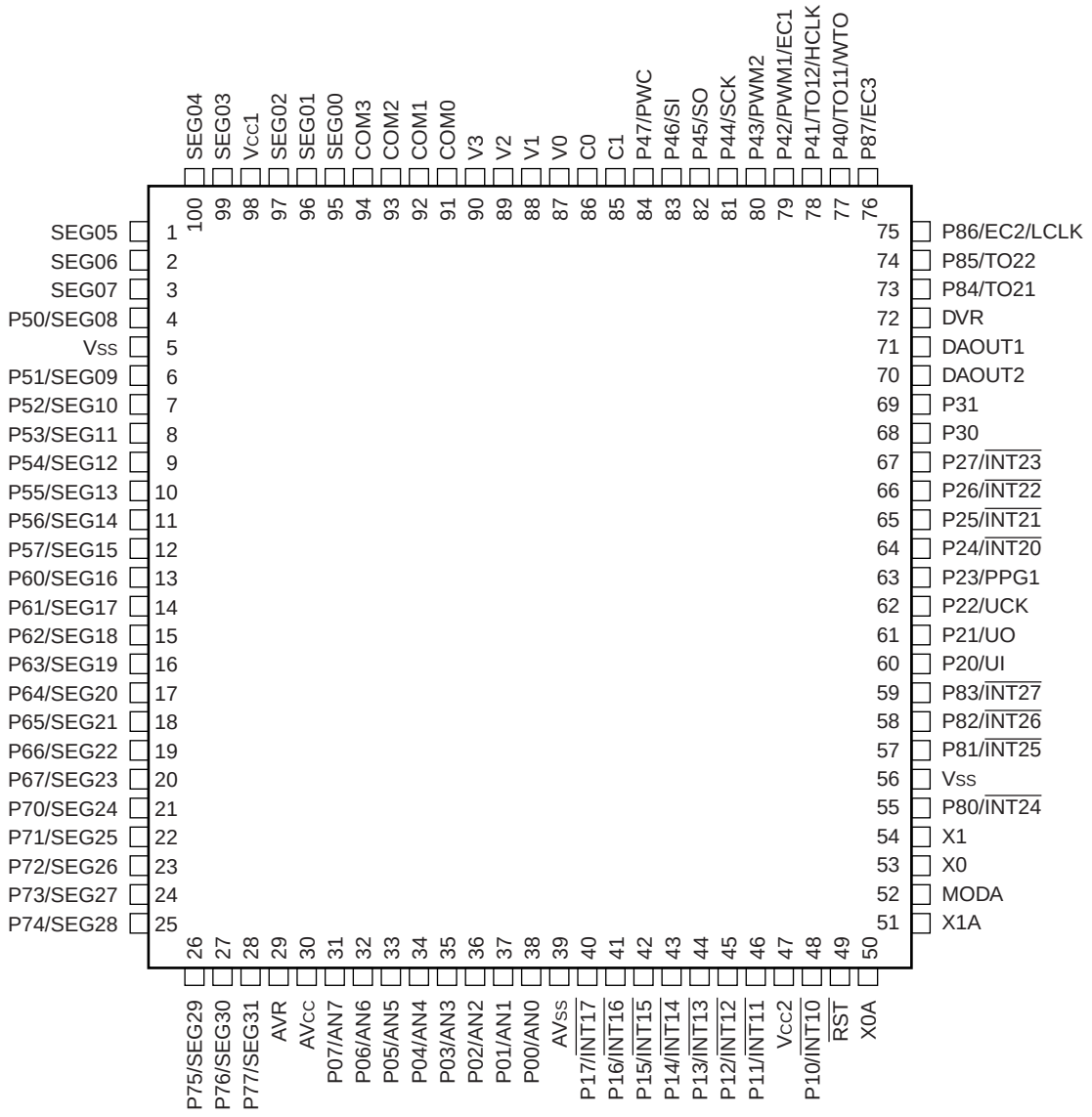
- The P40, P41, P84, P85 Pins

  On the MB889PV550A, an external oscillator signal equivalent to 64 clock pulses is required to initialize the P40, P41, P84, and P85 pins. Note therefore that at power-on there is an interval in which the values of these ports is undefined.

  On the MB89P558A, MB89558A, and MB89557A, these ports are set to "Hi-Z" status at power-on.

■ PIN ASSIGNMENTS

(TOP VIEW)



(QFP-100)

■ PIN DESCRIPTION

Pin No.	Pin Name	Circuit Type	Function
1	SEG05	H	Segment output pins for LCDC duty drive.
2	SEG06	H	
3	SEG07	H	
4	P50/ SEG08	G	N-ch open drain I/O pin. Also functions as a segment output pin for LCDC duty drive.
5	V_{SS}	—	Power supply (GND) pin.
6	P51/ SEG09	G	N-ch open drain I/O pins. Also function as segment output pins for LCDC duty drive.
7	P52/ SEG10		
8	P53/ SEG11		
9	P54/ SEG12		
10	P55/ SEG13		
11	P56/ SEG14		
12	P57/ SEG15		
13	P60/ SEG16	G	N-ch open drain I/O pins. Also function as segment output pins for LCDC duty drive or static drive.
14	P61/ SEG17		
15	P62/ SEG18		
16	P63/ SEG19		
17	P64/ SEG20		
18	P65/ SEG21		
19	P66/ SEG22		
20	P67/ SEG23		
21	P70/ SEG24		
22	P71/ SEG25		

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Pin No.	Pin Name	Circuit Type	Function
23	P72/ SEG26	G	N-ch open drain I/O pins. Also function as segment output pins for LCDC duty drive or static drive.
24	P73/ SEG27		
25	P74/ SEG28		
26	P75/ SEG29		
27	P76/ SEG30		
28	P77/ SEG31		
29	AVR	—	A/D converter reference voltage input pin.
30	AV_{CC}	—	A/D converter and D/A converter power supply pin.
31	P07/AN7	D	General purpose I/O ports. Also function as analog input pins.
32	P06/AN6		
33	P05/AN5		
34	P04/AN4		
35	P03/AN3		
36	P02/AN2		
37	P01/AN1		
38	P00/AN0		
39	AV_{SS}	—	A/D converter and D/A converter power supply pin (GND).
40	P17/$\overline{INT17}$	E	General purpose I/O ports. Also function as external interrupt 1 input pins. External interrupt 1 input signals are hysteresis signals (edge detection).
41	P16/$\overline{INT16}$		
42	P15/$\overline{INT15}$		
43	P14/$\overline{INT14}$		
44	P13/$\overline{INT13}$		
45	P12/$\overline{INT12}$		
46	P11/$\overline{INT11}$		
47	$V_{CC}2$	—	Power supply (5V) pin.
48	P10/$\overline{INT10}$	E	General purpose I/O port. Also functions as an external interrupt 1 input pin. External interrupt 1 input signals are hysteresis signals (edge detection).
49	RST	I	Reset input pin.
50	X0A	A	Crystal oscillator pins (32 KHz) .
51	X1A		

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Pin No.	Pin Name	Circuit Type	Function
52	MODA	F	Operating mode setting pin.
53	X0	A	Crystal oscillator pins (Max12.5 MHz) .
54	X1		
55	P80/$\overline{INT24}$	E	General purpose I/O port. Also functions as an external interrupt 2 input pin. External interrupt 2 input signals are hysteresis signals (level detection).
56	V_{SS}	—	Power supply (GND) pin.
57	P81/$\overline{INT25}$	E	General purpose I/O ports. Also function as external interrupt 2 input pins. External interrupt 2 input signals are hysteresis signals (level detection).
58	P82/$\overline{INT26}$		
59	P83/$\overline{INT27}$		
60	P20/UI	E	General purpose I/O ports. Also function as 8-bit serial I/O pins.
61	P21/UO	B	
62	P22/UCK	E	
63	P23/PPG1	B	General purpose I/O port. Also functions as the 6-bit PPG timer output.
64	P24/$\overline{INT20}$	E	General purpose I/O ports. Also function as external interrupt 2 input pins. External interrupt 2 input signals are hysteresis signals (level detection).
65	P25/$\overline{INT21}$		
66	P26/$\overline{INT22}$		
67	P27/$\overline{INT23}$		
68	P30	K	N-ch open drain I/O pins.
69	P31		
70	DAOUT2	C	D/A converter output pins.
71	DAOUT1		
72	DVR	—	D/A converter reference voltage input pin.
73	P84/TO21	B	General purpose I/O ports. Also function as 8/16-bit timer pins. • P84 can be used as the output for the main clock×2 pulse. • P86 can be used as the event counter input or sub-clock pulse output.
74	P85/TO22		
75	P86/EC2/ LCLK	E	
76	P87/EC3	E	General purpose I/O port. Also functions as a 16-bit timer pin.
77	P40/TO11/ WTO	B	General purpose I/O ports. Also function as 8/16-bit timer pins.
78	P41/TO12/ HCLK		
79	P42/ PWM1/ EC1	E	General purpose I/O ports. Also function as PWM timer pins.
80	P43/PWM2	B	

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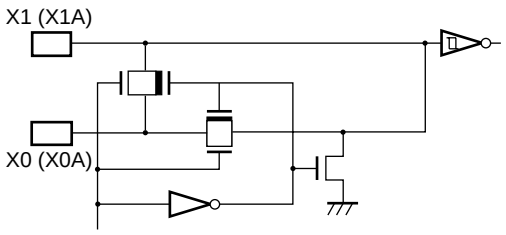
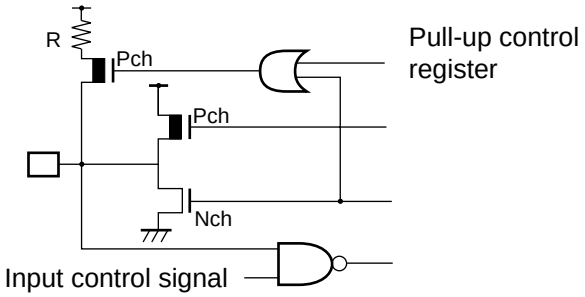
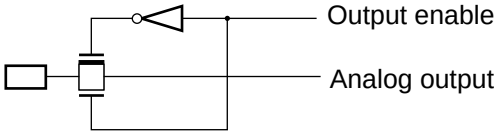
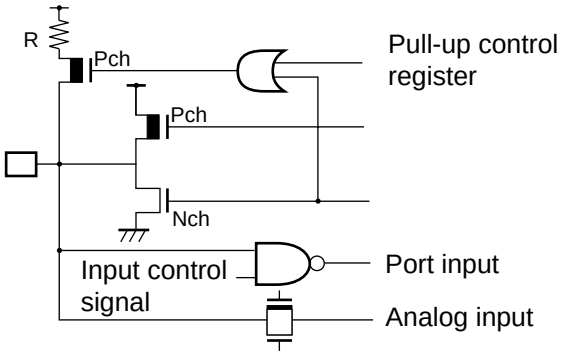
Pin No.	Pin Name	Circuit Type	Function
81	P44/SCK	E	General purpose I/O ports. Also function as UART pins.
82	P45/SO	B	
83	P46/SI	J	
84	P47/PWC	J	General purpose I/O port. Also functions as the PWC timer pin.
85	C1	—	Step-up voltage circuit capacitance connection pins.
86	C0		
87	V0	—	LCD drive power supply pins.
88	V1		
89	V2		
90	V3		
91	COM0	H	Dedicated LCDC common output pins.
92	COM1		
93	COM2		
94	COM3		
95	SEG00	H	Dedicated LCDC segment output pins.
96	SEG01		
97	SEG02		
98	$V_{CC}1$	—	Power supply (3V) pin.
99	SEG03	H	Dedicated LCDC segment output pins.
100	SEG04		

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A	 Main clock control signal (Sub-clock control signal)	Oscillation feedback resistance • High speed side = approx. 1 MΩ • Low speed side = approx. 4.5 MΩ
B		• CMOS I/O
C		• D/A output
D		• A/D input • CMOS I/O

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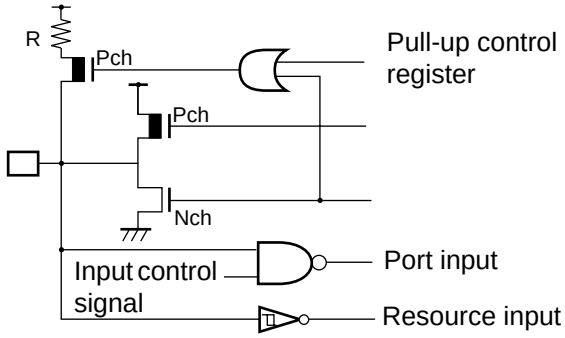
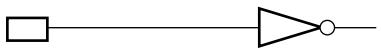
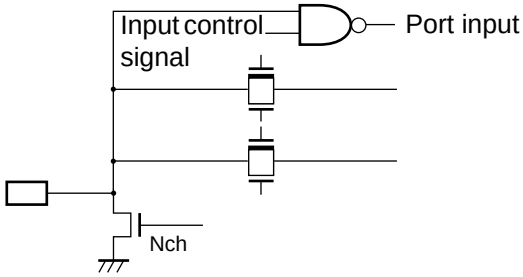
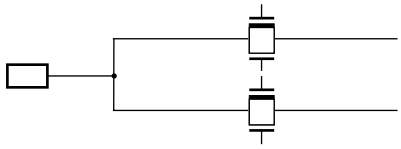
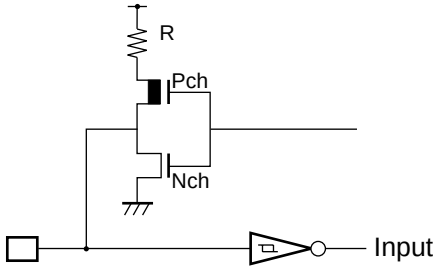
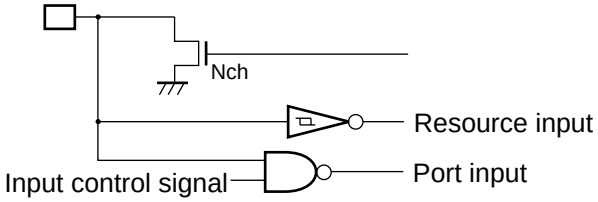
Type	Circuit	Remarks
E		• CMOS I/O • Hysteresis input (for external interrupt 0, 1, 2 input)
F		• CMOS input
G		• LCDC output • N-ch open drain I/O
H		• LCDC output
I		• Hysteresis input • Pull-up resistance
J		• Hysteresis input • N-ch open drain I/O

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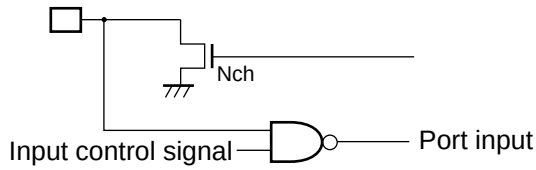
Type	Circuit	Remarks
K		• N-ch open drain I/O

■ HANDLING DEVICES

- Maximum rated voltage (Prevention of latchup)
  Be careful never to exceed maximum rated voltages.
  In CMOS IC devices, a condition known as latch-up may occur if voltages higher than Vcc or loser than Vss are applied to input or output pins other than medium- or high-voltage pins, or if the voltage applied between Vcc and Vss exceeds the rated voltage level.
  When latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore it is necessary to ensure that maximum ratings are not exceeded in circuit operation.
  Similarly, when turning the analog power supply on or off, it is necessary to ensure that the analog power supply voltages (AVcc, AVR, and DVR) and analog input voltages do not exceed the digital power supply (Vcc).

- Power supply voltages
  Power supply voltages should be kept as stable as possible.
  Rapid fluctuation of the voltage may cause the device to operate abnormally, even if the voltage remains within the allowed operating range.
  As a standard for power supply voltage stability, it is recommended that the peak-to-peak Vcc ripple voltage at commercial supply frequency (50 Hz to 60 Hz) be 10% or less of Vcc. Also when the power supply is turned on or off the transient voltage fluctuation be no more than 0.1V/ms or less.

- Treatment of unused input pins
  Leaving unused input pins unconnected can cause abnormal operation. Unused input pins should always be pulled up or down.

- Treatment of N.C. pins
  N.C. (not connected) pins should always be left open.

- Treatment of power supply pins on devices with A/D or D/A converters
  Even when the A/D or D/A converters are not in use, be sure to make the necessary connections to ensure that $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = DVR = V_{SS}$.

- Precautions on using an external clock
  An oscillation stabilization delay occurs after a power-on reset or when recovering from sub-clock or stop mode, even if an external clock is used.

- Treatment of unused dedicated LCD pins
  Dedicated SEG output pins should be left open when not in use.

- Handling of ports also used as segment pins
  When a ports is used as a segment pin, take care to ensure that the voltage applied to the pin does not exceed V3 (the segment drive voltage). This precaution is particularly necessary in models with step-up voltage circuits.
  Note also that after power-on or during a reset, an “L” level default signal is output form the segment/port pin.

- Treatment of unused LCD pins
  Connect the V3 pin to V_{CC2}. The other dedicated LCD pins V0, V1, V2, C0, and C1 should be pulled down.

- Executing programs on RAM
  When programs are executed on RAM, debugging cannot be performed even with the use of the MB89PV550A.

- Wild register functions
  Wild registers cannot be debugged with the MB89PV550A or tools. To verify operation, use the MB89P558A and perform in-place testing.

■ PROGRAMMING SPECIFICATIONS FOR ONE-TIME PROM PRODUCTS

The MB89P558A has a "PROM mode" with functions equivalent to the MBM27C1001, that enables the microcontroller to be programmed by writing from a general-purpose ROM programmer with the use of a special adapter. Note however that electronic signature mode is not available.

ROM Programmer Adapters

With some ROM programmers the insertion of approximately 0.1µF capacitance between V_{PP} and V_{SS} or between V_{CC} and V_{SS} allows more stable writing performance. The following table lists ROM programmer adapters.

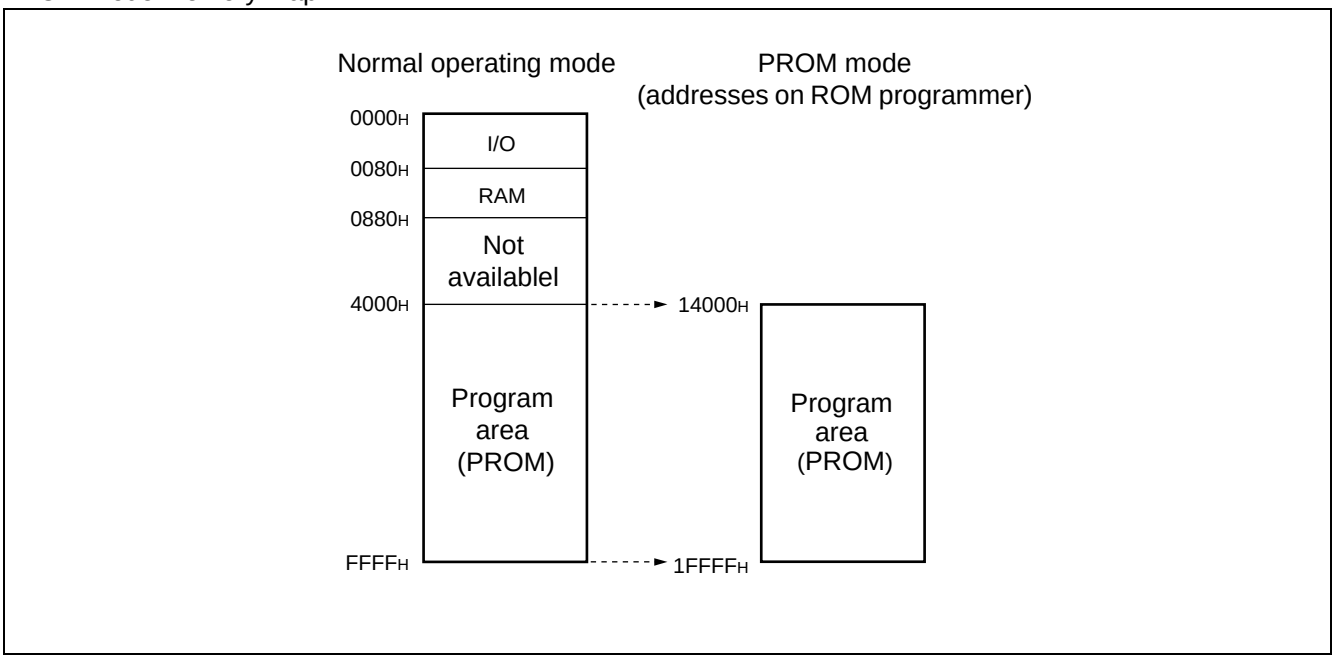
ROM Programmer Adapters

Part No.	Package	Adapter Part No.
MB89P558A	FPT-100P-M05	ROM-100SQF-32DP-8LA2
	FPT-100P-M18	ROM-100SQF-32DP-8LA

- Inquiries
  Sun Hayato Co., Ltd. : TEL 03-3986-0403

- PROM Mode Memory Map
  The PROM mode memory map is shown below.

PROM Mode Memory Map



- EPROM Programming Procedure

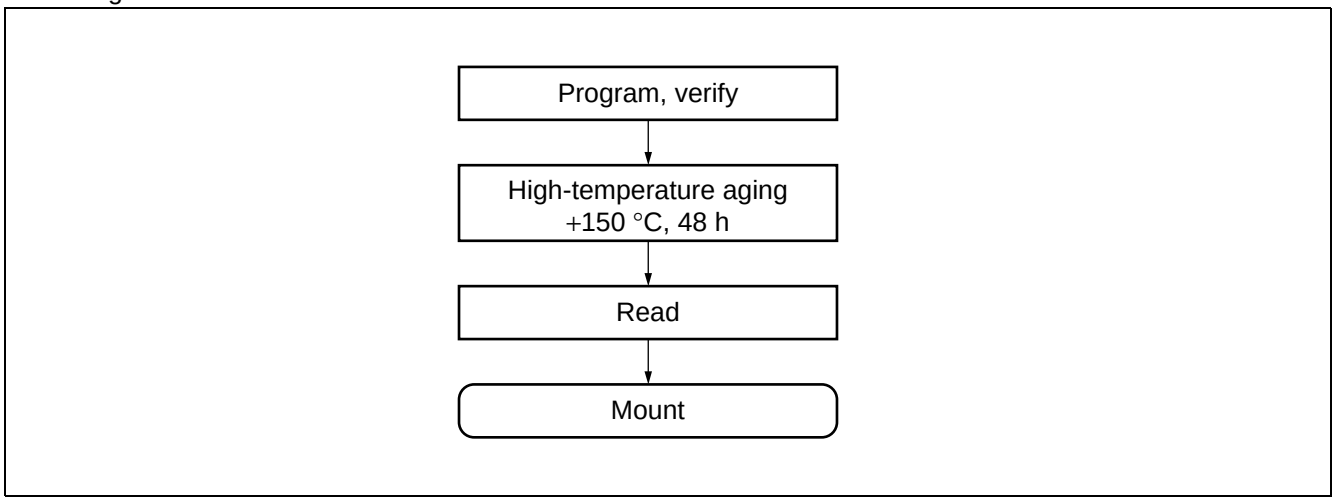
1) Set the EPROM programmer type to MBM27C1001.

2) Load the program data into addresses 14000_H to $1FFFF_H$ in the EPROM programmer.

3) Use the EPROM programmer to program to addresses 14000_H to $1FFFF_H$.

- Recommended Screening Conditions
  High-temperature aging is the recommended method of screening unprogrammed one-time PROM microcontrollers before mounting.
  The flow of the screening process is shown below.

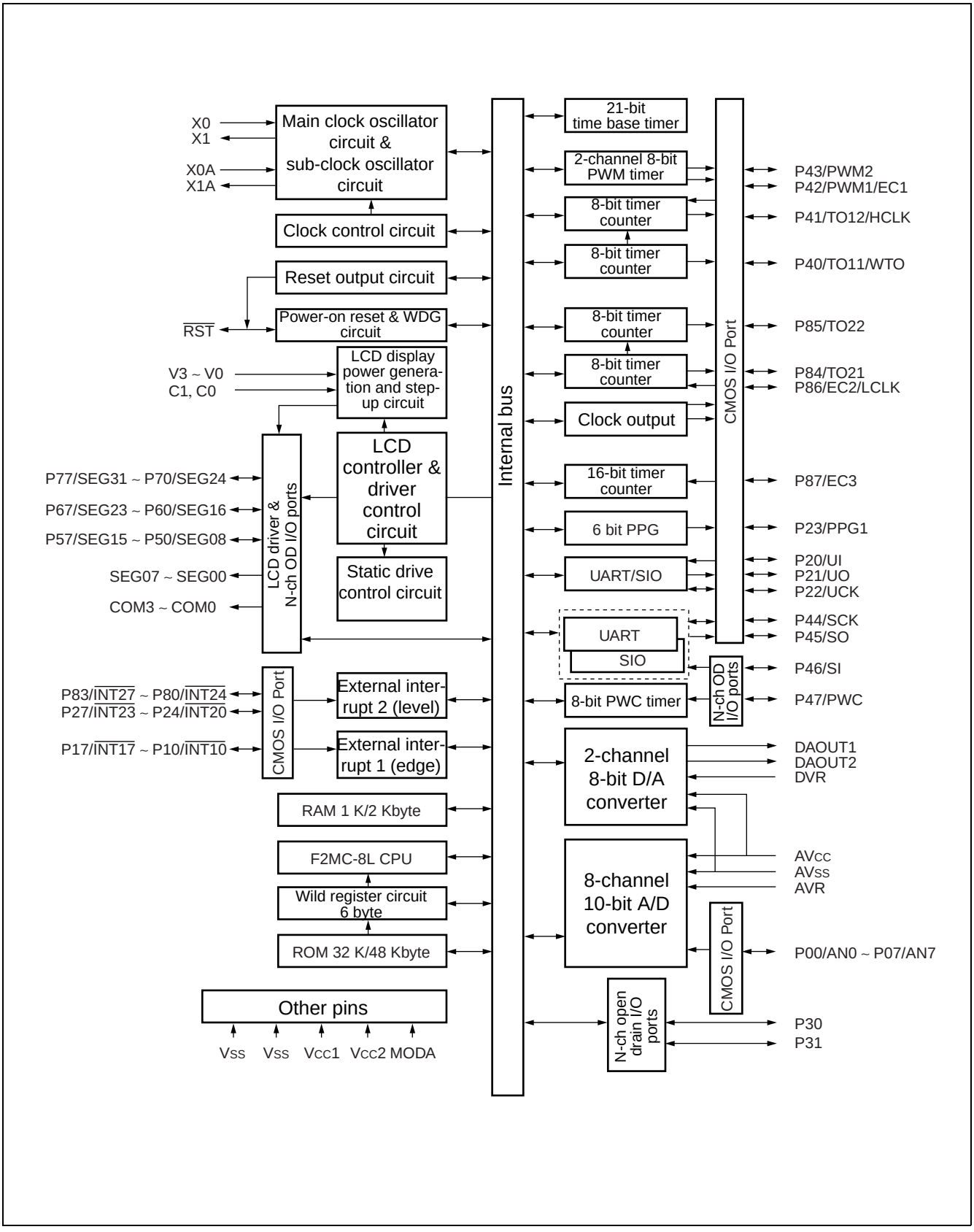
Screening Flow



- About Writing Yields

The nature of chips before one-time writing of microcontroller programs to PROM prevents the use of all-bit writing tests. Therefore it is not possible to guarantee writing yields of 100% in some cases.

■ BLOCK DIAGRAM



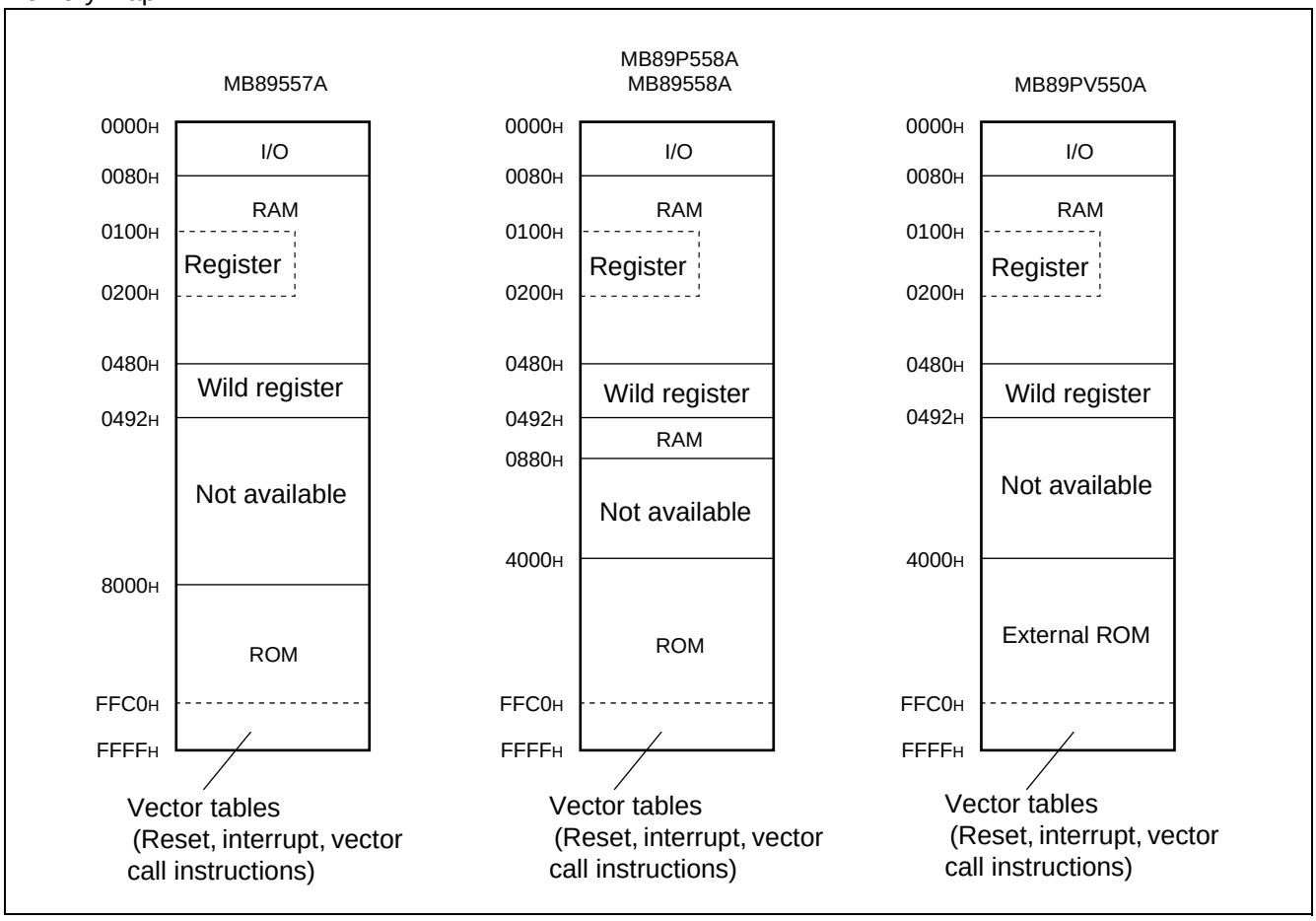
■ CPU CORE

Memory space

The MB89550A has 64 Kbytes of memory space, composed of the I/O area, RAM area, ROM area, and external area. The memory space includes general purpose registers, as well as areas used for special purposes such as vector tables.

- I/O Area (address : 0000_H to $007F_H$)
  - This area is allocated to control registers and data registers for internal peripheral functions.
  - Because the I/O area is part of memory space, it can be accessed in the same ways. Direct addressing provides faster access.
- RAM Area
  - Static RAM is provided for use as an internal data area.
  - The size of internal RAM differs between product models.
  - High speed access is available to addresses 80_H to FF_H using direct addressing (the area available for use is restricted on some models).
  - Addresses 100_H to $1FF_H$ are used as the general-purpose register area.
  - If a reset is applied during writing to RAM, the value of date at the target addresses is not assured.
- ROM Area
  - ROM is provided for use as the internal program area.
  - The size of internal ROM differs between product models.
  - Addresses $FFC0_H$ to $FFFF_H$ are used for special purpose data such as vector tables.

Memory Map



■ I/O MAP

Address	Abbreviation	Resister Name	Read/Write	Initial Value
00_H	PDR0	Port 0 data register	R/W	XXXXXXXX$_B$
01_H	DDR0	Port 0 direction register	W	00000000$_B$
02_H	PDR1	Port 1 data register	R/W	XXXXXXXX$_B$
03_H	DDR1	Port 1 direction register	W	00000000$_B$
04_H to 06_H	Unused area			
07_H	SYCC	System clock control register	R/W	XXXMM100$_B$
08_H	STBC	Standby control register	R/W	00010XXX$_B$
09_H	WDTC	Watchdog control register	R/W	0XXXXXXX$_B$
$0A_H$	TBTC	Time base time control register	R/W	X0XXX000$_B$
$0B_H$	WPCR	Clock prescaler control register	R/W	X0XX0000$_B$
$0C_H$	PDR2	Port 2 data register	R/W	XXXXXXXX$_B$
$0D_H$	DDR2	Port 2 direction register	R/W	00000000$_B$
$0E_H$	PDR3	Port 3 data register	R/W	------11$_B$
$0F_H$	PDR4	Port 4 data register	R/W	11XXXXXX$_B$
10_H	DDR4	Port 4 direction register	R/W	--000000$_B$
11_H	PDR5	Port 5 data register	R/W	00000000$_B$
12_H	Unused area			
13_H	PDR6	Port 6 data register	R/W	00000000$_B$
14_H	Unused area			
15_H	PDR7	Port 7 data register	R/W	00000000$_B$
16_H	Unused area			
17_H	PDR8	Port 8 data register	R/W	XXXXXXXX$_B$
18_H	DDR8	Port 8 direction register	R/W	00000000$_B$
19_H	Unused area			
$1A_H$	T2CR#2	Timer 2 control register # 2(8/16-bit timer/counter -1)	R/W	X00000X0$_B$
$1B_H$	T1CR#1	Timer 1 control register # 1(8/16-bit timer/counter -1)	R/W	X00000X0$_B$
$1C_H$	T2DR#2	Timer 2 data register # 2(8/16-bit timer/counter -1)	R/W	XXXXXXXX$_B$
$1D_H$	T1DR#1	Timer 1 data register # 1(8/16-bit timer/counter -1)	R/W	XXXXXXXX$_B$
$1E_H$	T2CR#4	Timer 2 control register # 4(8/16-bit timer/counter -2)	R/W	X00000X0$_B$
$1F_H$	T1CR#3	Timer 1 control register # 3(8/16-bit timer/counter -2)	R/W	X00000X0$_B$
20_H	T2DR#4	Timer 2 data register # 4(8/16-bit timer/counter -2)	R/W	XXXXXXXX$_B$
21_H	T1DR#3	Timer 1 data register # 3(8/16-bit timer/counter -2)	R/W	XXXXXXXX$_B$
22_H	SMC1	Serial mode control register 1 (UART)	R/W	00000000$_B$
23_H	SRC1	Serial rate control register (UART)	R/W	--011000$_B$

(Continued)

Address	Abbreviation	Resister Name	Read/Write	Initial Value
24H	SSD1	Serial status and data register (UART)	R/W	00100-1XB
25H	SIDR1/ SODR1	Serial input/serial output data register (UART)	R/W	XXXXXXXXB
26H	SMC2	Serial mode control register 2 (UART)	R/W	--100001B
27H	CNTR1	PWM control register 1	R/W	00000000B
28H	CNTR2	PWM control register 2	R/W	000X0000B
29H	CNTR3	PWM control register 3	R/W	X000 XXXXB
2AH	COMR1	PWM compare register 1	W	XXXXXXXXB
2BH	COMR2	PWM compare register 2	W	XXXXXXXXB
2CH	PCR1	PWC pulse width control register 1	R/W	000 XX 000B
2DH	PCR2	PWC pulse width control register 2	R/W	00000000B
2EH	PLBR	PWC reload buffer register	R/W	XXXXXXXXB
2FH	SMC21	Serial mode control register 1 (UART/SIO)	R/W	00000000B
30H	SMC22	Serial rate control register 2 (UART/SIO)	R/W	00000000B
31H	SSD2	Serial status and data register (UART/SIO)	R/W	00001XXXB
32H	SIDR2/ SODR2	Serial input/serial output date register (UART/SIO)	R/W	XXXXXXXXB
33H	SRC2	Baud rate generator reload register (UART/SIO)	R/W	XXXXXXXXB
34H	ADC1	A/D control register 1	R/W	00000000B
35H	ADC2	A/D control register 2	R/W	X0000001B
36H	ADDL	A/D data register low	R/W	XXXXXXXXB
37H	ADDH	A/D data register high	R/W	000000 XXB
38H to 3BH	Unused area			
3CH	TMCR	Timer control register (16-bit timer/counter)	R/W	XX000000B
3DH	TCHR	Timer count register high (16-bit timer/counter)	R/W	00000000B
3EH	TCLR	Timer count register low (16-bit timer/counter)	R/W	00000000B
3FH	EIC1	External interrupt register 1	R/W	00000000B
40H	EIC2	External interrupt register 2	R/W	00000000B
41H	EIC3	External interrupt register 3	R/W	00000000B
42H	EIC4	External interrupt register 4	R/W	00000000B
43H	DACR	D/A control register	R/W	XXXXXX00B
44H	DADR1	D/A data register 1	R/W	XXXXXXXXB
45H	DADR2	D/A data register 2	R/W	XXXXXXXXB
46H to 55H	Unused area			
56H	EIE2	External interrupt 2 control register	R/W	00000000B

(Continued)

(Continued)

Address	Abbreviation	Resister Name	Read/Write	Initial Value
57H	EIF2	External interrupt 2 flag register	R/W	XXXXXXX0B
58H	RCR1	6-bit PPG control register 1	R/W	00000000B
59H	RCR2	6-bit PPG control register 2	R/W	0-000000B
5AH	CKR	Clock output control register	R/W	XXXXXX00B
5BH	LCR1	LCDC control register 1	R/W	00010000B
5CH	LCR2	LCDC control register 2	R/W	00000000B
5DH	LCR3	LCDC control register 3	R/W	---00000B
5EH	LCD1	LCD static display register 1	R/W	XXXXXXXXB
5FH	LCD2	LCD static display register 2	R/W	XXXXXXXXB
60H to 6FH	VRAM	LCD display RAM	R/W	XXXXXXXXB
70H	SMR	Serial mode register (8-bit serial I/O)	R/W	00000000B
71H	SDR	Serial data register (8-bit serial I/O)	R/W	XXXXXXXXB
72H	PORR0	Port 0 pull-up option setting register	R/W	11111111B
73H	PURR1	Port 1 pull-up option setting register	R/W	11111111B
74H	PURR2	Port 2 pull-up option setting register	R/W	11111111B
75H	PURR4	Port 4 pull-up option setting register	R/W	11111111B
76H	PURR8	Port 8 pull-up option setting register	R/W	11111111B
77H	WREN	Wild register/address comparator enable register	R/W	--000000B
78H	Unused area			
79H	ADEN	A/D port input enable register	R/W	11111111B
7AH	Unused area			
7BH	ILR1	Interrupt level setting register 1	W	11111111B
7CH	ILR2	Interrupt level setting register 2	W	11111111B
7DH	ILR3	Interrupt level setting register 3	W	11111111B
7EH	ILR4	Interrupt level setting register 4	W	11111111B
7FH	Unused area			

• **Extended I/O Area**

Address	Abbreviation	Resister Name	Read/Write	Initial Value
480H	WRARH1	H address setting register 1	R/W	XXXXXXXX
481H	WRARL1	L address setting register 1	R/W	XXXXXXXX
482H	WRDR1	Data setting register 1	W	XXXXXXXX
483H	WRARH2	H address setting register 2	R/W	XXXXXXXX
484H	WRARL2	L address setting register 2	R/W	XXXXXXXX
485H	WRDR2	Data setting register 2	W	XXXXXXXX
486H	WRARH3	H address setting register 3	R/W	XXXXXXXX
487H	WRARL3	L address setting register 3	R/W	XXXXXXXX
488H	WRDR3	Data setting register 3	W	XXXXXXXX
489H	WRARH4	H address setting register 4	R/W	XXXXXXXX
48AH	WRARL4	L address setting register 4	R/W	XXXXXXXX
48BH	WRDR4	Data setting register 4	W	XXXXXXXX
48CH	WRARH5	H address setting register 5	R/W	XXXXXXXX
48DH	WRARL5	L address setting register 5	R/W	XXXXXXXX
48EH	WRDR5	Data setting register 5	W	XXXXXXXX
48FH	WRARH6	H address setting register 6	R/W	XXXXXXXX
490H	WRARL6	L address setting register 6	R/W	XXXXXXXX
491H	WRDR6	Data setting register 6	W	XXXXXXXX

O Read/write notation
- R/W : Reading and writing enabled
- R : Read-only
- W : Write only

O Initial value notation
- 0 : Initial value of bit is “0”.
- 1 : Initial value of bit is “1”.
- X : Initial value of bit is undefined.

Note : Areas indicated as "unused area" are not to be used.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AVss = Vss = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC1}	V_{SS} – 0.3	V_{SS} + 4.0	V	V_{CC1} not to exceed V_{CC2}.*
	V_{CC2}	V_{SS} – 0.3	V_{SS} + 6.0	V	
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	
D/A converter reference input voltage	DVR	V_{SS} – 0.3	V_{SS} + 6.0	V	
LCD power supply voltage	V0-V3	V_{SS} – 0.3	V_{SS} + 6.0	V	On models without step-up circuits V0-V3 are not to exceed V_{CC2}.
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC}2 + 0.3	V	Pins other than P50 to P57, P60 to P67, P70 to P77, P46, P47, P30, P31
	V_{I2}	V_{SS} – 0.3	V3	V	P50 to P57, P60 to P67, P70 to P77
	V_{I3}	V_{SS} – 0.3	V_{SS} + 6.0	V	P46, P47, P30, P31
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC}2	V	Pins other than P50 to P57, P60 to P67, P70 to P77, P46, P47, P30, P31
	V_{O2}	V_{SS} – 0.3	V3	V	P50 to P57, P60 to P67, P70 to P77
	V_{O3}	V_{SS} – 0.3	V_{SS} + 6.0	V	P46, P47, P30, P31
“L” level maximum output current	I_{OL1}	—	15	mA	Pins other than P22/UCK, P23/PPG1
	I_{OL2}	—	30	mA	P22/UCK, P23/PPG1
“L” level average output current	I_{OLAV1}	—	4	mA	Pins other than P22/UCK, P23/PPG1 average value (operating current × operating ratio)
	I_{OLAV2}	—	15	mA	P22/UCK, P23/PPG1 average value (operating current × operating ratio)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	60	mA	average value (operating current × operating ratio)
“H” level maximum output current	I_{OH1}	—	–15	mA	Pins other than P22/UCK, P23/PPG1
	I_{OH2}	—	–30	mA	P22/UCK, P23/PPG1

(Continued)

(Continued)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level average output current	I_{OHAV}	—	–4	mA	Pins other than P22/UCK, P23/PPG1 and open drain output pins average value (operating current × operating ratio)
	I_{OHAV}	—	–15	mA	P22/UCK, P23/PPG1 average value (operating current × operating ratio)
"H" level total maximum output current	ΣI_{OH}	—	–50	mA	
"H" level total average output current	ΣI_{OHAV}	—	–30	mA	average value (operating current × operating ratio)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Set AV_{CC} to the same potential as V_{CC}.
Also ensure that AVR and DVR do not exceed AV_{CC} + 0.3 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AVss = Vss = 0 V)

Item	Symbol	Rating		Unit	Remark
		Min	Max		
Power supply voltage*3	V_{CC1}	2.2*1	3.6	V	Guaranteed normal operating range (MB89557A/558A)
	V_{CC2}	2.2*1	5.5	V	
	V_{CC1}	—	—	V	Guaranteed normal operating range (MB89P558A)
	V_{CC2}	2.7*2	5.5	V	
	V_{CC1}, V_{CC2}	1.5	3.6	V	To maintain RAM state in stop mode
A/D converter reference voltage input*4	AVR	V_{CC1}	AV_{CC}	V	Guaranteed normal operating range
D/A converter reference voltage input*4	DVR	V_{CC1}	AV_{CC}	V	Guaranteed normal operating range
LCD supply voltage	V0-V3	V_{SS}	V_{CC2}	V	Models without step-up circuit, pins V0 to V3. LCD power supply range and maximum value are determined by the characteristics of the LCD display element used.
Operating temperature	T_A	–40	+85	°C	

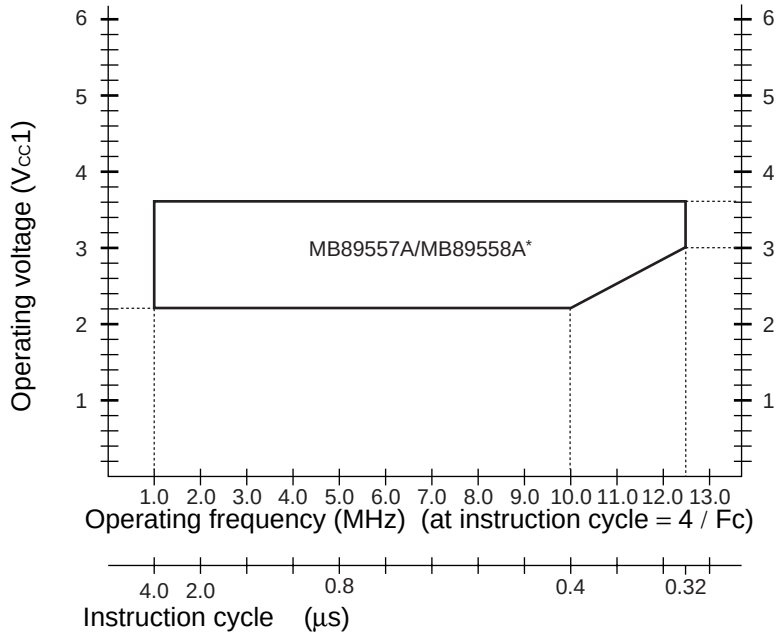
*1 : The operating power supply voltage differs depending on the instruction cycle time of the operating frequency. See Figure 1.

*2 : The operating power supply voltage differs depending on the instruction cycle time of the operating frequency. See Figure 2. Note also that on the MB89PV550A the input to the V_{CC1} pin is cut off internally, and on the MB89P558A the V_{CC1} pin is used as the V_{PP} pin for on-board writing.

*3 : AVcc and V_{CC2} should be set to the same potential. Also, care must be taken to ensure that V_{CC1} does not exceed V_{CC2}.

*4 : Care must be taken to ensure that the relation between AVR and DVR is such that "$V_{CC1} \leq$ AVR (DVR) $\leq AV_{CC} + 0.3$ V".

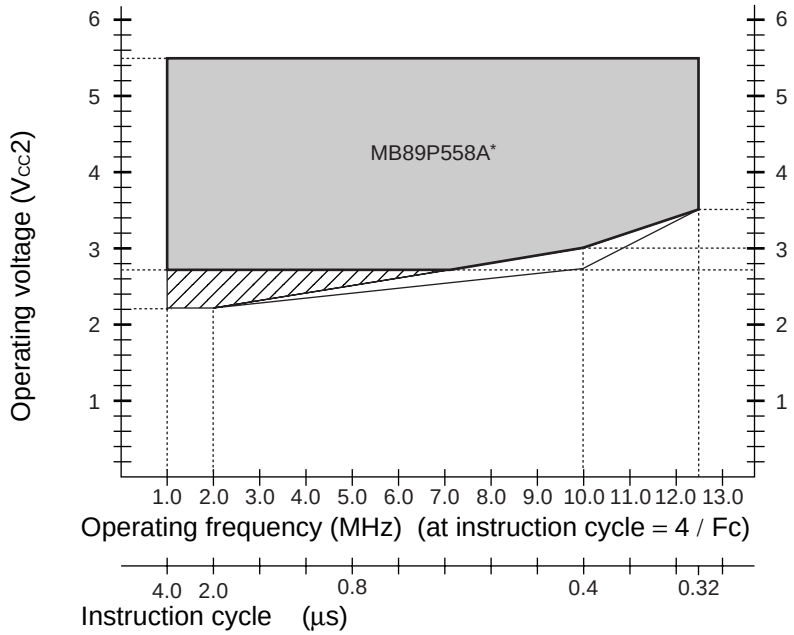
Figure 1. Operating Voltage vs. Operating Frequency (MB89558A/557A)



* : Analog precision warranted range : AV_{CC} = 3.5 V to 5.5 V

: T_A = –40 °C ~ +85 °C

Figure 2. Operating Voltage vs. Operating Frequency (MB89P558A)



: T_A = –40 °C ~ +85 °C

: T_A = –10 °C ~ +55 °C

: T_A = +25 °C

* : $V_{CC}2$ = 2.2 V to 5.5 V ($V_{CC}2 \geq V_{CC}1$)

Analog precision warranted range : AV_{CC} = 3.5 V to 5.5 V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(AV_{CC} = AVR = DVR = V_{CC2} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P00 to P07, P10 to P17, P20 to P27, P40 to P45, P80 to P87	—	0.7 V_{CC2}	—	V_{CC2} + 0.3	V	
	V_{IH2}	P50 to P57, P60 to P67, P70 to P77	—	0.7 V_{CC2}	—	V3	V	V_{IH2} not to exceed V3.
	V_{IH3}	P46, P47, P30, P31	—	0.7 V_{CC2}	—	V_{SS} + 5.5	V	
	V_{IHS1}	$\overline{INT10}$ to $\overline{INT17}$, UI, UCK, $\overline{INT20}$ to $\overline{INT27}$, SCK, EC1, EC2, EC3, $\overline{RST}$, MODA	—	0.8 V_{CC2}	—	V_{CC2} + 0.3	V	Hysteresis input
	V_{IHS2}	SI, PWC	—	0.8 V_{CC2}	—	V_{SS} + 5.5	V	Hysteresis input
"L" level input voltage	V_{IL1}	P00 to P07, P10 to P17, P20 to P27, P30, P31, P40 to P47, P80 to P87	—	V_{SS} – 0.3	—	0.3 V_{CC2}	V	
	V_{IL2}	P50 to P57, P60 to P67, P70 to P77	—	V_{SS} – 0.3	—	0.3 V_{CC2}	V	V_{IL2} not to exceed V3.
	V_{ILS}	$\overline{INT10}$ to $\overline{INT17}$, UI, UCK, $\overline{INT20}$ to $\overline{INT27}$, SCK, EC1, EC2, EC3, $\overline{RST}$, MODA, SI, PWC	—	V_{SS} – 0.3	—	0.2 V_{CC2}	V	Hysteresis input
Voltage applied to open drain output pins	V_{D1}	P46, P47, P30, P31	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
	V_{D2}	P50 to P57, P60 to P67, P70 to P77	—	V_{SS} – 0.3	—	V3	V	V_{D2} not to exceed V3.
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17, P20, P21, P24 to P27, P40 to P45, P80 to P87	I_{OH} = –2.0 mA	4.0	—	—	V	
	V_{OH2}	P22, P23	I_{OH} = –4.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20, P21, P24 to P27, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P22, P23	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30, P31 P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, MODA	0.0V < V_I < V_{CC2}	—	—	±5	µA	Without pull-up resistor option

(Continued)

(AV_{CC} = AVR = DVR = V_{CC2} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P45, P80 to P87, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor option
Power supply current	I_{CC1}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 5.0 V F_{CH} = 12.5 MHz	—	4.5	6	mA	t_{inst} = 0.32 µs MB89557A/558A
		V_{CC2}	V_{CC2} = 5.0 V F_{CH} = 12.5 MHz	—	22	25	mA	t_{inst} = 0.32 µs MB89P558A
	I_{CC2}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 5.0 V F_{CH} = 10.0 MHz	—	1.4	2.1	mA	t_{inst} = 6.4 µs MB89557A/558A
		V_{CC2}	V_{CC2} = 3.0 V F_{CH} = 10.0 MHz	—	5.3	9	mA	t_{inst} = 6.4 µs MB89P558A
	I_{CCS1}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 3.0 V F_{CH} = 12.5 MHz	—	2	3	mA	Sleep mode t_{inst} = 0.32 µs MB89557A/558A
		V_{CC2}	V_{CC2} = 5.0 V F_{CH} = 12.5 MHz	—	6.2	10	mA	Sleep mode t_{inst} = 0.32 µs MB89P558A
	I_{CCS2}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 3.0 V F_{CH} = 10.0 MHz	—	0.35	1	mA	Sleep mode t_{inst} = 6.4 µs MB89557A/558A
		V_{CC2}	V_{CC2} = 3.0 V F_{CH} = 10.0 Hz	—	0.6	2	mA	Sleep mode t_{inst} = 6.4 µs MB89P558A
	I_{CCL}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 5.0 V F_{CL} = 32 kHz T_A = + 25 °C	—	30	50	µA	Sub-mode MB89557A/558A
		V_{CC2}	V_{CC2} = 3.0 V F_{CL} = 32 kHz T_A = + 25 °C	—	4	8	mA	Sub-mode MB89P558A
	I_{CCLS}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 3.0 V F_{CL} = 32 kHz T_A = + 25 °C	—	10	20	µA	Sub-sleep mode MB89557A/558A
		V_{CC2}	V_{CC2} = 3.0 V F_{CL} = 32 kHz T_A = + 25 °C	—	20	50	µA	Sub-sleep mode MB89P558A

(Continued)

(AV_{CC} = AVR = DVR = V_{CC2} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCT}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 3.0 V T_A = + 25 °C F_{CL} = 32 kHz	—	5	15	µA	Clock mode Main stop MB89557A/558A
		V_{CC2}	V_{CC2} = 3.0 V F_{CL} = 32 kHz T_A = + 25 °C	—	12	25	µA	Clock mode Main stop MB89P558A
	I_{CCH}	V_{CC1}	V_{CC1} = 3.0 V V_{CC2} = 3.0 V F_{CL} = 32 kHz T_A = + 25 °C	—	5	10	µA	T_A = +25 °C Sub- stop MB89557A/558A
		V_{CC2}	V_{CC2} = 3.0 V F_{CL} = 32 kHz T_A = + 25 °C	—	5	10	µA	T_A = +25 °C Sub- stop MB89P558A
	I_A	AV_{CC}	V_{CC1} = 3.0 V AV_{CC} = V_{CC2} = 5.0 V F_{CH} = 12.5 MHz	—	2	5	mA	A/D converter running MB89557A/558A
		AV_{CC}	V_{CC2} = 5.0 V F_{CH} = 12.5 MHz	—	3	6	mA	A/D converter running MB89P558A
	I_{AH}	AV_{CC}	V_{CC1} = 3.0 V, AV_{CC} = V_{CC2} = 5.0 V F_{CH} = 12.5 MHz T_A = + 25 °C	—	—	10	µA	T_A = +25 °C A/D converter stopped MB89557A/558A
		AV_{CC}	V_{CC2} = 5.0 V F_{CH} = 12.5 MHz T_A = + 25 °C	—	—	10	µA	T_A = +25 °C A/D converter stopped MB89P558A
LCD divider resistance	R_{LCD}	—	V_{CC} to V_0 at V_{CC} = 5 V	—	500	—	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 5 V	—	—	5	kΩ	
SEG0 to SEG31 output impedance	R_{VSEG}	SEG0 to SEG31		—	—	15	kΩ	
LCD leak current	I_{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG31	—	—	—	±5	µA	

(Continued)

(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
LCD step-up output voltage	V_{OV3}	V3	V1 = 1.5 V	—	4.5	—	V	Models with step-up circuits only
	V_{OV2}	V2		—	3.0	—	V	
Reference voltage input impedance	R_{RIN}	V1	—	600	1000	1400	kΩ	Models with step-up circuits only
Input capacitance	C_{IN}	Pins other than V_{CC},V_{SS}	F_{CH} = 1 MHz	—	10	—	pF	
V1 input voltage	V_{I1}	V1	I_{IN} = 0 µA	—	1.5	—	V	Models with step-up circuits only

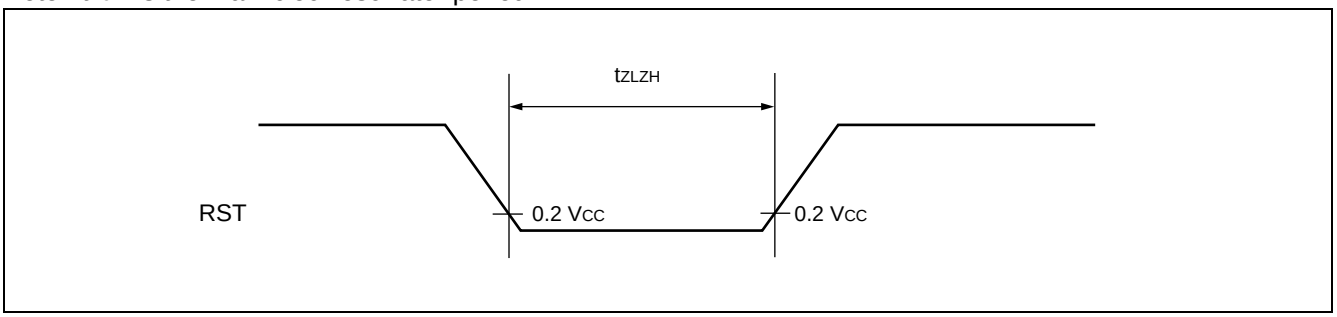
4. AC Characteristics

(1) Reset Timing

($DVR = V_{CC1} = 3$ V, $AVss = Vss = 0$ V, $T_A = -40$ °C to +85 °C)

Parameter	Symbol	Confition	Rating		Unit	Remarks
			Min	Max		
RST "L" pulse width	t_{ZLZH}	—	48 t_{HCLY}	—	ns	

Note : t_{HCLY} is the main clock oscillator period.

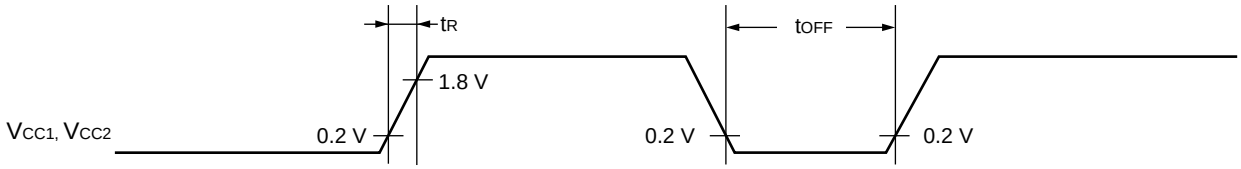


(2) Power-on Reset

($AVss = Vss = 0$ V, $T_A = -40$ °C to +85 °C)

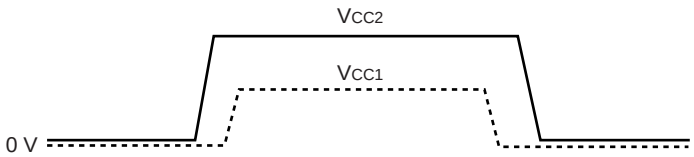
Parameter	Symbol	Confition	Rating		Unit	Remarks
			Min	Max		
Power supply rise time	t_R	—	0.05	50	ms	
Power supply cutoff time	t_{OFF}		1	—	ms	For repeated operation

Note : Be sure that the power supply rise time is less than the selected oscillator stabilization period. Also, when varying the supply voltage during operation, it is recommended that the supply voltage be increased gradually.



On the MB89PV550A and MB89548A oscillation begins and the power-on reset is applied on the rise of the V_{CC2}.On the MB89558A and MB89557A, oscillation begins and the power-on reset is applied on the rise of the V_{CC1}.

(3) Power Supply Voltage



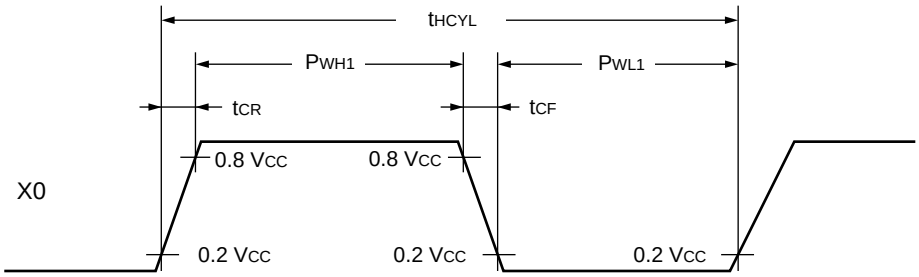
Be sure that the power supply is set so that $V_{CC2} \geq V_{CC1}$.
The MB89PV550A and MB89P558A operate on the V_{CC2} power supply only.
On the MB89558A and MB89557A, V_{CC1} is the power supply for internal CPU operation, and V_{CC2} is the I/O power supply.

(4) Clock Timing

(AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

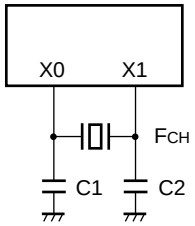
Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	12.5	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{HCYL}	X0, X1		80	—	1000	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH1} P_{WL1}	X0		20	—	—	ns	External clock
	P_{WH2} P_{WL2}	X0A		—	15.2	—	µs	External clock
Input clock rise, fall time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

- X0 and X1 clock timing and input conditions

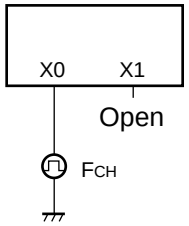


- Clock configurations

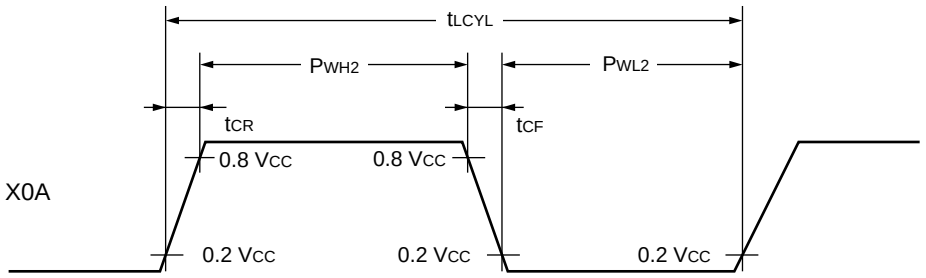
When using a crystal oscillator or ceramic oscillator



When using an external clock

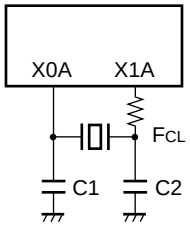


• X0A and X1A clock timing conditions

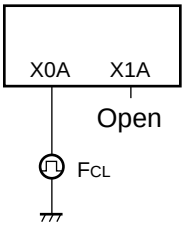


• Clock configurations

When using a crystal oscillator or ceramic oscillator



When using an external clock



(5) Instruction Cycle

(AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum instruction execution time)	t_{inst}	4/F_{CH}, 8/F_{CH}, 16/F_{CH}, 64/F_{CH},	µs	Operating at F_{CH} = 12.5 MHz (4/F_{CH}) t_{inst} = 0.32 µs
		2/F_{CL}	µs	Operating at F_{CL} = 32.768 kHz t_{inst} = 61.036 µs

Note : Instruction execution time settings differ for 12.5 MHz operation.

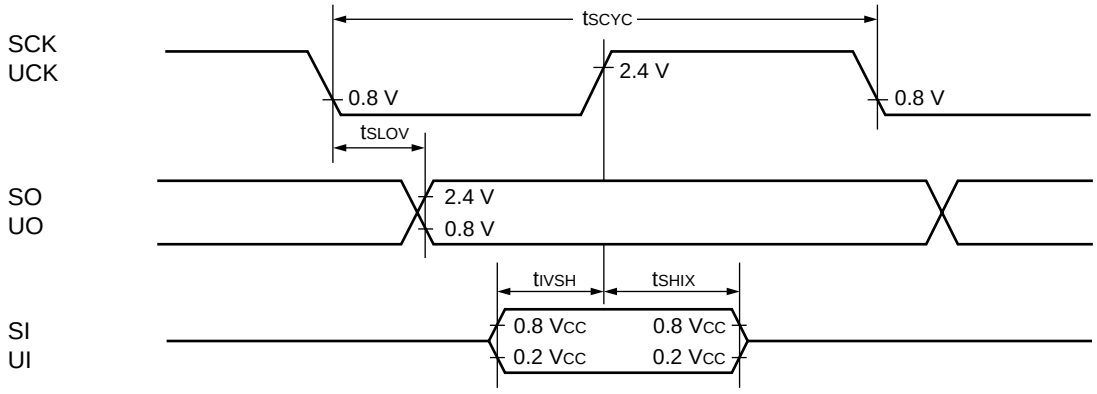
(6) Serial I/O timing

(V_{CC1} = 3.0 V, AV_{CC} = AVR = DVR = V_{CC2} = 5 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

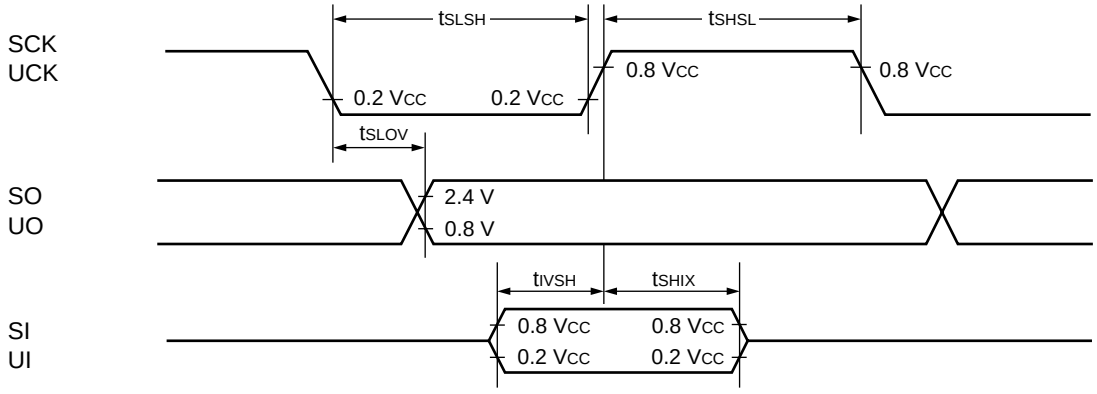
Parameter	Sym-bol	Pin Nme	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK, UCK	Internal clock operation	2 t_{inst}*	—	µs	
SCK↓→SO time UCK↓→UO time	t_{SLOV}	SCK, SO, UCK, UO		–200	+200	ns	
Valid SI→SCK↑ Valid UI→UCK↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK↑→ valid SI hold time UCK↑→ valid UI hold time	t_{SHIX}	SCK, SI, UCK, UI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK, UCK	External clock operation	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK↓→SO time UCK↓→UO time	t_{SLOV}	SCK, SO, UCK, UO		0	200	ns	
Valid SI→SCK↑ Valid UI→UCK↑	t_{IVSH}	SI, SCK, UI, UCK		1/2 t_{inst}*	—	µs	
SCK↑→ valid SI hold time UCK↑→ valid UI hold time	t_{SHIX}	SCK, SI, UCK, UI		1/2 t_{inst}*	—	µs	

* : For a definition of t_{inst} see “ (5) Instruction Cycle”.

• Internal shift clock mode



• External shift clock mode

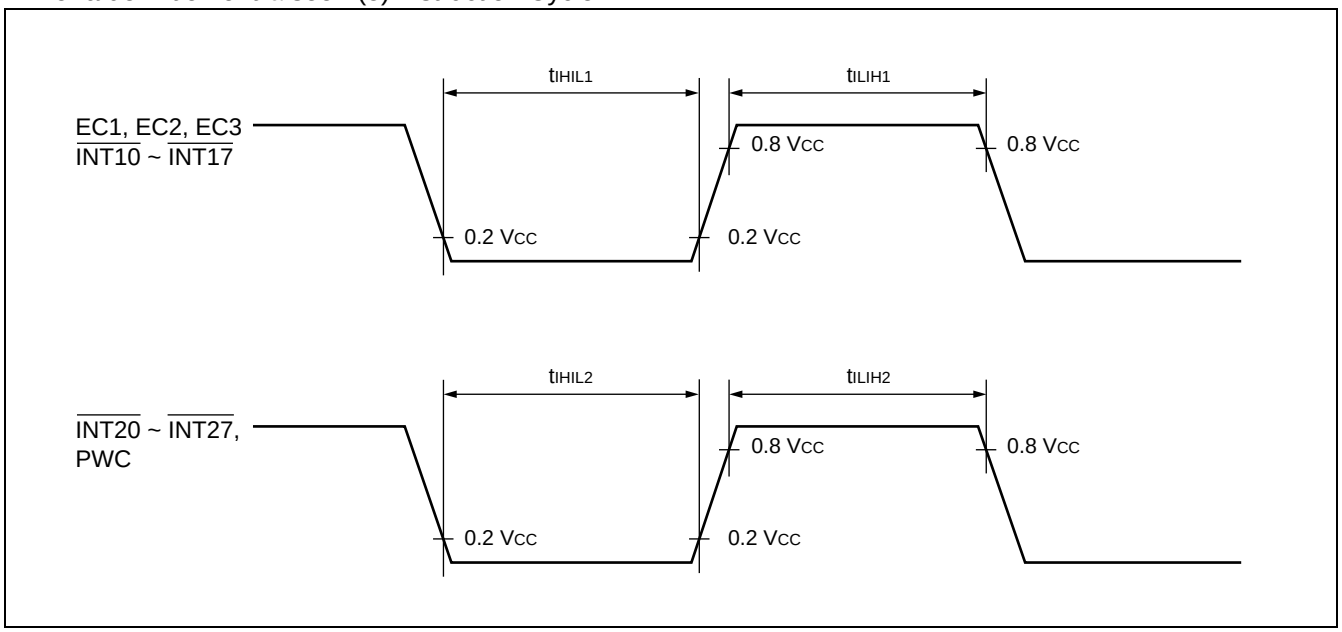


(7) Peripheral Input Timing

(V_{CC1} = 3 V, AV_{CC} = AVR = DVR = V_{CC2} = 5.0 V, AVss = Vss = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin Nme	Condition	Value		Unit	Remarks
				Min	Max		
Peripheral input “H” level pulse width 1	t_{ILIH1}	EC1, EC2, EC3 $\overline{INT10}$ to $\overline{INT17}$	—	1 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 1	t_{IHIL1}	EC1, EC2, EC3 $\overline{INT10}$ to $\overline{INT17}$	—	1 t_{inst}*	—	µs	
Peripheral input “H” level pulse width 1	t_{ILIH2}	PWC, $\overline{INT20}$ to $\overline{INT27}$	—	2 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 1	t_{IHIL2}	PWC, $\overline{INT20}$ to $\overline{INT27}$	—	2 t_{inst}*	—	µs	

* : For a definition of t_{inst} see “ (5) Instruction Cycle”.



(8) Electrical Characteristics for the A/D Converter

(V_{CC1} = 3 V, AV_{CC} = AVR = DVR = V_{CC2} = 3.5 V to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Item	Sym-bol	Pin Nme	Condition	Rating			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	10	—	bit	
Total error			AVR = AV_{CC}	—	—	±5.0	LSB	
Linearity error				—	—	±2.5	LSB	
Differential linearity error				—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7		AV_{SS} – 3.5	+ 0.5	AV_{SS} + 4.5	LSB	
Full scale transition voltage	V_{FST}			AVR – 6.5	AVR – 1.5	AVR + 1.5	LSB	
Variation between channels	—			—	—	4	LSB	
Conversion time		—	—	—	60 tinst	—	µs	*
Sampling time				—	16 tinst	—	µs	
Analog input current	I_{AIN}	AN0 to AN7	—	—	—	10	µA	
Analog input voltage	V_{AIN}			AV_{SS}	—	AVR	V	
Reference voltage	—	AVR		AV_{SS} + 2.7	—	AV_{CC}	V	
Reference voltage supply current	I_R		A/D operating	—	400	—	µA	
	I_{RH}		A/D stop	—	—	5	µA	

* : Includes sampling time.

(9) Electrical Characteristics for the D/A Converter

(V_{CC1} = 3 V, AV_{CC} = AVR = DVR = V_{CC2} = 3.5 V to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Item	Sym-bol	Pin Nme	Condition	Rating			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Differential linearity error			AVR = AV_{CC}	—	—	±0.9	LSB	
Linearity error				—	—	±1.5	LSB	
Conversion time				—	10	20	µs	*1
Analog reference voltage		DVR		V_{SS} + 3.0	—	AV_{CC}	V	
Reference voltage supply current	I_{DVR}		D/A running	—	120	300	µA	*2
	I_{DVRS}		D/A off	—	—	10	µA	*3
Analog output impedance	—	—	—	—	20	—	kΩ	MB89P558A
				—	30	—	kΩ	MB89558A/ 557A

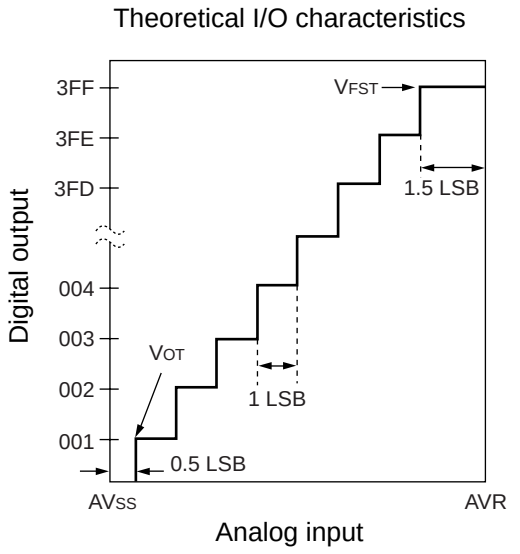
*1 : With load capacitance 20 pF.

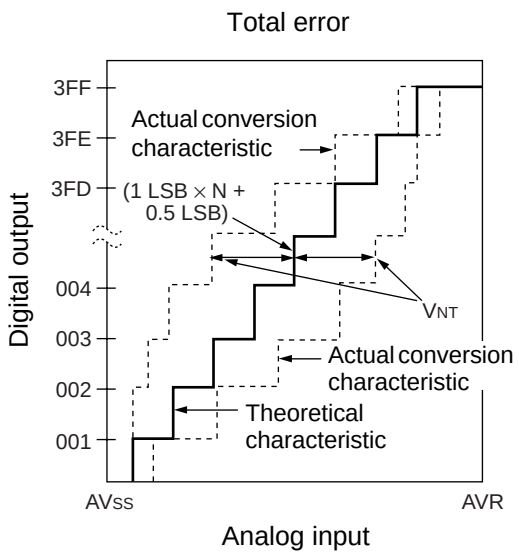
*2 : No-load conversion

*3 : Stop mode

(10) A/D Converter Glossary

- Resolution
  The level of analog variation that can be recognized by the A/D converter.
- Linearity error (Unit : LSB)
  The deviation between the actual conversion characteristics and the line linking the zero transition point (“00 0000 0000”←→“00 0000 0001”) and the full-scale transition point (“11 1111 1110”←→“11 1111 1111”) .
- Differential linearity error (Unit : LSB)
  The variation from the theoretical input voltage required to change the output code by 1 LSB.
- Total error (Unit : LSB)
  The total error is the difference between the actual value and the theoretical value.



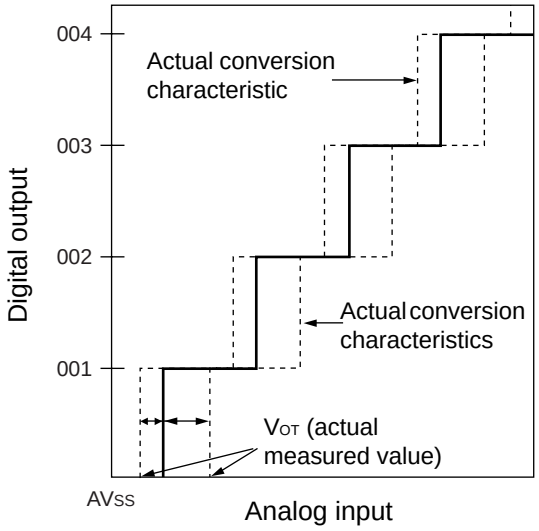


$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{(V)} \qquad \text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times \text{N} + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

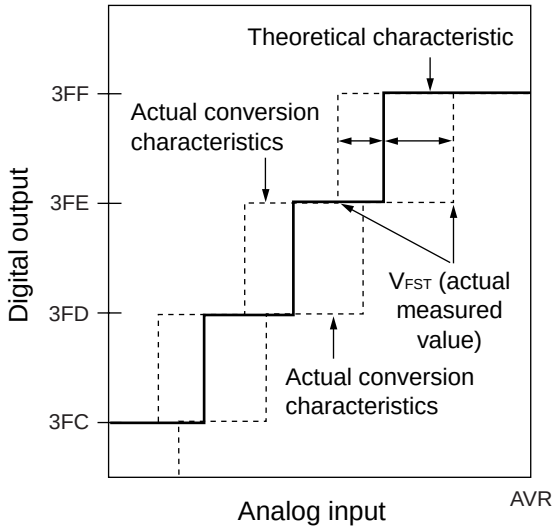
(Continued)

(Continued)

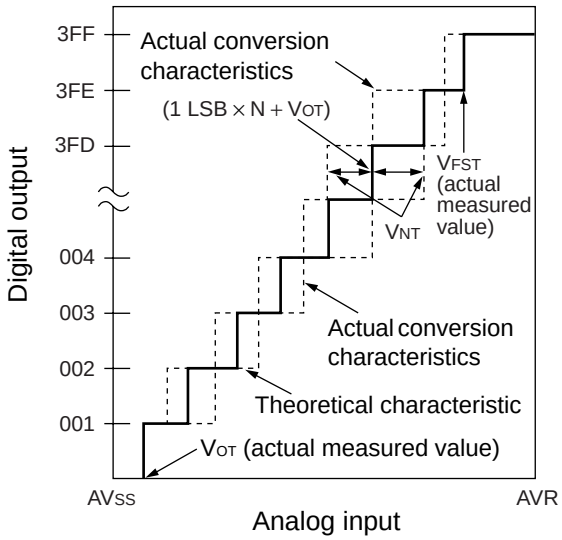
Zero transition error



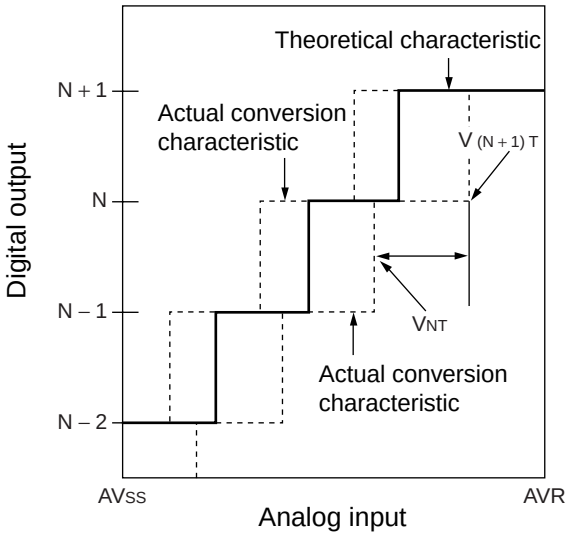
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

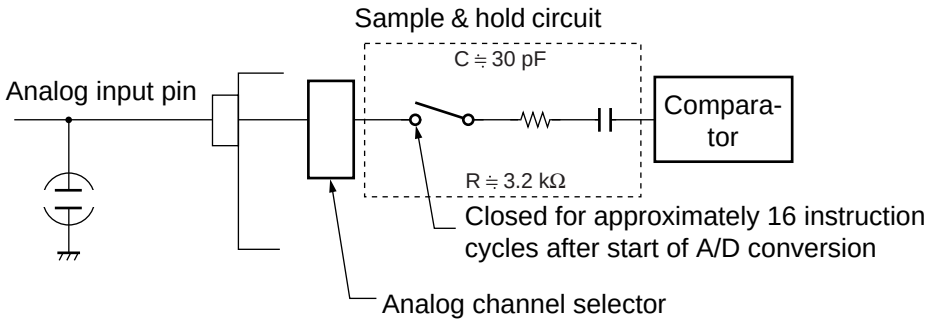
$$\text{Differential linearity error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

(11) Notes for A/D Conversion

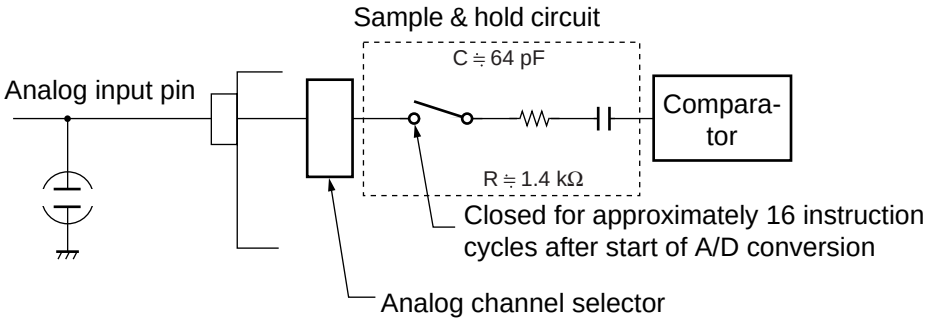
- Analog input pins and input impedance

The A/D converter in the MB89550A series incorporates a sample & hold circuit as shown below. When an A/D conversion starts, the voltage at the analog input pin is captured by the sample & hold capacitor for a period of 16 instruction cycles.
Accordingly, if the output impedance of the external circuit connected to the analog input is high, the analog input voltage may not stabilize within the period of the analog input sampling time. Therefore, it is recommended that the output impedance of the external circuit be sufficiently low (10 kΩ or less) .

- Equivalent circuit for MB89558A and MB89557A analog input



- Equivalent circuit for MB89P558A and MB89PV550A analog input

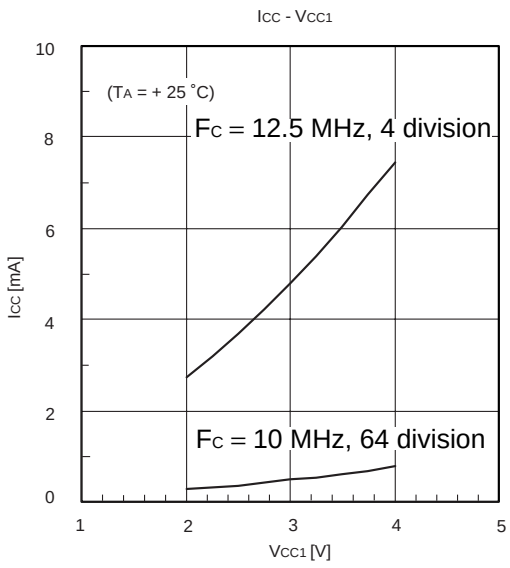


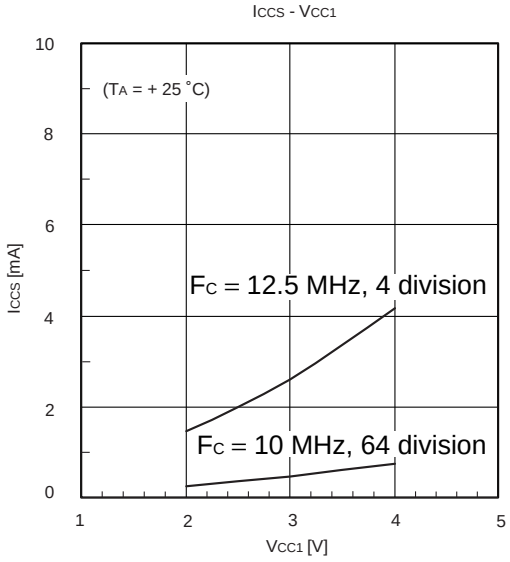
- Error

The relative error increases as |AVR – AVSS| becomes smaller.

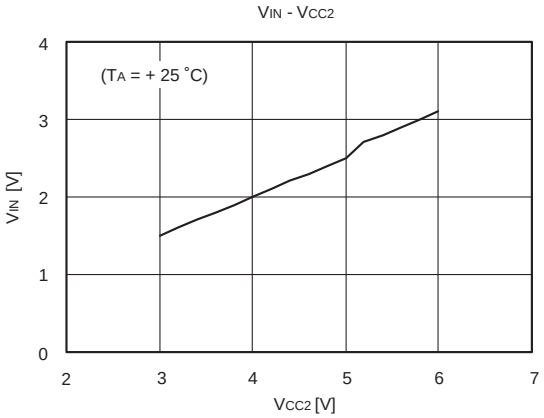
■ EXAMPLE CHARACTERISTICS

(1) Power Supply Current (External Clock)

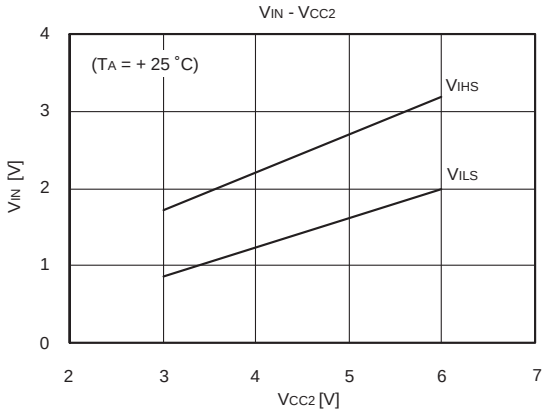




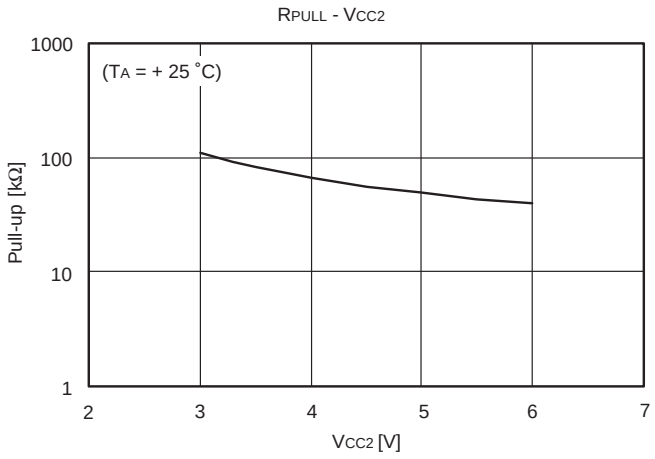
(2) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



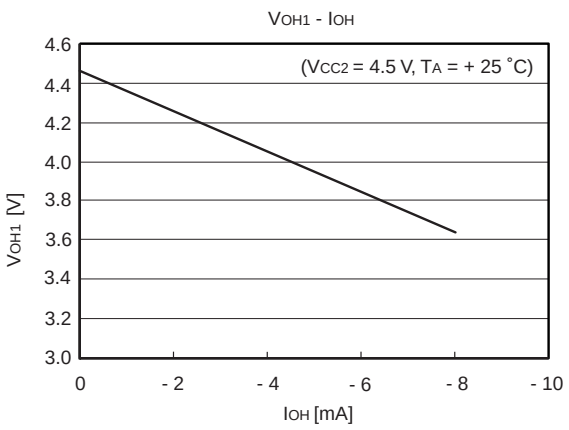
(3) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

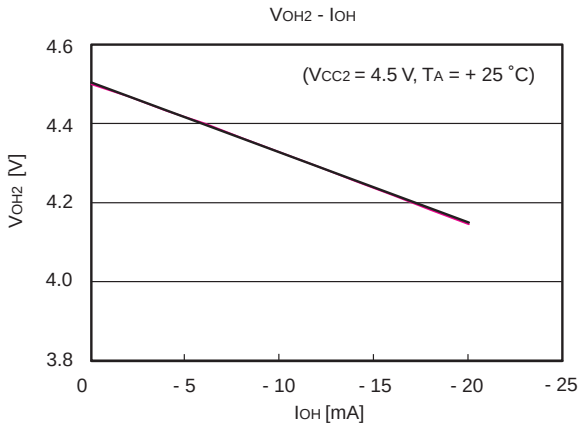


(4) Pull-up Resistance

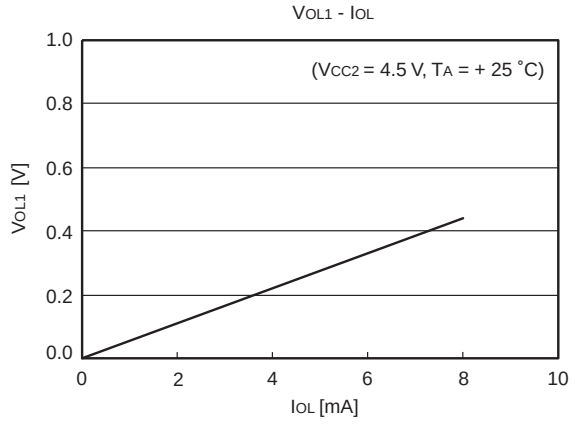


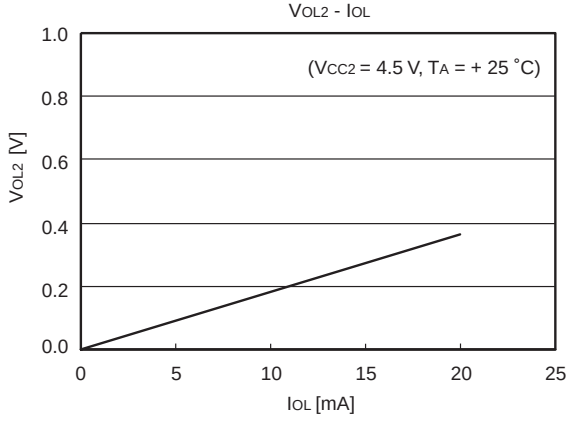
(5) “H” Level Output Voltage



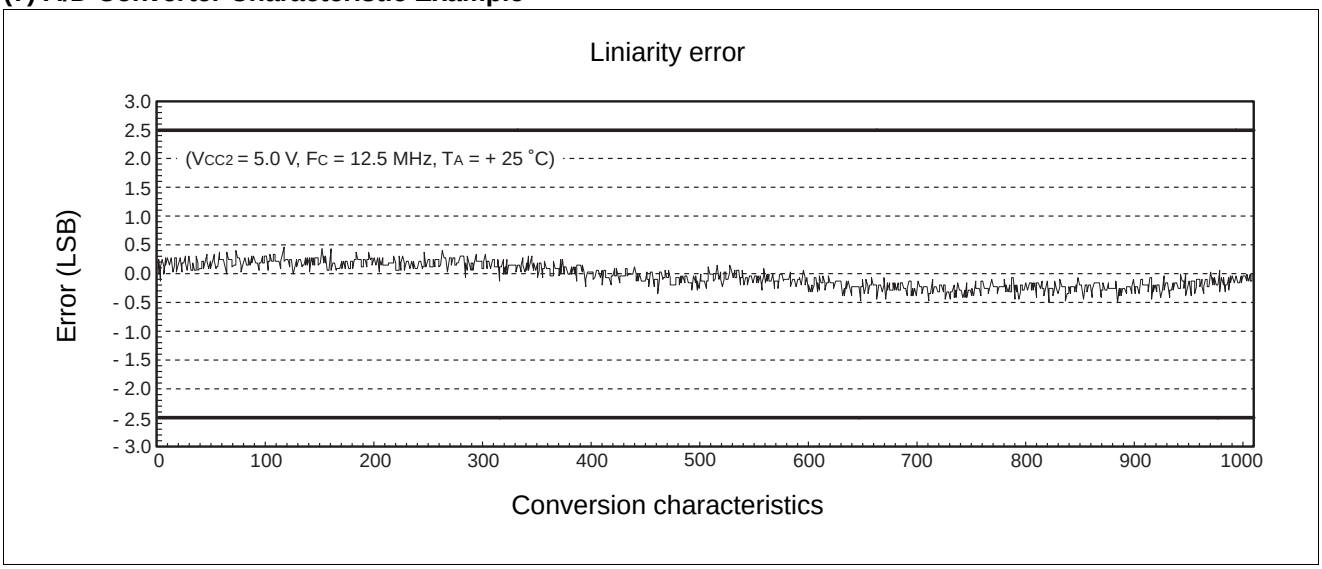


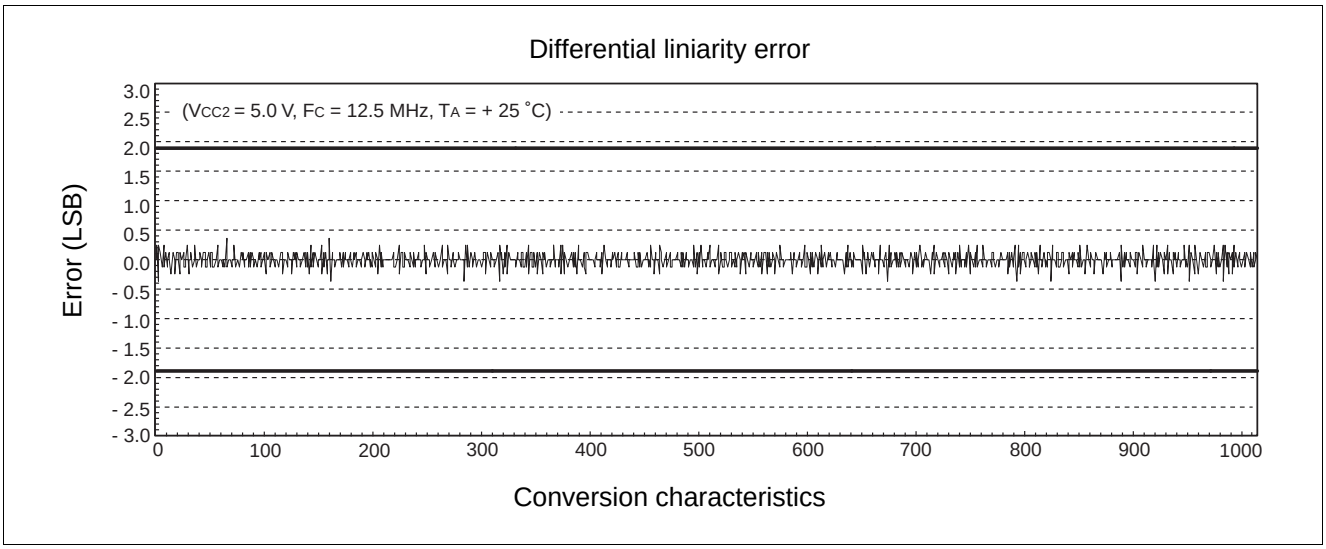
(6) “L” Level Output Voltage





(7) A/D Converter Characteristic Example





■ MASK OPTIONS

No.	Part No.	MB89557A MB89558A	MB89P558A	MB89PV550A
	Specifying procedure	Specify when ordering mask	Specify at time of order	Specify at time of order
1	LCD drive power supply • Built-in step-up circuit • Built-in multiplier resistance (for external connection)	Selectable	-201 built-in multiplier resistance	-201 built-in multiplier resistance
			-202 built-in step-up circuit	-202 built-in step-up circuit
			-203 built-in step-up circuit	-203 built-in step-up circuit
2	Port/segment selection*1 P66 (SEG22), P67 (SEG23), P70 (SEG24), P71 (SEG25), P72 (SEG26), P73 (SEG27), P74 (SEG28), P75 (SEG29), P76 (SEG30), P77 (SEG31)	Selectable	-201 segment selected (SEG22-SEG31 selected)	-201 segment selected (SEG22-SEG31 selected)
			-202 segment selected (SEG22-SEG31 selected)	-202 segment selected (SEG22-SEG31 selected)
			-203 port selected (P66, P67, P70-P77 selected)	-203 port selected (P66, P67, P70-P77 selected)
3	Main clock Initial value*2 selection for oscillator stabilization wait period (Fch = 12.5 MHz) • 01 : 2^{14}/Fch (approx. 1.31 ms) • 10 : 2^{17}/Fch (approx. 10.48 ms) • 11 : 2^{18}/Fch (approx. 20.97 ms)	Selectable	2^{18}/Fch (approx. 20.97 ms)	2^{18}/Fch (approx. 20.97 ms)

*1 : This selection determines whether pins P66, P67, P70-P77 are used as I/O ports or as segment output pins. If they are used as ports, then SEG22-SEG31 (Nch open drain) are not restricted by the condition for input voltage to pins (V_{IN}), namely that "V_{IN} must be lower than the voltage at the V3 pin".

*2 : This represents the initial value of the oscillator stabilization period select bit (SYCC : WT1, WT0) of the system clock control register.

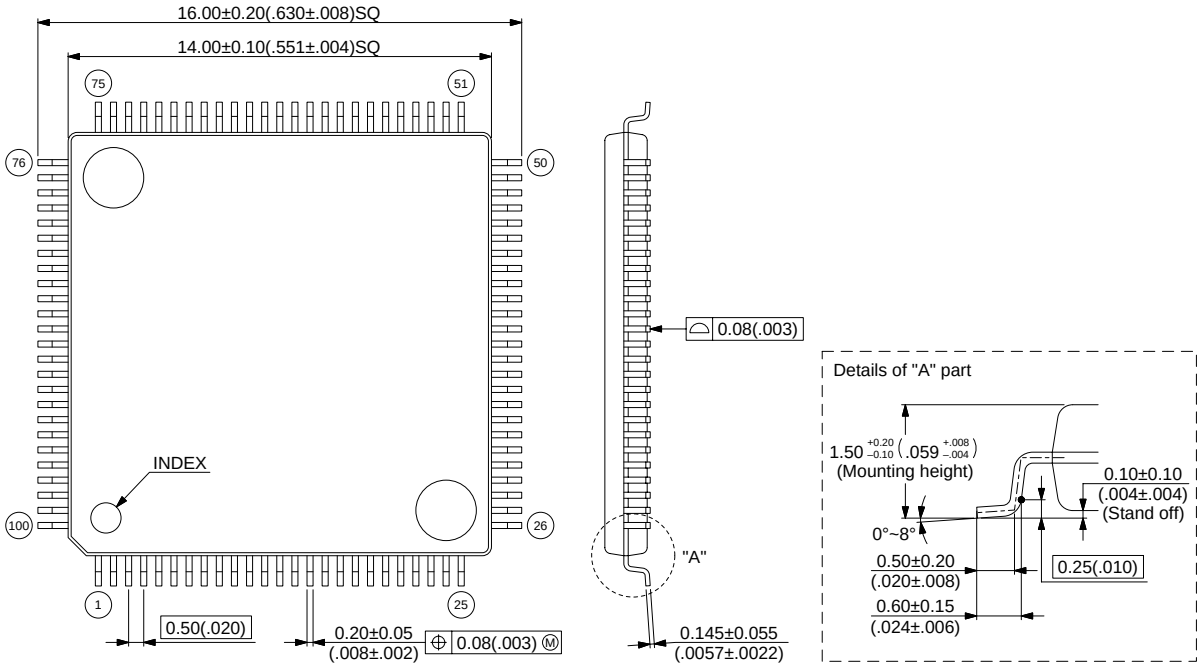
■ ORDERING INFORMATION

Part No.	Package	Remarks
MB89558APFV-XXX	100-pin Plastic LQFP (FPT-100P-M05)	
MB89558APFT-XXX	100-pin Plastic TQFP (FPT-100P-M18)	
MB89P558A-201PFV versions without step-up MB89P558A-202PFV with step-up 32 Segment MB89P558A-203PFV with step-up 22 Segment	100-pin Plastic LQFP (FPT-100P-M05)	
MB89P558A-201PFT versions without step-up MB89P558A-202PFT with step-up 32 Segment MB89P558A-203PFT with step-up 22 Segment	100-pin Plastic TQFP (FPT-100P-M18)	
MB89PV550A-201CF versions without step-up MB89PV550A-202CF with step-up 32Segment MB89PV550A-203CF with step-up 22Segment	100-pin Ceramic MQFP (MQP-100C-P02)	

■ PACKAGE DIMENSIONS

100-pin plasic LQFP
(FPT-100P-M05)

Note) Pins width and pins thickness include plating thickness.

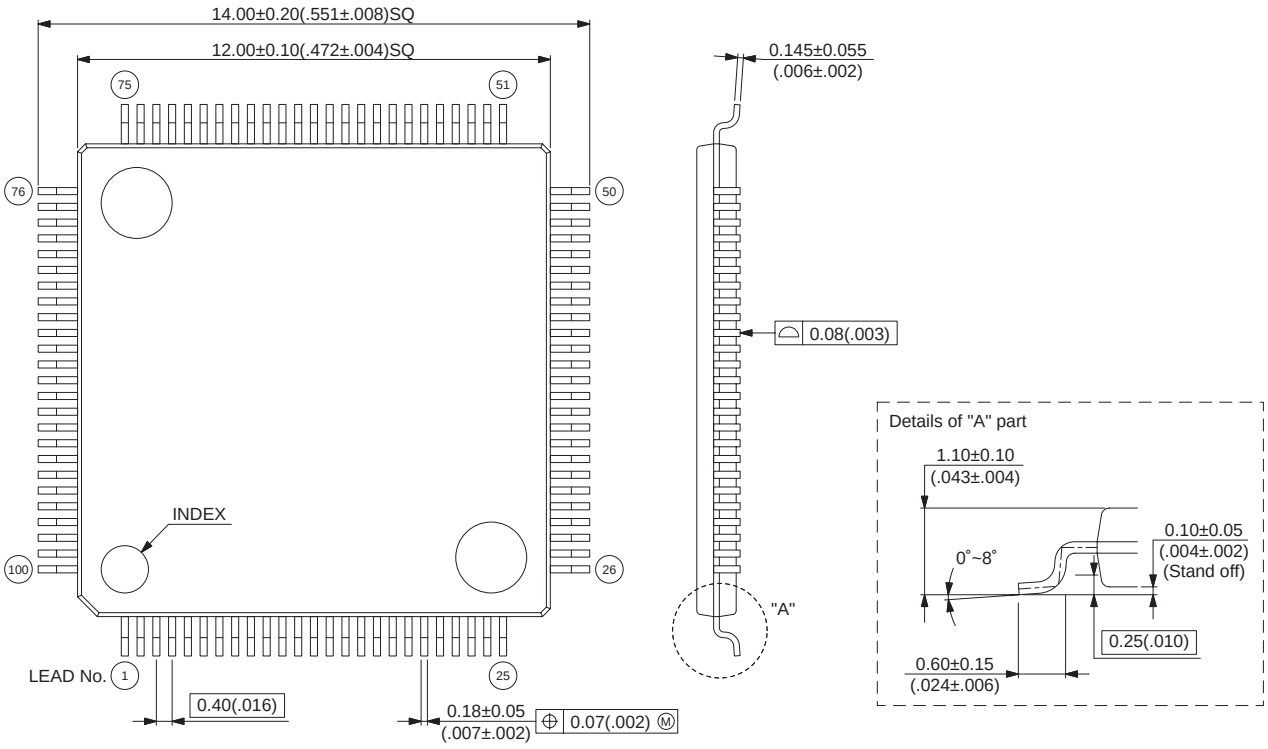


Dimensions in mm (inches)

(Continued)

100-pin plasic TQFP
(FPT-100P-M18)

Note) Pins width and pins thickness include plating thickness.

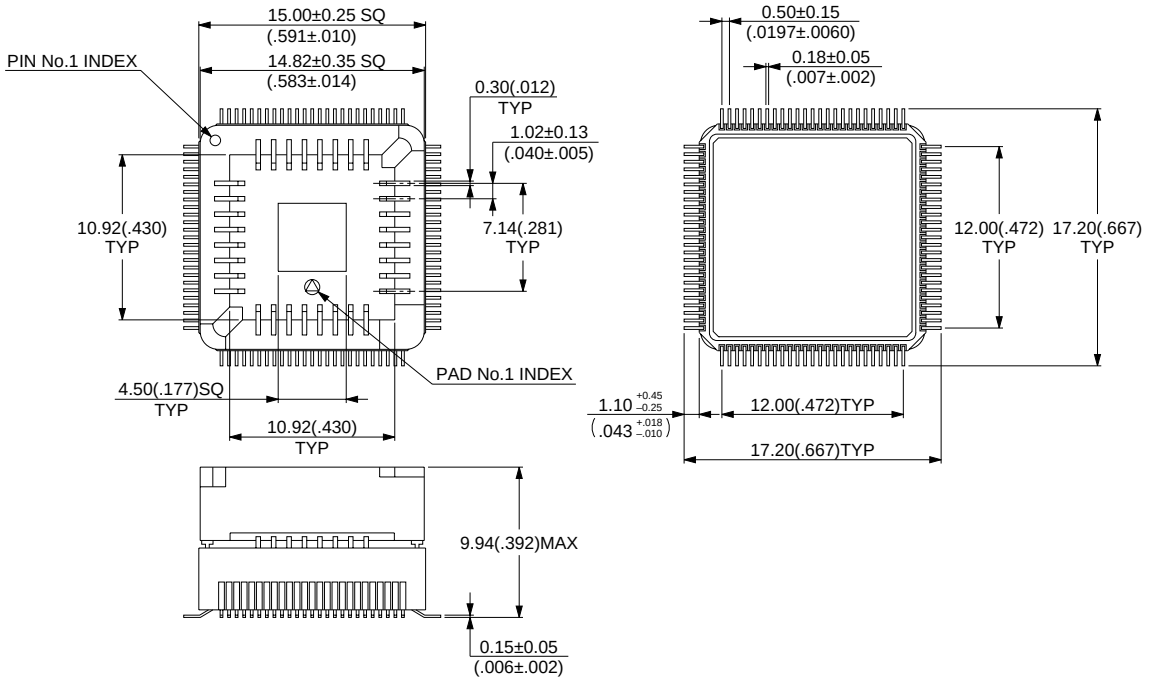


Dimensions in mm (inches)

(Continued)

(Continued)

100-pin Ceramic MQFP
(MQP-100C-P02)



Dimensions in mm (inches)

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