

# 8-bit Proprietary Microcontrollers

CMOS

## F<sup>2</sup>MC-8L MB89580B/580BW Series

### MB89583B/585B/589B/P585B/P589B/ MB89583BW/585BW/P585BW

#### ■ DESCRIPTION

The MB89580B/BW series is a line of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, these microcontrollers contain a variety of peripheral functions, such as PLL clock control, timers, a serial interface, a PWM timer, and the USB function. In particular, these microcontrollers contain one USB function channel to support both full and low speeds.

#### ■ FEATURES

- **Package type**

64-pin LQFP package (0.5 mm and 0.65 mm pitch)

- **High-speed operations at low voltage**

Minimum execution time : 0.33  $\mu$ s (Automatically generates a 12 MHz main clock and a 48 MHz USB interface synchronization clock with an externally supplied 6 MHz clock and the internal PLL circuit.)

- **F<sup>2</sup>MC-8L CPU core**

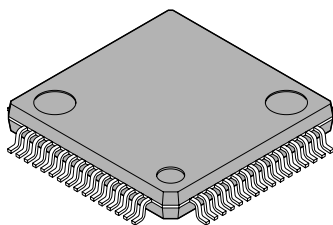
Instruction set that is optimum to the controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- branch instructions by bit testing
- bit manipulation instructions, etc.

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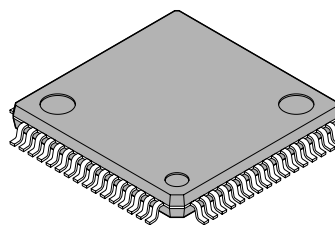
#### ■ PACKAGES

64-pin plastic LQFP



(FPT-64P-M03)

64-pin plastic LQFP



(FPT-64P-M09)

# MB89580B/580BW series

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- **PLL clock control**

The internal PLL clock circuit allows the use of low-speed clocks which are advantageous to noise characteristics.

(6 MHz externally-supplied clock→12 MHz internal system clock)

- **Various timers**

8-bit PWM timer (can be used as either 8-bit PWM timer × 2 channels or PPG timer × 1 channel)

Internal 21-bit timebase timer

- **Internal USB transceiver circuit (Compatible with full and low speeds)**

- **USB function**

Compliant to USB Protocol Revision 1.0

Support for both low and full speeds (selectable)

Allows four endpoints to be specified at maximum.

Types of transfer supported : control/interrupt/bulk/isochronous

Built-in DMAC (Maps the buffer for each endpoint on to the internal RAM to directly access the memory for function's send and receive data.)

- **UART/serial interface**

Built-in UART/SIO function (selectable by switching)

- **External interrupt**

External interrupt (level detection × 8 channels)

Eight inputs are independent of one another and can also be used for resetting from low-power consumption mode (the L-level detection feature available) .

- **Low power consumption (standby mode supported)**

Stop mode (There is almost no current consumption since oscillation stops.)

Sleep mode (This mode stops the running CPU.)

- **A maximum of 53 general-purpose I/O ports**

General-purpose I/O ports (CMOS) : 34

General-purpose output ports (CMOS) : 8

General-purpose I/O ports (Nch open drain) : 3

General-purpose input ports (CMOS 3.3 V input-compatible) : 8

- **Parallel ports**

Also serve as eight of the general-purpose I/O ports (CMOS)

Interrupt function available

Allows asynchronous read and write by external signals

- **Power supply**

Supply voltage : 3.0 V to 5.5 V

# MB89580B/580BW series

## ■ PRODUCT LINEUP

Part number		MB89583B	MB89585B	MB89P585B	MB89589B	MB89P589B	MB89583BW	MB89585BW	MB89P585BW		
Parameter											
ROM size		8 KB	16 KB				8 KB	16 KB			
RAM size		512 B	1 KB		18 KB		512 B	1 KB			
Package		LQFP-64 (FPT-64P-M03)			LQFP-64 (FPT-64P-M09)		LQFP-64 (FPT-64P-M03)				
Operation at USB reset		High impedance state					Low-level output				
Others		MASK product		OTP/EVA product	MASK product	OTP/EVA product	MASK product		OTP/EVA product		
CPU functions		Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum execution time : 0.33 μs (6 MHz) Interrupt processing time : 3 μs (6 MHz)									
Peripheral functions	General-purpose ports	General-purpose I/O ports (34 : CMOS, 3 : Nch open drain) General-purpose output ports (8 : CMOS) General-purpose input ports (8 : CMOS 3.3 V input)									
	Parallel ports	Shares eight (P40 through P47) of the above general-purpose I/O ports. Allows asynchronous read and write by external signals. An interrupt function is available to set data.									
	USB function	Can be set to full/low speed. Four endpoints at maximum Power supply mode : Can be set to own power supply/bus power supply mode. FIFO 8 bits × 8 built in Built-in DMAC (Can be set to DMA transfer to the internal RAM or to the external FIFO.)									
	PWM timer	8-bit PWM timer operation × 2 channels (can also be used as a PPG × 1 channel timer)									
	UART	SIO	Allows switching between UART (clock-synchronous/asynchronous data transfer allowed) and SIO (simple serial transfer) .								
	Timebase timer	21-bit timebase timer									
	Clock output	Allows output of two main clock divisions									
Standby mode		Sleep mode and Stop mode									

## ■ PACKAGES AND CORRESPONDING PRODUCTS

Package	MB89583B	MB89585B	MB89P585B	MB89589B	MB89P589B	MB89583BW	MB89585BW	MB89P585BW
FPT-64P-M03	○	○	○	×	×	○	○	○
FPT-64P-M09	×	×	×	○	○	×	×	×

○ : Available    × : Not available

# MB89580B/580BW series

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the OTP product, verify its differences from the product that will actually be used.

### 2. Current Consumption

When operated at low speeds, a product mounted with either one-time PROM or EPROM consumes more current than a product mounted with a mask ROM. However, in sleep/stop mode the current consumption is the same.

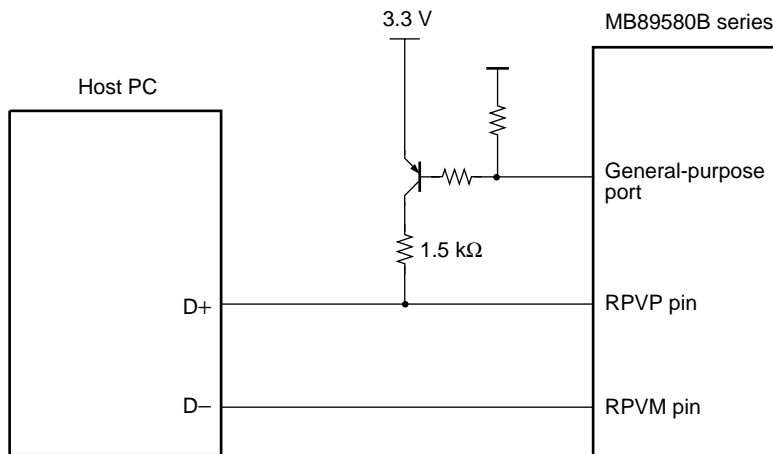
For detailed information on each package, see “■ PACKAGE DIMENSIONS.”

### 3. Differences Between the MB89580B series and the MB89580BW Series

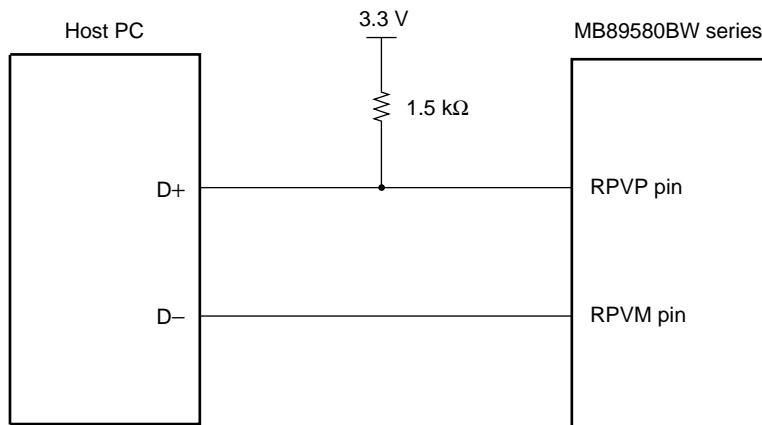
MB89580B series : Remains in high impedance state until USB connection takes place. Before the USB connection, use one general-purpose port output to control pullup resistance connection of this port by software.

MB89580BW : Outputs at low level until USB connection takes place.

#### • Example MB89580B product connection



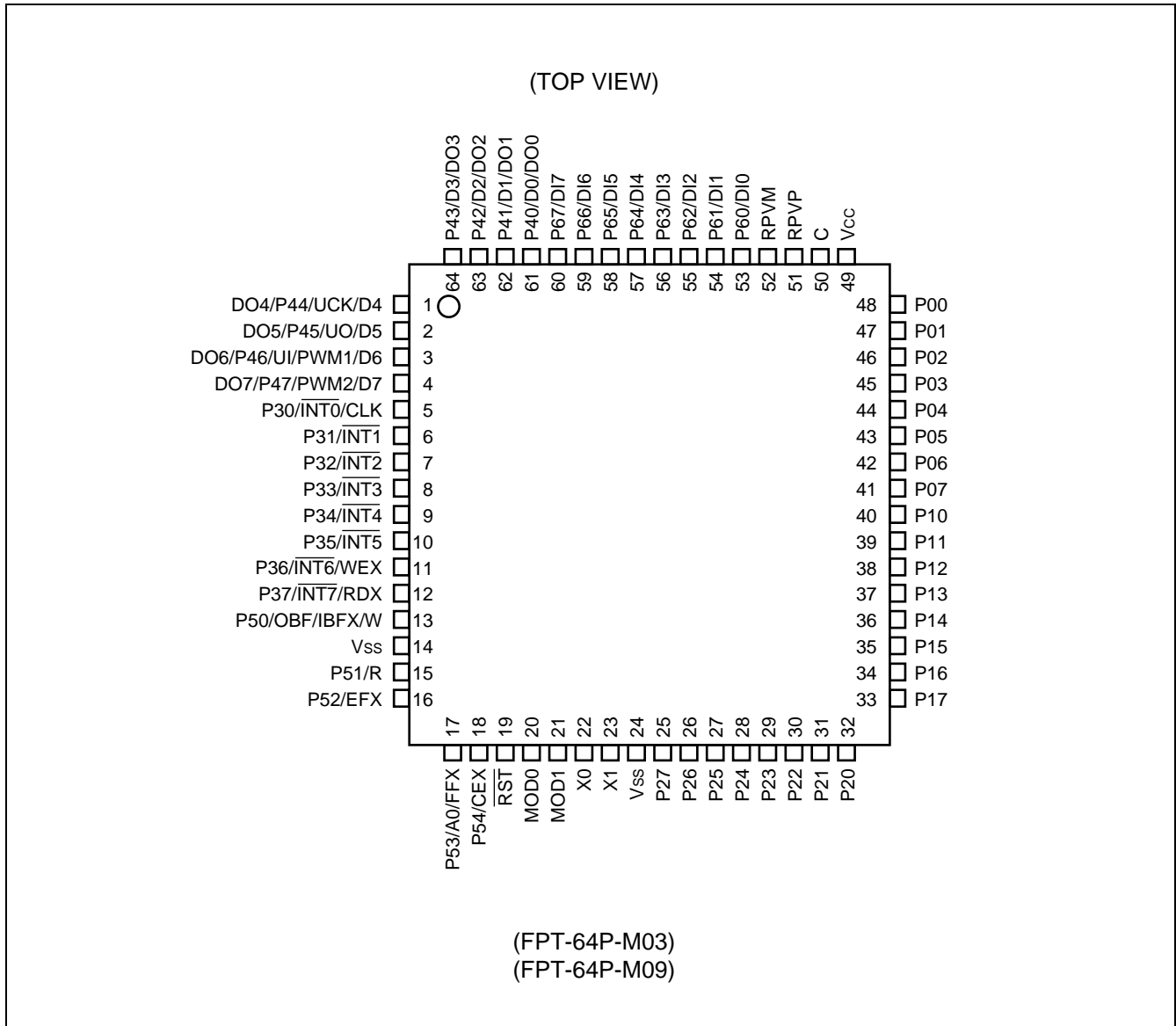
#### • Example MB89580BW product connection



Note : Full speed is assumed in the above examples.

# MB89580B/580BW series

## ■ PIN ASSIGNMENT



# MB89580B/580BW series

## ■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
1	P44/U $\overline{C}$ K/D4/ DO4	E	General-purpose CMOS I/O pin UART/S10 clock I/O This pin also serves as a parallel interface/external FIFO data output pin.
2	P45/UO/D5/ DO5	B	General-purpose CMOS I/O pin UART/S10 serial data output This pin also serves as a parallel interface/external FIFO data output pin.
3	P46/UI/ PWM1/D6/ DO6	E	General-purpose CMOS I/O pin UART/S10 serial data input PWM timer This pin also serves as a parallel interface/external FIFO data output pin.
4	P47/PWM2/ D7/DO7	B	General-purpose CMOS I/O pin PWM timer This pin also serves as a parallel interface/external FIFO data output pin.
5	P30/ $\overline{INT0}$ / CLK	E	General-purpose CMOS I/O pin Clock output pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
6	P31/ $\overline{INT1}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
7	P32/ $\overline{INT2}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
8	P33/ $\overline{INT3}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
9	P34/ $\overline{INT4}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
10	P35/ $\overline{INT5}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
11	P36/ $\overline{INT6}$ / WEX	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection) This pin also serves as the parallel interface write strobe input pin.
12	P37/ $\overline{INT7}$ / RDX	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection) This pin also serves as the parallel interface read strobe input pin.
13	P50/OBF/ IBFX/W	B	General-purpose CMOS I/O pin Interrupt output to the parallel interface host. This pin also serves the OUT FIFO data strobe pin.

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# MB89580B/580BW series

Pin No.	Pin name	Circuit type	Function
14	V <sub>SS</sub>	—	Power supply pin (GND)
15	P51/R	B	General-purpose CMOS I/O pin. This pin also serves the IN FIFO data strobe pin.
16	P52/EFX	K	General-purpose Nch open drain I/O pin. This pin also serves as the IN FIFO data enable input pin.
17	P53/A0/FFX	K	General-purpose Nch open drain I/O pin. Parallel interface's data select input This pin also serves as the OUT FIFO data enable input pin.
18	P54/CEX	K	General-purpose Nch open drain I/O pin. This pin also serves as the parallel interface device select input pin.
19	$\overline{\text{RST}}$	I	Reset pin. (Reset on the negative logic low level.)
20	MOD0	F	An operating mode designation pin. Connect directly to V <sub>SS</sub> .
21	MOD1	F	An operating mode designation pin. Connect directly to V <sub>SS</sub> .
22	X0	A	Pins for the connection of crystal oscillatoion circuit (6 MHz)
23	X1		
24	V <sub>SS</sub>	—	Power supply pin (GND)
25	P27	B	General-purpose CMOS output pin
26	P26	B	General-purpose CMOS output pin
27	P25	B	General-purpose CMOS output pin
28	P24	B	General-purpose CMOS output pin
29	P23	B	General-purpose CMOS output pin
30	P22	B	General-purpose CMOS output pin
31	P21	B	General-purpose CMOS output pin
32	P20	B	General-purpose CMOS output pin
33	P17	B	General-purpose CMOS I/O pin
34	P16	B	General-purpose CMOS I/O pin
35	P15	B	General-purpose CMOS I/O pin
36	P14	B	General-purpose CMOS I/O pin
37	P13	B	General-purpose CMOS I/O pin
38	P12	B	General-purpose CMOS I/O pin
39	P11	B	General-purpose CMOS I/O pin
40	P10	B	General-purpose CMOS I/O pin
41	P07	B	General-purpose CMOS I/O pin
42	P06	B	General-purpose CMOS I/O pin
43	P05	B	General-purpose CMOS I/O pin
44	P04	B	General-purpose CMOS I/O pin

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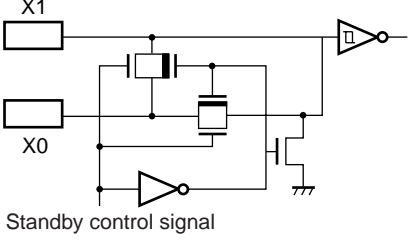
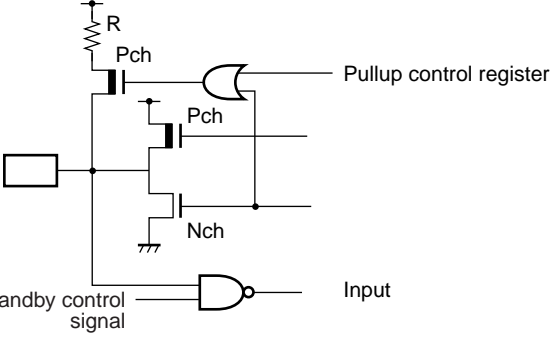
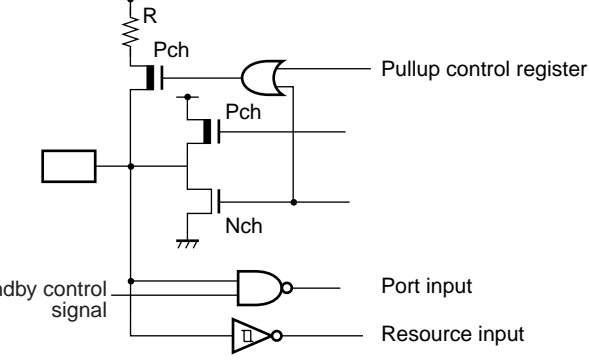
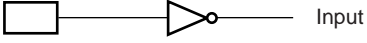
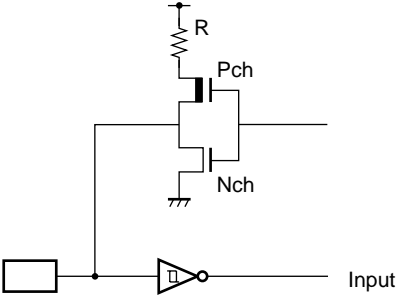
# MB89580B/580BW series

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Pin No.	Pin name	Circuit type	Function
45	P03	B	General-purpose CMOS I/O pin
46	P02	B	General-purpose CMOS I/O pin
47	P01	B	General-purpose CMOS I/O pin
48	P00	B	General-purpose CMOS I/O pin
49	V <sub>cc</sub>	—	Power supply pin
50	C	—	Connect an external capacitor of 0.1 $\mu$ F. When using with 3.3 V power supply, connect this pin with the V <sub>cc</sub> pin to set to 3.3 V input.
51	RPVP	USBDRV	USB route port + pin
52	RPVM	USBDRV	USB router port – pin
53	P60/DI0	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin. (LSB)
54	P61/DI1	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
55	P62/DI2	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
56	P63/DI3	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
57	P64/DI4	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
58	P65/DI5	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
59	P66/DI6	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
60	P67/DI7	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin. (MSB)
61	P40/D0/DO0	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.
62	P41/D1/DO1	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.
63	P42/D2/DO2	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.
64	P43/D3/DO3	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.



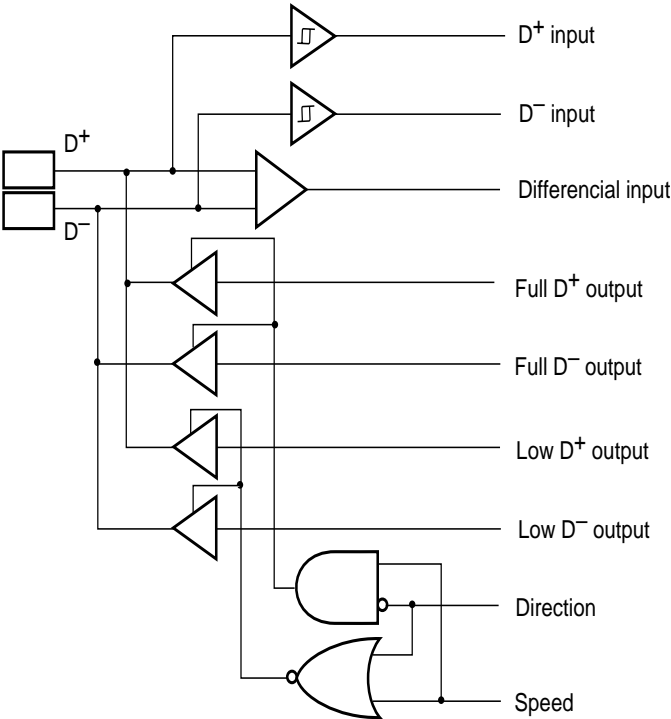
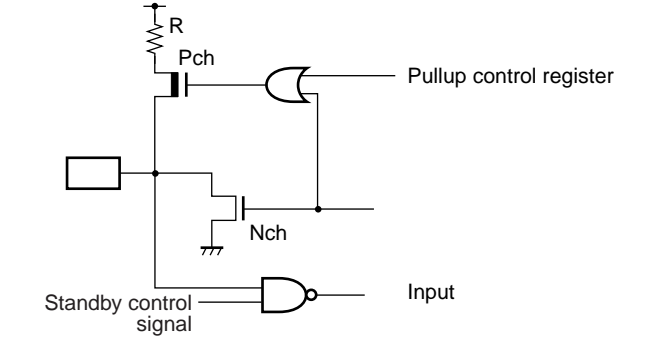
## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 <p style="text-align: center;">Standby control signal</p>	<ul style="list-style-type: none"> <li>• Oscillation feedback resistance : 1 MΩ approx.</li> </ul>
B	 <p style="text-align: center;">Standby control signal</p>	<ul style="list-style-type: none"> <li>• CMOS I/O</li> </ul>
E	 <p style="text-align: center;">Standby control signal</p>	<ul style="list-style-type: none"> <li>• CMOS I/O</li> <li>• Hysteresis input</li> </ul>
F	 <p style="text-align: center;">Input</p>	<ul style="list-style-type: none"> <li>• CMOS input</li> </ul>
I	 <p style="text-align: center;">Input</p>	<ul style="list-style-type: none"> <li>• Hysteresis I/O</li> <li>• Pullup resistance</li> </ul>

(Continued)

# MB89580B/580BW series

(Continued)

Type	Circuit	Remarks
USBDRV	 <p>The circuit diagram for USBDRV shows two input pins, D+ and D-. The D+ input is connected to a buffer and a differential input. The D- input is connected to a buffer and a differential input. The differential input is connected to a differential input. The D+ input is also connected to a full D+ output, a low D+ output, and a direction control signal. The D- input is also connected to a full D- output, a low D- output, and a speed control signal. The direction control signal is connected to a direction control register. The speed control signal is connected to a speed control register.</p>	<ul style="list-style-type: none"> <li>• USB I/O</li> </ul>
K	 <p>The circuit diagram for K shows an input pin connected to a pullup resistor (R) and a pullup control register (Pch). The input pin is also connected to a standby control signal and an input control register. The standby control signal is connected to a standby control register. The input control register is connected to an input control register.</p>	<ul style="list-style-type: none"> <li>• Nch open drain I/O</li> </ul>

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than  $V_{cc}$  or lower than  $V_{ss}$  is applied to input or output pins other than the medium- and high-voltage pins or if voltage higher than the rating is applied between  $V_{cc}$  and  $V_{ss}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also take care to prevent the analog input from exceeding the digital power supply ( $V_{cc}$ ) when the power supply to the analog power system is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions and latchup leading to permanent damage to the pins. These unused pins should be connected to a pullup or pulldown resistance of at least  $2\text{ k}\Omega$  between the pin and the power supply.

Unused I/O pins should be placed in output state to leave it open or pins that are in input state should be handled the same as unused input pins.

### 3. Power Supply Voltage Fluctuations

Although  $V_{cc}$  power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that  $V_{cc}$  ripple fluctuations (P-P value) will be less than 10% of the standard  $V_{cc}$  value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than  $0.1\text{ V/ms}$  at the time of a momentary fluctuation such as when power is switched.

# MB89580B/580BW series

## ■ ONE-TIME PROM AND EPROM MICROCONTROLLER PROGRAMMING SPECIFICATIONS

PROM mode is available on the MB89P585B/BW microcontrollers. The use of a dedicated adapter allows you to program the devices with a general-purpose ROM programmer. However, keep in mind that electronic signature mode is not available.

### 1. ROM programmer adapter and its compatible programmers

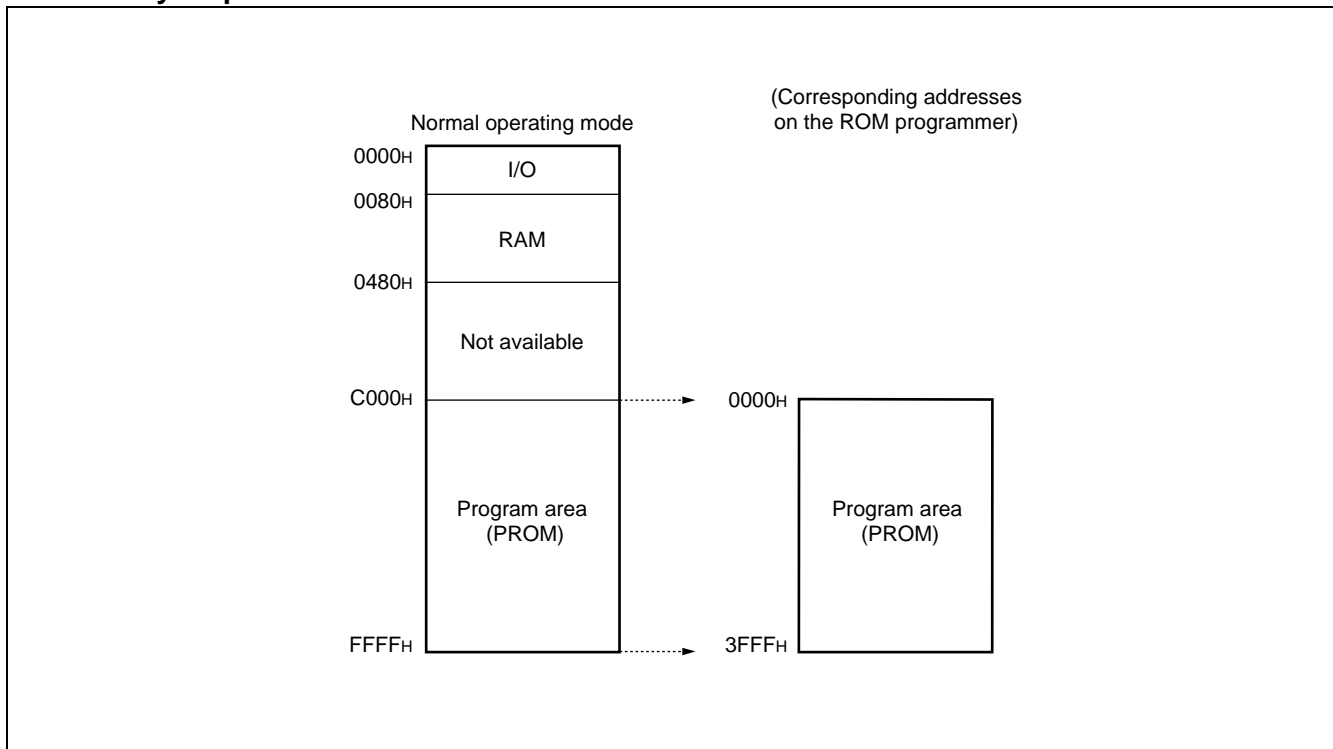
Package	Compatible adapter	Compatible programmers and models
	Sun Hayato Co, Ltd.	Ando Denki K. K.
FTP-64P-M03	ROM2-64LQF-32DP-8LA	AF9708 (Version 1.40 or higher) AF9709 (Version 1.40 or higher) AF9723 (Version 1.50 or higher)
FTP-64P-M09	ROM2-64QF2-32DP-8LA2	

Inquiry:

Sun Hayato Co., Ltd. : TEL. 81-3-3986-0403

Ando Denki K. K. : TEL. 81-3-3733-1160

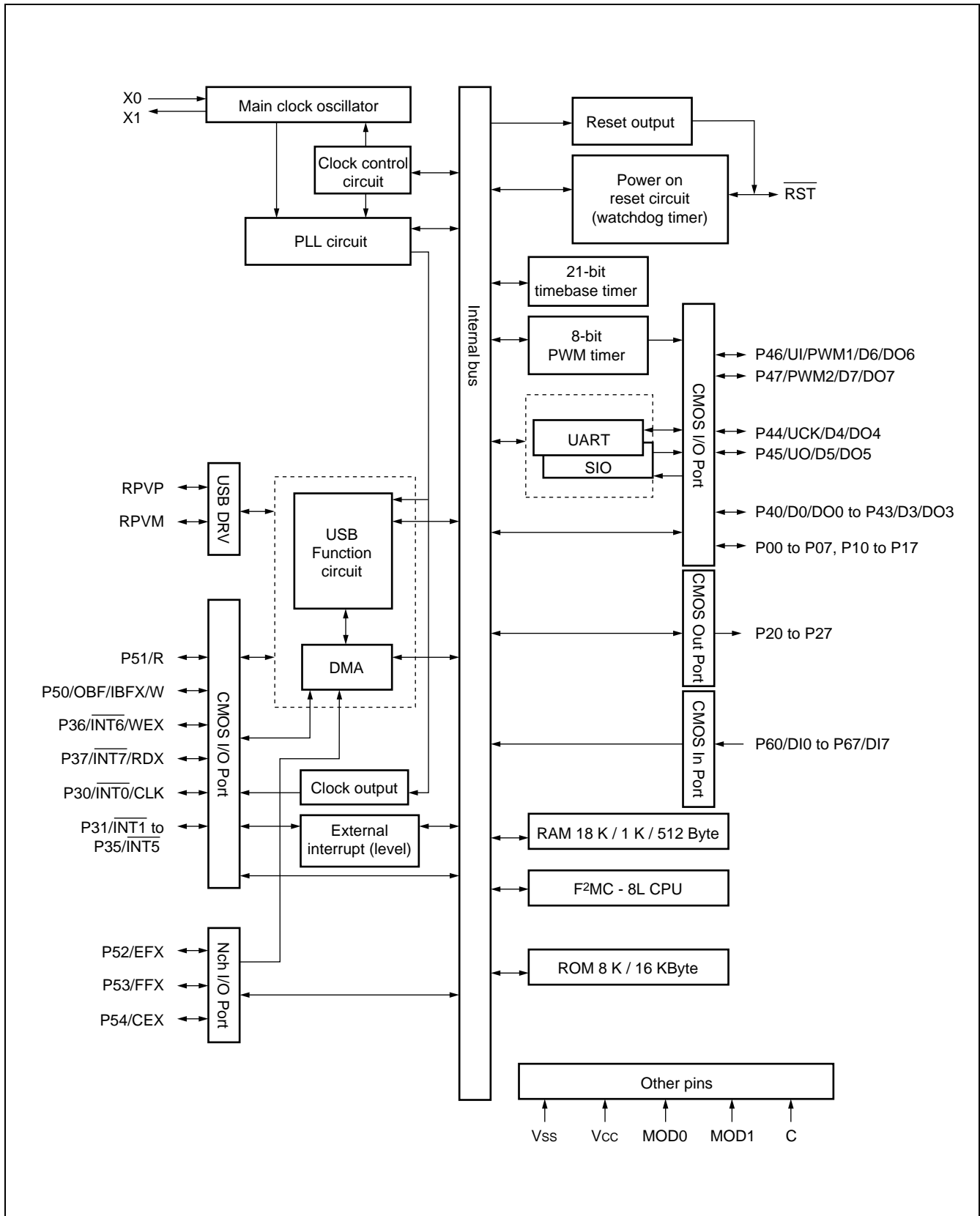
### 2. Memory map in PROM mode



### 3. Programming the EPROM (Using the Ando Denki K.K. programmer)

- (1) Set the EPROM programmer type code to 17209.
- (2) Load program data on to the EPROM programmer at 0000H to 3FFFH.
- (3) Program C000H to FFFFH with the EPROM programmer.

## ■ BLOCK DIAGRAM



# MB89580B/580BW series

## ■ CPU CORE

### 1. Memory Space

The MB89580B/BW microcontrollers offer a memory space of 64 Kbytes consisting of the I/O, RAM and ROM areas. The memory space contains areas that are used for specific purposes, such as a general-purpose register and a vector table.

- I/O area (addresses : 0000H through 007FH)

This area is assigned with the control and data registers, for example, of peripheral functions to be built in. The I/O area is as accessible as the memory since the area is assigned to a part of the memory space. Direct addressing also allows the area to be accessed faster.

- RAM area

As an internal data area, a static RAM is built in.

The internal RAM capacity varies with the product type.

The area 80H to FFH can be accessed at high speed with direct addressing.

The area 100H to 1FFH can be used a general-purpose register area. (The usable area is limited depending on the product.)

When reset, RAM data becomes undefined.

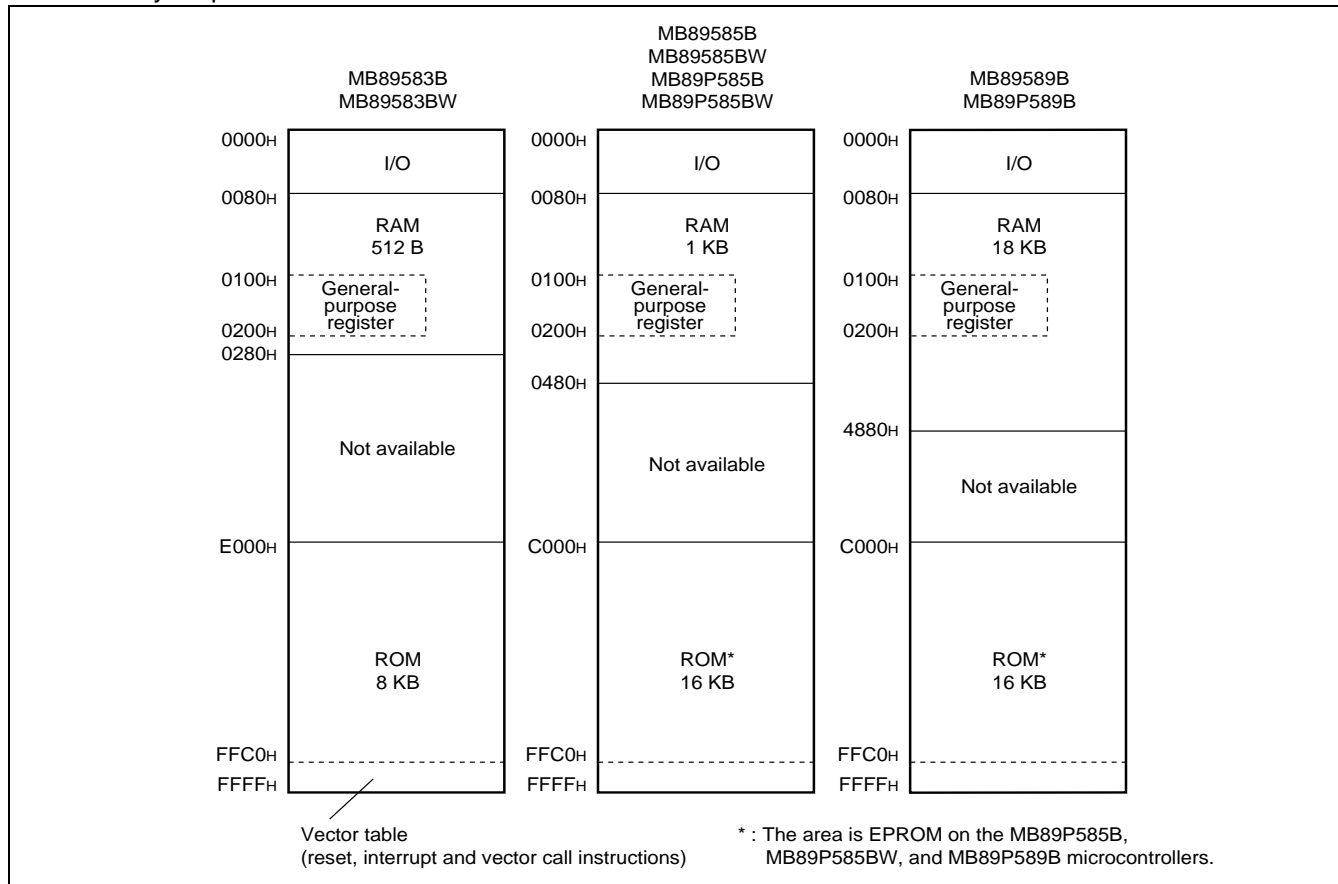
- ROM area

As an internal program area, a ROM is built in.

The internal ROM capacity varies with the product type.

The area FFC0H to FFFFH should be used for a vector table, for example.

- Memory map

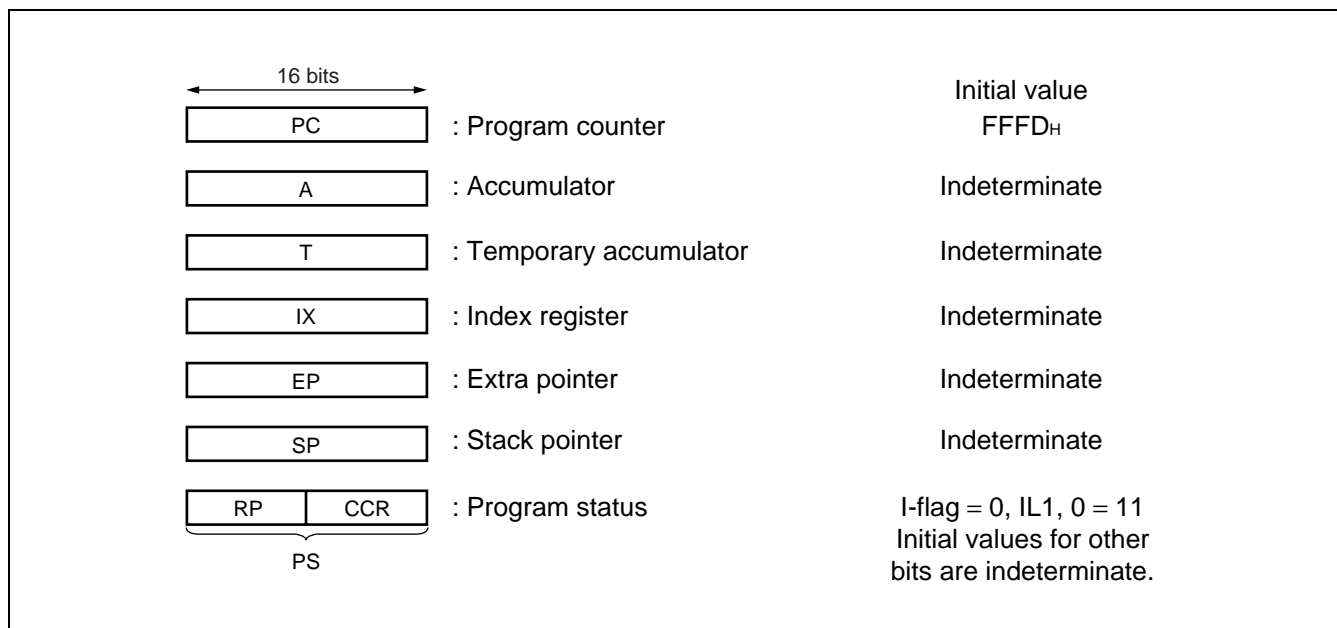


## 2. Registers

The MB89580B/BW series has two types of registers; the registers dedicated to specific purposes in the CPU and the general-purpose registers.

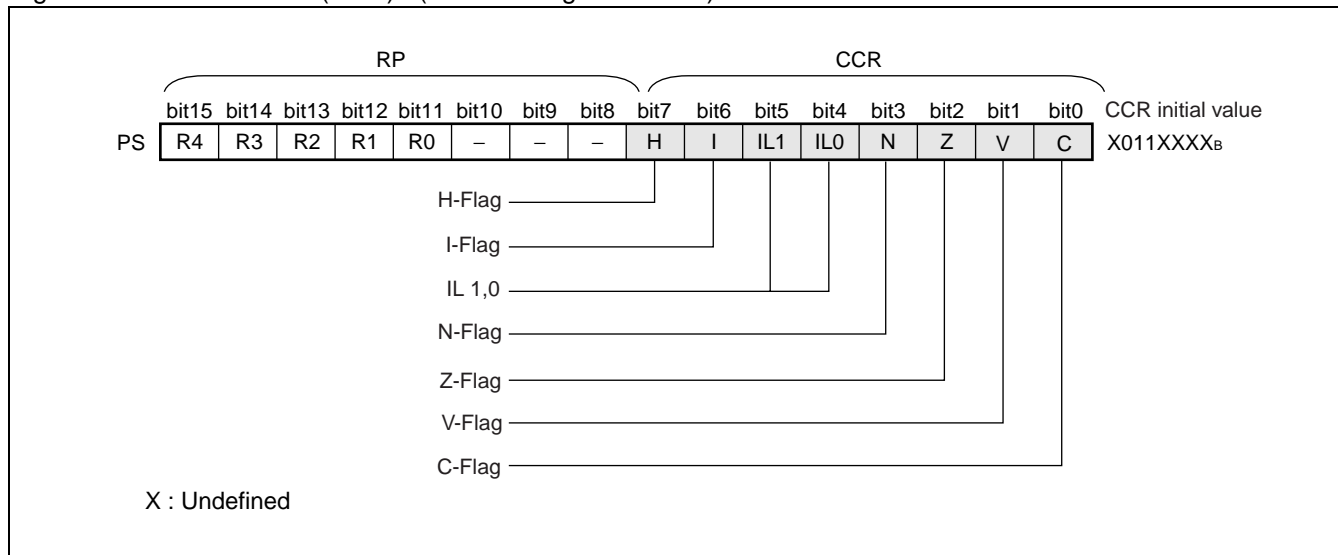
The dedicated registers are as follows:

- Program counter (PC) : A 16-bit register to indicate locations where instructions are stored.
- Accumulator (A) : A 16-bit register for temporary storage of operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
- Temporary accumulator (T) : A 16-bit register which performs operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
- Index register (IX) : A 16-bit register for index modification.
- Extra pointer (EP) : A 16-bit register to point to a memory address.
- Stack pointer (SP) : A 16-bit register to indicate a stack area.
- Program status (PS) : A 16-bit register to store a register pointer or a condition code.

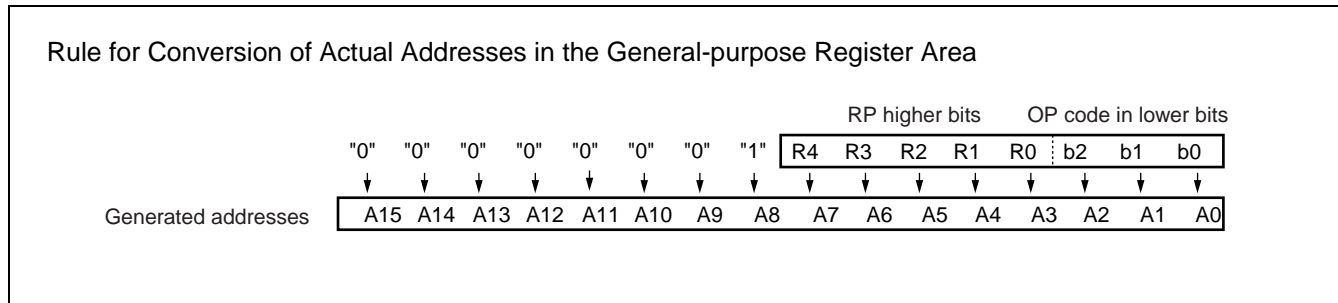


# MB89580B/580BW series

The PS register can further be divided into the register bank pointer in the higher 8 bits (RP) and the condition code register in the lower 8 bits (CCR) . (See the diagram below.)



The RP points to the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule shown next.



The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at the time of an interrupt.

- H flag : The flag is set to "1" when an arithmetic operation results in a carry from bit 3 to bit 4 or in a borrow from bit 4 to bit 3. The bit is cleared to "0" in other instances. The flag is for decimal adjustment instructions; do not use for other than additions and subtractions.
- I flag : Interrupt is enabled when this flag is set to "1." Interrupt is disabled when this flag is set to "0." The flag is set to "0" when reset.
- IL1, 0 : Indicates the level of the interrupt currently enabled. An interrupt is processed only if its level is higher than the value this bit indicates.

IL1	IL0	Interrupt level	High-low
0	0	1	Higher
0	1		
1	0	2	Lower = no interruption
1	1	3	



# MB89580B/580BW series

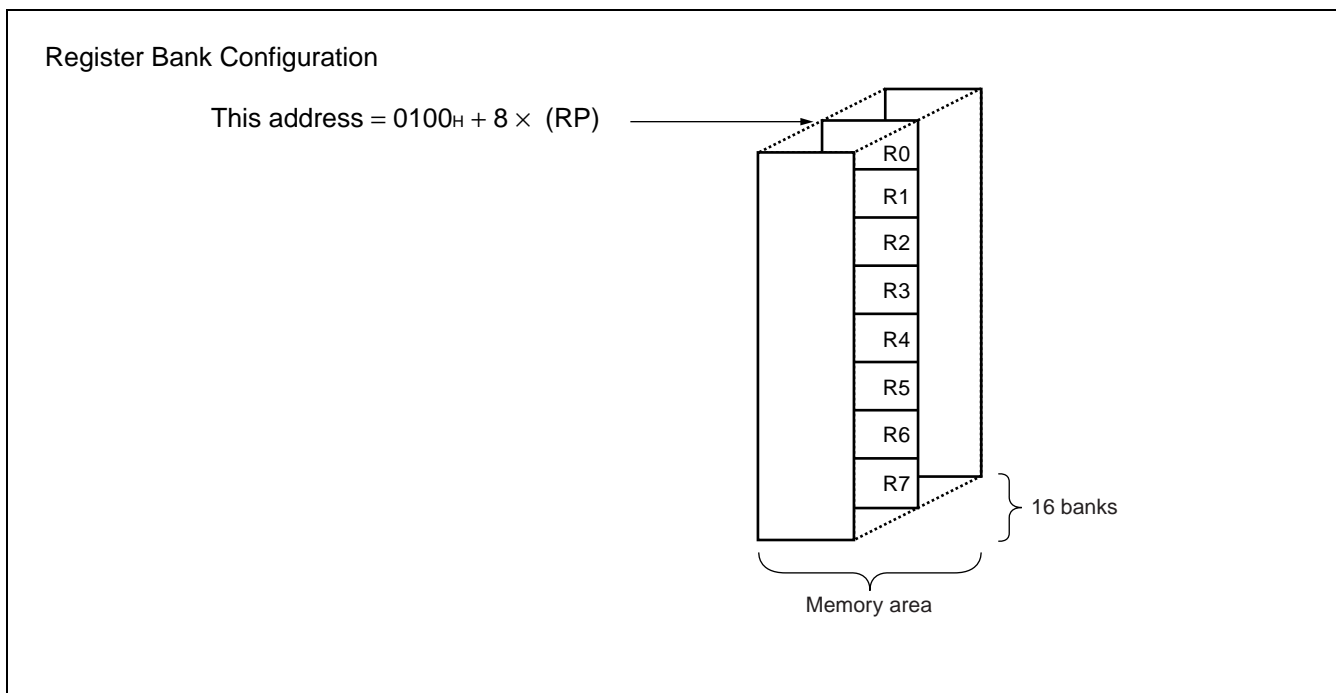
- N flag : The flag is set to "1" when an arithmetic operation results in setting of the MSB to "1" or is cleared to "0" when the MSB is set to "1."
- Z flag : The flag is set to "1" when an arithmetic operation results in "0" or is set to "0" in other instances.
- V flag : The flag is set to "1" when an arithmetic operation results in two's complement overflow or is cleared to "0" if no overflow occurs.
- C flag : The flag is set to "1" when an arithmetic operation results in a carry from bit 7 or in a borrow to bit 7. The flag is cleared to "0" if neither of them occurs. In the case of a shift instruction, the flag is set to the shift-out value.

The following general-purpose registers are provided:

- General-purpose registers : 8-bit data storage registers

The general-purpose registers are 8 bits in length and located in the register banks in the memory. One bank contains eight registers and the MB89580B/BW microcontrollers allow a total of 16 banks to be used at maximum.

The bank currently in use is indicated by the register bank pointer (RP) .



# MB89580B/580BW series

## ■ I/O MAP

Address	Register name	Register description	Read/write	Initial value
00 <sub>H</sub>	PDR0	Port 0 data register	R/W	XXXXXXXX
01 <sub>H</sub>	DDR0	Port 0 direction register	W	00000000
02 <sub>H</sub>	PDR1	Port 1 data register	R/W	XXXXXXXX
03 <sub>H</sub>	DDR1	Port 1 direction register	W	00000000
04 <sub>H</sub>	PDR2	Port 2 data register	R/W	00000000
05 <sub>H</sub>	Vacancy			
06 <sub>H</sub>	Vacancy			
07 <sub>H</sub>	SYCC	System clock control register	R/W	XXX11X00
08 <sub>H</sub>	STBC	Standby control register	R/W	0001XXXX
09 <sub>H</sub>	WDTC	Watchdog timer control register	R/W	0XXXXXXXX
0A <sub>H</sub>	TBTC	Timebase timer control register	R/W	00XXX000
0B <sub>H</sub>	Vacancy			
0C <sub>H</sub>	PDR3	Port 3 data register	R/W	XXXXXXXX
0D <sub>H</sub>	DDR3	Port 3 direction register	R/W	00000000
0E <sub>H</sub>	Vacancy			
0F <sub>H</sub>	Vacancy			
10 <sub>H</sub>	PDR4	Port 4 data register	R/W	XXXXXXXX
11 <sub>H</sub>	DDR4	Port 4 direction register	R/W	00000000
12 <sub>H</sub>	PDR5	Port 5 data register	R/W	XXX111XX
13 <sub>H</sub>	DDR5	Port 5 direction register	R/W	XXXXXX00
14 <sub>H</sub>	PDR6	Port 6 data register	R/W	XXXXXXXX
15 <sub>H</sub>	PDCR	Parallel port data control register	R/W	XXX00000
16 <sub>H</sub> to 20 <sub>H</sub>	Vacancy			
21 <sub>H</sub>	PURR0	Port 0 pullup option setting register	R/W	11111111
22 <sub>H</sub>	PURR1	Port 1 pullup option setting register	R/W	11111111
23 <sub>H</sub>	PURR2	Port 2 pullup option setting register	R/W	11111111
24 <sub>H</sub>	PURR3	Port 3 pullup option setting register	R/W	11111111
25 <sub>H</sub>	PURR4	Port 4 pullup option setting register	R/W	11111111
26 <sub>H</sub>	PURR5	Port 5 pullup option setting register	R/W	XXX11111
27 <sub>H</sub>	CTR1	PWM control register 1	R/W	00000000
28 <sub>H</sub>	CTR2	PWM control register 2	R/W	000X0000
29 <sub>H</sub>	CTR3	PWM control register 3	R/W	X000XXXX
2A <sub>H</sub>	CMR1	PWM compare register 1	W	XXXXXXXX
2B <sub>H</sub>	CMR2	PWM compare register 2	W	XXXXXXXX

(Continued)

# MB89580B/580BW series

Address	Register name	Register description	Read/write	Initial value
2C <sub>H</sub>	CKR	Clock output control register	R/W	XXXXXXXX0
2D <sub>H</sub>	SCS	Serial clock switching register	R/W	XXXXXXXX0
2E <sub>H</sub>	Vacancy			
2F <sub>H</sub>	SMC1	Serial mode control register 1	R/W	00000000
30 <sub>H</sub>	SMC2	Serial mode control register 2	R/W	00000000
31 <sub>H</sub>	SSD	Serial status and control register	R	00001XXX
32 <sub>H</sub>	SIDR/SODR	Serial input/serial output data register	R/W	XXXXXXXXX
33 <sub>H</sub>	SRC	Serial rate control register	R/W	XXXXXXXXX
34 <sub>H</sub> to 3B <sub>H</sub>	Vacancy			
3C <sub>H</sub>	EIE	External interrupt control register	R/W	00000000
3D <sub>H</sub>	EIF	External interrupt flag register	R/W	XXXXXXXX0
3E <sub>H</sub> to 3F <sub>H</sub>	Vacancy			
40 <sub>H</sub>	DMDR	USB power supply mode register	R/W	XXXXXXXX0
41 <sub>H</sub> to 4E <sub>H</sub>	Vacancy			
4F <sub>H</sub>	DBARH	DMA base address register H	R/W	000000XX
50 <sub>H</sub>	UMDR	USB reset mode register	R/W	1000XX00
51 <sub>H</sub>	DBAR	DMA base address register	R/W	XXXXXXXXX
52 <sub>H</sub>	TDCR0	Transfer data count register 0	R/W	X0000000
53 <sub>H</sub>	TDCR11	Transfer data count register 11	R/W	00000000
54 <sub>H</sub>	TDCR12	Transfer data count register 12	R/W	XXXXXX00
55 <sub>H</sub>	TDCR21	Transfer data count register 21	R/W	00000000
56 <sub>H</sub>	TDCR22	Transfer data count register 22	R/W	XXXXXX00
57 <sub>H</sub>	TDCR3	Transfer data count register 3	R/W	X0000000
58 <sub>H</sub>	UCTR	USB control register	R/W	00000000
59 <sub>H</sub>	USTR1	USB status register 1	R/W	00000000
5A <sub>H</sub>	USTR2	USB status register 2	R	XXXXXX00
5B <sub>H</sub>	UMSKR	USB interrupt mask register	R/W	00000000
5C <sub>H</sub>	UFRMR1	USB frame status register 1	R	XXXXXXXXX
5D <sub>H</sub>	UFRMR2	USB frame status register 2	R	XXXXXXXXX
5E <sub>H</sub>	EPER	USB endpoint enable register	R/W	XXXX0001
5F <sub>H</sub>	EPBR0	Endpoint 0 setup register	R/W	X0000000
60 <sub>H</sub>	EPBR11	Endpoint setup register 11	R/W	0X000000
61 <sub>H</sub>	EPBR12	Endpoint setup register 12	R/W	00000000

(Continued)

# MB89580B/580BW series

(Continued)

Address	Register name	Register description	Read/write	Initial value
62 <sub>H</sub>	EPBR21	Endpoint setup register 21	R/W	0X000000
63 <sub>H</sub>	EPBR22	Endpoint setup register 22	R/W	00000000
64 <sub>H</sub>	EPBR31	Endpoint setup register 31	R/W	XX0000XX
65 <sub>H</sub>	EPBR32	Endpoint setup register 32	R/W	X0000000
66 <sub>H</sub> to 7B <sub>H</sub>	Vacancy			
7C <sub>H</sub>	ILR1	Interrupt level setting register 1	W	11111111
7D <sub>H</sub>	ILR2	Interrupt level setting register 2	W	11111111
7E <sub>H</sub>	ILR3	level setting register 3	W	11111111
7F <sub>H</sub>	Vacancy			
<ul style="list-style-type: none"> <li>• Information about read/write R/W : Read/write enabled, R : Read only, W : Write only</li> <li>• Information about initial values 0 : The initial value of this bit is "0". 1 : The initial bit of this bit is "1". X : The initial value of this bit is undefined.</li> </ul>				

Note : Vacancies are not for use.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
Input voltage	$V_I$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Other than P60 to P67
		$V_{SS} - 0.5$	$V_{SS} + 4.0$	V	P60 to P67
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
"L" level average output current	$I_{OLAV}$	—	4	mA	Average value (operating current × operating rate)
"L" level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
"L" level total average output current	$\Sigma I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	$I_{OH}$	—	-15	mA	
"H" level average output current	$I_{OHAV}$	—	-4	mA	Average value (operating current × operating rate)
"H" level total maximum output current	$\Sigma I_{OH}$	—	-50	mA	
"H" level total average output current	$\Sigma I_{OHAV}$	—	-20	mA	Average value (operating current × operating rate)
Power consumption	$P_D$	—	300	mW	
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB89580B/580BW series

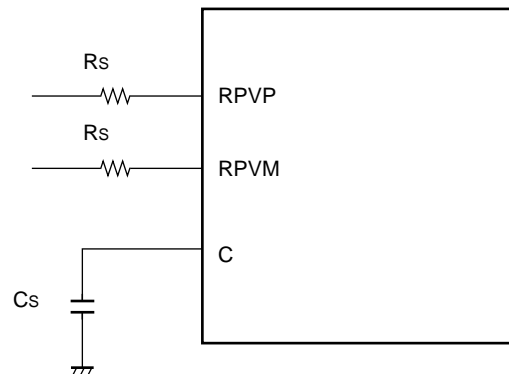
## 2. Recommended Operating Conditions

( $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}$	3.0	—	5.5	V	
Operating temperature	$T_A$	-40	—	+85	°C	
Smoothing capacitor	$C_S$	0.1	—	1.0	$\mu\text{F}$	At $V_{CC} = 5.0\text{ V}^*$
Series resistance	$R_S$	—	16	—	$\Omega$	When the USB function is in use

\* : Use either a ceramic capacitor or a capacitor with similar frequency characteristics. The capacity of the smoothing capacitor for the  $V_{CC}$  pin should be greater than that of the  $C_S$ . When using with a supply voltage of 3.3 V, connect pin C with  $V_{CC}$  to input 3.3 V.

- C, RPVP and RPVM Pin Connection Diagram



# MB89580B/580BW series

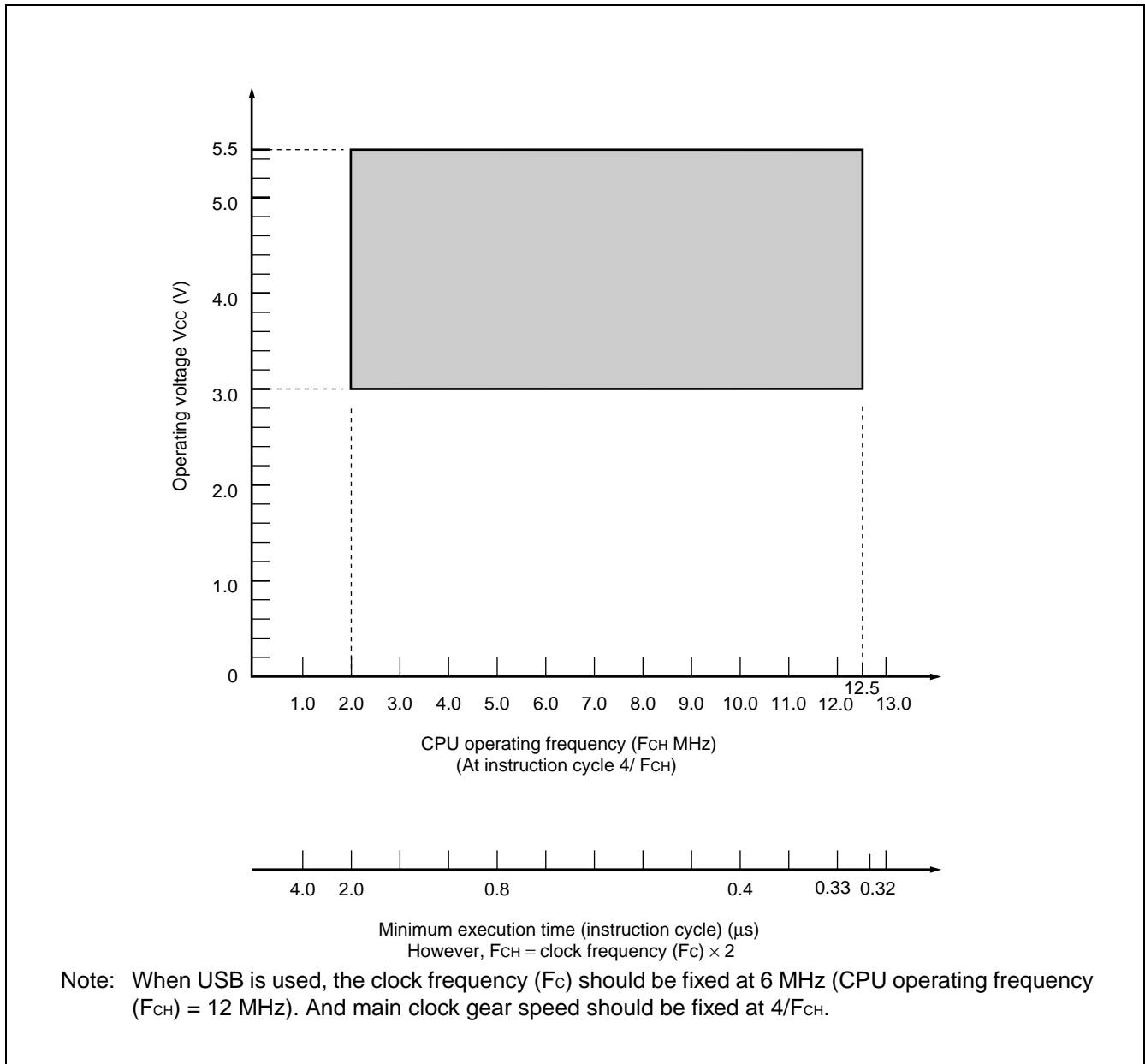


Figure 1 Operating voltage - operating frequency

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB89580B/580BW series

## 3. DC Characteristics

( $V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, MOD0, MOD1	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	$V_{IHS}$	$\overline{RST}$ , $\overline{INT0}$ to $\overline{INT7}$ , UCK, UI	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	$V_{IH1}$	P60 to P67	—	$V_{SS} + 2.0$	—	$V_{SS} + 3.6$	V	
"L" level input voltage	$V_{IL}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, MOD0, MOD1	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	$V_{ILS}$	$\overline{RST}$ , $\overline{INT0}$ to $\overline{INT7}$ , UCK, UI	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
	$V_{IL1}$	P60 to P67	—	$V_{SS} - 0.5$	—	$V_{SS} + 0.8$	V	
Open-drain output application voltage	$V_{D1}$	P52 to P54	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
"H" level output voltage	$V_{OH}$	P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50, P51	$I_{OH} = -2.0\text{ mA}$	4.0	—	—	V	
"L" level output voltage	$V_{OL}$	P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P54, $\overline{RST}$	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	

(Continued)



# MB89580B/580BW series

(Continued)

( $V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current (Hi-Z output leakage current)	$I_{LI}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50, P51, P60 to P67	$0.0 < V_i < V_{CC}$	-5	—	+5	$\mu\text{A}$	When no pullup resistance is specified
Open-drain output leakage current	$I_{LIOD}$	P52 to P54	$0.0 < V_i < V_{SS} + 5.5$	—	—	+5	$\mu\text{A}$	
Pullup resistance	$R_{PULL}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, $\overline{\text{RST}}$	$V_i = 0.0\text{ V}$	25	50	100	$\text{k}\Omega$	$\overline{\text{RST}}$ is excluded when pullup resistance available is specified.
Power supply current	$I_{CC}$	$V_{CC}$	$F_{CH} = 12.0\text{ MHz}$ $V_{CC} = 5.0\text{ V}$ $t_{inst} = 0.333\text{ }\mu\text{s}$	—	25	38	$\text{mA}$	MB89P585B/BW, MB89585B/BW, MB89583B/BW MB89P589B, MB89589B
	$I_{CCS1}$		$F_{CH} = 12.0\text{ MHz}$ $V_{CC} = 5.0\text{ V}$ $t_{inst} = 0.333\text{ }\mu\text{s}$	—	20	30	$\text{mA}$	Sleep mode
	$I_{CCH}$		$T_A = 25\text{ }^{\circ}\text{C}$	—	5	20	$\mu\text{A}$	Stop
Input capacitance	$C_{IN}$	Other than $V_{CC}$ and $V_{SS}$	$f = 1\text{ MHz}$	—	10	—	$\text{pF}$	

# MB89580B/580BW series

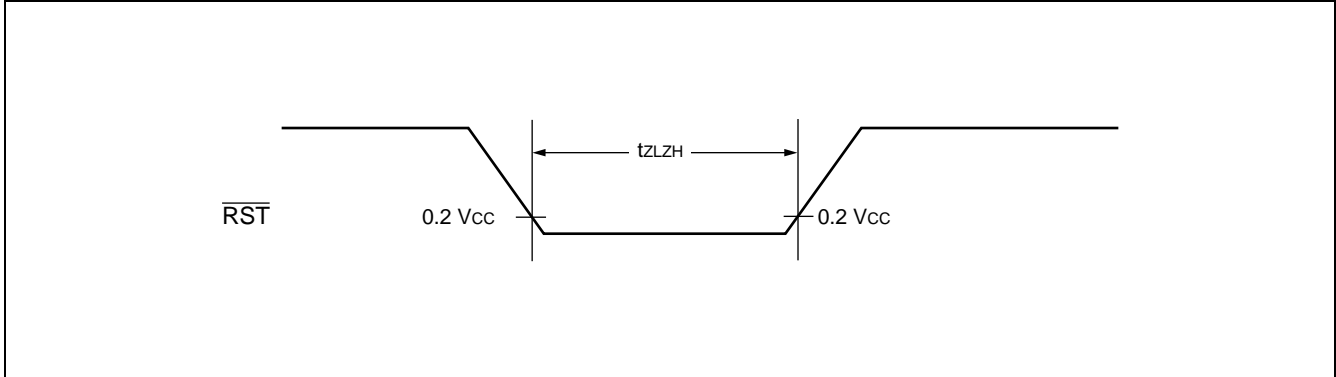
## 4. AC Characteristics

### (1) Reset Timing

( $V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{\text{RST}}$ "L" pulse width	$t_{\text{ZLZH}}$	—	$48 t_{\text{HCLY}}$	—	ns	

Note :  $t_{\text{HCLY}}$  is the internal main clock oscillating cycle ( $1/2 F_c$ ) .



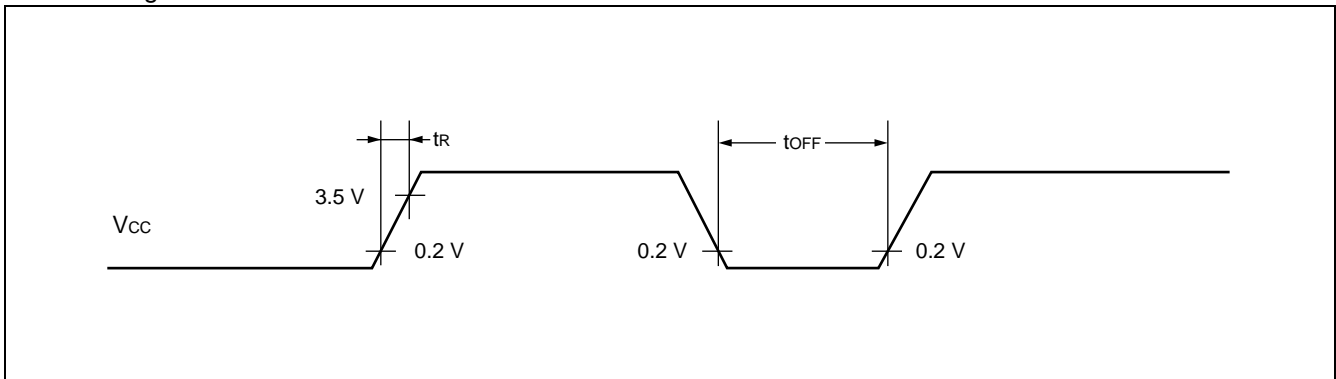
### (2) Power-on Reset and Power On Time

( $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_{\text{R}}$	—	0.066	50	ms	
Power supply cutoff time	$t_{\text{OFF}}$	—	4	—	ns	Due to repeated operations

Note : The power supply must be up within the selected oscillation stabilization time.

When the supply voltage needs to be varied while operating, it is recommended to smoothly start up the voltage.



# MB89580B/580BW series

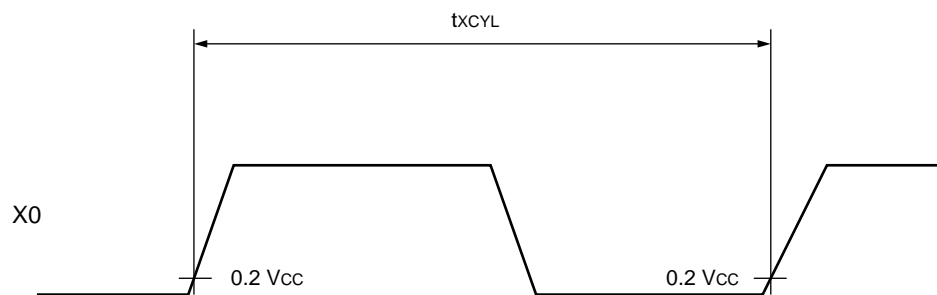
## (3) Clock Timing

( $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	$F_C$	X0, X1	—	1	6	6.25	MHz	
Clock cycle time	$t_{XCYL}$	X0, X1		160	166.6	1000	ns	
Internal main clock frequency	$F_{CH}$	—		2	12	12.5	MHz	Twice the $F_C$
Internal clock cycle	$t_{HCYL}$	—		80	83.3	500	ns	$t_{XCYL}/2$

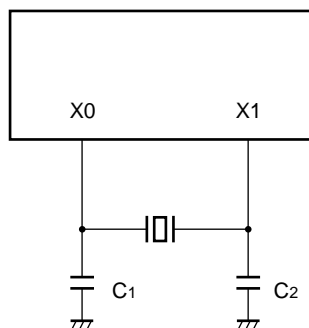
Note: When USB is used, the clock frequency ( $F_C$ ) should be fixed at 6 MHz (CPU operating frequency ( $F_{CH}$ ) = 12 MHz). And main clock gear speed should be fixed at  $4/F_{CH}$ .

### • X0 and X1 Timing and Conditions



### • Clock Conditions

When a crystal resonator is used



## (4) Instruction Cycle

( $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (Min execution time)	$t_{inst}$	$4 / F_{CH}$ , $8 / F_{CH}$ , $16 / F_{CH}$ , $64 / F_{CH}$	$\mu\text{s}$	When operating at $F_{CH} = 12\text{ MHz}$ $t_{inst} = 0.33\text{ } \mu\text{s}$ ( $4 / F_{CH}$ )

# MB89580B/580BW series

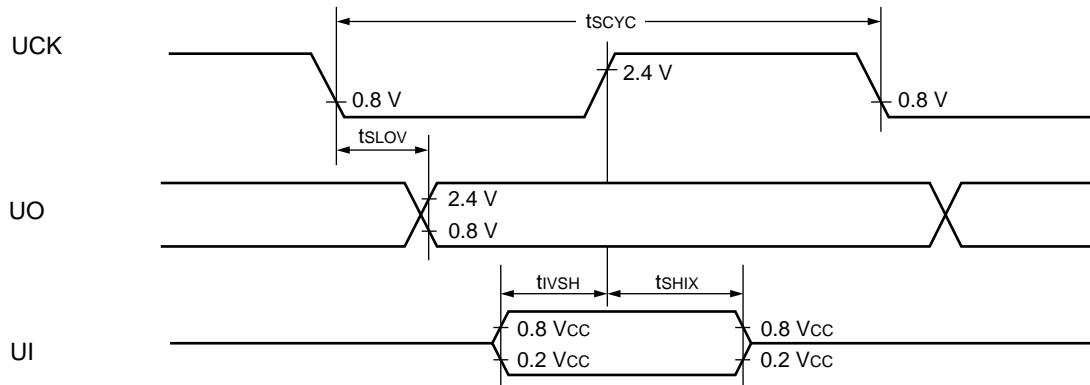
## (5) UART Serial I/O Timing

( $V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

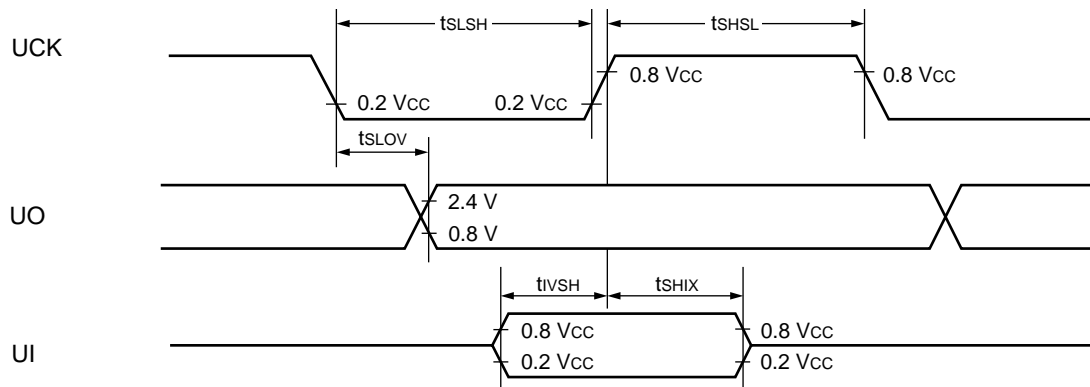
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	UCK	Internal shift clock mode	$2 t_{inst}^*$	—	$\mu\text{s}$	
UCK $\downarrow \rightarrow$ UO	$t_{SLOV}$	UCK, UO		-200	200	ns	
Valid UI $\rightarrow$ UCK $\uparrow$	$t_{VSH}$	UI, UCK		200	—	ns	
UCK $\uparrow \rightarrow$ valid UI hold time	$t_{SHIX}$	UCK, UI		200	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	UCK	External shift clock mode	$1 t_{inst}^*$	—	$\mu\text{s}$	
Serial clock "L" pulse width	$t_{SLSH}$			$1 t_{inst}^*$	—	$\mu\text{s}$	
UCK $\downarrow \rightarrow$ UO time	$t_{SLOV}$	UCK, UO		0	200	ns	
Valid UI $\rightarrow$ UCK $\uparrow$	$t_{VSH}$	UI, UCK		200	—	ns	
UCK $\uparrow \rightarrow$ valid UI hold time	$t_{SHIX}$	UCK, UI	200	—	ns		

\* : For information about  $t_{inst}$ , see "Instruction Cycle."

### • Internal shift clock mode



### • External shift clock mode



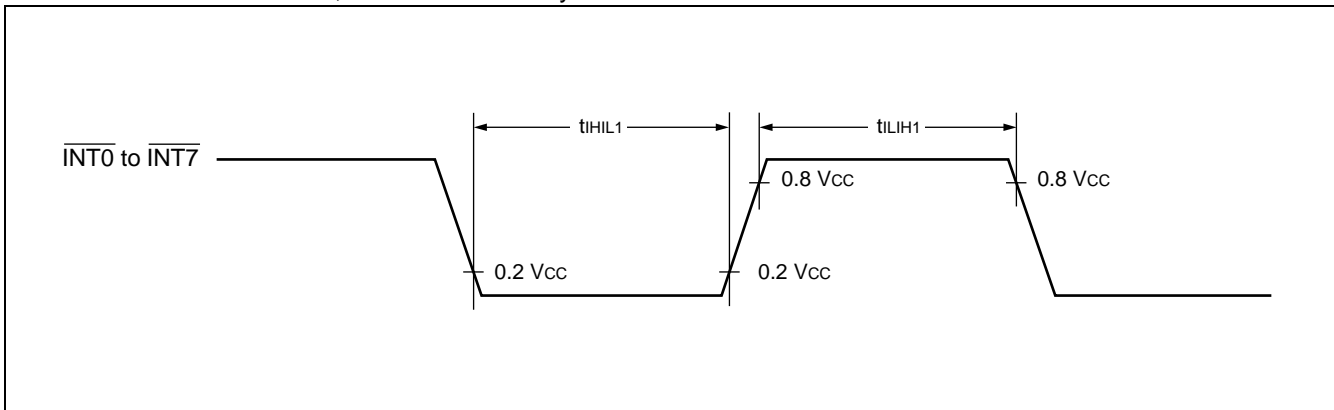
# MB89580B/580BW series

## (6) Peripheral Input Timing

( $V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Peripheral input "H" pulse width 1	$t_{LIH1}$	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	—	$2 t_{inst}^*$	—	$\mu\text{s}$	
Peripheral input "L" pulse width 1	$t_{HIL1}$		—	$2 t_{inst}^*$	—	$\mu\text{s}$	

\* : For information about  $t_{inst}$ , see "Instruction Cycle."



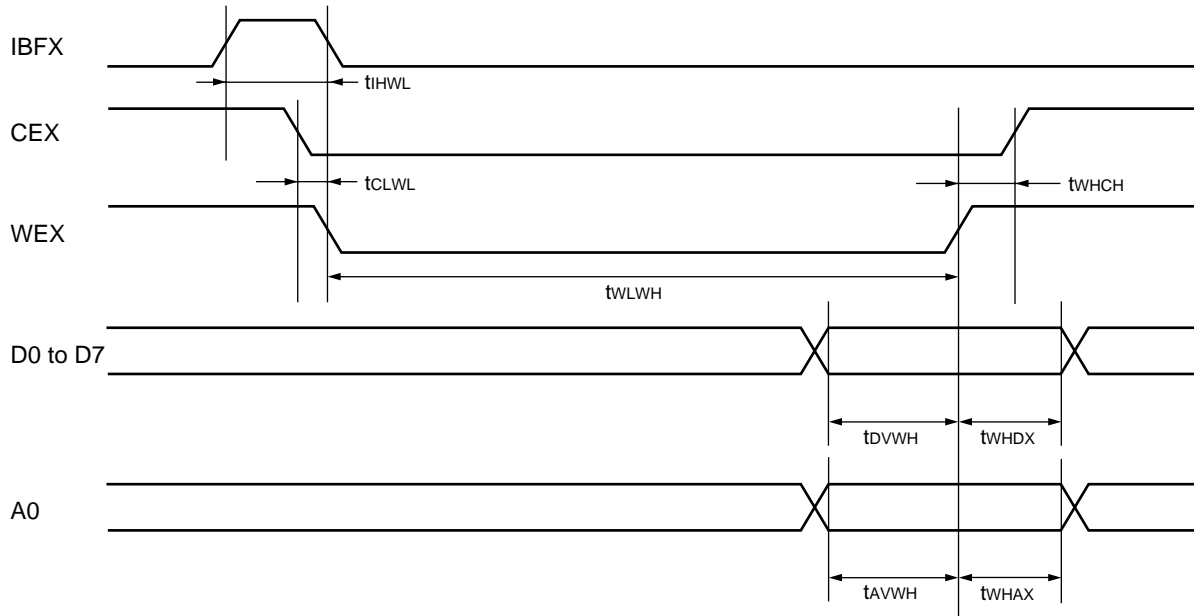
# MB89580B/580BW series

## (7) Parallel Port Timing

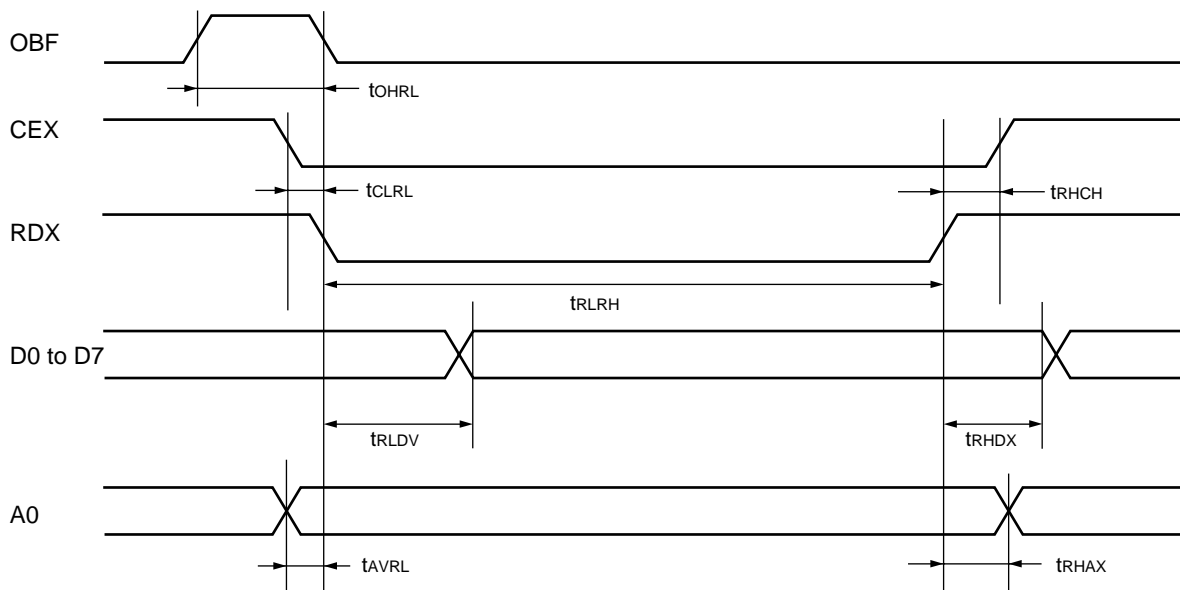
(V<sub>CC</sub> = 5.0 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
IBFX ↑ → WEX ↓ timing	t <sub>IHWL</sub>	IBFX WEX	—	1 / 2 • t <sub>inst</sub>	—	μs	
CEX ↓ → WEX ↓ delay	t <sub>CLWL</sub>	CEX WEX	—	0	—	ns	
WEX ↑ → CEX ↑ delay	t <sub>WHCH</sub>	CEX WEX	—	0	—	ns	
WEX pulse width	t <sub>WLWH</sub>	WEX	—	40	—	ns	
Write data setup	t <sub>DVWH</sub>	D0 to D7 WEX	—	10	—	ns	
Write data hold	t <sub>WHDX</sub>	D0 to D7 WEX	—	10	—	ns	
Write address setup	t <sub>AVWH</sub>	A0 WEX	—	10	—	ns	
Write address hold	t <sub>WHAX</sub>	A0 WEX	—	10	—	ns	
OBF ↑ → RDX ↓ timing	t <sub>OHRL</sub>	OBF RDX	—	1 / 2 • t <sub>inst</sub>	—	μs	
CEX ↓ → RDX ↓ delay	t <sub>CLRL</sub>	CEX RDX	—	0	—	ns	
RDX ↑ → CEX ↑ delay	t <sub>RHCH</sub>	CEX RDX	—	0	—	ns	
RDX pulse width	t <sub>RLRH</sub>	RDX	—	40	—	ns	
Read data delay	t <sub>RLDV</sub>	D0 to D7 RDX	—	—	15	ns	
Read data hold	t <sub>RHDX</sub>	D0 to D7 RDX	—	0	—	ns	
Read address setup	t <sub>AVRL</sub>	A0 RDX	—	10	—	ns	
Read address hold	t <sub>RHAX</sub>	A0 RDX	—	10	—	ns	

## • Write Timing



## • Read Timing



# MB89580B/580BW series

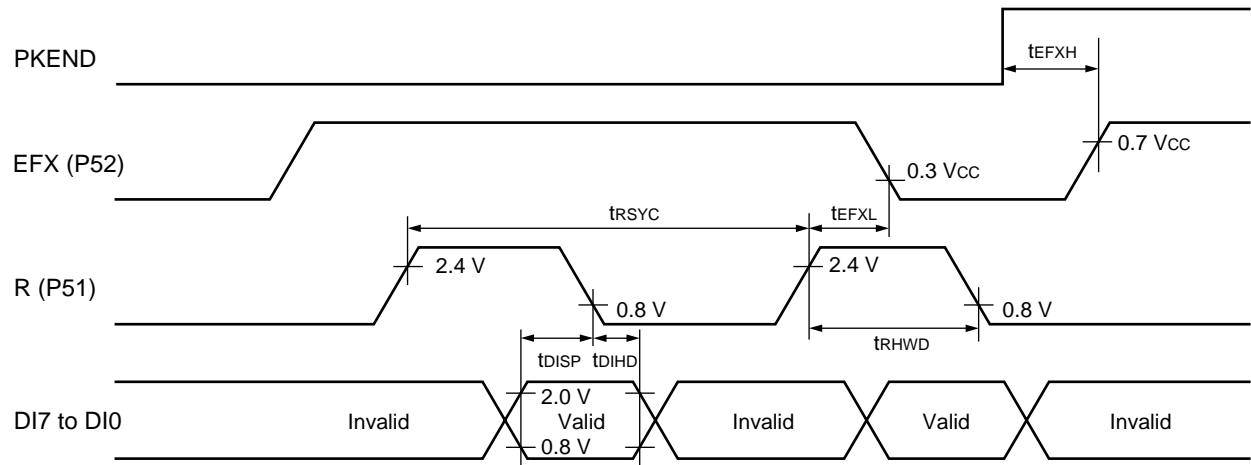
## (8) External FIFO Connection Timing

( $V_{CC} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $F_C = 6\text{ MHz}$ )

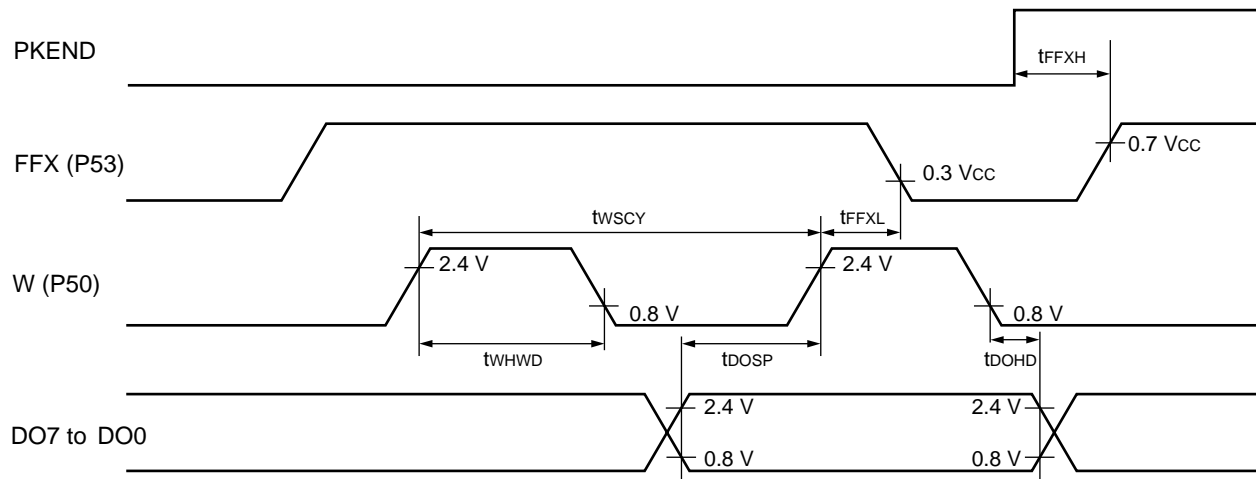
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
FIFO empty resetting timing	$t_{EFXH}$	EFX	Not including the initial resetting after reset	0	—	ns	Resetting before PKEND is not allowed.
FIFO empty timing	$t_{EFXL}$	EFX, R	—	0	360	ns	
Read cycle time	$t_{RSCY}$	R	—	645	—	ns	
Read clock "H" pulse width	$t_{RHWD}$		—	145	—	ns	
Valid DI $\rightarrow$ R $\downarrow$ setup time	$t_{DISP}$	DI7 to DI0, R	—	50	—	ns	
R $\downarrow$ $\rightarrow$ valid DI hold time	$t_{DIHD}$		—	0	—	ns	
FIFO full reset timing	$t_{FFXH}$	FFX	—	0	—	ns	Resetting before PKEND is not allowed.
FIFO full timing	$t_{FFXL}$	FFX, W	—	0	360	ns	
Write recycle time	$t_{WSCY}$	W	—	645	—	ns	
Write clock "H" pulse width	$t_{WHWD}$		—	145	—	ns	
Valid DO $\rightarrow$ W $\uparrow$ setup time	$t_{DOSP}$	DO7 to DO0, W	—	200	—	ns	
W $\downarrow$ $\rightarrow$ valid DO hold time	$t_{DOHD}$		—	40	—	ns	



- Read Data from External FIFO



- Write Data to External FIFO



# MB89580B/580BW series

## ■ ORDERING INFORMATION

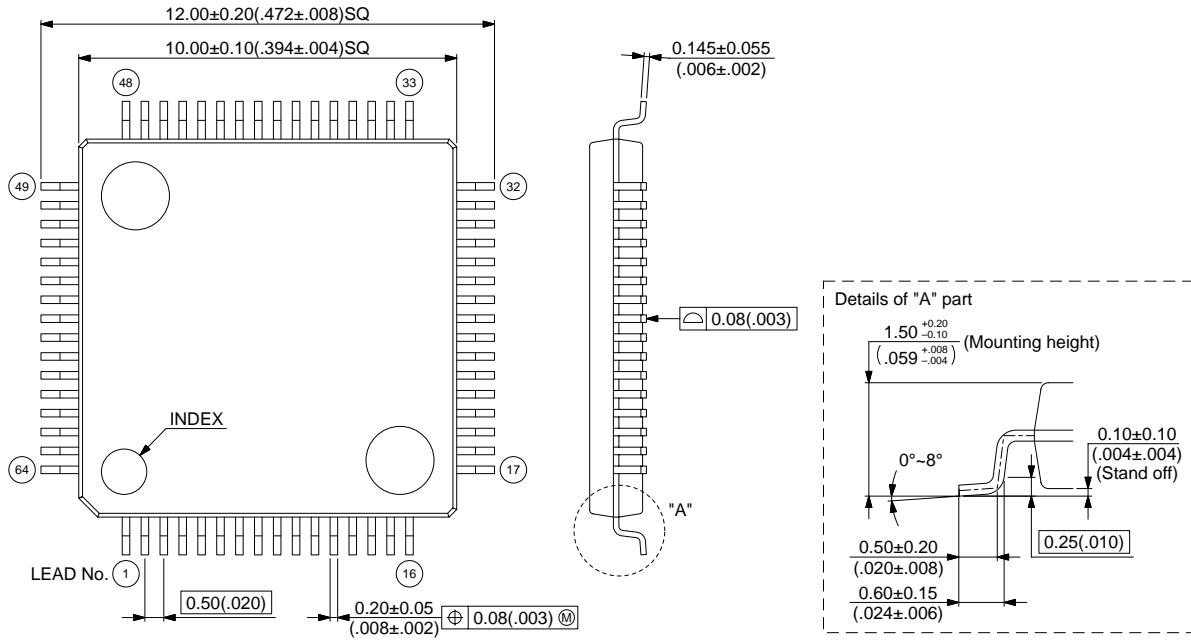
Part number	Package	Remarks
MB89589BPFM MB89P589BPFM	64-pin plastic LQFP (FPT-64P-M09)	
MB89583BPFV MB89585BPFV MB89P585BPFV MB89583BWPFV MB89585BWPFV MB89P585BWPFV	64-pin plastic LQFP (FPT-64P-M03)	

# MB89580B/580BW series

## ■ PACKAGE DIMENSIONS

64-pin plastic LQFP  
(FPT-64P-M03)

Note: Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches)

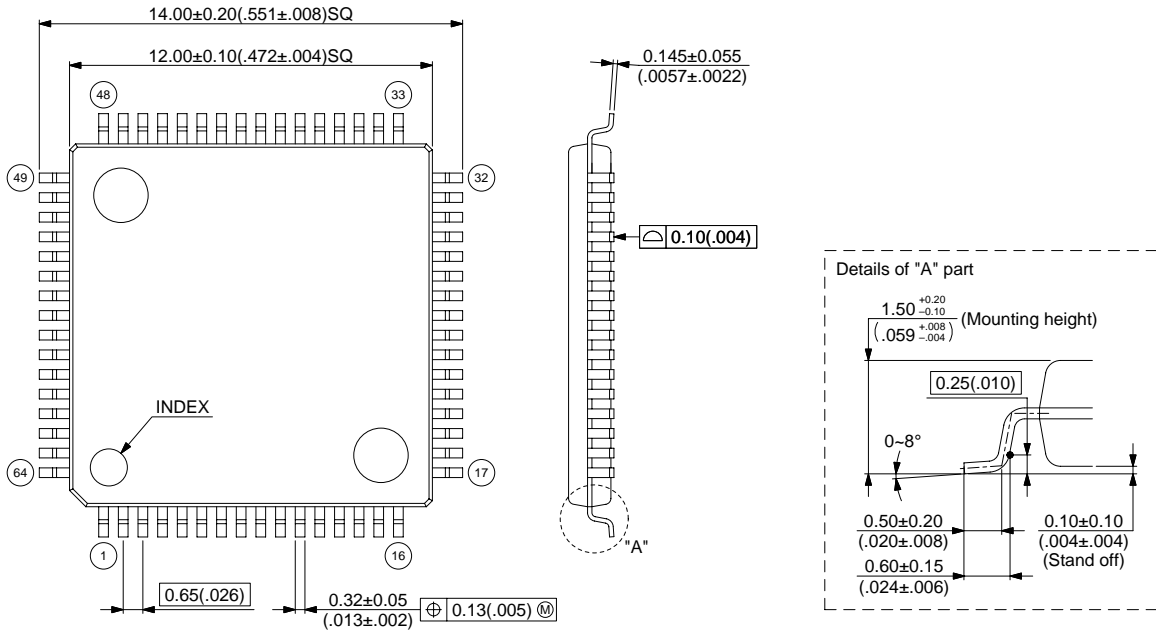
(Continued)

# MB89580B/580BW series

(Continued)

64-pin plastic LQFP  
(FPT-64P-M09)

Note: Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches)

# MB89580B/580BW series

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