FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12507-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89810A Series

MB89816A/P817A

■ DESCRIPTION

The MB89810A series is a line of single-chip microcontrollers based on the F²MC*-8L CPU core which can operate at low voltage but at high speed. The microcontrollers contain peripheral function such as timer, serial interface, a UART, and an external interrupt. The MB89810A series is applicable to a wide range of applications from welfare products to industrial equipment, including portable devices.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

High speed processing at low voltage
Minimum execution time: 0.8 µs/3.0 V, 1.33 µs/2.2 V

- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Four types of timers
  8-bit PWM timer: 2 channels (also serve as reload timers)
  16-bit timer/counter
  21-bit time-base timer
- Two serial interface
  8-bit synchronous serial (Switchable transfer direction allows communication with various equipment.)
  UART (5-, 7-, or 8-bit transfer capable)

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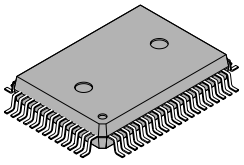
■ PACKAGE

64-pin Plastic QFP



(FPT-64P-M06)

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- External interrupt: 8 channels
  Eight channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal)

■ PRODUCT LINEUP

Parameter \ Part number	MB89816A	MB89P817A
Classification	Mass-production product (mask ROM products)	One-time PROM product (for evaluation and development)
ROM size	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)
RAM size	2048 × 8 bits	
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.8 µs/5 MHz Interrupt processing time: 7.2 µs/5 MHz	
Ports	Input ports: 8 (All also serve as peripherals.) Output ports: 8 I/O ports (N-ch open-drain): 5 (for LED driving) I/O ports (CMOS): 32 (14 ports also serve as peripherals.) Total: 53	
8-bit PWM timer	Two internal channels 8-bit reload timer operation (toggled output capable, operating clock cycle: 3 different cycles) 8-bit resolution PWM operation (conversion cycle: 3 different cycles)	
8-bit timer/counter	16-bit timer operation 16-bit event counter operation	
UART	5-, 7-, or 8-bit transfer capable Built-in baud rate generator Clock synchronous/asynchronous data transfer capable	
8-bit Serial I/O	8-bits LSB-first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks)	
External interrupt	8 independent channels (edge selection, interrupt vector, source flag) 4 channels: Level detection (level selectable) 4 channels: Edge detection (edge selectable) Used also for wake-up from the stop/sleep mode. (Edge detection is also permitted in stop mode.)	

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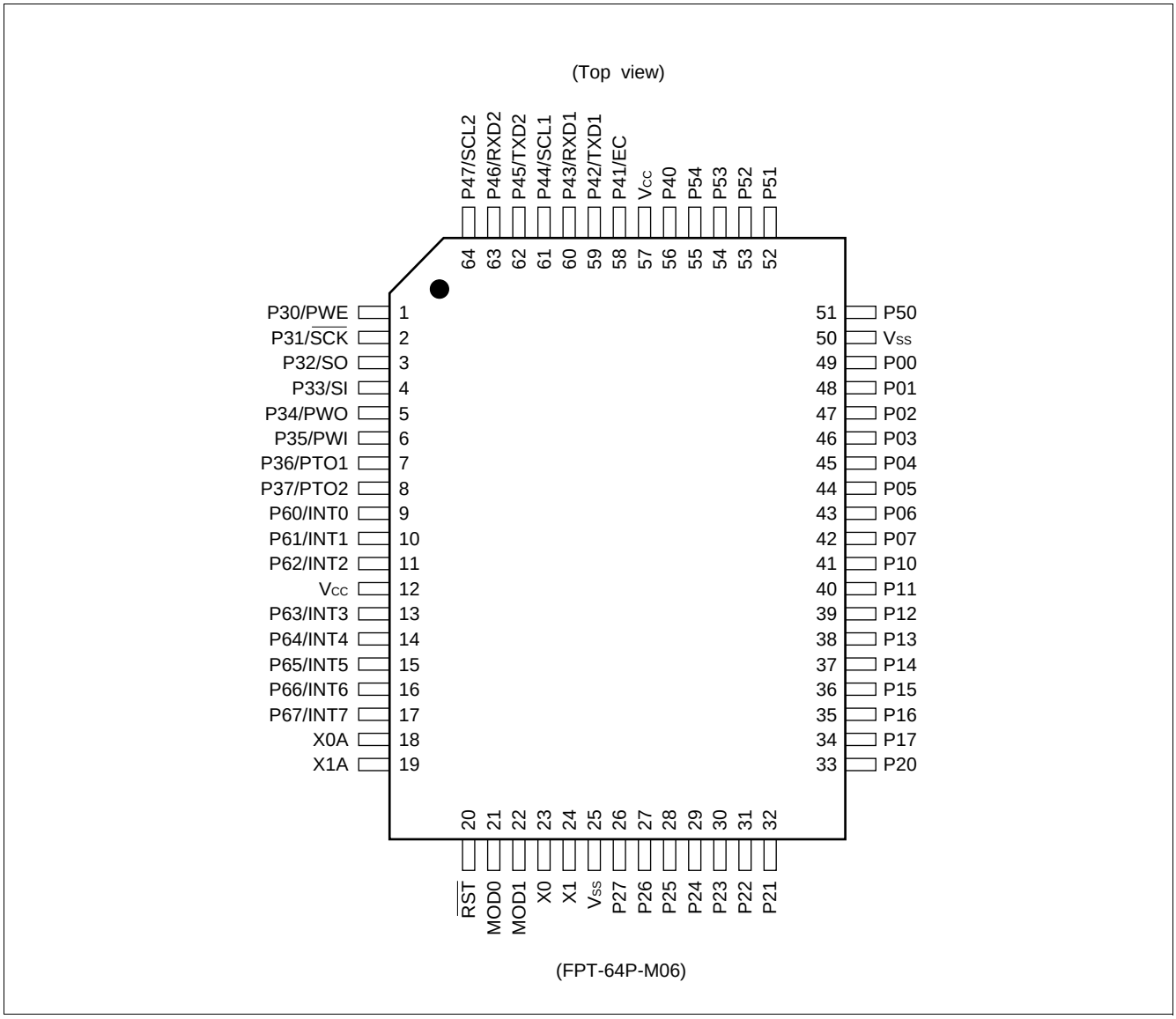
Part number / Parameter	MB89816A	MB89P817A
Watch interrupt	Interrupt cycles: 4 different cycles (subclock)	
Watchdog timer reset	Reset occurrence cycle: 839 ms/5 MHz	
Standby mode	Sleep mode, stop mode	
Process	CMOS	
Package	FPT-64P-M06	
Operating voltage	2.2 V to 6.0 V*	2.7 V to 6.0 V*

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
23	X0	A	Main clock oscillator pins
24	X1		
18	X0A	I	Subclock crystal oscillator pins
19	X1A		
21	MOD0	B	Operating mode selection pins Connect directly these pins directly to V_{SS}.
22	MOD1		
20	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
49 to 42	P00 to P07	D	General-purpose I/O ports A pull-up resistor option is provided. These ports have the port output inverting function.
41 to 34	P10 to P17	D	General-purpose I/O ports A pull-up resistor option is provided. These ports have the port output inverting function.
33 to 30	P20 to P23	F	General-purpose output ports These ports have the port output inverting function.
29 to 26	P24 to P27	F	General-purpose output ports
1	P30 /PWE	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a pulse width detection enable input (PWE). PWE input is hysteresis input.
2	P31/$\overline{SCK}$	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the clock I/O for the 8-bit serial I/O (SCK). SCK input is hysteresis input.
3	P32/SO	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data output for the 8-bit serial I/O (SO).
4	P33/SI	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data input for the 8-bit serial I/O (SI). SI input is hysteresis input.
5	P34/PWO	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as a pulse width detection output (PWO).
6	P35/PWI	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a pulse width detection input (PWI). PWI input is hysteresis input.
7	P36/PTO1	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as the toggle output for the 8-bit PWM timer 1 (PTO1).

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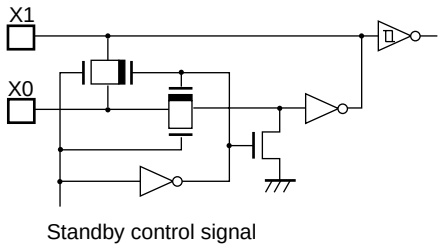
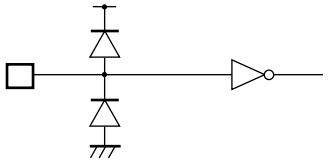
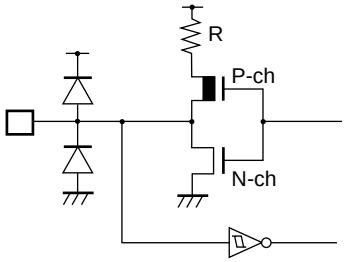
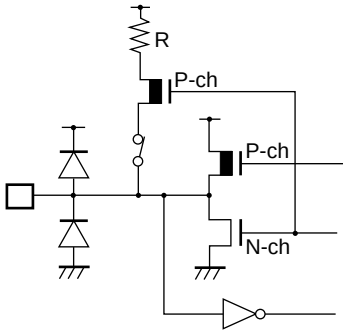
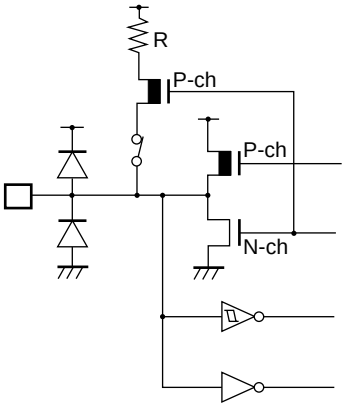
Pin no.	Pin name	Circuit type	Function
8	P37/PTO2	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as the toggle output for the 8-bit PWM timer 2 (PTO2).
56	P40	D	General-purpose I/O port A pull-up resistor option is provided.
58	P41/EC	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a 16-bit timer/counter input (EC). EC input is hysteresis input.
59	P42/TXD1	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data output 1 for the UART (TXD1).
60	P43/RXD1	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data input 1 for the UART (RXD1). RXD1 input is hysteresis input.
61	P44/SCL1	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the clock I/O 1 for the UART (SCL1). SCL1 input is hysteresis input.
62	P45/TXD2	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data output 2 for the UART (TXD2).
63	P46/RXD2	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data input 2 for the UART (RXD2). RXD2 input is hysteresis input.
64	P47/SCL2	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the clock I/O 2 for the UART (SCL2). SCL2 input is hysteresis input.
51 to 55	P50 to P54	G	N-channel open-drain I/O ports A pull-up resistor option is provided only for the MB89816A.
9 to 11	P60/INT0 to P62/INT2	H	General-purpose I/O ports A pull-up resistor option is provided. Also serve as an external interrupt input (INT0 to INT2). These ports are a hysteresis input type.
13 to 17	P63/INT3 to P67/INT7	H	General-purpose I/O ports A pull-up resistor option is provided. Also serve as an external interrupt input (INT3 to INT7). These ports are a hysteresis input type.
12, 57	V_{CC}	–	Power supply pin
25, 50	V_{SS}	–	Power supply (GND) pin

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Main clock • At an oscillation feedback resistor of approximately 2 MΩ (1 to 5 MHz) • CR oscillator circuit selectability
B		
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• CMOS output • CMOS input • Pull-up resistor optional
E		• CMOS output • CMOS input • Hysteresis input (resource input) • Pull-up resistor optional

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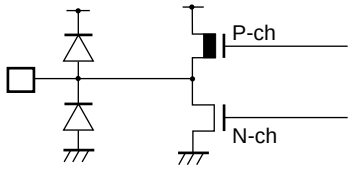
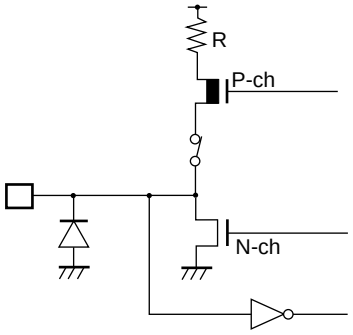
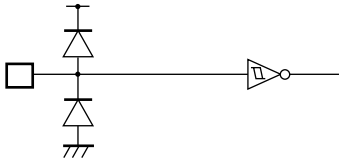
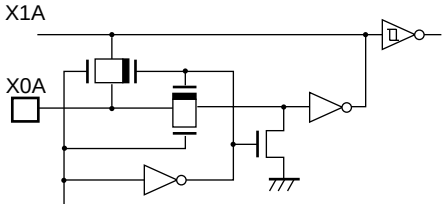
Type	Circuit	Remarks
F		• CMOS output
G		• N-ch open-drain output • CMOS input • Pull-up resistor optional (only for the MB89816A)
H		• Hysteresis input • Pull-up resistor optional
I		• Subclock (30 to 40 kHz) • At an oscillation feedback resistor of approximately 4.5 MΩ

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

4. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P817A

In EPROM mode, the MB89P817A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Writing Procedure**

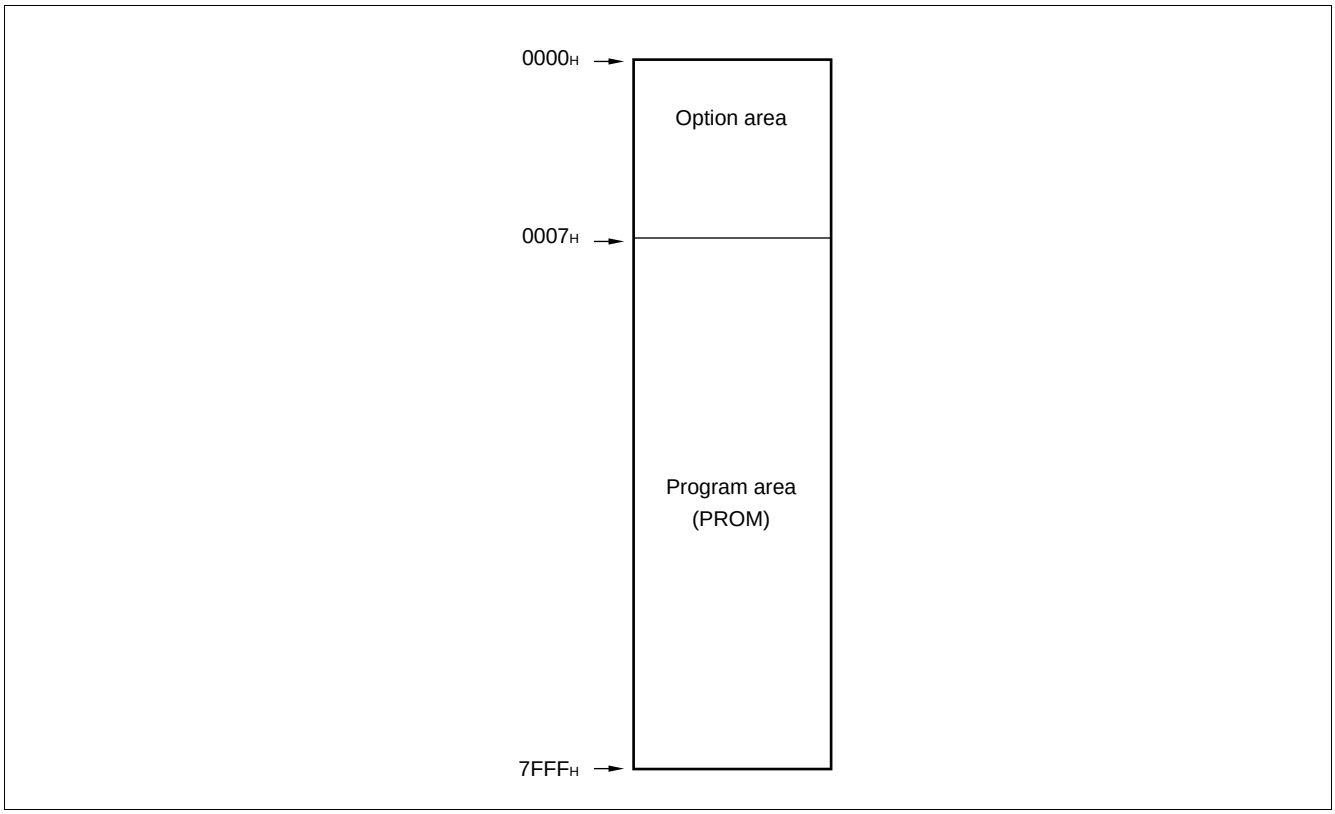
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$ (note that addresses 8007_H to $FFFF_H$ while operating as operating mode assign to 0007_H to $7FFF_H$ in EPROM mode).
Load option data into addresses 0000_H to 0006_H of the EPROM programmer. (For information about each corresponding option, see "• Setting OTPROM Option Bit Map.")

(3) Program with the EPROM programmer.

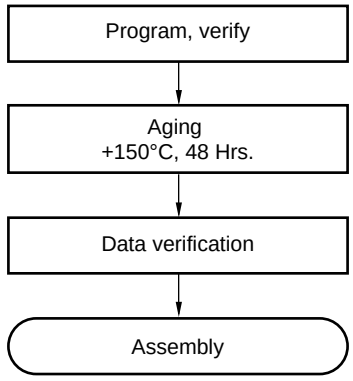
- **Memory Space**

Memory space is diagrammed below.



- **Recommended Screening Conditions**

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM (one-time PROM) microcomputer program.



- **Programming Yield**

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

- **EPROM Programmer Socket Adapter**

Package	Compatible socket adapter
FPT-64P-M06	ROM-64QF-28DP-8L

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

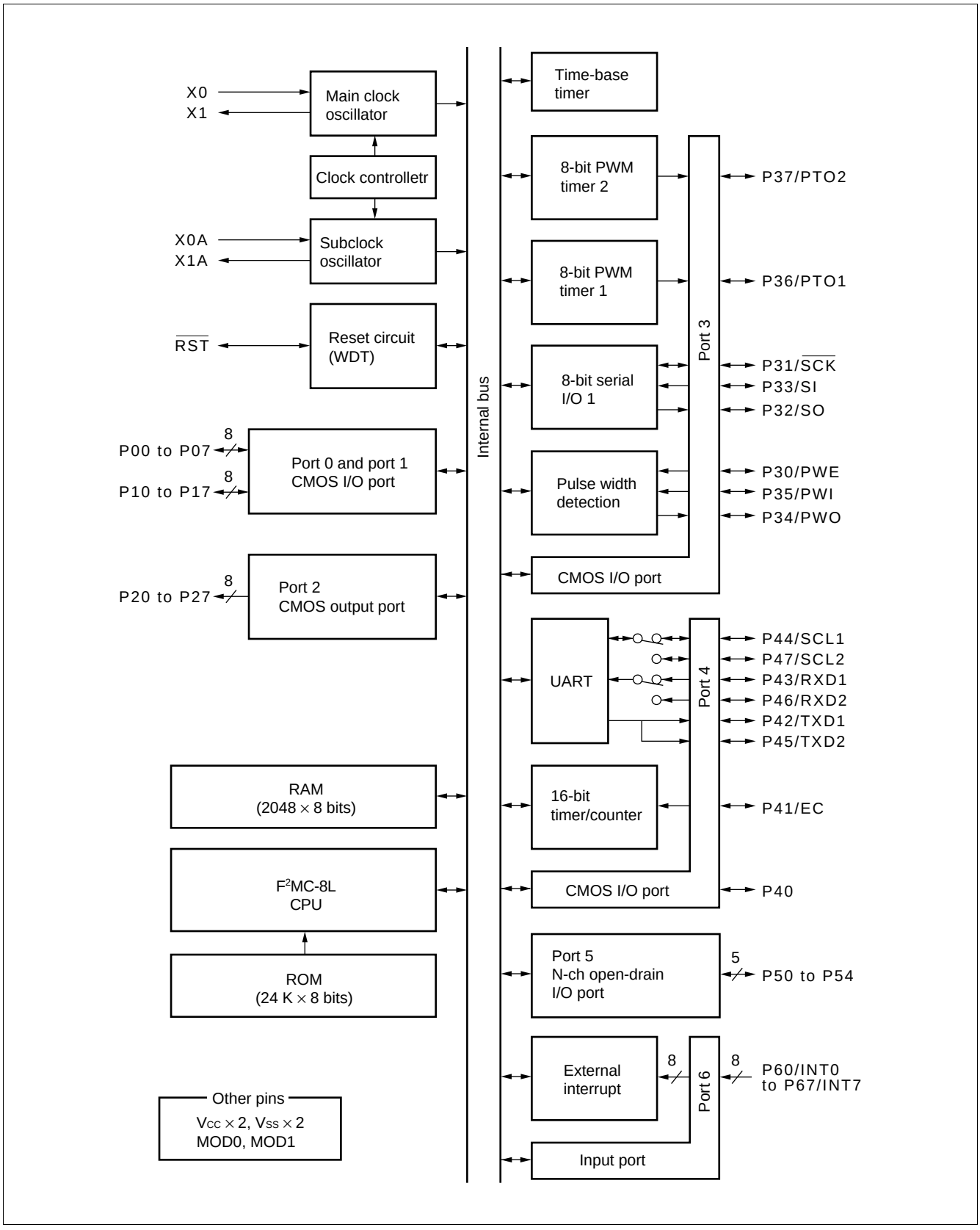
Note: Connect the jumper pin to V_{SS} when using.
Depending on the EPROM programmer, inserting a capacitor of approx. 0.1 µF between V_{PP} and V_{SS} or V_{CC} and V_{SS} can stabilize programming operations.

- **OTPROM Option Bit Map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Single-clock setting 1: Dual-clock 0: Single-clock	Reset pin output 1: Enabled 0: Disabled	Power-on reset 1: Enabled 0: Disabled	Oscillation stabilization time 00 $2^4/F_{CH}$ 10 $2^{17}/F_{CH}$	 01 $2^{14}/F_{CH}$ 11 $2^{18}/F_{CH}$
0001_H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0002_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0003_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0004_H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0005_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
0006_H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writables	Oscillator type 1: Crystal 0: CR	P67 Pull-up 1: No 0: Yes	P66 Pull-up 1: No 0: Yes	P65 Pull-up 1: No 0: Yes

Note: Each bit defaults to 1.

■ BLOCK DIAGRAM

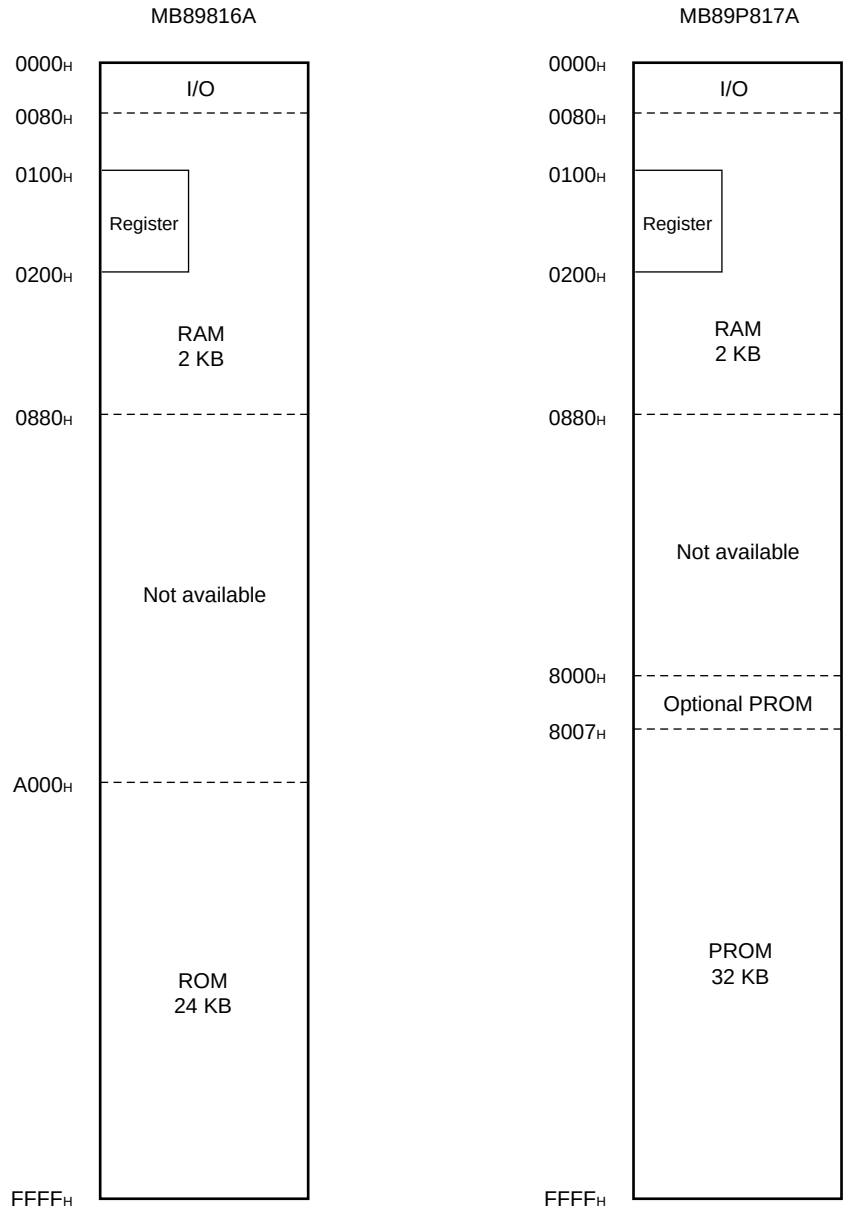


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89810A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89810A series is structured as illustrated below.

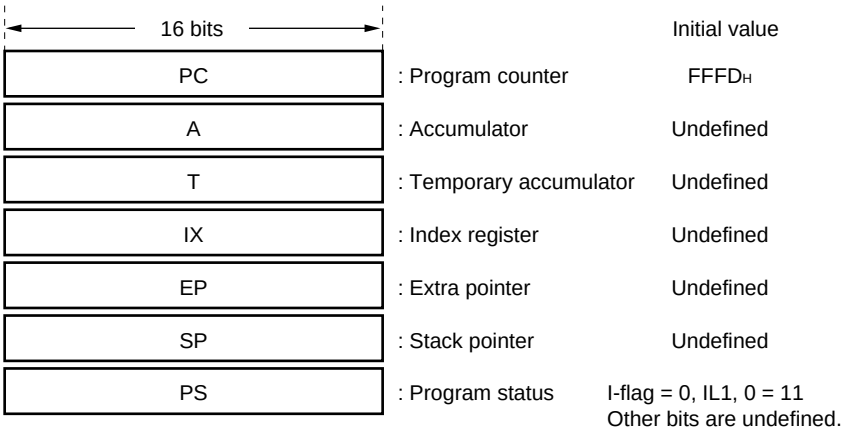
Memory Space



2. Registers

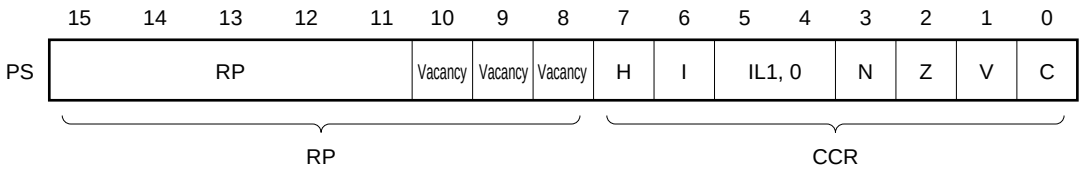
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



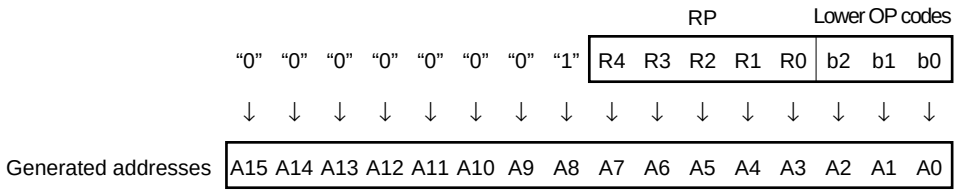
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

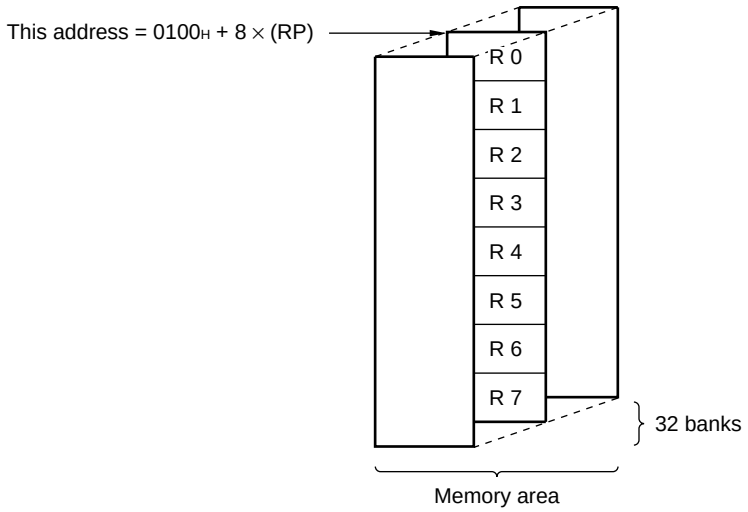
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89816A. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H			Vacancy
06H			Vacancy
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBCR	Time-base timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H	(R/W)	PDR5	Port 5 data register
11H	(R)	PDR6	Port 6 data register
12H			Vacancy
13H			Vacancy
14H			Vacancy
15H			Vacancy
16H			Vacancy
17H	(R/W)	PIVE	Port inverting operation enable register
18H	(R/W)	TMCR	16-bit timer count register
19H	(R/W)	TCHR	16-bit timer count register (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH			Vacancy
1CH	(R/W)	SMR	Serial I/O mode register
1DH	(R/W)	SDR	Serial I/O data register
1EH			Vacancy
1FH			Vacancy

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Address	Read/write	Register name	Register description
20_H	(R/W)	SMC1	UART serial I/O mode control register 1
21_H	(R/W)	SRC	UART serial I/O rate control register
22_H	(R/W)	SSD	UART serial I/O status/data control register
23_H	(R/W)	SIDR/SODR	UART serial I/O data control register
24_H	(R/W)	SMC2	UART serial I/O mode control register 2
25_H			Vacancy
26_H			Vacancy
27_H			Vacancy
28_H	(R/W)	CNTR1	PWM timer control register 1
29_H	(R/W)	CNTR2	PWM timer control register 2
$2A_H$	(R/W)	CNTR3	PWM timer control register 3
$2B_H$	(W)	COMR2	PWM timer compare register 2
$2C_H$	(W)	COMR1	PWM timer compare register 1
$2D_H$			Vacancy
$2E_H$			Vacancy
$2F_H$	(R/W)	PWCR	Pulse width detection control register
30_H	(R/W)	EIC1	External interrupt 1 control register 1
31_H	(R/W)	EIC2	External interrupt 1 control register 2
32_H	(R/W)	EI2E	External interrupt 2 enable register
33_H	(R/W)	EI2F	External interrupt 2 flag register
34_H			Vacancy
35_H to $7A_H$			Vacancy
$7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level register 1
$7D_H$	(W)	ILR2	Interrupt level register 2
$7E_H$	(W)	ILR3	Interrupt level register 3
$7F_H$	Not available	ITR	Interrupt test register

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P50 to P54
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P50 to P54
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P50 to P54
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P50 to P54
“L” level maximum output current	I_{OL}	—	20	mA	Peak value
“L” level average output current	I_{OLAV1}	—	4	mA	Average value except pins other than P50 to P54
	I_{OLAV2}	—	10	mA	Average value for P50 to P54
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	Peak value
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value
“H” level maximum output current	I_{OH}	—	–20	mA	Peak value
“H” level average output current	I_{OHAV}	—	–4	mA	Average value
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	Peak value
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

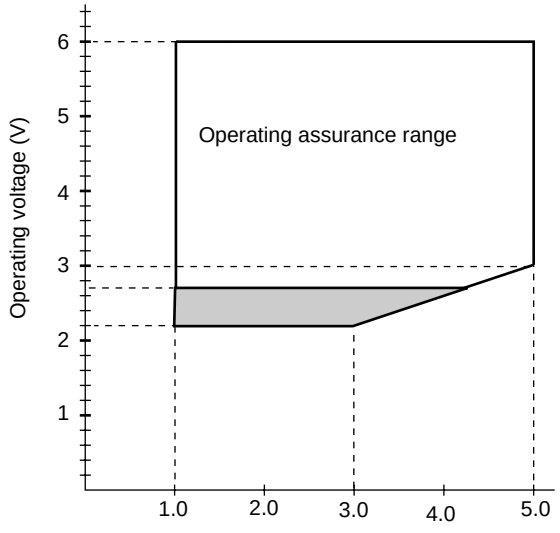
Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0	V	Normal operation assurance range MB89816A
		2.7*	6.0	V	Normal operation assurance range MB89P817A
		1.5	6.0	V	Retains the RAM state in stop mode
"H" level voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P54 (with pull-up resistor)
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	$\overline{RST}$, MOD0, MOD1, P60 to P67, Pheripheral input for port 3 and port 4
	V_{IHS2}	0.8 V_{CC}	V_{SS} + 6.0	V	P50 to P54 (without pull-up resistor)
"L" level voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P54
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	$\overline{RST}$, MOD0, MOD1, P60 to P67, Pheripheral input for port 3 and port4
Open-drain output pin application voltage	V_D	V_{SS} – 0.3	V_{SS} + 6.0	V	P50 to P54 (without pull-up resistor)
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency. See Figure 1.



Note: The shaded area is assured only for the MB89816A

Figure 1 Operating Voltage vs. Main Clock Operating Frequency (for MB89816A)

3. DC Characteristics

(V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47	I_{OH} = –2.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54 P60 to P67	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	P50 to P54	I_{OL} = 6 mA V_{CC} = 3 V	—	—	0.5	V	
	V_{OL3}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, P60 to P67, MOD0, MOD1	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P54, P60 to P67, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Power supply current*	I_{CC1}	V_{CC}	F_{CH} = 5 MHz V_{CC} = 5.0 V t_{inst} = 0.8 µs	—	4	6	mA	MB89816A
				—	4.8	7.5	mA	MB89P817A
	I_{CC2}		F_{CH} = 5 MHz V_{CC} = 3.0 V t_{inst} = 6.4 µs	—	0.4	0.6	mA	MB89816A
				—	1.0	1.5	mA	MB89P817A
	I_{CCS1}		F_{CH} = 5 MHz V_{CC} = 5.0 V t_{inst} = 0.8 µs	—	1.2	1.8	mA	Sleep mode
	I_{CCS2}		F_{CH} = 5 MHz V_{CC} = 3.0 V t_{inst} = 12.8 µs	—	0.3	0.5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V	—	50	100	µA	Subclock mode
				—	500	700	µA	MB89P817A

(Continued)

(Continued)

(V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*	I_{CCLS}	V_{CC}	F_{CL} = 32.768 kHz V_{CC} = 3.0 V	—	15	50	µA	Subclock sleep mode
	I_{CCT}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V	—	—	15	µA	Watch mode Main clock stop mode at dual-clock system
	I_{CCH}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V	—	—	10	µA	Subclock stop mode Main clock stop mode at single-clock system
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	10	—	pF	

* : The measurement conditions of power supply current are as follows: the external clock and T_A = +25°C.

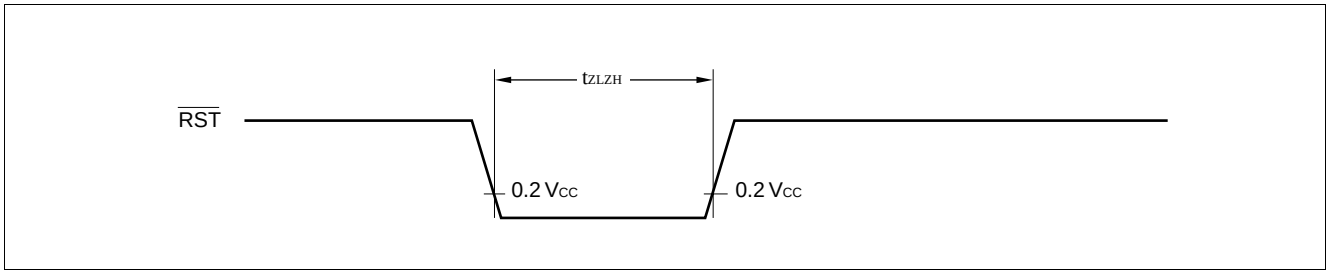
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{CH}	—	ns	

Note: t_{CH} is the cycle time of the main clock.

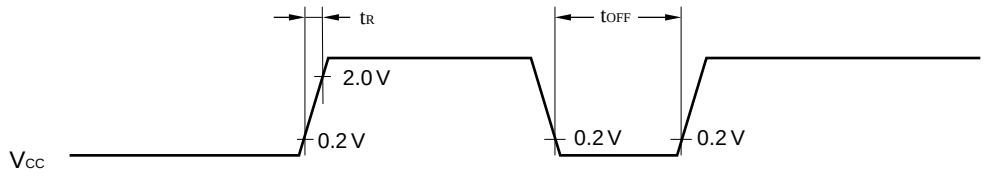


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



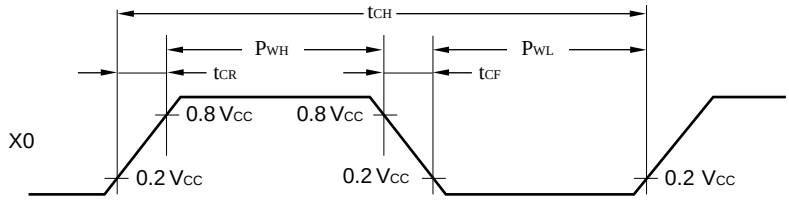
Note that a sudden increase in supply voltage may result in a power-on reset.
When increasing the supply voltage during operation, voltage variation should be within twice the intended increment so that the voltage rises as smoothly as possible.

(3) Clock Timing

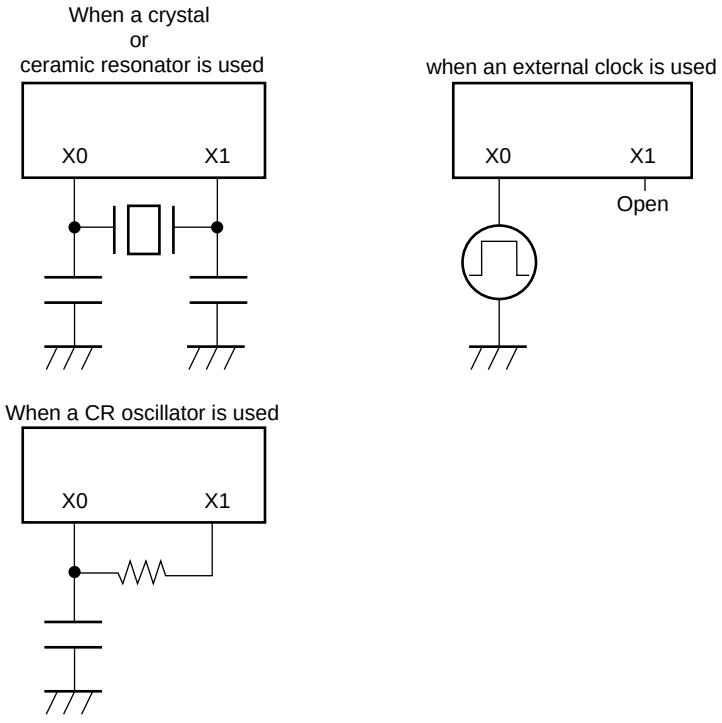
($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	5	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CH}	X0, X1		200	—	1000	ns	
	t_{CL}	X0A, X1A		—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A		—	15.2	—	µs	
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	—	10	ns	External clock

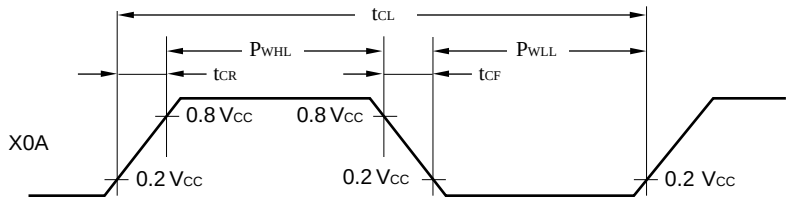
X0 and X1 Timing and Conditions



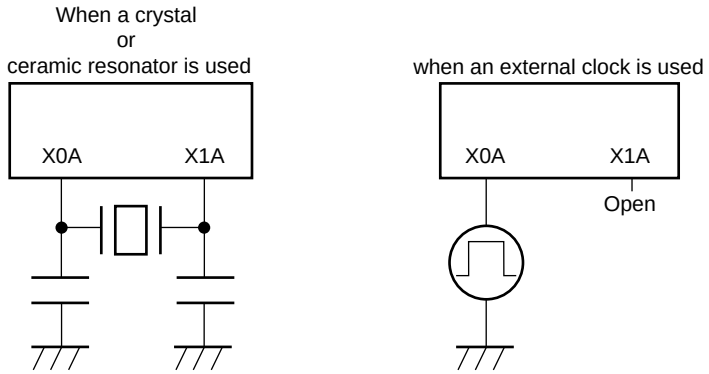
Main Clock Conditions



X0A and X1A Timings and Conditions



Subclock Conditions



(4) Serial I/O Timings

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC1}	$\overline{SCK}$	Internal shift clock mode	2 t_{inst}	—	ns	
$\overline{SCK}$ ↓ → SO time	t_{SLOV1}	$\overline{SCK}$, SO		–200	200	ns	
Valid SI → $\overline{SCK}$ ↑	t_{IVSH1}	SI, $\overline{SCK}$		1/2 t_{inst}	—	ns	
$\overline{SCK}$ ↑ → valid SI hold time	t_{SHIX1}	$\overline{SCK}$, SI		1/2 t_{inst}	—	ns	
Serial clock “H” pulse width	t_{SHSL}	$\overline{SCK}$	External shift clock mode	1 t_{inst}	—	ns	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}	—	ns	
SCK ↓ → SO time	t_{SLOV2}	$\overline{SCK}$, SO		0	200	ns	
Valid SI → $\overline{SCK}$ ↑	t_{IVSH2}	SI, $\overline{SCK}$		1/2 t_{inst}	—	ns	
$\overline{SCK}$ ↑ → valid SI hold time	t_{SHIX2}	$\overline{SCK}$, SI		1/2 t_{inst}	—	ns	

* : t_{inst} represents the minimum instruction execution time. It varies with the selected system clock and operating mode.

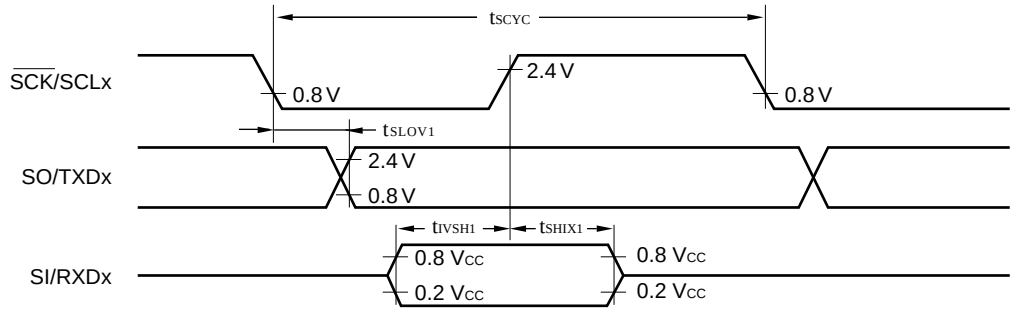
(5) UART Timings

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

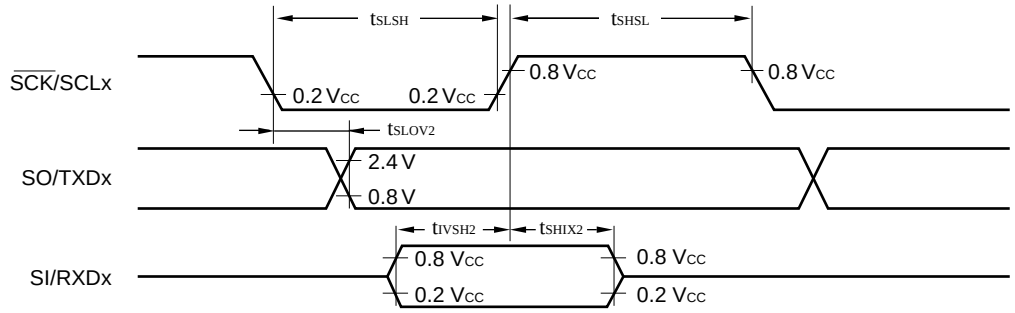
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCL1, SCL2	Internal shift clock mode	2 t_{inst}	—	ns	
SCL ↓ → TXDx time	t_{SLOV1}	SCLx, TXDx		–200	200	ns	
Valid RXDx → SCLx ↑	t_{IVSH1}	RXDx, SCLx		1/2 t_{inst}	—	ns	
SCLx ↑ → valid RXDx hold time	t_{SHIX1}	SCL1, RXD2		1/2 t_{inst}	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCL1, SCL2	External shift clock mode	1 t_{inst}	—	ns	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}	—	ns	
SCLx ↓ → TXDx time	t_{SLOV2}	SCLx, TXDx		0	200	ns	
Valid RXDx → SCLx ↑	t_{IVSH2}	RXDx, SCLx		1/2 t_{inst}	—	ns	
SCLx ↑ → valid RXDx hold time	t_{SHIX2}	SCL1, RXD2		1/2 t_{inst}	—	ns	

Notes:
- t_{inst} represents the minimum instruction execution time. It varies with the selected system clock and operating mode.
- The edge polarity for the SLCx input is assumed when LSEL bit = 0 for SMC2. The polarity is inverted when LSEL = 1.

Internal Shift Clock Mode



External Shift Clock Mode

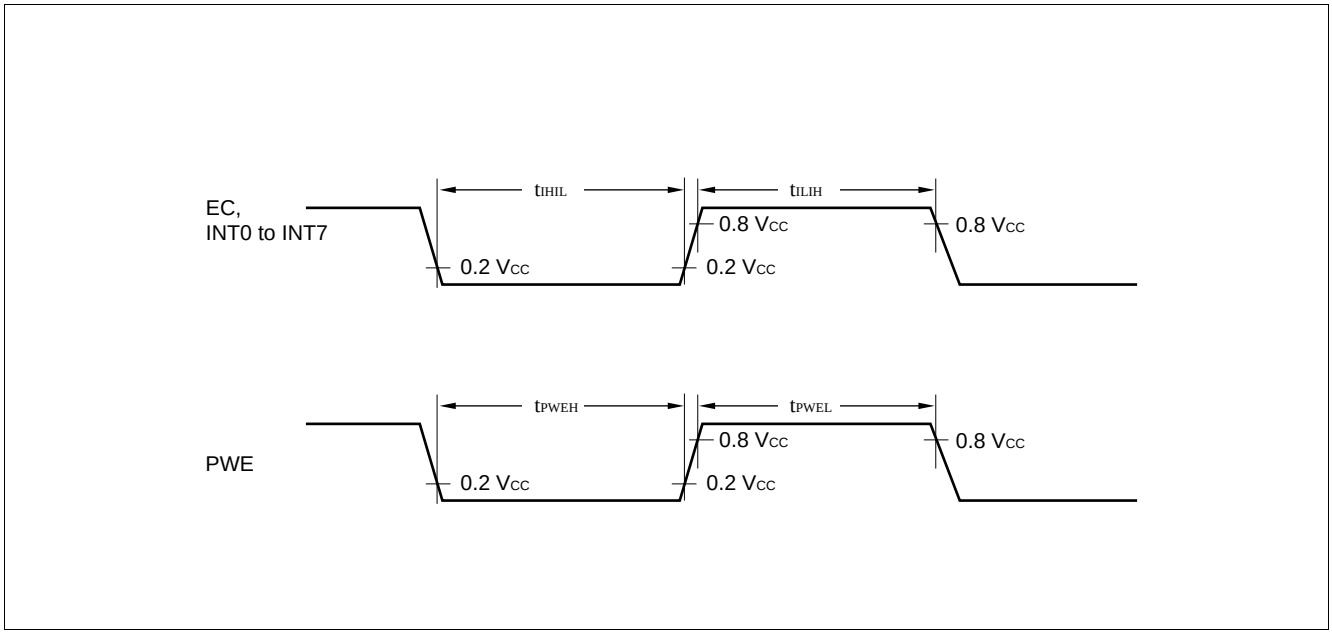


(6) Peripheral Input Timings

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width	t_{ILIH}	EC, INT0 to INT7	—	2 t_{inst}	—	ns	
Peripheral input “L” pulse width	t_{IHIL}	EC, INT0 to INT7	—	2 t_{inst}	—	ns	
“H” input pulse width of pulse width detection enable signal	t_{PWEH}	PWE	—	512 t_{CL} + 200 or 480 t_{CL} + 200	—	ns	
“L” input pulse width of pulse width detection enable signal	t_{PWEL}		—	512 t_{CL} + 200 or 480 t_{CL} + 200	—	ns	

Notes:
- t_{inst} represents the minimum instruction execution time. It varies with the selected system clock and operating mode.
- t_{CL} represents the subclock cycle time.
- The PWE pulse width value varies with the first divider selection bit of the watch prescaler. The pulse width is “512 t_{CL} + 200” when divide by 16 is selected; or "480 t_{CL} + 200" when divide by 15 is selected.



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
•Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89816A	MB89P817A
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer
1	Pull-up resistors P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P54, P60 to P67	Specify by pin	Can be set per pin. (P50 to P54 are available only for without a pull-up resistor.)
2	Power-on reset selection With power-on reset Without power-on reset	Selectable	Setting possible
3	Main clock oscillation (5 MHz) stabilization time selection approx. 218/F_{CH} (approx. 52.4 ms) approx. 217/F_{CH} (approx. 26.2 ms) approx. 214/F_{CH} (approx. 3.2 ms) approx. 24/F_{CH} (approx. 0 ms)	Selectable	Setting possible
4	Reset pin ouotput selection With reset output Without reset output	Selectable	Setting possible
5	Selection either single- or dual-clock system Single clock Dual clock	Selectable	Setting possible
6	Main clock oscillator type selection Crystal or ceramic oscillator CR	Selectable	Setting possible

F_{CH}: Main clock frequency

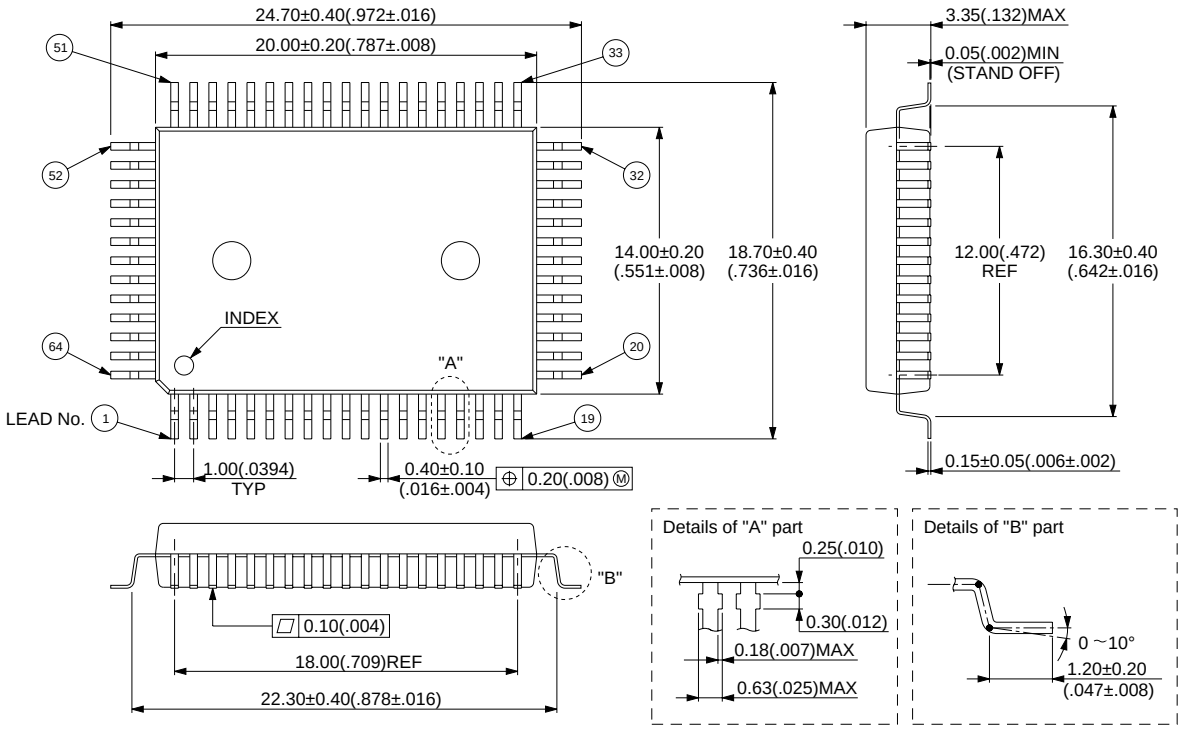
* : The main clock oscillation setting time is generated by dividing the main clock frequency. Note that the oscillation cycle is not stable immediately after oscillation is started. The settling time value in this data sheet should be used as a reference.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89816APF MB89P817APF	64-pin Plastic QFP (FPT-64P-M06)	

■ PACKAGE DIMENSIONS

64-pin Plastic QFP
(FPT-64P-M06)



Dimensions in mm (inches)

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