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# F<sup>2</sup>MC-16LX 16-bit Microcontroller Datasheet

The MB90340E series with up to 2 FULL-CAN interfaces is especially designed for automotive and other industrial applications. Its main feature are the on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The power to the MCU core (3 V) is supplied by a built-in regulator circuit, giving these microcontrollers superior performance in terms of power consumption and tolerance to EMI.

## Features

### CPU

- Instruction system best suited to controller
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced functionality with signed multiply and divide instructions and the RETI instruction
  - Enhanced high-precision computing with 32-bit accumulator
- Instruction system compatible with high-level language (C language) and multitask
  - Employing system stack pointer
  - Various enhanced pointer indirect instructions
  - Barrel shift instructions
- Increased processing speed
  - 4-byte instruction queue

### Serial interface

- LIN-UART : 4 channels
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
- I<sup>2</sup>C interface : 2 channels (only for devices with a C suffix in the part number)
  - Up to 400 kbps transfer rate

### Interrupt controller

- Powerful 8-level, 34-condition interrupt feature
- Up to 16 external interrupts are supported
- Automatic data transfer function independent of CPU
  - Expanded intelligent I/O service function (EI<sup>2</sup>OS) : up to 16 channels

### I/O ports

- General-purpose input/output port (CMOS output)
  - 80 ports (for devices without an S suffix in the part number - i.e. devices that support the sub clock)
  - 82 ports (for devices with an S suffix in the part number - i.e. devices that do not support the sub clock)

### 8/10-bit A/D converter

- 16 channels (only for devices without a C suffix in the part number)
- 24 channels (only for devices with a C suffix in the part number)

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 μs (at 24 MHz machine clock, including sampling time)

### Address match detection (program patch) function

- Detects address matches against 6 address pointers

### Timer

- Time-base timer, watch timer, watchdog timer : 1 channel
- 8/16-bit PPG timer : 8-bit × 16 channels, or 16-bit × 8 channels
- 16-bit reload timer : 4 channels
- 16-bit input/output timer
  - 16-bit free-run timer : 2 channels (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
  - 16-bit input capture: (ICU): 8 channels
  - 16-bit output compare: (OCU): 8 channels

### Full-CAN controller

- Up to 2 channels
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 16 built-in message buffers
- CAN wake-up function

### Low power consumption (standby) mode

- Sleep mode (a mode that halts CPU operating clock)
- Timebase timer mode (a mode where only the oscillation clock, sub clock, timebase timer and watch timer operate)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode

### Clock modulation circuit

### Technology

- CMOS technology

**Contents**

<b>Product Lineup</b> .....	<b>3</b>	Clock Output Timing .....	59
<b>Pin Assignments</b> .....	<b>6</b>	Bus Timing (Read) .....	60
<b>Pin Description</b> .....	<b>12</b>	Bus Timing (Write) .....	61
<b>I/O Circuit Type</b> .....	<b>19</b>	Ready Input Timing .....	62
<b>Handling Devices</b> .....	<b>23</b>	Hold Timing .....	63
<b>Block Diagrams</b> .....	<b>26</b>	LIN-UART0/1/2/3 .....	64
<b>Memory Map</b> .....	<b>28</b>	Trigger Input Timing .....	69
<b>I/O Map</b> .....	<b>30</b>	Timer Related Resource Input Timing .....	70
<b>CAN Controllers</b> .....	<b>41</b>	Timer Related Resource Output Timing .....	70
<b>Interrupt Factors, Interrupt Vectors,</b>		I2C Timing .....	71
<b>Interrupt Control Register</b> .....	<b>48</b>	A/D Converter .....	72
<b>Electrical Characteristics</b> .....	<b>50</b>	Definition of A/D Converter Terms .....	73
Absolute Maximum Ratings .....	50	Notes on A/D Converter Section .....	74
Recommended Operating Conditions .....	52	Flash Memory Program/Erase Characteristics .....	76
DC Characteristics .....	53	<b>Example Characteristics</b> .....	<b>77</b>
AC Characteristics .....	55	<b>Ordering Information</b> .....	<b>86</b>
Clock Timing .....	55	<b>Package Dimensions</b> .....	<b>89</b>
Reset Standby Input .....	58	<b>Major Changes</b> .....	<b>91</b>
Power On Reset .....	59		

**1. Product Lineup**

Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Parameter			
Type	Evaluation products	Flash memory products	MASK ROM products
CPU	F <sup>2</sup> MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	External	512 Kbytes : MB90F345E(S), MB90F345CE(S) 256 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 128 Kbytes : MB90F347E(S), MB90F347CE(S) 64 Kbytes : MB90F346E(S), MB90F346CE(S)	256 Kbytes : MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S) 128 Kbytes : MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S) 64 Kbytes : MB90346E(S), MB90346CE(S)
RAM	30 Kbytes	20 Kbytes : MB90F345E(S), MB90F345CE(S) 16 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 6 Kbytes : MB90F347E(S), MB90F347CE(S) 2 Kbytes : MB90F346E(S), MB90F346CE(S)	16 Kbytes : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) 6 Kbytes : MB90347E(S), MB90347CE(S) 2 Kbytes : MB90346E(S), MB90346CE(S)
Emulator-specific power supply*	Yes	—	
Technology	0.35 μm CMOS with regulator for built-in power supply	0.35 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%	3.5 V to 5.5 V : When normal operating (not using A/D converter) 4.0 V to 5.5 V : When using the A/D converter/Flash programming 4.5 V to 5.5 V : When using the external bus	
Temperature range	—	-40°C to +105°C	
Package	PGA-299	QFP-100, LQFP-100	
LIN-UART	5 channels	4 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I <sup>2</sup> C (400 kbps)	2 channels	Devices with a C suffix in the part number : 2 channels Devices without a C suffix in the part number : —	

*(Continued)*

Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Parameter			
A/D Converter	24 input channels	Devices with a C suffix in the part number : 24 channels Devices without a C suffix in the part number : 16 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 $\mu$ s include sample time (per one channel)		
16-bit Reload Timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$ , $f_{sys}/2^3$ , $f_{sys}/2^5$ ( $f_{sys}$ = Machine clock frequency) Supports External Event Count function		
16-bit Free-run Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ , $f_{sys}/2^5$ , $f_{sys}/2^6$ , $f_{sys}/2^7$ ( $f_{sys}$ = Machine clock freq.) Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit free-run timer matches the output compare register A pair of compare registers can be used to generate an output signal.		
16-bit Input Capture (8 channels)	Captures the value of the 16-bit free-run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges).		
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width		
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ or 128 $\mu$ s@ $f_{osc}$ = 4 MHz ( $f_{sys}$ = Machine clock frequency, $f_{osc}$ = Oscillation clock frequency)		
CAN Interface	3 channels	2 channels : MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S) 1 channel : MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	2 channels : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S) 1 channel : MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		

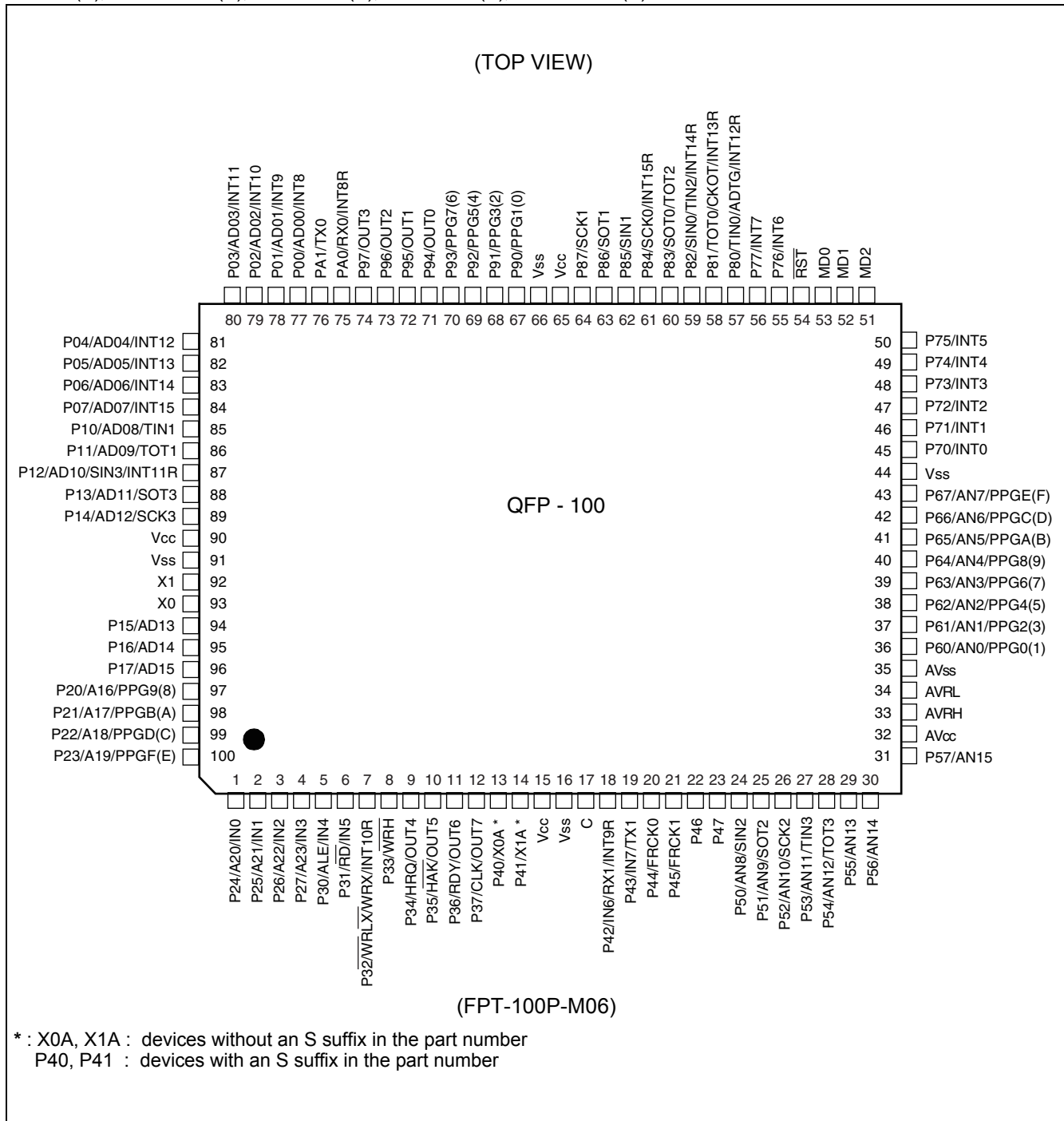
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Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
External Interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI <sup>2</sup> OS) and DMA		
D/A Converter	2 channels	—	
Sub clock (maximum 100 kHz)	Only for MB90V340E-102	Devices with sub clock : devices without an S suffix in the part number Devices without sub clock : devices with an S suffix in the part number	
I/O Ports	Virtually all external pins can be used as general purpose I/O port All ports are push-pull outputs Bit-wise settable as input/output or peripheral signal Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins) TTL input level settable for external bus (32-pin only for external bus)		
Flash Memory	—	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 cycles Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (except for MB90F346E(S) and MB90F346CE (S) )	

\* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01-E) is used.  
Please refer to the Emulator operation manual for details.

## 2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)

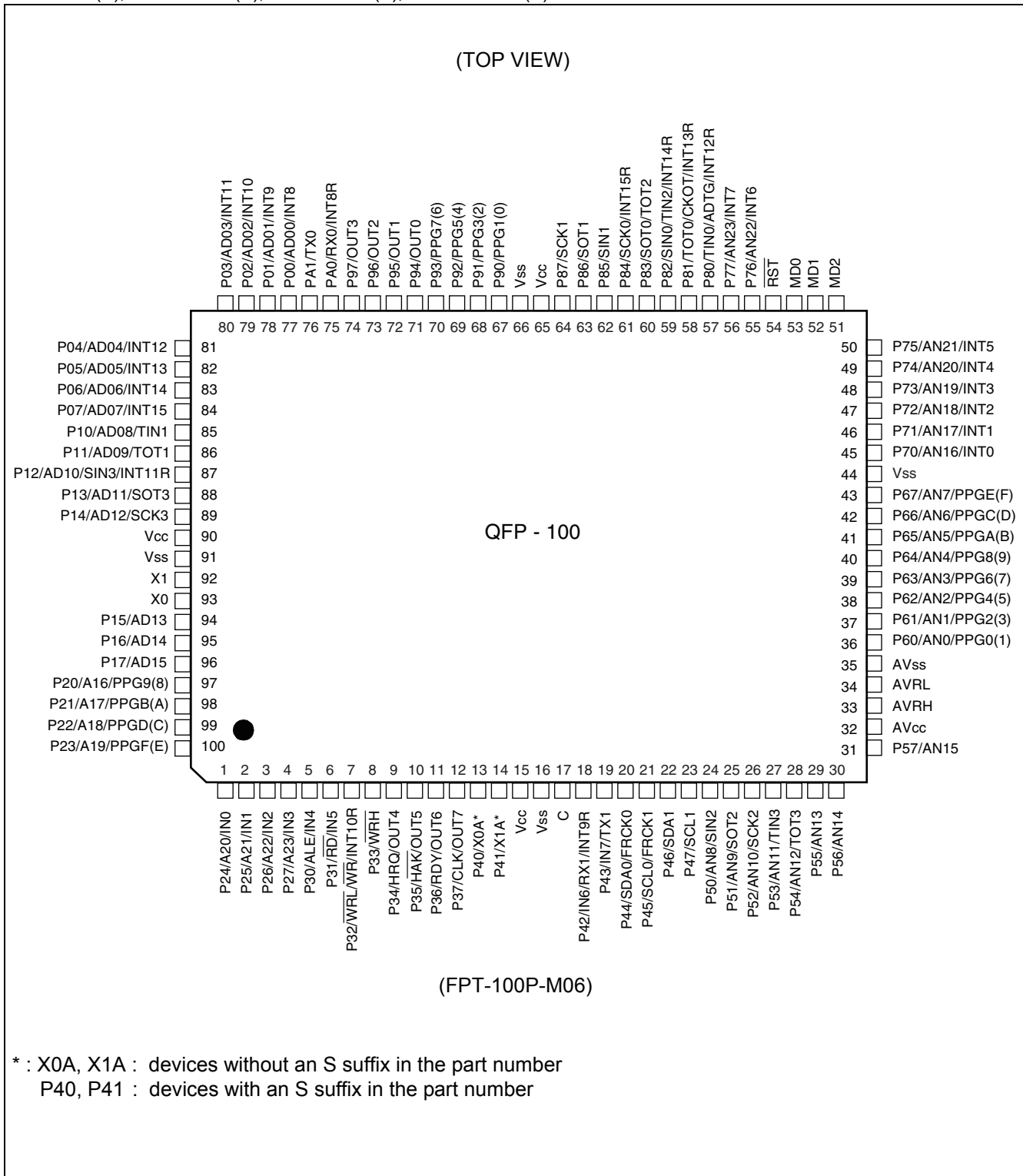


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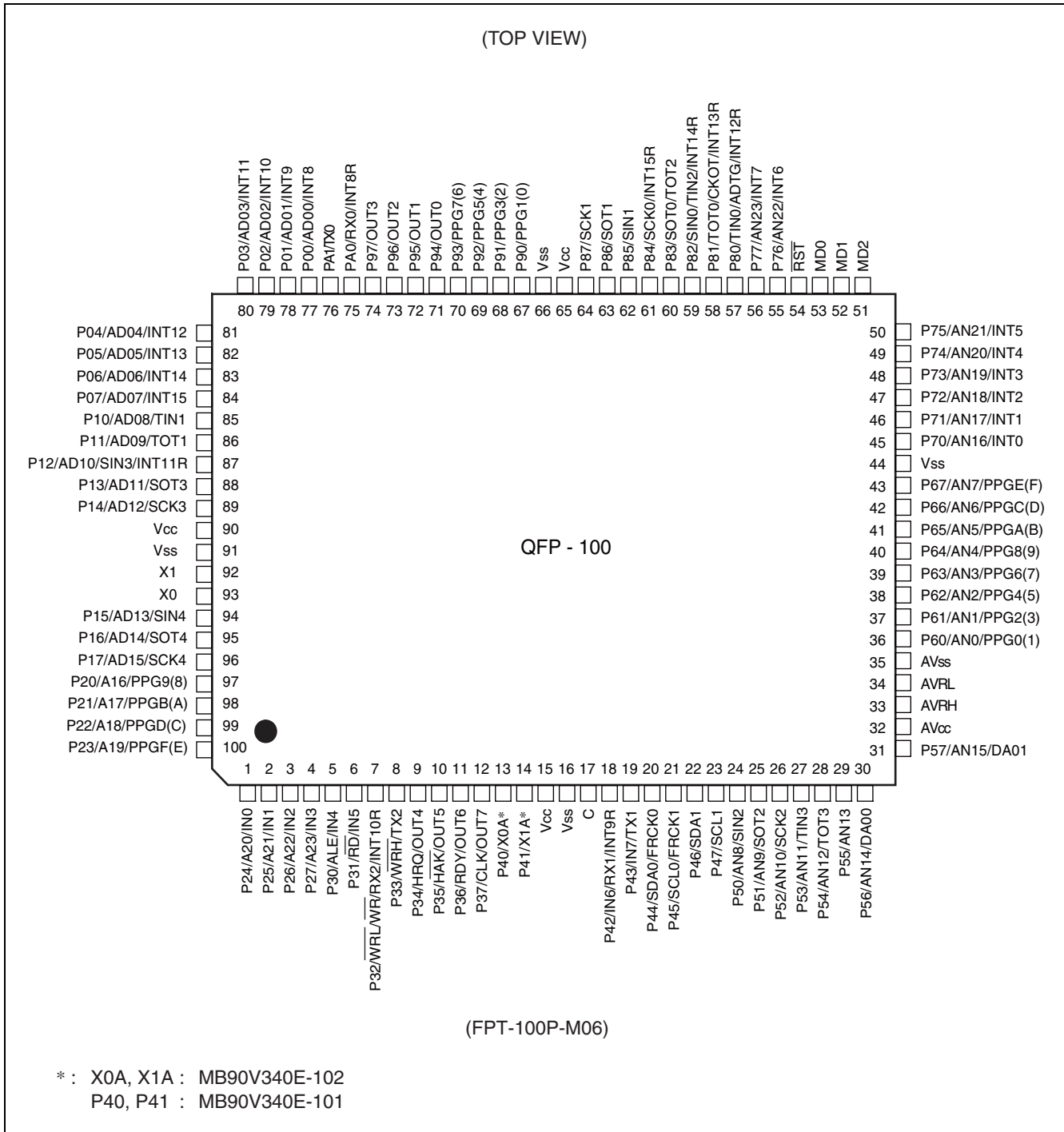
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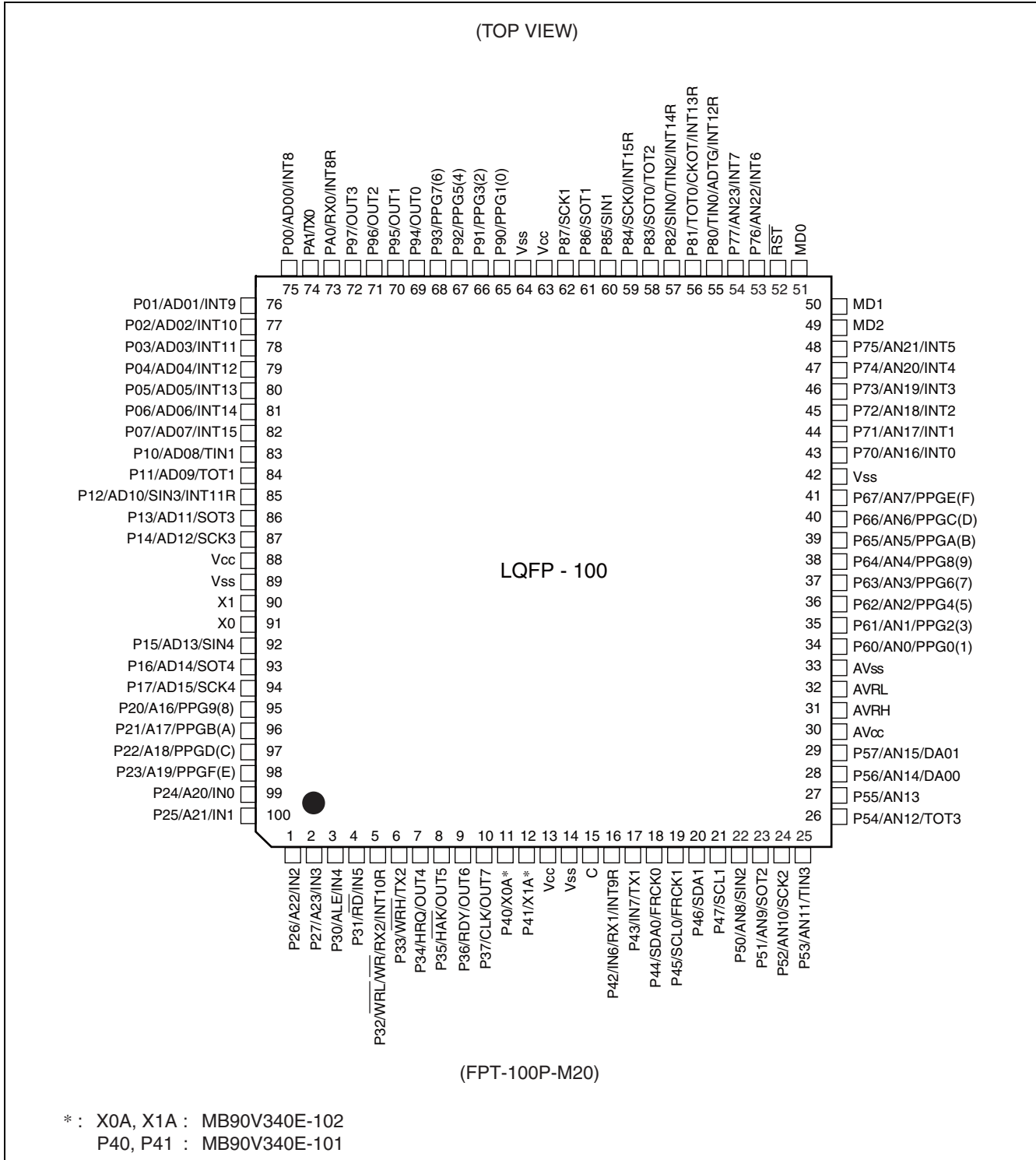
■ MB90V340E-101/MB90V340E-102



This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

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This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

### 3. Pin Description

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures.
5	3	P30	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture.
6	4	P31	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WR/WRL}$ pin output is disabled.
		$\overline{WR} / \overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR/WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin.
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WRH}$ pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
16	14	V <sub>SS</sub>	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 $\mu\text{F}$ .
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV <sub>CC</sub>	K	Analog power input pin for the A/D Converter

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV <sub>CC</sub> .
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV <sub>SS</sub>	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V <sub>SS</sub>	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	RST	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

(Continued)



Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
66	64	V <sub>SS</sub>	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
91	89	V <sub>SS</sub>	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

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(Continued)

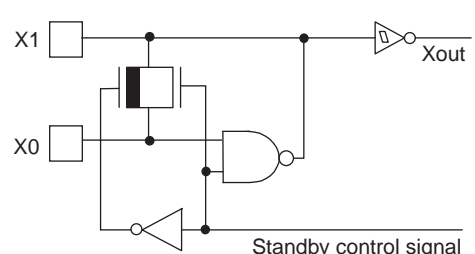
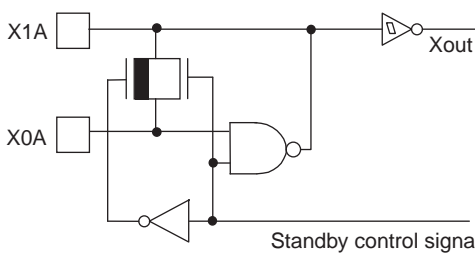
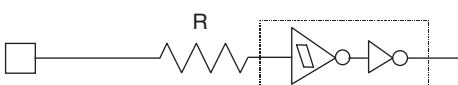
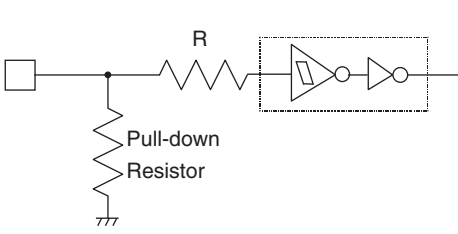
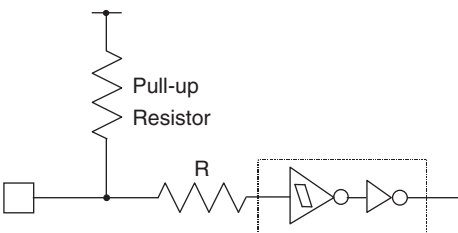
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, PPGB, PP GD, PPGF		Output pins for PPGs

1 : FPT-100P-M06

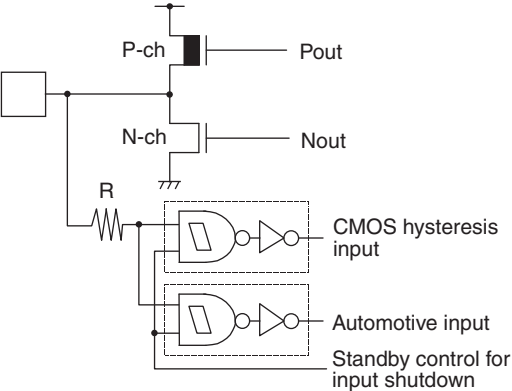
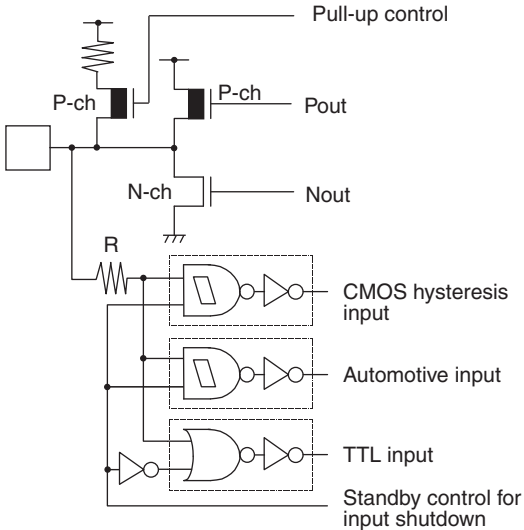
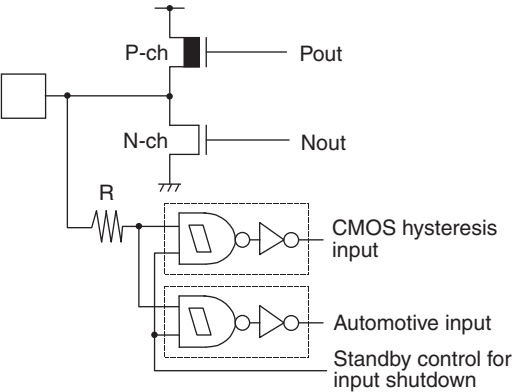
2 : FPT-100P-M20

3 : For I/O circuit type, refer to "I/O Circuit Type".

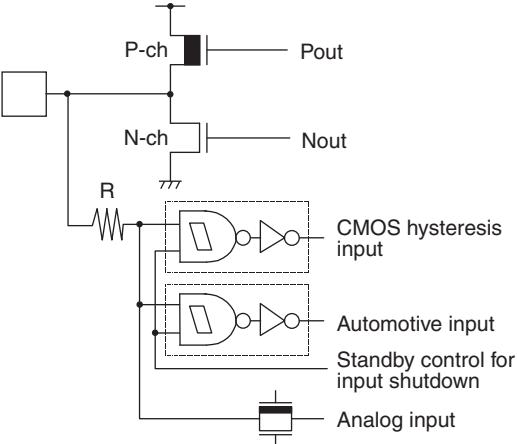
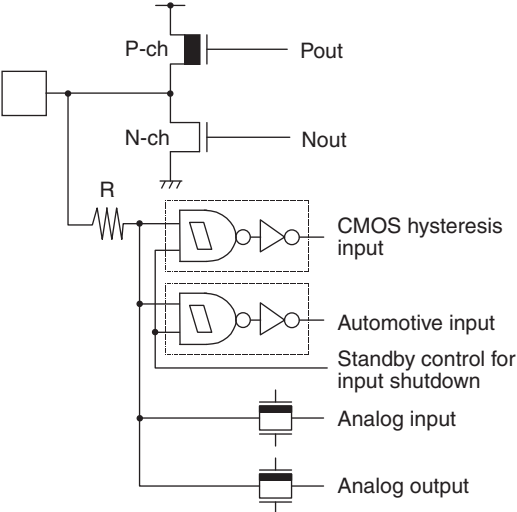
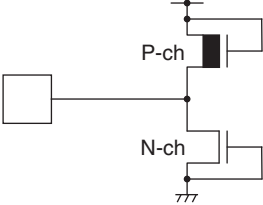
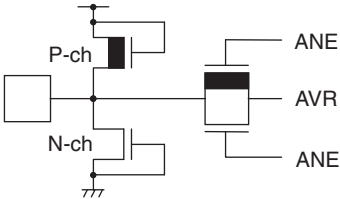
**4. I/O Circuit Type**

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 M $\Omega$
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 M $\Omega$
C		<ul style="list-style-type: none"> <li>■ MASK ROM and evaluation products: CMOS hysteresis input pin</li> <li>■ Flash memory products: CMOS input pin</li> </ul>
D		MASK ROM and evaluation products: <ul style="list-style-type: none"> <li>■ CMOS hysteresis input pin</li> <li>■ Pull-down resistor value: approx. 50 k<math>\Omega</math></li> </ul> Flash memory products: <ul style="list-style-type: none"> <li>■ CMOS input pin</li> <li>■ No pull-down</li> </ul>
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 k $\Omega$

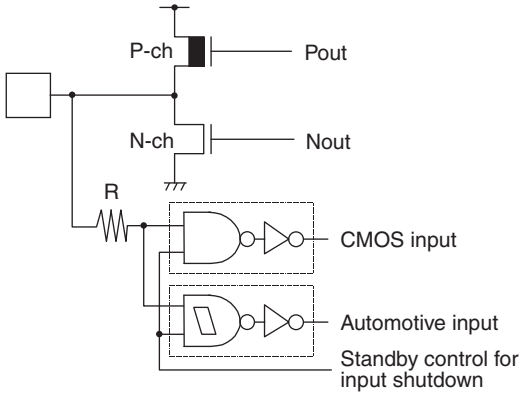
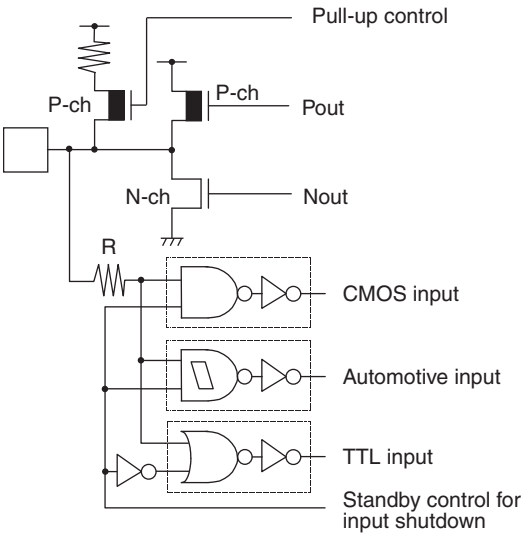
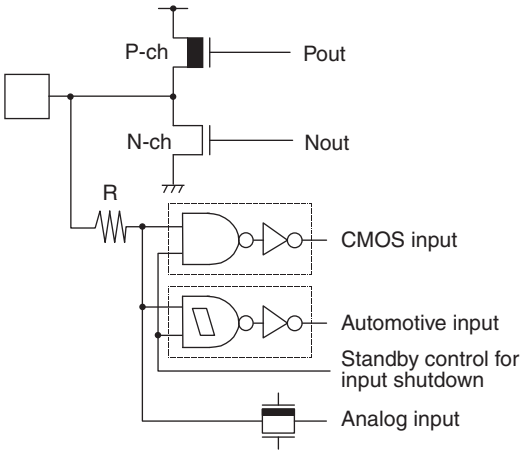
*(Continued)*

Type	Circuit	Remarks
F		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>
G		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ TTL input (with function to disconnect input during standby)</li> <li>■ Programmable pull-up resistor: 50 k<math>\Omega</math> approx.</li> </ul>
H		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 3 \text{ mA}</math>, <math>I_{OH} = -3 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>

(Continued)

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
J		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ D/A analog output</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
K		<p>Power supply input protection circuit</p>
L		<ul style="list-style-type: none"> <li>■ A/D converter reference voltage power supply input pin, with the protection circuit</li> <li>■ Flash memory devices do not have a protection circuit against <math>V_{CC}</math> for pin AVRH</li> </ul>

*(Continued)*

Type	Circuit	Remarks
M		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>
N		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ TTL input (with function to disconnect input during standby)</li> </ul> Programmable pull-up resistor: 50 kΩ approx
O		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>

## 5. Handling Devices

### 1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins.
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AVRH$ ) exceed the digital power-supply voltage.

### 2. Handling unused pins

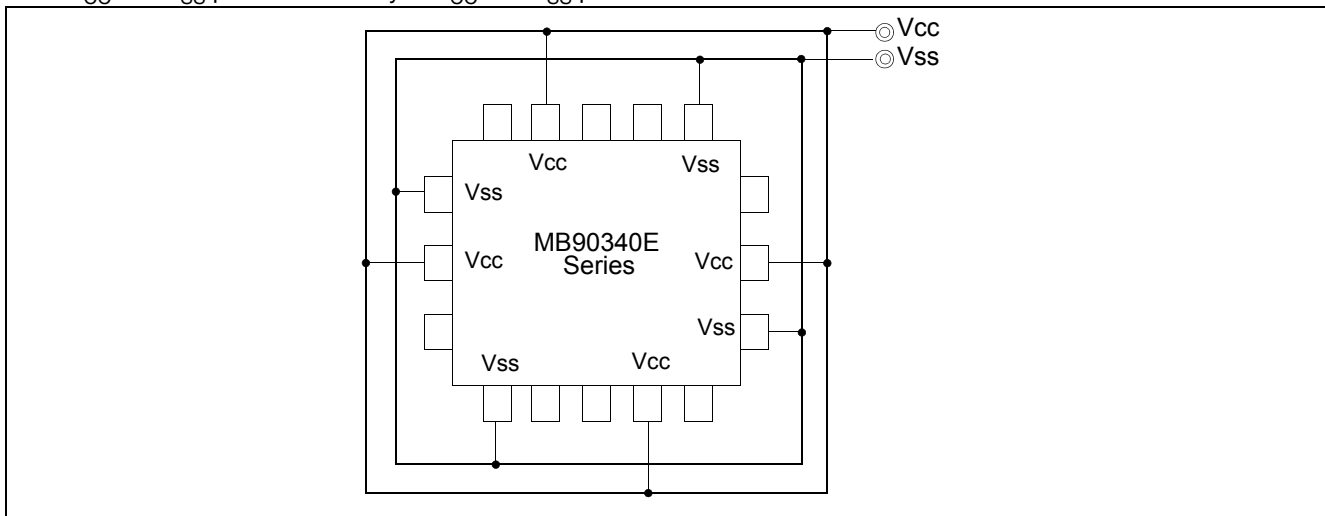
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k $\Omega$  or more.

### 3. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally. Connect  $V_{CC}$  and  $V_{SS}$  pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1  $\mu F$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



### 4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to  $V_{CC}$  or  $V_{SS}$  pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.



**5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs**

Make sure to turn on the A/D converter power supply ( $AV_{CC}$ ,  $AVRH$ ,  $AVRL$ ) and analog inputs ( $AN0$  to  $AN23$ ) after turning-on the digital power supply ( $V_{CC}$ ).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed  $AVRH$  or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

**6. Connection of Unused A/D Converter Pins when the A/D Converter is Used**

Connect unused pins of A/D converter to  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVRH = AVRL = V_{SS}$ .

**7. Crystal Oscillator Circuit**

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

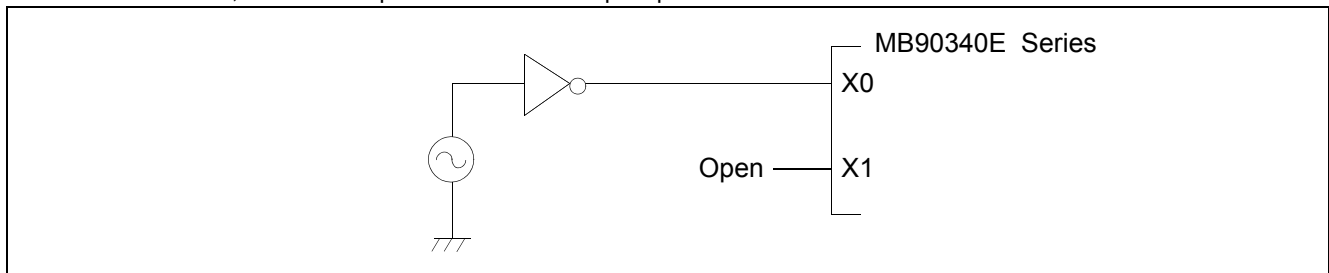
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

**8. Pull-up/down resistors**

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

**9. Using external clock**

To use an external clock, drive the X0 pin and leave the X1 pin open.



**10. Precautions when not using a sub clock signal**

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

**11. Notes on operation in PLL clock mode**

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

**12. Notes on Power-On**

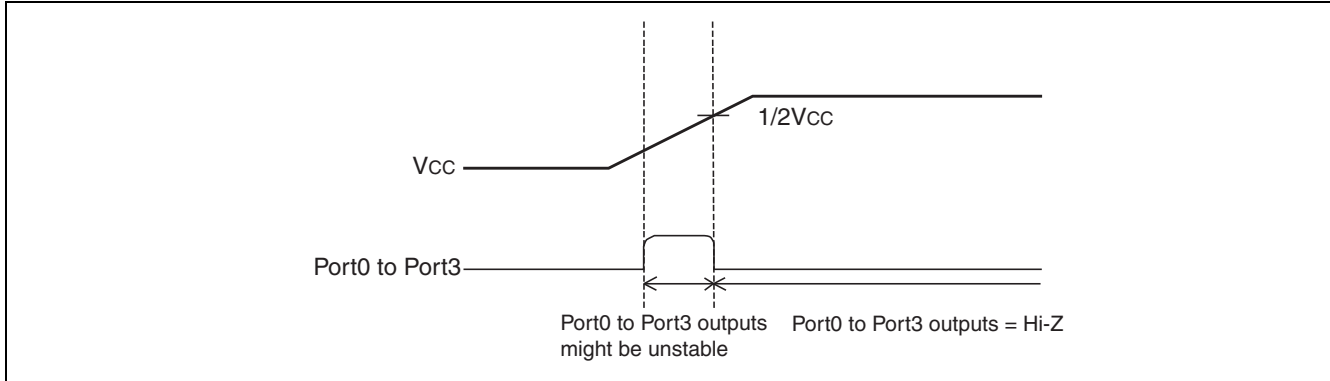
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50  $\mu$ s or more (0.2 V to 2.7 V)

**13. Stabilization of power supply voltage**

A sudden change in the supply voltage may cause the device to malfunction even within the  $V_{CC}$  supply voltage operating range. Therefore, the  $V_{CC}$  supply voltage should be stabilized. For reference, the supply voltage should be controlled so that  $V_{CC}$  ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard  $V_{CC}$  supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

**14. Port 0 to Port 3 Output During Power-on (External-bus Mode)**

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



**15. Notes on Using the CAN Function**

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

**16. Flash Security Function (except for MB90F346E)**

A security bit is located in the area of the flash memory.

If protection code 01<sub>H</sub> is written in the security bit, the flash memory is in the protected state by security.

Therefore please do not write 01<sub>H</sub> in this address if you do not use the security function.

Refer to following table for the address of the security bit.

	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	FE0001 <sub>H</sub>
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	FC0001 <sub>H</sub>
MB90F345E	Embedded 4 Mbits Flash Memory	F80001 <sub>H</sub>

**17. Serial Communication**

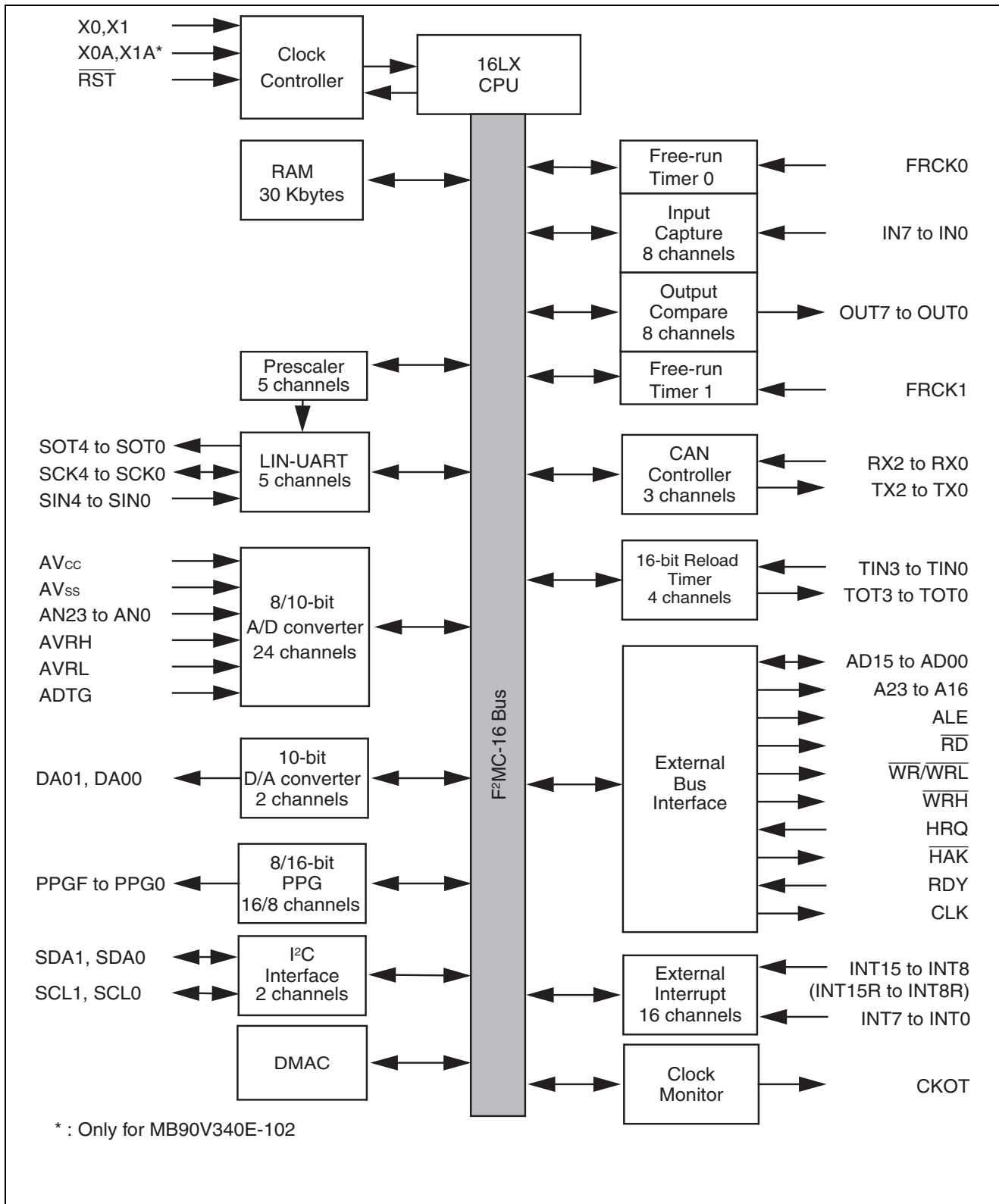
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

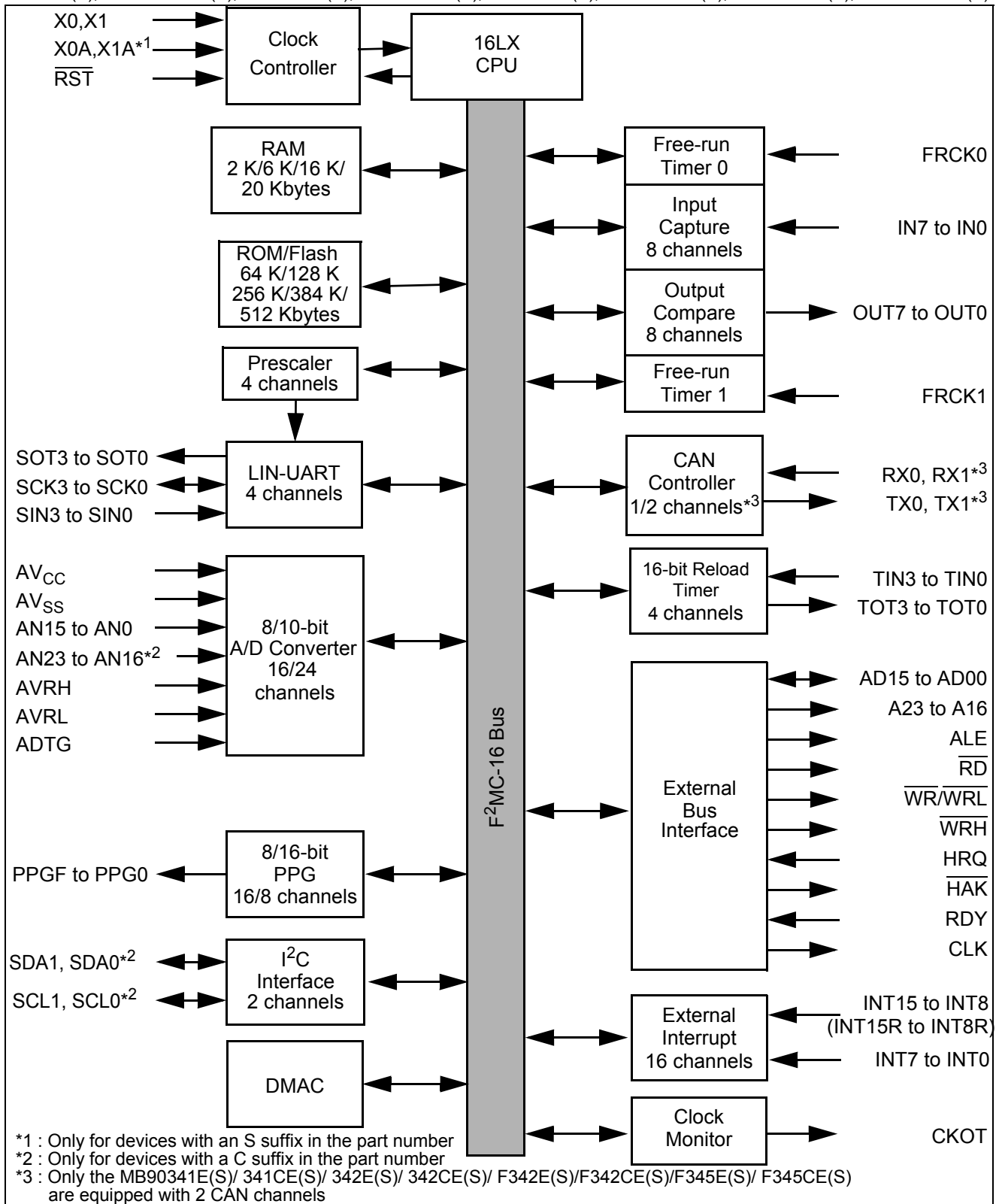
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

**6. Block Diagrams**

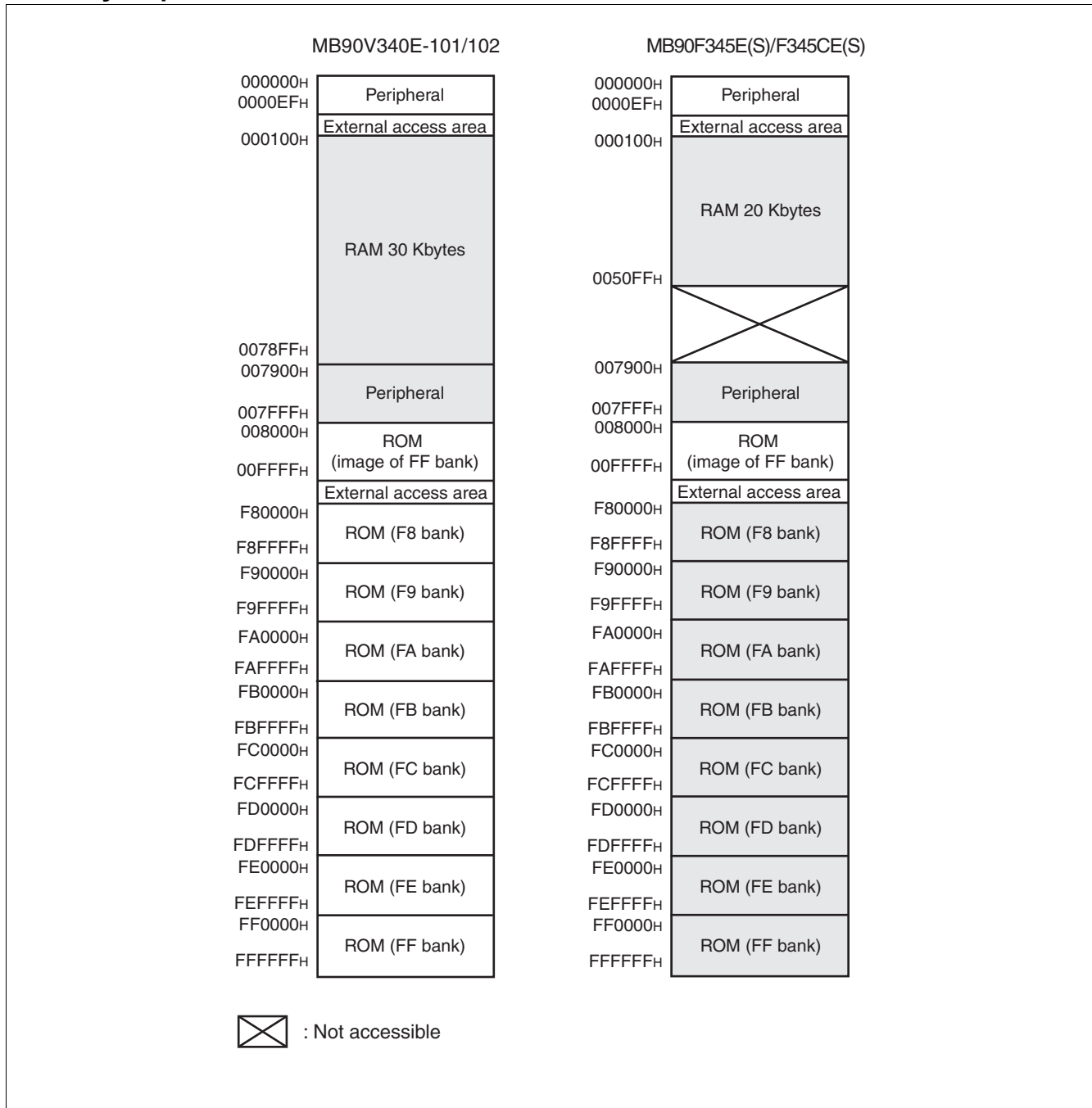
■ MB90V340E-101/102

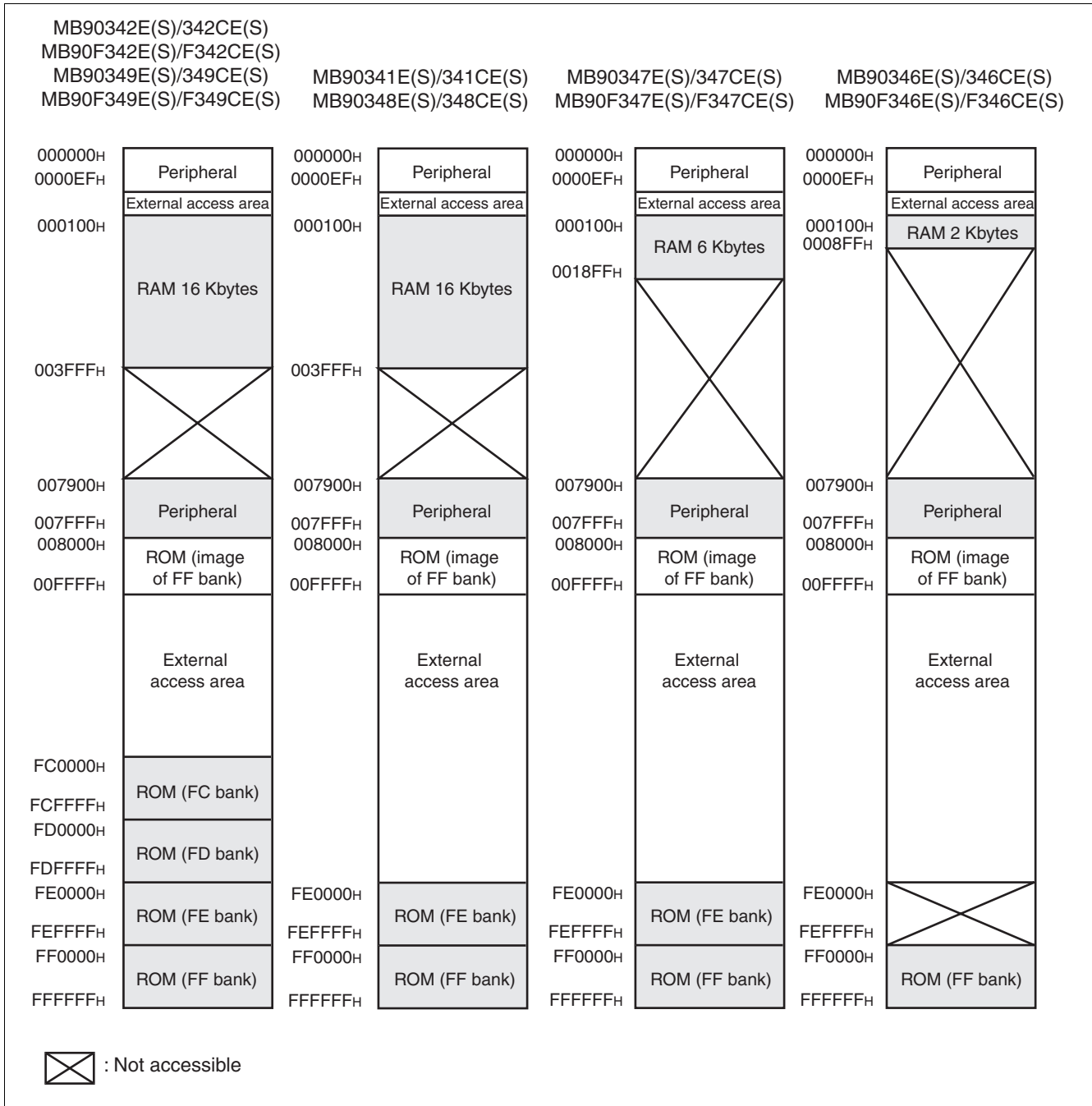


■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



## 7. Memory Map





**Note:** :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.

For example, when the address 00C000<sub>H</sub> is accessed, the data at FFC000<sub>H</sub> in ROM is actually accessed. The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00. As a result, the image between FF8000<sub>H</sub> and FFFFFFF<sub>H</sub> is visible in bank 00, while the image between FF0000<sub>H</sub> and FF7FFF<sub>H</sub> is visible only in bank FF.

**8. I/O Map**

Address	Register	Abbreviation	Access	Resource name	Initial value
000000 <sub>H</sub>	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX <sub>B</sub>
000001 <sub>H</sub>	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX <sub>B</sub>
000002 <sub>H</sub>	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX <sub>B</sub>
000003 <sub>H</sub>	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX <sub>B</sub>
000004 <sub>H</sub>	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX <sub>B</sub>
000005 <sub>H</sub>	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX <sub>B</sub>
000006 <sub>H</sub>	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX <sub>B</sub>
000007 <sub>H</sub>	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX <sub>B</sub>
000008 <sub>H</sub>	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX <sub>B</sub>
000009 <sub>H</sub>	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX <sub>B</sub>
00000A <sub>H</sub>	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX <sub>B</sub>
00000B <sub>H</sub>	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	1111111 <sub>B</sub>
00000C <sub>H</sub>	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	1111111 <sub>B</sub>
00000D <sub>H</sub>	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	1111111 <sub>B</sub>
00000E <sub>H</sub>	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXX <sub>B</sub>
00000F <sub>H</sub>	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXX <sub>B</sub>
000010 <sub>H</sub>	Port 0 Direction Register	DDR0	R/W	Port 0	0000000 <sub>B</sub>
000011 <sub>H</sub>	Port 1 Direction Register	DDR1	R/W	Port 1	0000000 <sub>B</sub>
000012 <sub>H</sub>	Port 2 Direction Register	DDR2	R/W	Port 2	0000000 <sub>B</sub>
000013 <sub>H</sub>	Port 3 Direction Register	DDR3	R/W	Port 3	0000000 <sub>B</sub>
000014 <sub>H</sub>	Port 4 Direction Register	DDR4	R/W	Port 4	0000000 <sub>B</sub>
000015 <sub>H</sub>	Port 5 Direction Register	DDR5	R/W	Port 5	0000000 <sub>B</sub>
000016 <sub>H</sub>	Port 6 Direction Register	DDR6	R/W	Port 6	0000000 <sub>B</sub>
000017 <sub>H</sub>	Port 7 Direction Register	DDR7	R/W	Port 7	0000000 <sub>B</sub>
000018 <sub>H</sub>	Port 8 Direction Register	DDR8	R/W	Port 8	0000000 <sub>B</sub>
000019 <sub>H</sub>	Port 9 Direction Register	DDR9	R/W	Port 9	0000000 <sub>B</sub>
00001A <sub>H</sub>	Port A Direction Register	DDRA	R/W	Port A	0000100 <sub>B</sub>
00001B <sub>H</sub>	Reserved				
00001C <sub>H</sub>	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	0000000 <sub>B</sub>
00001D <sub>H</sub>	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	0000000 <sub>B</sub>
00001E <sub>H</sub>	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	0000000 <sub>B</sub>
00001F <sub>H</sub>	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	0000000 <sub>B</sub>

*(Continued)*

Address	Register	Abbreviation	Access	Resource name	Initial value
000020 <sub>H</sub>	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000 <sub>B</sub>
000021 <sub>H</sub>	Serial Control Register 0	SCR0	W,R/W		00000000 <sub>B</sub>
000022 <sub>H</sub>	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000 <sub>B</sub>
000023 <sub>H</sub>	Serial Status Register 0	SSR0	R,R/W		00001000 <sub>B</sub>
000024 <sub>H</sub>	Extended Communication Control Register 0	ECCR0	R,W,R/W		000000XX <sub>B</sub>
000025 <sub>H</sub>	Extended Status/Control Register 0	ESCR0	R/W		00000100 <sub>B</sub>
000026 <sub>H</sub>	Baud Rate Generator Register 00	BGR00	R/W		00000000 <sub>B</sub>
000027 <sub>H</sub>	Baud Rate Generator Register 01	BGR01	R/W		00000000 <sub>B</sub>
000028 <sub>H</sub>	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000 <sub>B</sub>
000029 <sub>H</sub>	Serial Control Register 1	SCR1	W,R/W		00000000 <sub>B</sub>
00002A <sub>H</sub>	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000 <sub>B</sub>
00002B <sub>H</sub>	Serial Status Register 1	SSR1	R,R/W		00001000 <sub>B</sub>
00002C <sub>H</sub>	Extended Communication Control Register 1	ECCR1	R,W,R/W		000000XX <sub>B</sub>
00002D <sub>H</sub>	Extended Status/Control Register 1	ESCR1	R/W		00000100 <sub>B</sub>
00002E <sub>H</sub>	Baud Rate Generator Register 10	BGR10	R/W		00000000 <sub>B</sub>
00002F <sub>H</sub>	Baud Rate Generator Register 11	BGR11	R/W		00000000 <sub>B</sub>
000030 <sub>H</sub>	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1 <sub>B</sub>
000031 <sub>H</sub>	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001 <sub>B</sub>
000032 <sub>H</sub>	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0 <sub>B</sub>
000033 <sub>H</sub>	Reserved				
000034 <sub>H</sub>	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1 <sub>B</sub>
000035 <sub>H</sub>	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001 <sub>B</sub>
000036 <sub>H</sub>	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0 <sub>B</sub>
000037 <sub>H</sub>	Reserved				
000038 <sub>H</sub>	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1 <sub>B</sub>
000039 <sub>H</sub>	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001 <sub>B</sub>
00003A <sub>H</sub>	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0 <sub>B</sub>
00003B <sub>H</sub>	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 <sub>B</sub>
00003C <sub>H</sub>	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1 <sub>B</sub>
00003D <sub>H</sub>	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001 <sub>B</sub>
00003E <sub>H</sub>	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0 <sub>B</sub>
00003F <sub>H</sub>	Reserved				

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Address	Register	Abbreviation	Access	Resource name	Initial value
000040 <sub>H</sub>	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1 <sub>B</sub>
000041 <sub>H</sub>	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001 <sub>B</sub>
000042 <sub>H</sub>	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0 <sub>B</sub>
000043 <sub>H</sub>	Reserved				
000044 <sub>H</sub>	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1 <sub>B</sub>
000045 <sub>H</sub>	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001 <sub>B</sub>
000046 <sub>H</sub>	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0 <sub>B</sub>
000047 <sub>H</sub>	Reserved				
000048 <sub>H</sub>	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1 <sub>B</sub>
000049 <sub>H</sub>	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 <sub>B</sub>
00004A <sub>H</sub>	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 <sub>B</sub>
00004B <sub>H</sub>	Reserved				
00004C <sub>H</sub>	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1 <sub>B</sub>
00004D <sub>H</sub>	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 <sub>B</sub>
00004E <sub>H</sub>	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 <sub>B</sub>
00004F <sub>H</sub>	Reserved				
000050 <sub>H</sub>	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 <sub>B</sub>
000051 <sub>H</sub>	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX <sub>B</sub>
000052 <sub>H</sub>	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 <sub>B</sub>
000053 <sub>H</sub>	Input Capture Edge 2/3	ICE23	R		XXXXXXXX <sub>B</sub>
000054 <sub>H</sub>	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 <sub>B</sub>
000055 <sub>H</sub>	Input Capture Edge 4/5	ICE45	R		XXXXXXXX <sub>B</sub>
000056 <sub>H</sub>	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000 <sub>B</sub>
000057 <sub>H</sub>	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX <sub>B</sub>
000058 <sub>H</sub>	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 <sub>B</sub>
000059 <sub>H</sub>	Output Compare Control Status 1	OCS1	R/W		0XX00000 <sub>B</sub>
00005A <sub>H</sub>	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 <sub>B</sub>
00005B <sub>H</sub>	Output Compare Control Status 3	OCS3	R/W		0XX00000 <sub>B</sub>
00005C <sub>H</sub>	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 <sub>B</sub>
00005D <sub>H</sub>	Output Compare Control Status 5	OCS5	R/W		0XX00000 <sub>B</sub>
00005E <sub>H</sub>	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 <sub>B</sub>
00005F <sub>H</sub>	Output Compare Control Status 7	OCS7	R/W		0XX00000 <sub>B</sub>

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Address	Register	Abbreviation	Access	Resource name	Initial value
000060 <sub>H</sub>	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 <sub>B</sub>
000061 <sub>H</sub>	Timer Control Status 0	TMCSR0	R/W		XXXX0000 <sub>B</sub>
000062 <sub>H</sub>	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 <sub>B</sub>
000063 <sub>H</sub>	Timer Control Status 1	TMCSR1	R/W		XXXX0000 <sub>B</sub>
000064 <sub>H</sub>	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000 <sub>B</sub>
000065 <sub>H</sub>	Timer Control Status 2	TMCSR2	R/W		XXXX0000 <sub>B</sub>
000066 <sub>H</sub>	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000 <sub>B</sub>
000067 <sub>H</sub>	Timer Control Status 3	TMCSR3	R/W		XXXX0000 <sub>B</sub>
000068 <sub>H</sub>	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0 <sub>B</sub>
000069 <sub>H</sub>	A/D Control Status 1	ADCS1	R/W		0000000X <sub>B</sub>
00006A <sub>H</sub>	A/D Data 0	ADCR0	R		00000000 <sub>B</sub>
00006B <sub>H</sub>	A/D Data 1	ADCR1	R		XXXXXX00 <sub>B</sub>
00006C <sub>H</sub>	ADC Setting 0	ADSR0	R/W		00000000 <sub>B</sub>
00006D <sub>H</sub>	ADC Setting 1	ADSR1	R/W		00000000 <sub>B</sub>
00006E <sub>H</sub>	Reserved				
00006F <sub>H</sub>	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXXX1 <sub>B</sub>
000070 <sub>H</sub> to 00008F <sub>H</sub>	Reserved for CAN Controller 0/1. Refer to "CAN Controllers"				
000090 <sub>H</sub> to 00009A <sub>H</sub>	Reserved				
00009B <sub>H</sub>	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000 <sub>B</sub>
00009C <sub>H</sub>	DMA Status L Register	DSRL	R/W		00000000 <sub>B</sub>
00009D <sub>H</sub>	DMA Status H Register	DSRH	R/W		00000000 <sub>B</sub>
00009E <sub>H</sub>	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 <sub>B</sub>
00009F <sub>H</sub>	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXXX0 <sub>B</sub>
0000A0 <sub>H</sub>	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000 <sub>B</sub>
0000A1 <sub>H</sub>	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100 <sub>B</sub>
0000A2 <sub>H</sub> , 0000A3 <sub>H</sub>	Reserved				
0000A4 <sub>H</sub>	DMA Stop Status Register	DSSR	R/W	DMA	00000000 <sub>B</sub>

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Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5 <sub>H</sub>	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 <sub>B</sub>
0000A6 <sub>H</sub>	External Address Output Control Register	HACR	W		00000000 <sub>B</sub>
0000A7 <sub>H</sub>	Bus Control Signal Selection Register	ECSR	W		0000000X <sub>B</sub>
0000A8 <sub>H</sub>	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXXX11 <sub>B</sub>
0000A9 <sub>H</sub>	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 <sub>B</sub>
0000AA <sub>H</sub>	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 <sub>B</sub>
0000AB <sub>H</sub>	Reserved				
0000AC <sub>H</sub>	DMA Enable L Register	DERL	R/W	DMA	00000000 <sub>B</sub>
0000AD <sub>H</sub>	DMA Enable H Register	DERH	R/W		00000000 <sub>B</sub>
0000AE <sub>H</sub>	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 <sub>B</sub>
0000AF <sub>H</sub>	Reserved				
0000B0 <sub>H</sub>	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 <sub>B</sub>
0000B1 <sub>H</sub>	Interrupt Control Register 01	ICR01	W,R/W		00000111 <sub>B</sub>
0000B2 <sub>H</sub>	Interrupt Control Register 02	ICR02	W,R/W		00000111 <sub>B</sub>
0000B3 <sub>H</sub>	Interrupt Control Register 03	ICR03	W,R/W		00000111 <sub>B</sub>
0000B4 <sub>H</sub>	Interrupt Control Register 04	ICR04	W,R/W		00000111 <sub>B</sub>
0000B5 <sub>H</sub>	Interrupt Control Register 05	ICR05	W,R/W		00000111 <sub>B</sub>
0000B6 <sub>H</sub>	Interrupt Control Register 06	ICR06	W,R/W		00000111 <sub>B</sub>
0000B7 <sub>H</sub>	Interrupt Control Register 07	ICR07	W,R/W		00000111 <sub>B</sub>
0000B8 <sub>H</sub>	Interrupt Control Register 08	ICR08	W,R/W		00000111 <sub>B</sub>
0000B9 <sub>H</sub>	Interrupt Control Register 09	ICR09	W,R/W		00000111 <sub>B</sub>
0000BA <sub>H</sub>	Interrupt Control Register 10	ICR10	W,R/W		00000111 <sub>B</sub>
0000BB <sub>H</sub>	Interrupt Control Register 11	ICR11	W,R/W		00000111 <sub>B</sub>
0000BC <sub>H</sub>	Interrupt Control Register 12	ICR12	W,R/W		00000111 <sub>B</sub>
0000BD <sub>H</sub>	Interrupt Control Register 13	ICR13	W,R/W		00000111 <sub>B</sub>
0000BE <sub>H</sub>	Interrupt Control Register 14	ICR14	W,R/W		00000111 <sub>B</sub>
0000BF <sub>H</sub>	Interrupt Control Register 15	ICR15	W,R/W		00000111 <sub>B</sub>
0000C0 <sub>H</sub>	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX <sub>B</sub>
0000C1 <sub>H</sub>	D/A Converter Data 1	DAT1	R/W		XXXXXXXX <sub>B</sub>
0000C2 <sub>H</sub>	D/A Control 0	DACR0	R/W		XXXXXXXX0 <sub>B</sub>
0000C3 <sub>H</sub>	D/A Control 1	DACR1	R/W		XXXXXXXX0 <sub>B</sub>

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Address	Register	Abbreviation	Access	Resource name	Initial value
0000C4 <sub>H</sub> , 0000C5 <sub>H</sub>	Reserved				
0000C6 <sub>H</sub>	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000 <sub>B</sub>
0000C7 <sub>H</sub>	External Interrupt Source 0	EIRR0	R/W		XXXXXXXX <sub>B</sub>
0000C8 <sub>H</sub>	External Interrupt Level Setting 0	ELVR0	R/W		00000000 <sub>B</sub>
0000C9 <sub>H</sub>	External Interrupt Level Setting 0	ELVR0	R/W		00000000 <sub>B</sub>
0000CA <sub>H</sub>	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000 <sub>B</sub>
0000CB <sub>H</sub>	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX <sub>B</sub>
0000CC <sub>H</sub>	External Interrupt Level Setting 1	ELVR1	R/W		00000000 <sub>B</sub>
0000CD <sub>H</sub>	External Interrupt Level Setting 1	ELVR1	R/W		00000000 <sub>B</sub>
0000CE <sub>H</sub>	External Interrupt Source Select	EISSR	R/W		00000000 <sub>B</sub>
0000CF <sub>H</sub>	PLL/Sub clock Control Register	PSCCR	W	PLL	XXXX0000 <sub>B</sub>
0000D0 <sub>H</sub>	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXX <sub>B</sub>
0000D1 <sub>H</sub>	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXX <sub>B</sub>
0000D2 <sub>H</sub>	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXX <sub>B</sub>
0000D3 <sub>H</sub>	DMA Control Register	DMACS	R/W		XXXXXXXX <sub>B</sub>
0000D4 <sub>H</sub>	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX <sub>B</sub>
0000D5 <sub>H</sub>	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX <sub>B</sub>
0000D6 <sub>H</sub>	Data Counter L Register	DCTL	R/W		XXXXXXXX <sub>B</sub>
0000D7 <sub>H</sub>	Data Counter H Register	DCTH	R/W		XXXXXXXX <sub>B</sub>
0000D8 <sub>H</sub>	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000 <sub>B</sub>
0000D9 <sub>H</sub>	Serial Control Register 2	SCR2	W,R/W		00000000 <sub>B</sub>
0000DA <sub>H</sub>	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000 <sub>B</sub>
0000DB <sub>H</sub>	Serial Status Register 2	SSR2	R,R/W		00001000 <sub>B</sub>
0000DC <sub>H</sub>	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX <sub>B</sub>
0000DD <sub>H</sub>	Extended Status Control Register 2	ESCR2	R/W		00000100 <sub>B</sub>
0000DE <sub>H</sub>	Baud Rate Generator Register 20	BGR20	R/W		00000000 <sub>B</sub>
0000DF <sub>H</sub>	Baud Rate Generator Register 21	BGR21	R/W		00000000 <sub>B</sub>
0000E0 <sub>H</sub> to 0000EF <sub>H</sub>	Reserved for CAN Controller 2. Refer to "CAN Controllers"				
0000F0 <sub>H</sub> to 0000FF <sub>H</sub>	External				

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Address	Register	Abbreviation	Access	Resource name	Initial value
007900 <sub>H</sub>	Reload Register L0	PRL0	R/W	16-bit PPG 0/1	XXXXXXXX <sub>B</sub>
007901 <sub>H</sub>	Reload Register H0	PRLH0	R/W		XXXXXXXX <sub>B</sub>
007902 <sub>H</sub>	Reload Register L1	PRL1	R/W		XXXXXXXX <sub>B</sub>
007903 <sub>H</sub>	Reload Register H1	PRLH1	R/W		XXXXXXXX <sub>B</sub>
007904 <sub>H</sub>	Reload Register L2	PRL2	R/W	16-bit PPG 2/3	XXXXXXXX <sub>B</sub>
007905 <sub>H</sub>	Reload Register H2	PRLH2	R/W		XXXXXXXX <sub>B</sub>
007906 <sub>H</sub>	Reload Register L3	PRL3	R/W		XXXXXXXX <sub>B</sub>
007907 <sub>H</sub>	Reload Register H3	PRLH3	R/W		XXXXXXXX <sub>B</sub>
007908 <sub>H</sub>	Reload Register L4	PRL4	R/W	16-bit PPG 4/5	XXXXXXXX <sub>B</sub>
007909 <sub>H</sub>	Reload Register H4	PRLH4	R/W		XXXXXXXX <sub>B</sub>
00790A <sub>H</sub>	Reload Register L5	PRL5	R/W		XXXXXXXX <sub>B</sub>
00790B <sub>H</sub>	Reload Register H5	PRLH5	R/W		XXXXXXXX <sub>B</sub>
00790C <sub>H</sub>	Reload Register L6	PRL6	R/W	16-bit PPG 6/7	XXXXXXXX <sub>B</sub>
00790D <sub>H</sub>	Reload Register H6	PRLH6	R/W		XXXXXXXX <sub>B</sub>
00790E <sub>H</sub>	Reload Register L7	PRL7	R/W		XXXXXXXX <sub>B</sub>
00790F <sub>H</sub>	Reload Register H7	PRLH7	R/W		XXXXXXXX <sub>B</sub>
007910 <sub>H</sub>	Reload Register L8	PRL8	R/W	16-bit PPG 8/9	XXXXXXXX <sub>B</sub>
007911 <sub>H</sub>	Reload Register H8	PRLH8	R/W		XXXXXXXX <sub>B</sub>
007912 <sub>H</sub>	Reload Register L9	PRL9	R/W		XXXXXXXX <sub>B</sub>
007913 <sub>H</sub>	Reload Register H9	PRLH9	R/W		XXXXXXXX <sub>B</sub>
007914 <sub>H</sub>	Reload Register LA	PRLA	R/W	16-bit PPG A/B	XXXXXXXX <sub>B</sub>
007915 <sub>H</sub>	Reload Register HA	PRLHA	R/W		XXXXXXXX <sub>B</sub>
007916 <sub>H</sub>	Reload Register LB	PRLB	R/W		XXXXXXXX <sub>B</sub>
007917 <sub>H</sub>	Reload Register HB	PRLHB	R/W		XXXXXXXX <sub>B</sub>
007918 <sub>H</sub>	Reload Register LC	PRLC	R/W	16-bit PPG C/D	XXXXXXXX <sub>B</sub>
007919 <sub>H</sub>	Reload Register HC	PRLHC	R/W		XXXXXXXX <sub>B</sub>
00791A <sub>H</sub>	Reload Register LD	PRLD	R/W		XXXXXXXX <sub>B</sub>
00791B <sub>H</sub>	Reload Register HD	PRLHD	R/W		XXXXXXXX <sub>B</sub>
00791C <sub>H</sub>	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX <sub>B</sub>
00791D <sub>H</sub>	Reload Register HE	PRLHE	R/W		XXXXXXXX <sub>B</sub>
00791E <sub>H</sub>	Reload Register LF	PRLLF	R/W		XXXXXXXX <sub>B</sub>
00791F <sub>H</sub>	Reload Register HF	PRLHF	R/W		XXXXXXXX <sub>B</sub>
007920 <sub>H</sub>	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX <sub>B</sub>
007921 <sub>H</sub>	Input Capture 0	IPCP0	R		XXXXXXXX <sub>B</sub>
007922 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX <sub>B</sub>
007923 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX <sub>B</sub>

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Address	Register	Abbreviation	Access	Resource name	Initial value
007924 <sub>H</sub>	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX <sub>B</sub>
007925 <sub>H</sub>	Input Capture 2	IPCP2	R		XXXXXXXX <sub>B</sub>
007926 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX <sub>B</sub>
007927 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX <sub>B</sub>
007928 <sub>H</sub>	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX <sub>B</sub>
007929 <sub>H</sub>	Input Capture 4	IPCP4	R		XXXXXXXX <sub>B</sub>
00792A <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX <sub>B</sub>
00792B <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX <sub>B</sub>
00792C <sub>H</sub>	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX <sub>B</sub>
00792D <sub>H</sub>	Input Capture 6	IPCP6	R		XXXXXXXX <sub>B</sub>
00792E <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXX <sub>B</sub>
00792F <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXX <sub>B</sub>
007930 <sub>H</sub>	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX <sub>B</sub>
007931 <sub>H</sub>	Output Compare 0	OCCP0	R/W		XXXXXXXX <sub>B</sub>
007932 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
007933 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
007934 <sub>H</sub>	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX <sub>B</sub>
007935 <sub>H</sub>	Output Compare 2	OCCP2	R/W		XXXXXXXX <sub>B</sub>
007936 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
007937 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
007938 <sub>H</sub>	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX <sub>B</sub>
007939 <sub>H</sub>	Output Compare 4	OCCP4	R/W		XXXXXXXX <sub>B</sub>
00793A <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX <sub>B</sub>
00793B <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX <sub>B</sub>
00793C <sub>H</sub>	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX <sub>B</sub>
00793D <sub>H</sub>	Output Compare 6	OCCP6	R/W		XXXXXXXX <sub>B</sub>
00793E <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX <sub>B</sub>
00793F <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX <sub>B</sub>
007940 <sub>H</sub>	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 <sub>B</sub>
007941 <sub>H</sub>	Timer Data 0	TCDT0	R/W		00000000 <sub>B</sub>
007942 <sub>H</sub>	Timer Control Status 0	TCCSL0	R/W		00000000 <sub>B</sub>
007943 <sub>H</sub>	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX <sub>B</sub>
007944 <sub>H</sub>	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000 <sub>B</sub>
007945 <sub>H</sub>	Timer Data 1	TCDT1	R/W		00000000 <sub>B</sub>
007946 <sub>H</sub>	Timer Control Status 1	TCCSL1	R/W		00000000 <sub>B</sub>
007947 <sub>H</sub>	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXX <sub>B</sub>

*(Continued)*

Address	Register	Abbreviation	Access	Resource name	Initial value	
007948 <sub>H</sub>	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX <sub>B</sub>	
007949 <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>	
00794A <sub>H</sub>	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX <sub>B</sub>	
00794B <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>	
00794C <sub>H</sub>	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX <sub>B</sub>	
00794D <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>	
00794E <sub>H</sub>	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX <sub>B</sub>	
00794F <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>	
007950 <sub>H</sub>	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000 <sub>B</sub>	
007951 <sub>H</sub>	Serial Control Register 3	SCR3	W,R/W		00000000 <sub>B</sub>	
007952 <sub>H</sub>	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000 <sub>B</sub>	
007953 <sub>H</sub>	Serial Status Register 3	SSR3	R,R/W		00001000 <sub>B</sub>	
007954 <sub>H</sub>	Extended Communication Control Register 3	ECCR3	R,W,R/W		000000XX <sub>B</sub>	
007955 <sub>H</sub>	Extended Status Control Register	ESCR3	R/W		00000100 <sub>B</sub>	
007956 <sub>H</sub>	Baud Rate Generator Register 30	BGR30	R/W		00000000 <sub>B</sub>	
007957 <sub>H</sub>	Baud Rate Generator Register 31	BGR31	R/W		00000000 <sub>B</sub>	
007958 <sub>H</sub>	Serial Mode Register 4	SMR4	W,R/W		UART4	00000000 <sub>B</sub>
007959 <sub>H</sub>	Serial Control Register 4	SCR4	W,R/W			00000000 <sub>B</sub>
00795A <sub>H</sub>	Reception/Transmission Data Register 4	RDR4/TDR4	R/W	00000000 <sub>B</sub>		
00795B <sub>H</sub>	Serial Status Register 4	SSR4	R,R/W	00001000 <sub>B</sub>		
00795C <sub>H</sub>	Extended Communication Control Register 4	ECCR4	R,W,R/W	000000XX <sub>B</sub>		
00795D <sub>H</sub>	Extended Status Control Register	ESCR4	R/W	00000100 <sub>B</sub>		
00795E <sub>H</sub>	Baud Rate Generator Register 40	BGR40	R/W	00000000 <sub>B</sub>		
00795F <sub>H</sub>	Baud Rate Generator Register 41	BGR41	R/W	00000000 <sub>B</sub>		
007960 <sub>H</sub> to 00796B <sub>H</sub>	Reserved					
00796C <sub>H</sub>	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000 <sub>B</sub>	
00796D <sub>H</sub>	Reserved					
00796E <sub>H</sub>	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	XXXXXXXX0 <sub>B</sub>	
00796F <sub>H</sub>	CAN Switch Register	CANSWR	R/W	CAN 0/1	XXXXXXXX0 <sub>B</sub>	

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007970 <sub>H</sub>	I <sup>2</sup> C Bus Status Register 0	IBSR0	R	I <sup>2</sup> C Interface 0	00000000 <sub>B</sub>
007971 <sub>H</sub>	I <sup>2</sup> C Bus Control Register 0	IBCR0	W,R/W		00000000 <sub>B</sub>
007972 <sub>H</sub>	I <sup>2</sup> C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 <sub>B</sub>
007973 <sub>H</sub>		ITBAH0	R/W		00000000 <sub>B</sub>
007974 <sub>H</sub>	I <sup>2</sup> C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 <sub>B</sub>
007975 <sub>H</sub>		ITMKH0	R/W		00111111 <sub>B</sub>
007976 <sub>H</sub>	I <sup>2</sup> C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 <sub>B</sub>
007977 <sub>H</sub>	I <sup>2</sup> C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 <sub>B</sub>
007978 <sub>H</sub>	I <sup>2</sup> C Data Register 0	IDAR0	R/W		00000000 <sub>B</sub>
007979 <sub>H</sub> , 00797A <sub>H</sub>	Reserved				
00797B <sub>H</sub>	I <sup>2</sup> C Clock Control Register 0	ICCR0	R/W	I <sup>2</sup> C Interface 0	00011111 <sub>B</sub>
00797C <sub>H</sub> to 00797F <sub>H</sub>	Reserved				
007980 <sub>H</sub>	I <sup>2</sup> C Bus Status Register 1	IBSR1	R	I <sup>2</sup> C Interface 1	00000000 <sub>B</sub>
007981 <sub>H</sub>	I <sup>2</sup> C Bus Control Register 1	IBCR1	W,R/W		00000000 <sub>B</sub>
007982 <sub>H</sub>	I <sup>2</sup> C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000 <sub>B</sub>
007983 <sub>H</sub>		ITBAH1	R/W		00000000 <sub>B</sub>
007984 <sub>H</sub>	I <sup>2</sup> C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111 <sub>B</sub>
007985 <sub>H</sub>		ITMKH1	R/W		00111111 <sub>B</sub>
007986 <sub>H</sub>	I <sup>2</sup> C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 <sub>B</sub>
007987 <sub>H</sub>	I <sup>2</sup> C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 <sub>B</sub>
007988 <sub>H</sub>	I <sup>2</sup> C Data Register 1	IDAR1	R/W		00000000 <sub>B</sub>
007989 <sub>H</sub> , 00798A <sub>H</sub>	Reserved				
00798B <sub>H</sub>	I <sup>2</sup> C Clock Control Register 1	ICCR1	R/W	I <sup>2</sup> C Interface 1	00011111 <sub>B</sub>
00798C <sub>H</sub> to 0079C1 <sub>H</sub>	Reserved				
0079C2 <sub>H</sub>	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 <sub>B</sub>
0079C3 <sub>H</sub> to 0079DF <sub>H</sub>	Reserved				

(Continued)



(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0079E0 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX <sub>B</sub>
0079E1 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W		XXXXXXXX <sub>B</sub>
0079E2 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W		XXXXXXXX <sub>B</sub>
0079E3 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX <sub>B</sub>
0079E4 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX <sub>B</sub>
0079E5 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX <sub>B</sub>
0079E6 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX <sub>B</sub>
0079E7 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX <sub>B</sub>
0079E8 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX <sub>B</sub>
0079E9 <sub>H</sub> to 0079EF <sub>H</sub>	Reserved				
0079F0 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX <sub>B</sub>
0079F1 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W		XXXXXXXX <sub>B</sub>
0079F2 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W		XXXXXXXX <sub>B</sub>
0079F3 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX <sub>B</sub>
0079F4 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX <sub>B</sub>
0079F5 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX <sub>B</sub>
0079F6 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX <sub>B</sub>
0079F7 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX <sub>B</sub>
0079F8 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX <sub>B</sub>
0079F9 <sub>H</sub> to 0079FF <sub>H</sub>	Reserved				
007A00 <sub>H</sub> to 007AFF <sub>H</sub>	Reserved for CAN Controller 0. Refer to “CAN Controllers”				
007B00 <sub>H</sub> to 007BFF <sub>H</sub>	Reserved for CAN Controller 0. Refer to “CAN Controllers”				
007C00 <sub>H</sub> to 007CFF <sub>H</sub>	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
007D00 <sub>H</sub> to 007DFF <sub>H</sub>	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
007E00 <sub>H</sub> to 007FFF <sub>H</sub>	Reserved				

**Note:**

- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

## 9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

**List of Control Registers (1)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 <sub>H</sub>	000080 <sub>H</sub>	Message Buffer Valid Register	BVALR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000071 <sub>H</sub>	000081 <sub>H</sub>				
000072 <sub>H</sub>	000082 <sub>H</sub>	Transmit Request Register	TREQR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000073 <sub>H</sub>	000083 <sub>H</sub>				
000074 <sub>H</sub>	000084 <sub>H</sub>	Transmit Cancel Register	TCANR	W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000075 <sub>H</sub>	000085 <sub>H</sub>				
000076 <sub>H</sub>	000086 <sub>H</sub>	Transmission Complete Register	TCR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000077 <sub>H</sub>	000087 <sub>H</sub>				
000078 <sub>H</sub>	000088 <sub>H</sub>	Receive Complete Register	RCR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000079 <sub>H</sub>	000089 <sub>H</sub>				
00007A <sub>H</sub>	00008A <sub>H</sub>	Remote Request Receiving Register	RRTRR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00007B <sub>H</sub>	00008B <sub>H</sub>				
00007C <sub>H</sub>	00008C <sub>H</sub>	Receive Overrun Register	ROVRR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00007D <sub>H</sub>	00008D <sub>H</sub>				
00007E <sub>H</sub>	00008E <sub>H</sub>	Reception Interrupt Enable Register	RIER	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
00007F <sub>H</sub>	00008F <sub>H</sub>				

**List of Control Registers (2)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007B00 <sub>H</sub>	007D00 <sub>H</sub>	Control Status Register	CSR	R/W, W R/W, R	0XXXX0X1 <sub>B</sub> 00XXXX00 <sub>B</sub>
007B01 <sub>H</sub>	007D01 <sub>H</sub>				
007B02 <sub>H</sub>	007D02 <sub>H</sub>	Last Event Indicator Register	LEIR	R/W	000X0000 <sub>B</sub> XXXXXXXX <sub>B</sub>
007B03 <sub>H</sub>	007D03 <sub>H</sub>				
007B04 <sub>H</sub>	007D04 <sub>H</sub>	Receive And Transmit Error Counter	RTEC	R	00000000 <sub>B</sub> 00000000 <sub>B</sub>
007B05 <sub>H</sub>	007D05 <sub>H</sub>				
007B06 <sub>H</sub>	007D06 <sub>H</sub>	Bit Timing Register	BTR	R/W	11111111 <sub>B</sub> X1111111 <sub>B</sub>
007B07 <sub>H</sub>	007D07 <sub>H</sub>				
007B08 <sub>H</sub>	007D08 <sub>H</sub>	IDE Register	IDER	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B09 <sub>H</sub>	007D09 <sub>H</sub>				
007B0A <sub>H</sub>	007D0A <sub>H</sub>	Transmit RTR Register	TRTRR	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
007B0B <sub>H</sub>	007D0B <sub>H</sub>				
007B0C <sub>H</sub>	007D0C <sub>H</sub>	Remote Frame Receive Waiting Register	RFWTR	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B0D <sub>H</sub>	007D0D <sub>H</sub>				
007B0E <sub>H</sub>	007D0E <sub>H</sub>	Transmit Interrupt Enable Register	TIER	R/W	00000000 <sub>B</sub> 00000000 <sub>B</sub>
007B0F <sub>H</sub>	007D0F <sub>H</sub>				
007B10 <sub>H</sub>	007D10 <sub>H</sub>	Acceptance Mask Select Register	AMSR	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B11 <sub>H</sub>	007D11 <sub>H</sub>				
007B12 <sub>H</sub>	007D12 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B13 <sub>H</sub>	007D13 <sub>H</sub>				
007B14 <sub>H</sub>	007D14 <sub>H</sub>	Acceptance Mask Register 0	AMR0	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B15 <sub>H</sub>	007D15 <sub>H</sub>				
007B16 <sub>H</sub>	007D16 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B17 <sub>H</sub>	007D17 <sub>H</sub>				
007B18 <sub>H</sub>	007D18 <sub>H</sub>	Acceptance Mask Register 1	AMR1	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B19 <sub>H</sub>	007D19 <sub>H</sub>				
007B1A <sub>H</sub>	007D1A <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007B1B <sub>H</sub>	007D1B <sub>H</sub>				

**List of Message Buffers (ID Registers) (1)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A00 <sub>H</sub> to 007A1F <sub>H</sub>	007C00 <sub>H</sub> to 007C1F <sub>H</sub>	General- Purpose RAM	—	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007A20 <sub>H</sub>	007C20 <sub>H</sub>	ID Register 0	IDR0	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A21 <sub>H</sub>	007C21 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A22 <sub>H</sub>	007C22 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A23 <sub>H</sub>	007C23 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A24 <sub>H</sub>	007C24 <sub>H</sub>	ID Register 1	IDR1	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A25 <sub>H</sub>	007C25 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A26 <sub>H</sub>	007C26 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A27 <sub>H</sub>	007C27 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A28 <sub>H</sub>	007C28 <sub>H</sub>	ID Register 2	IDR2	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A29 <sub>H</sub>	007C29 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A2A <sub>H</sub>	007C2A <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A2B <sub>H</sub>	007C2B <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A2C <sub>H</sub>	007C2C <sub>H</sub>	ID Register 3	IDR3	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A2D <sub>H</sub>	007C2D <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A2E <sub>H</sub>	007C2E <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A2F <sub>H</sub>	007C2F <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A30 <sub>H</sub>	007C30 <sub>H</sub>	ID Register 4	IDR4	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A31 <sub>H</sub>	007C31 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A32 <sub>H</sub>	007C32 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A33 <sub>H</sub>	007C33 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A34 <sub>H</sub>	007C34 <sub>H</sub>	ID Register 5	IDR5	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A35 <sub>H</sub>	007C35 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A36 <sub>H</sub>	007C36 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A37 <sub>H</sub>	007C37 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A38 <sub>H</sub>	007C38 <sub>H</sub>	ID Register 6	IDR6	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A39 <sub>H</sub>	007C39 <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A3A <sub>H</sub>	007C3A <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A3B <sub>H</sub>	007C3B <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A3C <sub>H</sub>	007C3C <sub>H</sub>	ID Register 7	IDR7	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A3D <sub>H</sub>	007C3D <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A3E <sub>H</sub>	007C3E <sub>H</sub>				XXXXXXXX <sub>B</sub>
007A3F <sub>H</sub>	007C3F <sub>H</sub>				XXXXXXXX <sub>B</sub>

**List of Message Buffers (ID Registers) (2)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A40 <sub>H</sub>	007C40 <sub>H</sub>	ID Register 8	IDR8	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A41 <sub>H</sub>	007C41 <sub>H</sub>				
007A42 <sub>H</sub>	007C42 <sub>H</sub>				
007A43 <sub>H</sub>	007C43 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A44 <sub>H</sub>	007C44 <sub>H</sub>	ID Register 9	IDR9	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A45 <sub>H</sub>	007C45 <sub>H</sub>				
007A46 <sub>H</sub>	007C46 <sub>H</sub>				
007A47 <sub>H</sub>	007C47 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A48 <sub>H</sub>	007C48 <sub>H</sub>	ID Register 10	IDR10	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A49 <sub>H</sub>	007C49 <sub>H</sub>				
007A4A <sub>H</sub>	007C4A <sub>H</sub>				
007A4B <sub>H</sub>	007C4B <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A4C <sub>H</sub>	007C4C <sub>H</sub>	ID Register 11	IDR11	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A4D <sub>H</sub>	007C4D <sub>H</sub>				
007A4E <sub>H</sub>	007C4E <sub>H</sub>				
007A4F <sub>H</sub>	007C4F <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A50 <sub>H</sub>	007C50 <sub>H</sub>	ID Register 12	IDR12	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A51 <sub>H</sub>	007C51 <sub>H</sub>				
007A52 <sub>H</sub>	007C52 <sub>H</sub>				
007A53 <sub>H</sub>	007C53 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A54 <sub>H</sub>	007C54 <sub>H</sub>	ID Register 13	IDR13	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A55 <sub>H</sub>	007C55 <sub>H</sub>				
007A56 <sub>H</sub>	007C56 <sub>H</sub>				
007A57 <sub>H</sub>	007C57 <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A58 <sub>H</sub>	007C58 <sub>H</sub>	ID Register 14	IDR14	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A59 <sub>H</sub>	007C59 <sub>H</sub>				
007A5A <sub>H</sub>	007C5A <sub>H</sub>				
007A5B <sub>H</sub>	007C5B <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A5C <sub>H</sub>	007C5C <sub>H</sub>	ID Register 15	IDR15	R/W	XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
007A5D <sub>H</sub>	007C5D <sub>H</sub>				
007A5E <sub>H</sub>	007C5E <sub>H</sub>				
007A5F <sub>H</sub>	007C5F <sub>H</sub>				XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>

**List of Message Buffers (DLC Registers and Data Registers) (1)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A60 <sub>H</sub>	007C60 <sub>H</sub>	DLC Register 0	DLCR0	R/W	XXXXXXXX <sub>B</sub>
007A61 <sub>H</sub>	007C61 <sub>H</sub>				
007A62 <sub>H</sub>	007C62 <sub>H</sub>	DLC Register 1	DLCR1	R/W	XXXXXXXX <sub>B</sub>
007A63 <sub>H</sub>	007C63 <sub>H</sub>				
007A64 <sub>H</sub>	007C64 <sub>H</sub>	DLC Register 2	DLCR2	R/W	XXXXXXXX <sub>B</sub>
007A65 <sub>H</sub>	007C65 <sub>H</sub>				
007A66 <sub>H</sub>	007C66 <sub>H</sub>	DLC Register 3	DLCR3	R/W	XXXXXXXX <sub>B</sub>
007A67 <sub>H</sub>	007C67 <sub>H</sub>				
007A68 <sub>H</sub>	007C68 <sub>H</sub>	DLC Register 4	DLCR4	R/W	XXXXXXXX <sub>B</sub>
007A69 <sub>H</sub>	007C69 <sub>H</sub>				
007A6A <sub>H</sub>	007C6A <sub>H</sub>	DLC Register 5	DLCR5	R/W	XXXXXXXX <sub>B</sub>
007A6B <sub>H</sub>	007C6B <sub>H</sub>				
007A6C <sub>H</sub>	007C6C <sub>H</sub>	DLC Register 6	DLCR6	R/W	XXXXXXXX <sub>B</sub>
007A6D <sub>H</sub>	007C6D <sub>H</sub>				
007A6E <sub>H</sub>	007C6E <sub>H</sub>	DLC Register 7	DLCR7	R/W	XXXXXXXX <sub>B</sub>
007A6F <sub>H</sub>	007C6F <sub>H</sub>				
007A70 <sub>H</sub>	007C70 <sub>H</sub>	DLC Register 8	DLCR8	R/W	XXXXXXXX <sub>B</sub>
007A71 <sub>H</sub>	007C71 <sub>H</sub>				
007A72 <sub>H</sub>	007C72 <sub>H</sub>	DLC Register 9	DLCR9	R/W	XXXXXXXX <sub>B</sub>
007A73 <sub>H</sub>	007C73 <sub>H</sub>				
007A74 <sub>H</sub>	007C74 <sub>H</sub>	DLC Register 10	DLCR10	R/W	XXXXXXXX <sub>B</sub>
007A75 <sub>H</sub>	007C75 <sub>H</sub>				
007A76 <sub>H</sub>	007C76 <sub>H</sub>	DLC Register 11	DLCR11	R/W	XXXXXXXX <sub>B</sub>
007A77 <sub>H</sub>	007C77 <sub>H</sub>				
007A78 <sub>H</sub>	007C78 <sub>H</sub>	DLC Register 12	DLCR12	R/W	XXXXXXXX <sub>B</sub>
007A79 <sub>H</sub>	007C79 <sub>H</sub>				
007A7A <sub>H</sub>	007C7A <sub>H</sub>	DLC Register 13	DLCR13	R/W	XXXXXXXX <sub>B</sub>
007A7B <sub>H</sub>	007C7B <sub>H</sub>				
007A7C <sub>H</sub>	007C7C <sub>H</sub>	DLC Register 14	DLCR14	R/W	XXXXXXXX <sub>B</sub>
007A7D <sub>H</sub>	007C7D <sub>H</sub>				
007A7E <sub>H</sub>	007C7E <sub>H</sub>	DLC Register 15	DLCR15	R/W	XXXXXXXX <sub>B</sub>
007A7F <sub>H</sub>	007C7F <sub>H</sub>				

**List of Message Buffers (DLC Registers and Data Registers) (2)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A80 <sub>H</sub> to 007A87 <sub>H</sub>	007C80 <sub>H</sub> to 007C87 <sub>H</sub>	Data Register 0 (8 bytes)	DTR0	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007A88 <sub>H</sub> to 007A8F <sub>H</sub>	007C88 <sub>H</sub> to 007C8F <sub>H</sub>	Data Register 1 (8 bytes)	DTR1	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007A90 <sub>H</sub> to 007A97 <sub>H</sub>	007C90 <sub>H</sub> to 007C97 <sub>H</sub>	Data Register 2 (8 bytes)	DTR2	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007A98 <sub>H</sub> to 007A9F <sub>H</sub>	007C98 <sub>H</sub> to 007C9F <sub>H</sub>	Data Register 3 (8 bytes)	DTR3	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AA0 <sub>H</sub> to 007AA7 <sub>H</sub>	007CA0 <sub>H</sub> to 007CA7 <sub>H</sub>	Data Register 4 (8 bytes)	DTR4	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AA8 <sub>H</sub> to 007AAF <sub>H</sub>	007CA8 <sub>H</sub> to 007CAF <sub>H</sub>	Data Register 5 (8 bytes)	DTR5	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AB0 <sub>H</sub> to 007AB7 <sub>H</sub>	007CB0 <sub>H</sub> to 007CB7 <sub>H</sub>	Data Register 6 (8 bytes)	DTR6	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AB8 <sub>H</sub> to 007ABF <sub>H</sub>	007CB8 <sub>H</sub> to 007CBF <sub>H</sub>	Data Register 7 (8 bytes)	DTR7	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AC0 <sub>H</sub> to 007AC7 <sub>H</sub>	007CC0 <sub>H</sub> to 007CC7 <sub>H</sub>	Data Register 8 (8 bytes)	DTR8	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AC8 <sub>H</sub> to 007ACF <sub>H</sub>	007CC8 <sub>H</sub> to 007CCF <sub>H</sub>	Data Register 9 (8 bytes)	DTR9	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AD0 <sub>H</sub> to 007AD7 <sub>H</sub>	007CD0 <sub>H</sub> to 007CD7 <sub>H</sub>	Data Register 10 (8 bytes)	DTR10	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AD8 <sub>H</sub> to 007ADF <sub>H</sub>	007CD8 <sub>H</sub> to 007CDF <sub>H</sub>	Data Register 11 (8 bytes)	DTR11	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AE0 <sub>H</sub> to 007AE7 <sub>H</sub>	007CE0 <sub>H</sub> to 007CE7 <sub>H</sub>	Data Register 12 (8 bytes)	DTR12	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AE8 <sub>H</sub> to 007AEF <sub>H</sub>	007CE8 <sub>H</sub> to 007CEF <sub>H</sub>	Data Register 13 (8 bytes)	DTR13	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>

**List of Message Buffers (DLC Registers and Data Registers) (3)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007AF0 <sub>H</sub> to 007AF7 <sub>H</sub>	007CF0 <sub>H</sub> to 007CF7 <sub>H</sub>	Data Register 14 (8 bytes)	DTR14	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AF8 <sub>H</sub> to 007AFF <sub>H</sub>	007CF8 <sub>H</sub> to 007CFF <sub>H</sub>	Data Register 15 (8 bytes)	DTR15	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>



**10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register**

Interrupt cause	EI <sup>2</sup> OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC <sub>H</sub>	—	—
INT9 instruction	N	—	#09	FFFFD8 <sub>H</sub>	—	—
Exception	N	—	#10	FFFFD4 <sub>H</sub>	—	—
CAN 0 RX	N	—	#11	FFFFD0 <sub>H</sub>	ICR00	0000B0 <sub>H</sub>
CAN 0 TX/NS	N	—	#12	FFFFC8 <sub>H</sub>		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 <sub>H</sub>	ICR01	0000B1 <sub>H</sub>
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 <sub>H</sub>		
CAN 2 RX / I <sup>2</sup> C0	N	—	#15	FFFFC0 <sub>H</sub>	ICR02	0000B2 <sub>H</sub>
CAN 2 TX/NS	N	—	#16	FFFFBC <sub>H</sub>		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 <sub>H</sub>	ICR03	0000B3 <sub>H</sub>
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 <sub>H</sub>		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 <sub>H</sub>	ICR04	0000B4 <sub>H</sub>
16-bit Reload Timer 3	Y1	—	#20	FFFFAC <sub>H</sub>		
PPG 0/1/4/5	N	—	#21	FFFFA8 <sub>H</sub>	ICR05	0000B5 <sub>H</sub>
PPG 2/3/6/7	N	—	#22	FFFFA4 <sub>H</sub>		
PPG 8/9/C/D	N	—	#23	FFFFA0 <sub>H</sub>	ICR06	0000B6 <sub>H</sub>
PPG A/B/E/F	N	—	#24	FFFF9C <sub>H</sub>		
Time Base Timer	N	—	#25	FFFF98 <sub>H</sub>	ICR07	0000B7 <sub>H</sub>
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 <sub>H</sub>		
Watch Timer	N	—	#27	FFFF90 <sub>H</sub>	ICR08	0000B8 <sub>H</sub>
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C <sub>H</sub>		
A/D Converter	Y1	5	#29	FFFF88 <sub>H</sub>	ICR09	0000B9 <sub>H</sub>
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84 <sub>H</sub>		
Input Capture 4/5 / I <sup>2</sup> C1	Y1	6	#31	FFFF80 <sub>H</sub>	ICR10	0000BA <sub>H</sub>
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C <sub>H</sub>		
Input Capture 0 to 3	Y1	8	#33	FFFF78 <sub>H</sub>	ICR11	0000BB <sub>H</sub>
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 <sub>H</sub>		
UART 0 RX	Y2	10	#35	FFFF70 <sub>H</sub>	ICR12	0000BC <sub>H</sub>
UART 0 TX	Y1	11	#36	FFFF6C <sub>H</sub>		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 <sub>H</sub>	ICR13	0000BD <sub>H</sub>
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 <sub>H</sub>		

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Interrupt cause	EI <sup>2</sup> OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	FFFF60 <sub>H</sub>	ICR14	0000BE <sub>H</sub>
UART 2 TX / UART 4 TX	Y1	15	#40	FFFF5C <sub>H</sub>		
Flash Memory	N	—	#41	FFFF58 <sub>H</sub>	ICR15	0000BF <sub>H</sub>
Delayed Interrupt	N	—	#42	FFFF54 <sub>H</sub>		

Y1 : Usable

Y2 : Usable, with EI<sup>2</sup>OS stop function

N : Unusable

- Note:**
- The peripheral resources sharing the ICR register have the same interrupt level.
  - When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
  - When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

## 11. Electrical Characteristics

### 11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	$AV_{RH}$ , $AV_{RL}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AV_{RH}$ , $AV_{CC} \geq AV_{RL}$ , $AV_{RH} \geq AV_{RL}$
Input voltage*1	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	$I_{CLAMP}$	-4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\sum  I_{CLAMP} $	—	40	mA	*5
"L" level maximum output current	$I_{OL}$	—	15	mA	*4, *6
"L" level average output current	$I_{OLAV}$	—	4	mA	*4, *7
"L" level maximum overall output current	$\sum I_{OL}$	—	100	mA	*4
"L" level average overall output current	$\sum I_{OLAV}$	—	50	mA	*4, *8
"H" level maximum output current	$I_{OH}$	—	-15	mA	*4, *6
"H" level average output current	$I_{OHAV}$	—	-4	mA	*4, *7
"H" level maximum overall output current	$\sum I_{OH}$	—	-100	mA	*4
"H" level average overall output current	$\sum I_{OHAV}$	—	-50	mA	*4, *8
Power consumption	$P_D$	—	450	mW	
Operating temperature	$T_A$	-40	+105	°C	
Storage temperature	$T_{STG}$	-55	+150	°C	

\*1: This parameter is based on  $V_{SS} = AV_{SS} = 0$  V

\*2: Set  $AV_{CC}$  and  $V_{CC}$  to the same voltage. Make sure that  $AV_{CC}$  does not exceed  $V_{CC}$  and that the voltage at the analog inputs does not exceed  $AV_{CC}$  when the power is switched on.

\*3:  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3$  V.  $V_I$  should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating.

\*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

\*5: ● Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

● Use within recommended operating conditions.

● Use with DC voltage (current)

● The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.

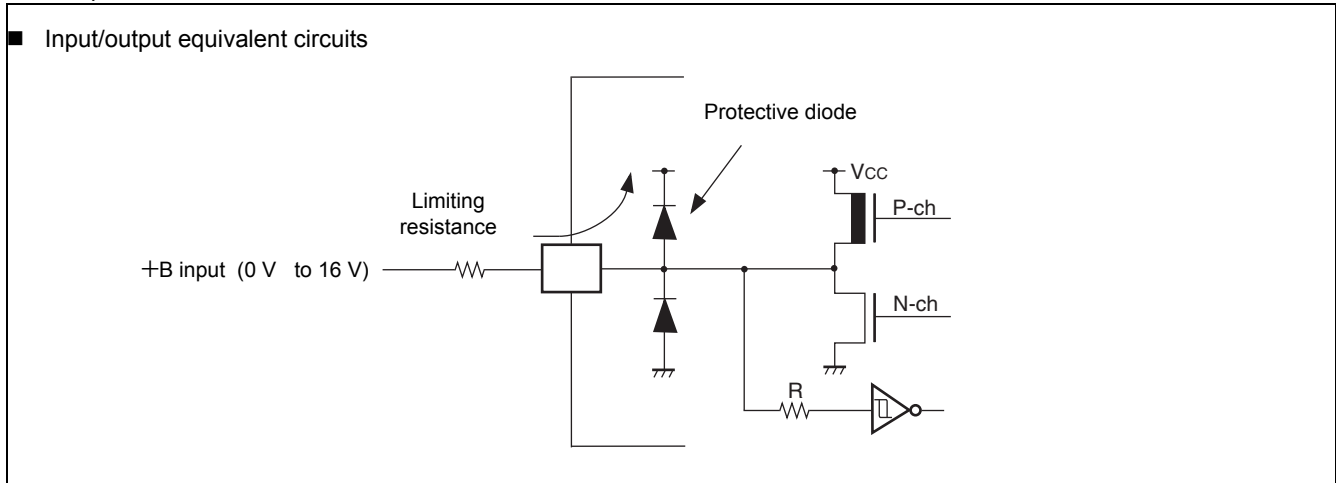
● The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.

● Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.

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- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

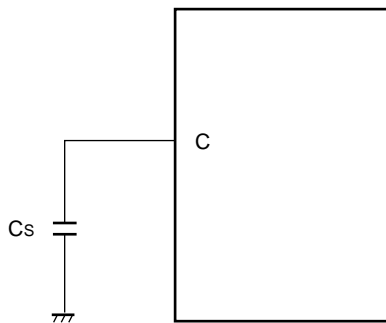


- \*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.
- \*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.
- \*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

**11.2 Recommended Operating Conditions**
 $(V_{SS} = AV_{SS} = 0\text{ V})$ 

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}, AV_{CC}$	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	$C_S$	0.1	—	1.0	$\mu\text{F}$	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the $V_{CC}$ should be greater than this capacitor.
Operating temperature	$T_A$	-40	—	+105	$^{\circ}\text{C}$	

**C Pin Connection Diagram**


**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

**11.3 DC Characteristics**

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{IHS}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	$V_{IHA}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	$V_{IHT}$	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	$V_{IHS}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{IHI}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{IHR}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	$V_{IHM}$	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	$V_{ILA}$	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if Automotive input levels are selected
	$V_{ILT}$	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{ILI}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{ILR}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	$V_{ILM}$	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	$V_{OH}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	$V_{OHI}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	$V_{OL}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	$V_{OLI}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

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 ( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	$I_{IL}$	—	$V_{CC} = 5.5\text{ V}$ , $V_{SS} < V_I < V_{CC}$	-1	—	+1	$\mu\text{A}$	
Pull-up resistance	$R_{UP}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{\text{RST}}$	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	$R_{DOWN}$	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash memory devices
Power supply current*	$I_{CC}$	$V_{CC}$	$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At writing Flash memory.	—	70	85	mA	Flash memory devices
			$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, At erasing Flash memory.	—	75	90	mA	Flash memory devices
	$I_{CCS}$		$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, In Sleep mode.	—	25	35	mA	
	$I_{CTS}$		$V_{CC} = 5.0\text{ V}$ , Internal frequency : 2 MHz, In Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$ , Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	$I_{CCL}$		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub operation $T_A = +25^{\circ}\text{C}$	—	70	140	$\mu\text{A}$	
	$I_{CCLS}$		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub sleep $T_A = +25^{\circ}\text{C}$	—	20	50	$\mu\text{A}$	
	$I_{CCT}$		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In watch mode $T_A = +25^{\circ}\text{C}$	—	10	35	$\mu\text{A}$	
$I_{CCH}$	$V_{CC} = 5.0\text{ V}$ , In Stop mode, $T_A = +25^{\circ}\text{C}$	—	7	25	$\mu\text{A}$			
Input capacitance	$C_{IN}$	Other than C, $AV_{CC}$ , $AV_{SS}$ , $AVRH$ , $AVRL$ , $V_{CC}$ , $V_{SS}$	—	—	5	15	pF	

\* : The power supply current is measured with an external clock.

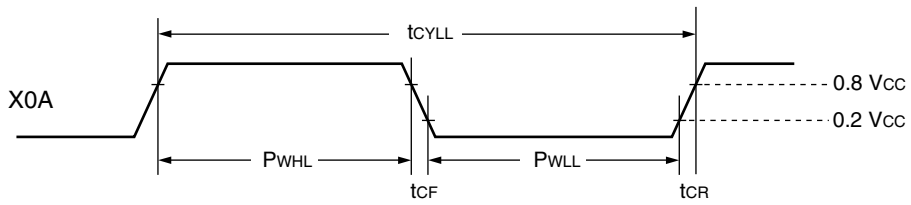
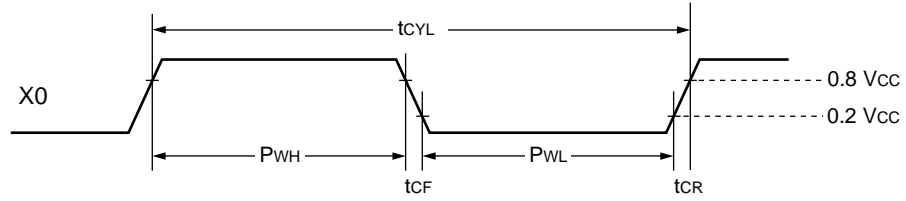
**11.4 AC Characteristics**
**11.4.1 Clock Timing**
 $(T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, f_{CP} \leq 24\text{ MHz}, V_{SS} = AV_{SS} = 0\text{ V})$ 

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_C$	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	$f_{CL}$	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	$t_{CYL}$	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	$t_{CYLL}$	X0A, X1A	10	30.5	—	$\mu\text{s}$	
Input clock pulse width	$P_{WH}, P_{WL}$	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	$P_{WHL}, P_{WLL}$	X0A	5	15.2	—	$\mu\text{s}$	
Input clock rise and fall time	$t_{CR}, t_{CF}$	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	$f_{CP}$	—	1.5	—	24	MHz	When using main clock
	$f_{CPL}$	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	$t_{CP}$	—	41.67	—	666	ns	When using main clock
	$t_{CPL}$	—	20	122.1	—	$\mu\text{s}$	When using sub clock

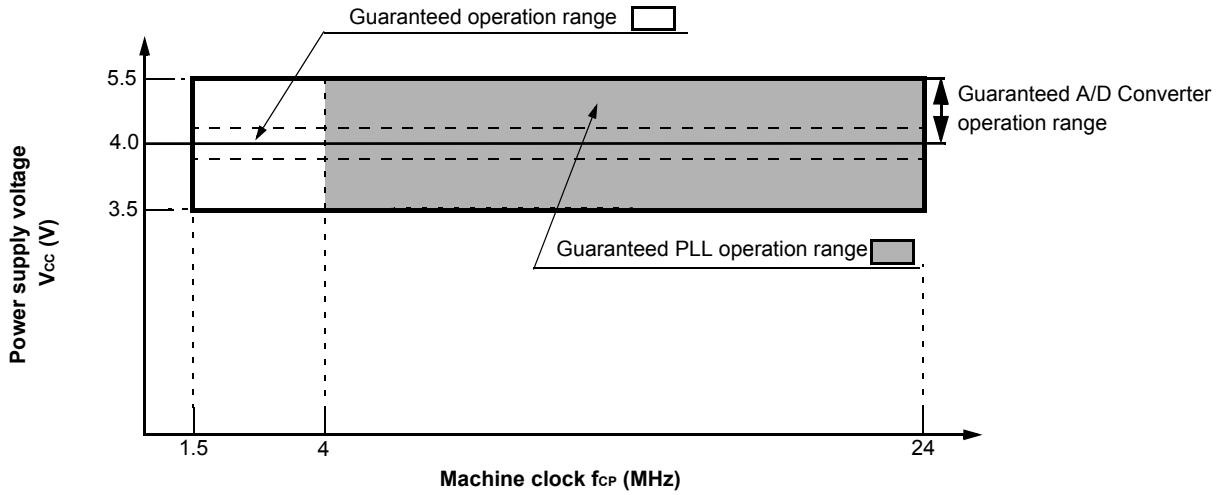
\* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".



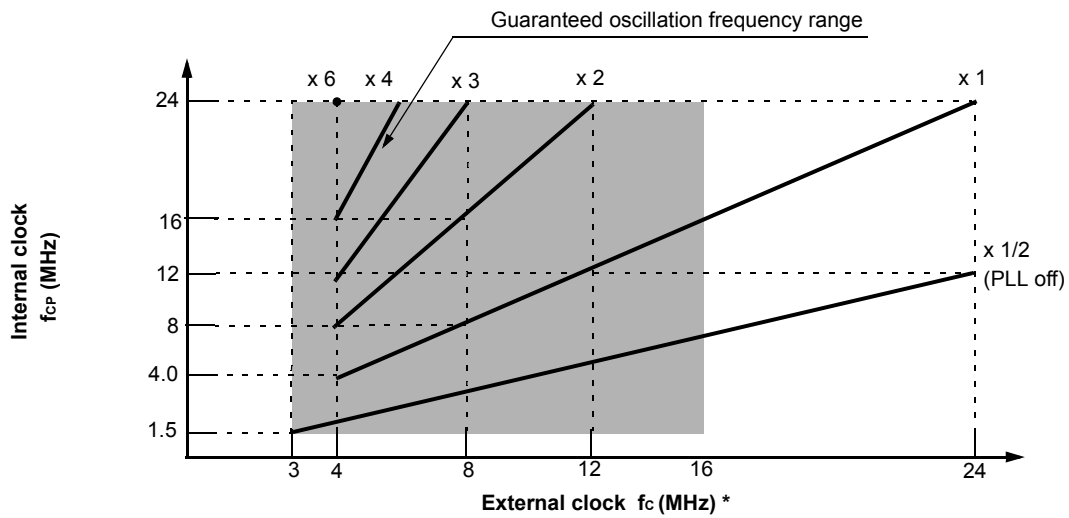
**Clock Timing**



**Guaranteed PLL operation range**



**Guaranteed operation range of MB90340E series**



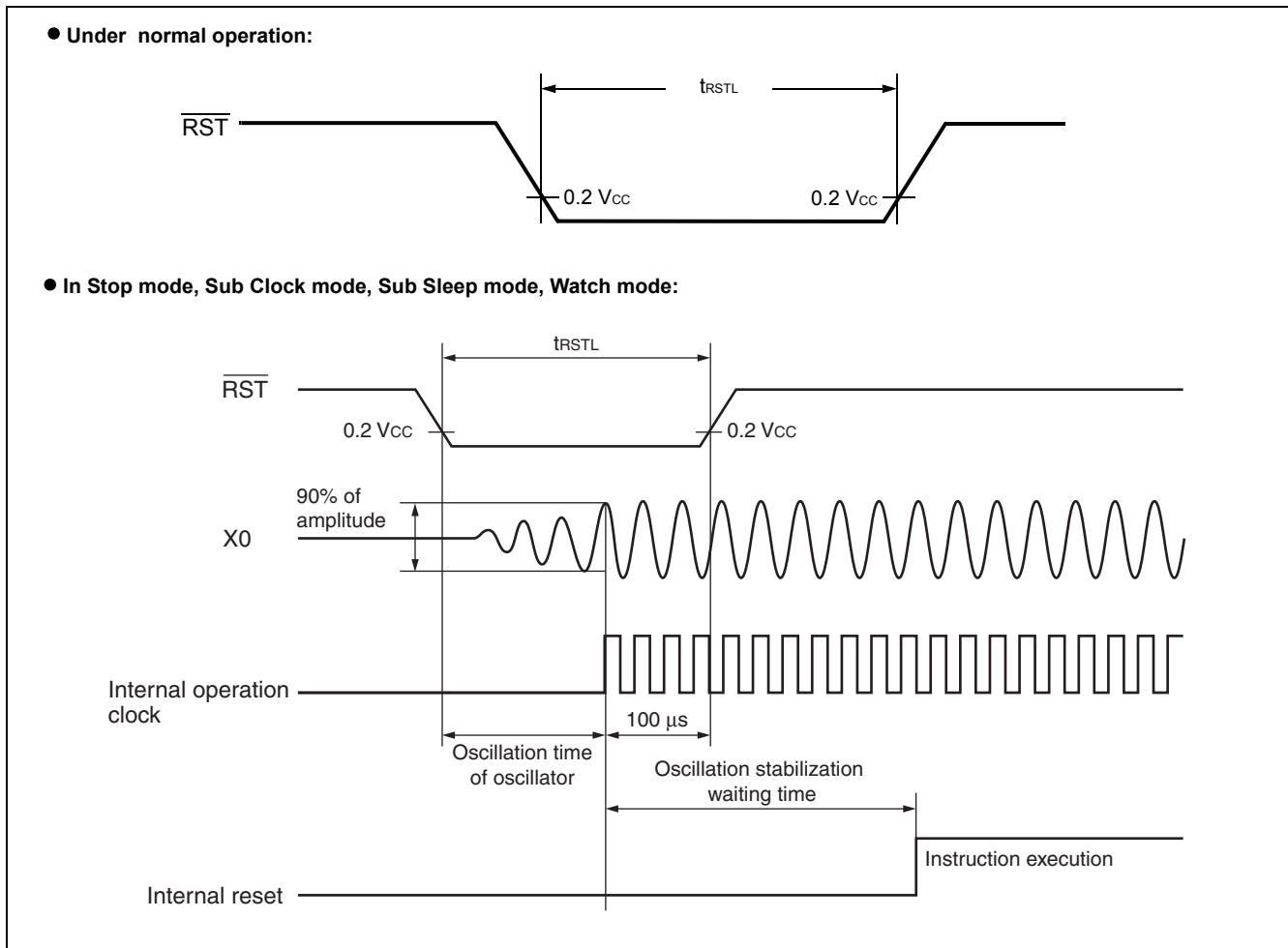
\* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

11.4.2 Reset Standby Input

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	$t_{RSTL}$	$\overline{\text{RST}}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 $\mu\text{s}$		$\mu\text{s}$	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	$\mu\text{s}$	In Time Timer mode

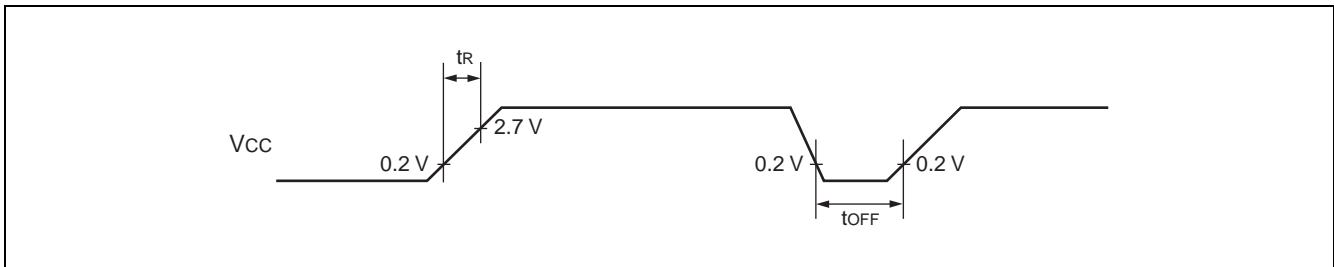
\* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred  $\mu\text{s}$  and several ms, and for an external clock, the time is 0 ms.



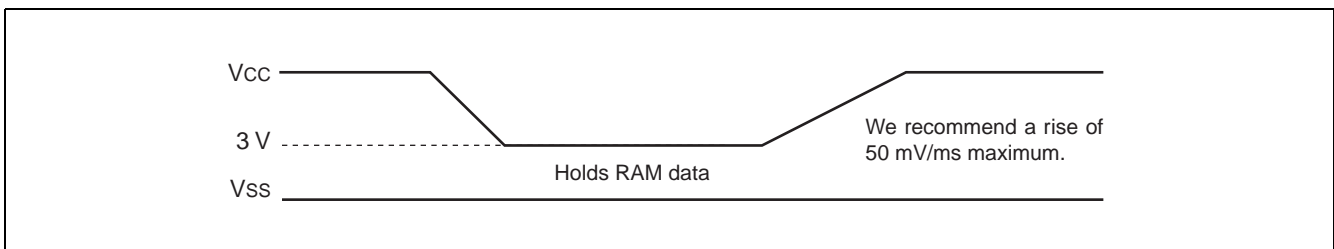
11.4.3 Power On Reset

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power off time	$t_{OFF}$	$V_{CC}$	—	1	—	ms	Waiting time until power-on



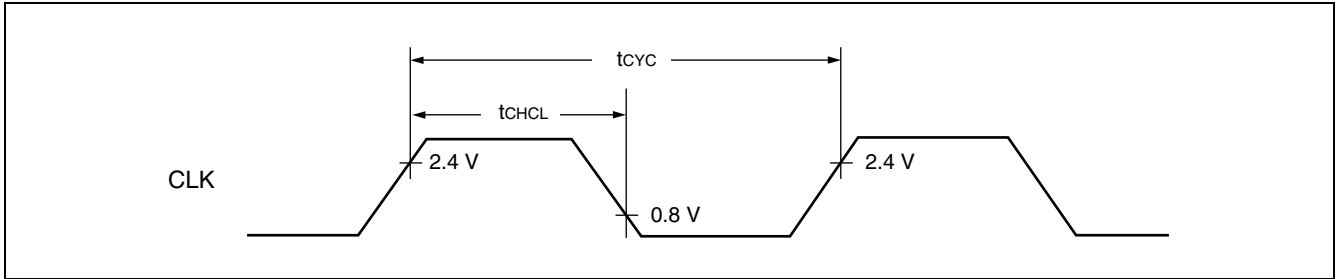
**Note:** : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 Clock Output Timing

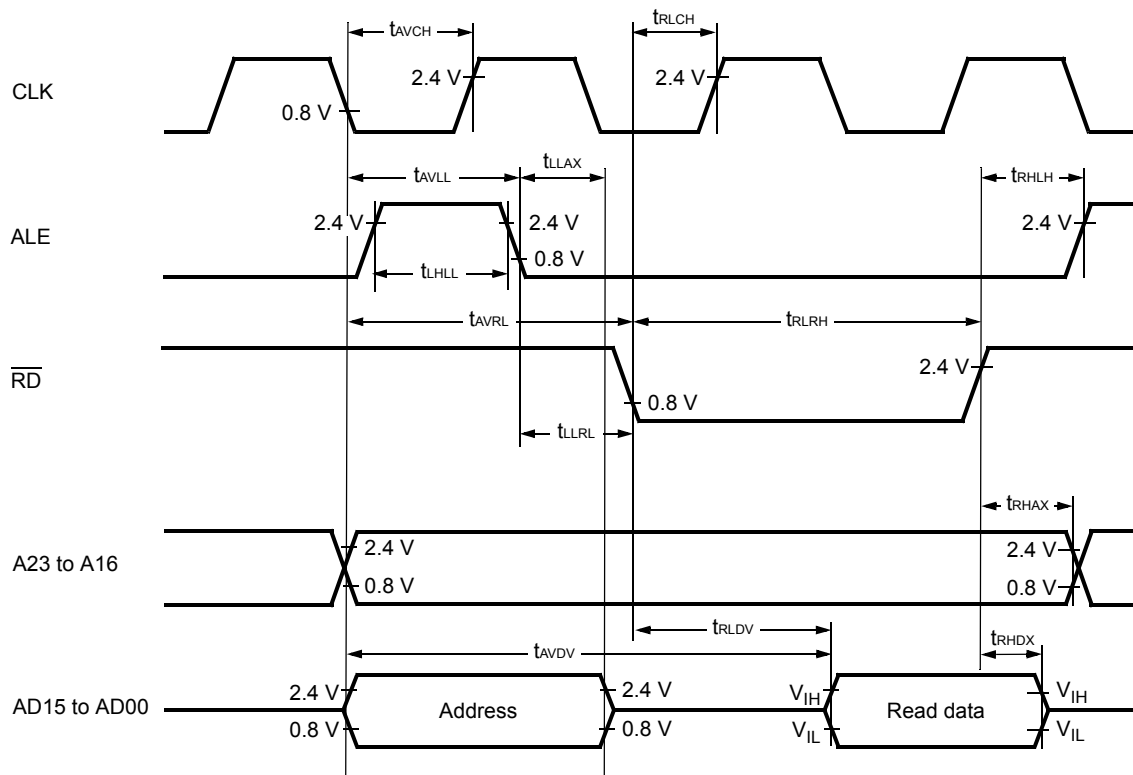
( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	$t_{CYC}$	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.67	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK $\downarrow$	$t_{CHCL}$	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$



**11.4.5 Bus Timing (Read)**
 $(T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, f_{CP} \leq 24\text{ MHz})$ 

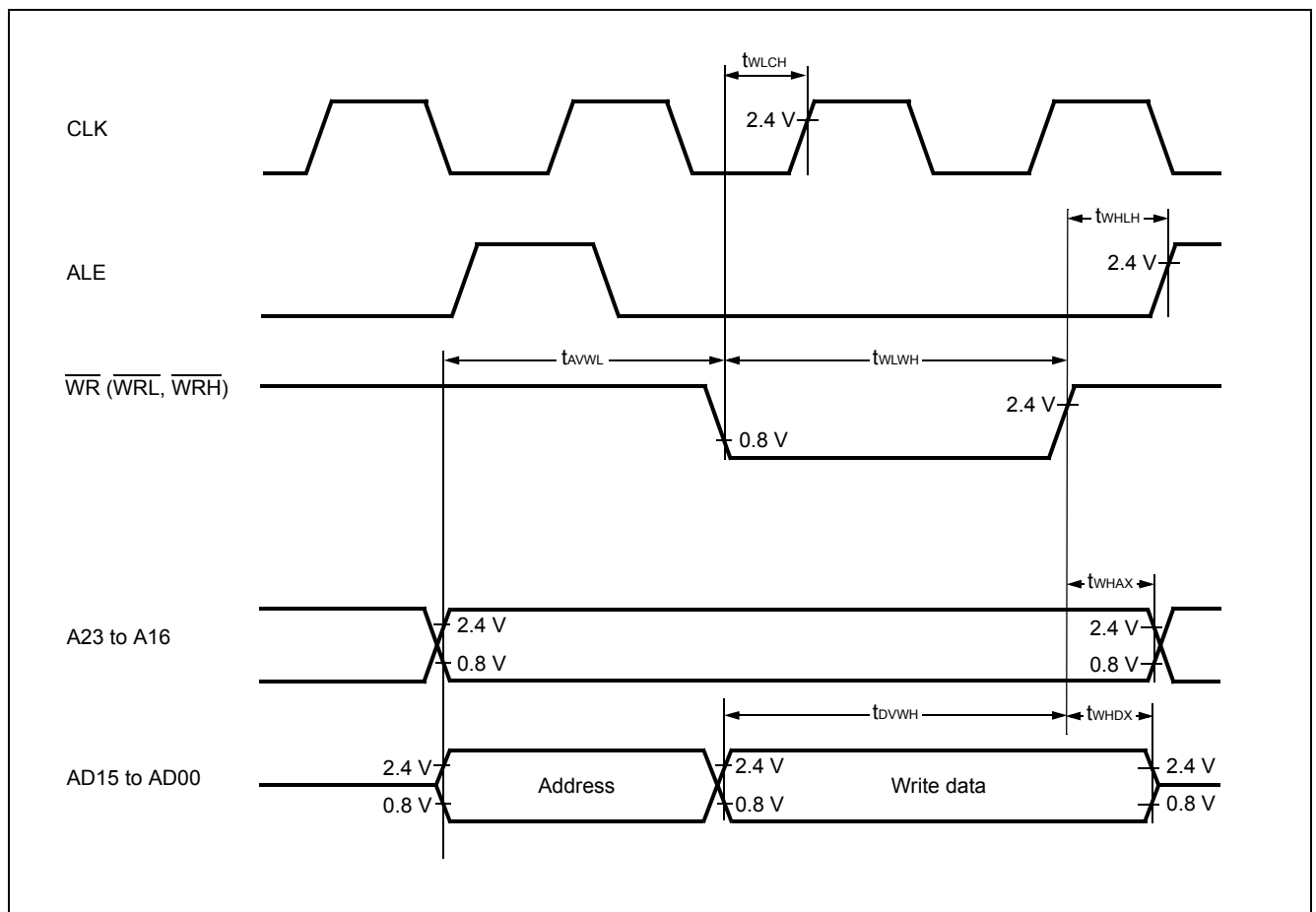
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	$t_{LHLL}$	ALE	—	$t_{CP}/2 - 10$	—	ns
Valid address → ALE ↓ time	$t_{AVLL}$	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE ↓ → Address valid time	$t_{LLAX}$	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address → RD ↓ time	$t_{AVRL}$	A23 to A16, AD15 to AD00, $\overline{\text{RD}}$		$t_{CP} - 15$	—	ns
Valid address → Valid data input	$t_{AVDV}$	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns
$\overline{\text{RD}}$ pulse width	$t_{RLRH}$	$\overline{\text{RD}}$		$3 t_{CP}/2 - 20$	—	ns
$\overline{\text{RD}}$ ↓ → Valid data input	$t_{RLDV}$	$\overline{\text{RD}}$ , AD15 to AD00		—	$3 t_{CP}/2 - 50$	ns
$\overline{\text{RD}}$ ↑ → Data hold time	$t_{RHDX}$	$\overline{\text{RD}}$ , AD15 to AD00		0	—	ns
$\overline{\text{RD}}$ ↑ → ALE ↑ time	$t_{RHLH}$	$\overline{\text{RD}}$ , ALE		$t_{CP}/2 - 15$	—	ns
$\overline{\text{RD}}$ ↑ → Address valid time	$t_{RHAX}$	$\overline{\text{RD}}$ , A23 to A16		$t_{CP}/2 - 10$	—	ns
Valid address → CLK ↑ time	$t_{AVCH}$	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
$\overline{\text{RD}}$ ↓ → CLK ↑ time	$t_{RLCH}$	$\overline{\text{RD}}$ , CLK		$t_{CP}/2 - 15$	—	ns
ALE ↓ → $\overline{\text{RD}}$ ↓ time	$t_{LLRL}$	ALE, $\overline{\text{RD}}$	$t_{CP}/2 - 15$	—	ns	



11.4.6 Bus Timing (Write)

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\rightarrow \overline{\text{WR}} \downarrow$ time	$t_{\text{AVWL}}$	A23 to A16, AD15 to AD00, $\overline{\text{WR}}$	—	$t_{\text{CP}} - 15$	—	ns
$\overline{\text{WR}}$ pulse width	$t_{\text{WLWH}}$	$\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns
Valid data output $\rightarrow \overline{\text{WR}} \uparrow$ time	$t_{\text{DVWH}}$	AD15 to AD00, $\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Data hold time	$t_{\text{WHDX}}$	AD15 to AD00, $\overline{\text{WR}}$		15	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Address valid time	$t_{\text{WHAX}}$	A23 to A16, $\overline{\text{WR}}$		$t_{\text{CP}}/2 - 10$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ ALE $\uparrow$ time	$t_{\text{WHLH}}$	$\overline{\text{WR}}$ , ALE		$t_{\text{CP}}/2 - 15$	—	ns
$\overline{\text{WR}} \downarrow \rightarrow$ CLK $\uparrow$ time	$t_{\text{WLCH}}$	$\overline{\text{WR}}$ , CLK	$t_{\text{CP}}/2 - 15$	—	ns	

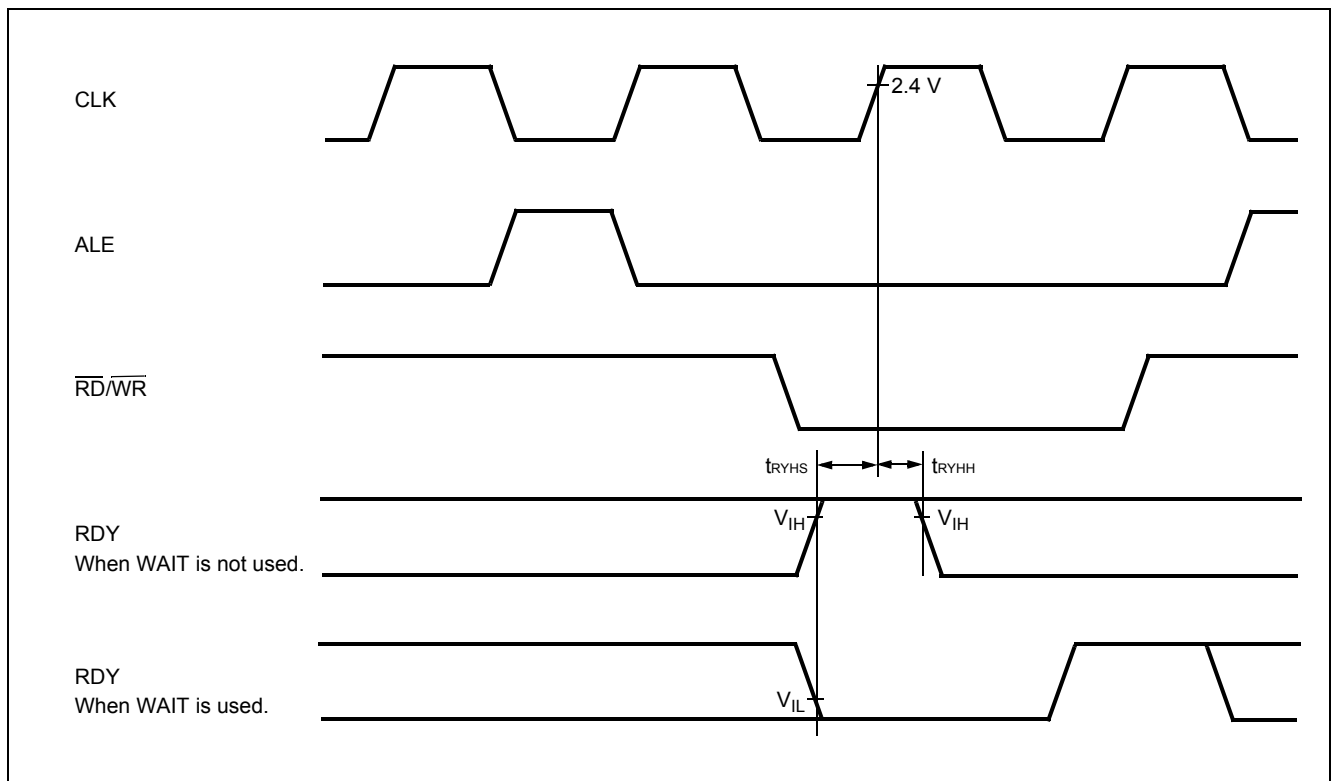


11.4.7 Ready Input Timing

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	$t_{RYHS}$	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	$t_{RYHH}$	RDY	—	0	—	ns	

**Note:** : If the RDY setup time is insufficient, use the auto-ready function.



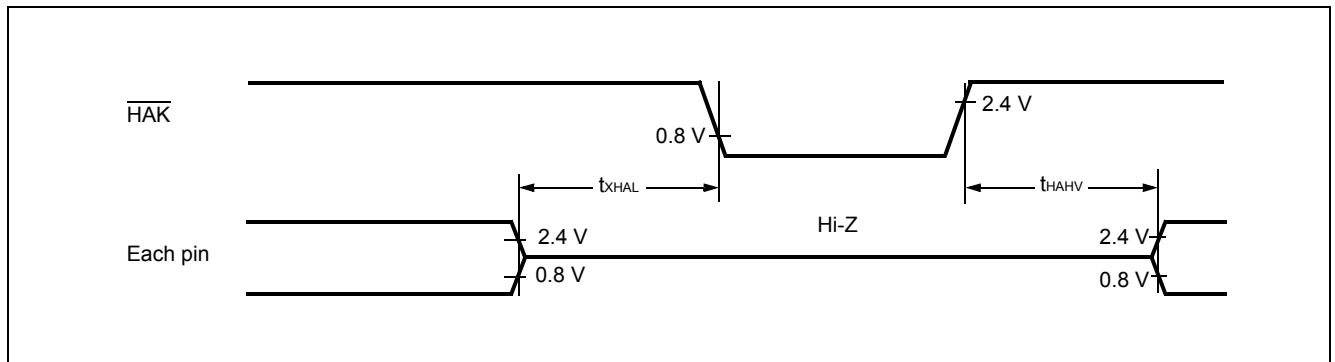


11.4.8 Hold Timing

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $f_{CP} \leq 24\text{ MHz}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Pin floating $\rightarrow$ $\overline{\text{HAK}} \downarrow$ time	$t_{\text{XHAL}}$	$\overline{\text{HAK}}$		30	$t_{\text{CP}}$	ns
$\overline{\text{HAK}} \uparrow$ time $\rightarrow$ Pin valid time	$t_{\text{HAHV}}$	$\overline{\text{HAK}}$		$t_{\text{CP}}$	$2 t_{\text{CP}}$	ns

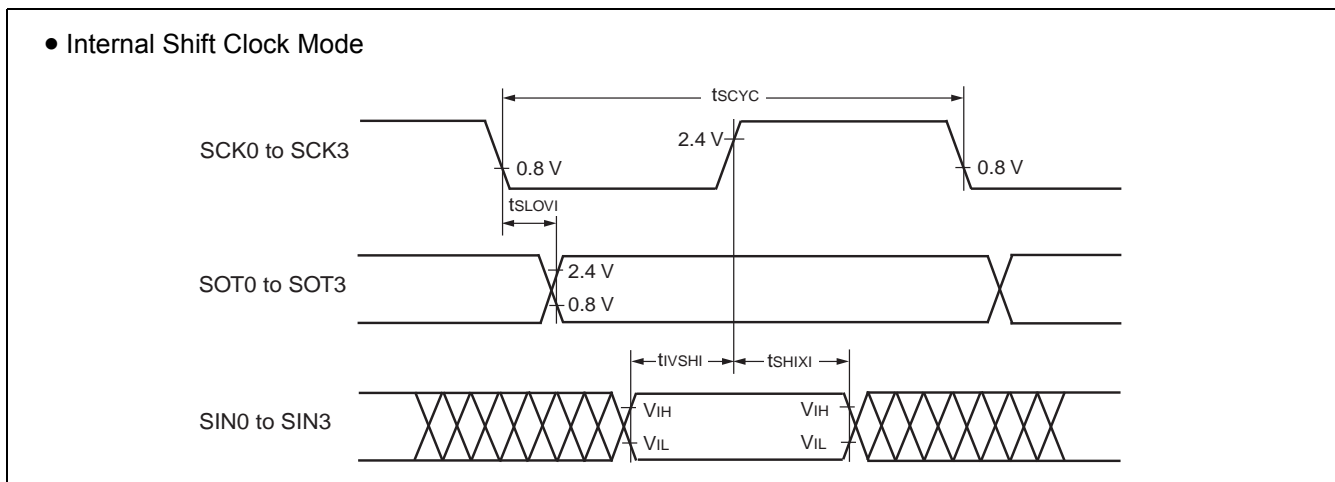
**Note:** : There is more than 1 cycle from when HRQ reads in until the  $\overline{\text{HAK}}$  is changed.



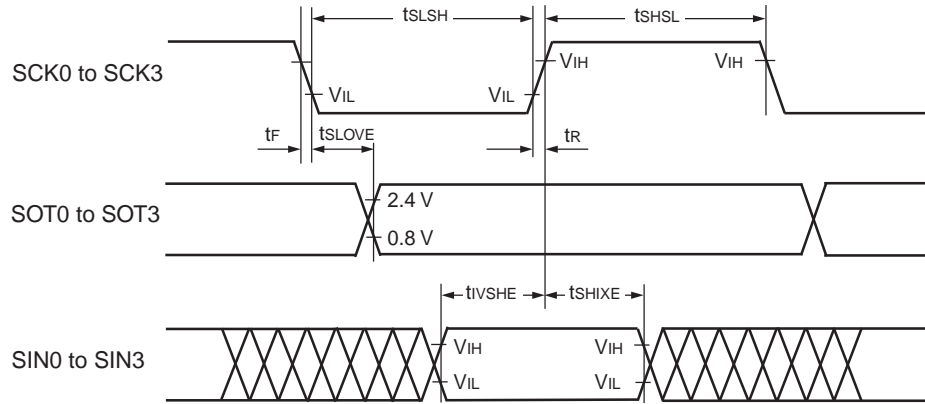
**11.4.9 LIN-UART0/1/2/3**
**■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**
 $(T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, f_{CP} \leq 24\text{ MHz}, V_{SS} = 0\text{ V})$ 

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN → SCK ↑	$t_{IVSHI}$	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK ↑ → Valid SIN hold time	$t_{SHIXI}$	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "L" pulse width	$t_{SHSL}$	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	$t_{SLSH}$	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN → SCK ↑	$t_{IVSHE}$	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	$t_{SHIXE}$	SCK0, SCK1, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	$t_F$	SCK0 to SCK3		—	10	ns
SCK rise time	$t_R$	SCK0 to SCK3		—	10	ns

- Note:**
- AC characteristic in CLK synchronized mode.
  - $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.



● External Shift Clock Mode



■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

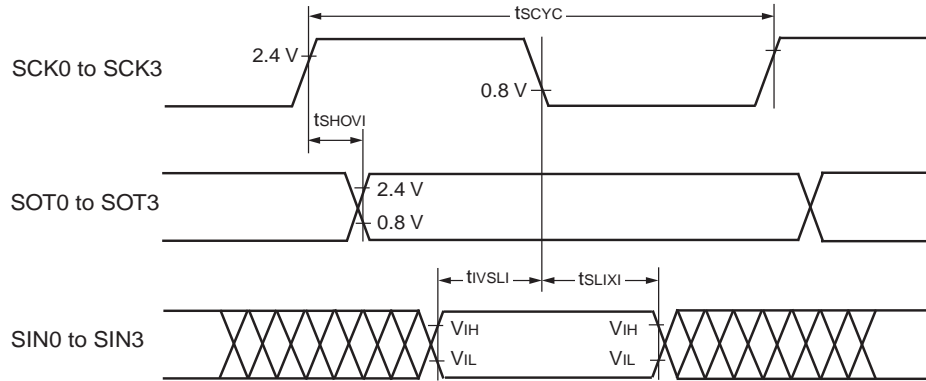
( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXI}$	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3 t_{CP} - t_R$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLE}$	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK $\downarrow$ $\rightarrow$ Valid SIN hold time	$t_{SLIXE}$	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	$t_F$	SCK0 to SCK3		—	10	ns
SCK rise time	$t_R$	SCK0 to SCK3		—	10	ns

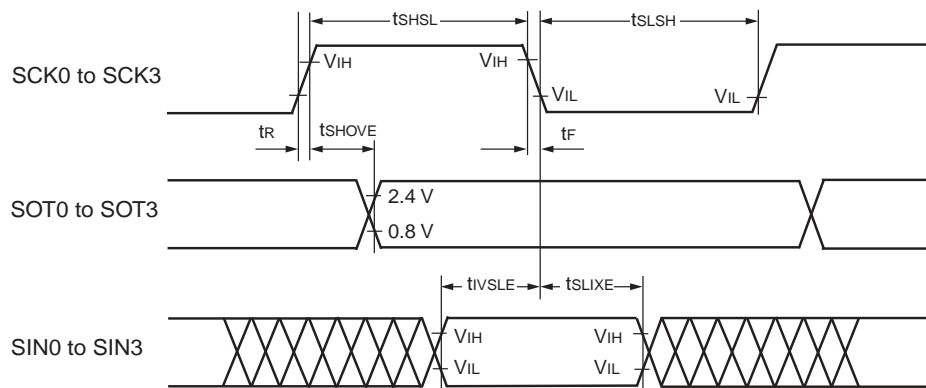
**Note:**

- $C_L$  is load capacity value of pins when testing.
- $t_{CP}$  is internal operating clock cycle time (machine clock). Refer to "Clock Timing".

• Internal Shift Clock Mode



• External Shift Clock Mode

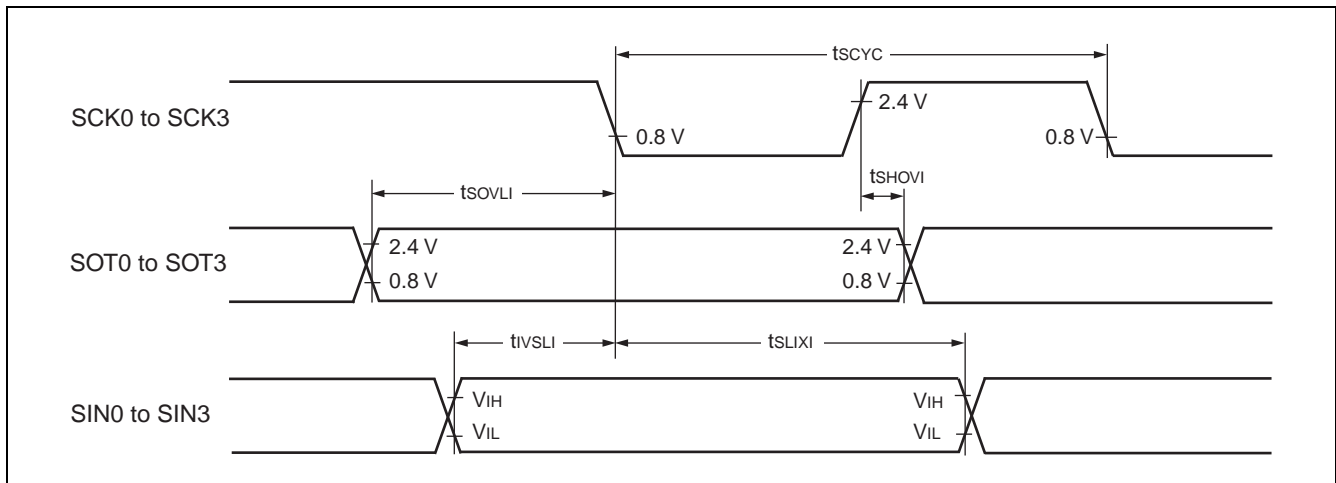


■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns
SCK $\uparrow$ → SOT delay time	$t_{SHOVI}$	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN → SCK $\downarrow$	$t_{IVSLI}$	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow$ → Valid SIN hold time	$t_{SLIXI}$	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT → SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK0 to SCK3, SOT0 to SOT3		$3 t_{CP} - 70$	—	ns

- Note:**
- $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

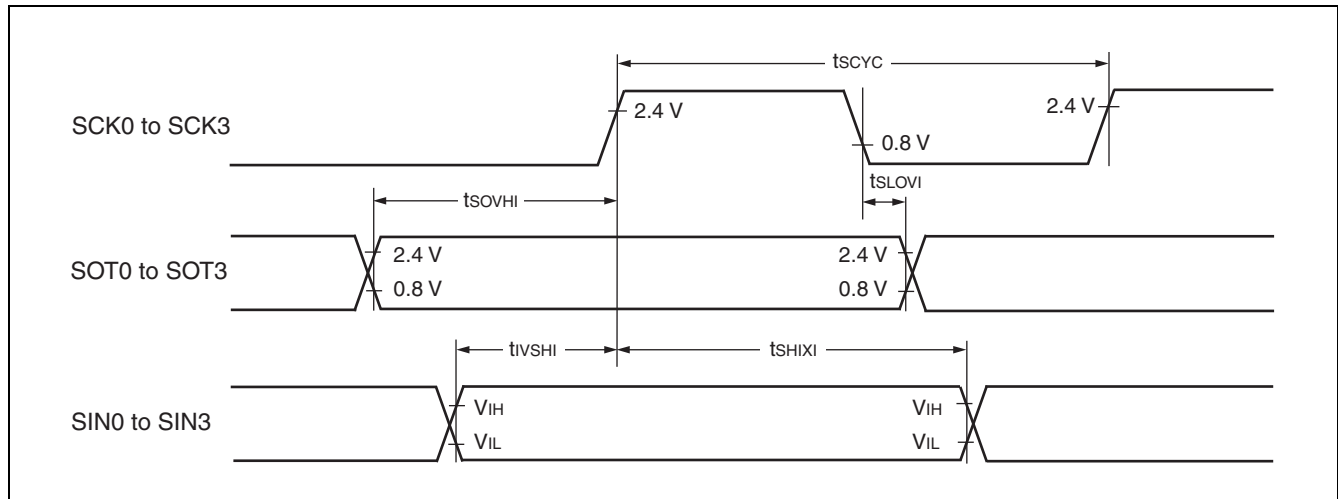


■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN → SCK ↑	$t_{IVSHI}$	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK ↑ → Valid SIN hold time	$t_{SHIXI}$	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT → SCK ↑ delay time	$t_{SOVHI}$	SCK0 to SCK3, SOT0 to SOT3		$3 t_{CP} - 70$	—	ns

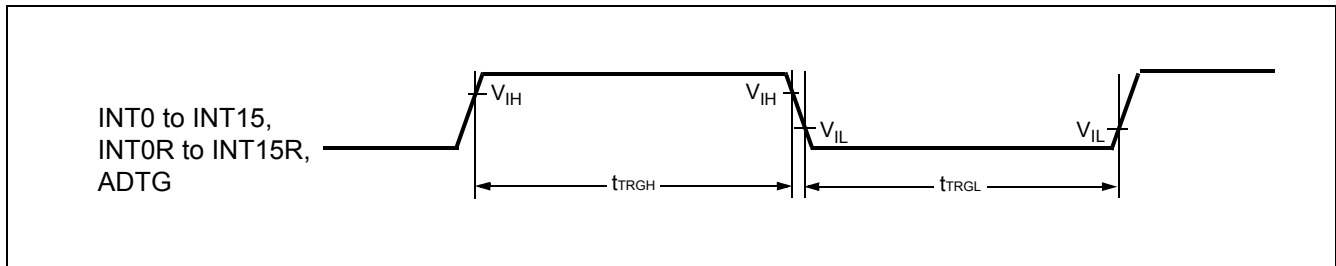
- Note:**
- $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.



11.4.10 Trigger Input Timing

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0.0\text{ V}$ )

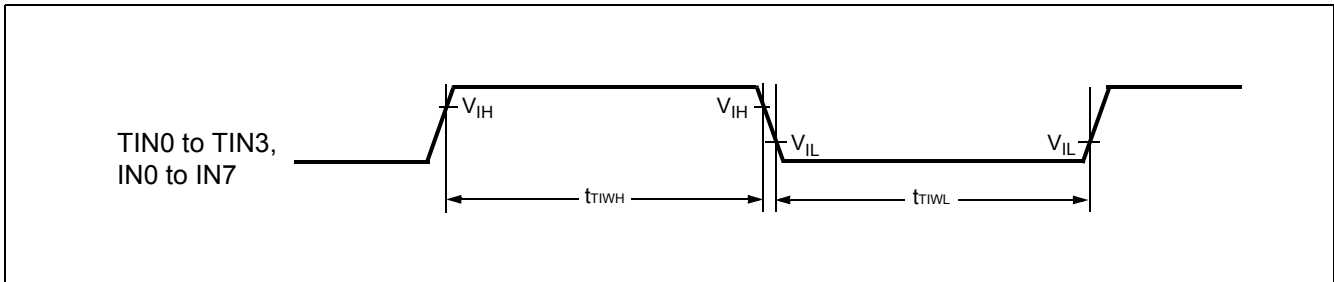
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	$t_{TRGH}$ $t_{TRGL}$	INT0 to INT15, INT0R to INT15R, ADTG	—	$5 t_{CP}$	—	ns



11.4.11 Timer Related Resource Input Timing

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

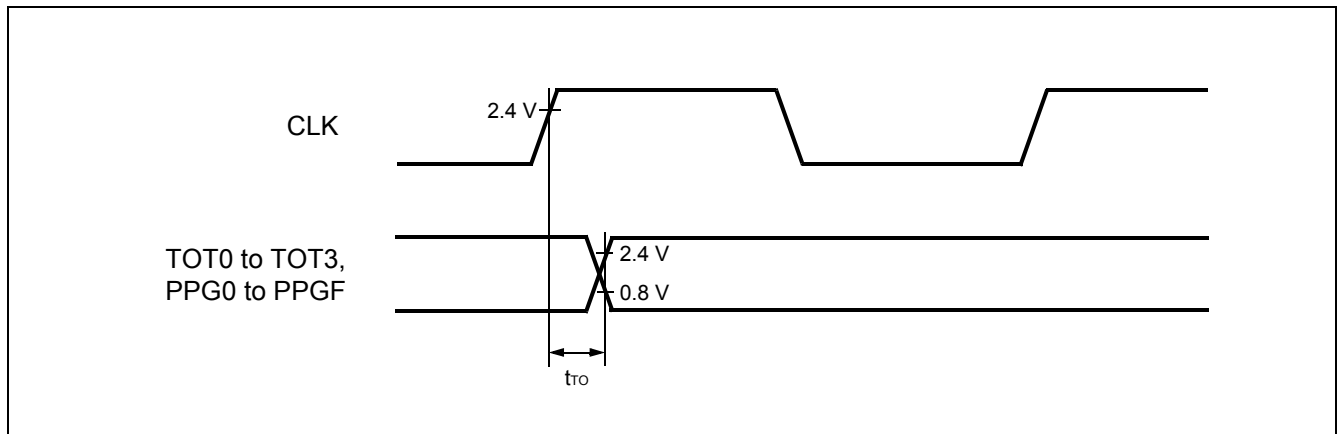
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	$t_{TIWH}$	TIN0 to TIN3, IN0 to IN7	—	4 $t_{CP}$	—	ns
	$t_{TIWL}$					



11.4.12 Timer Related Resource Output Timing

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK $\uparrow$ $\rightarrow$ $T_{OUT}$ change time	$t_{TO}$	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns





11.4.13 I<sup>2</sup>C Timing

(T<sub>A</sub> = -40°C to +105°C, V<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = 0.0 V)

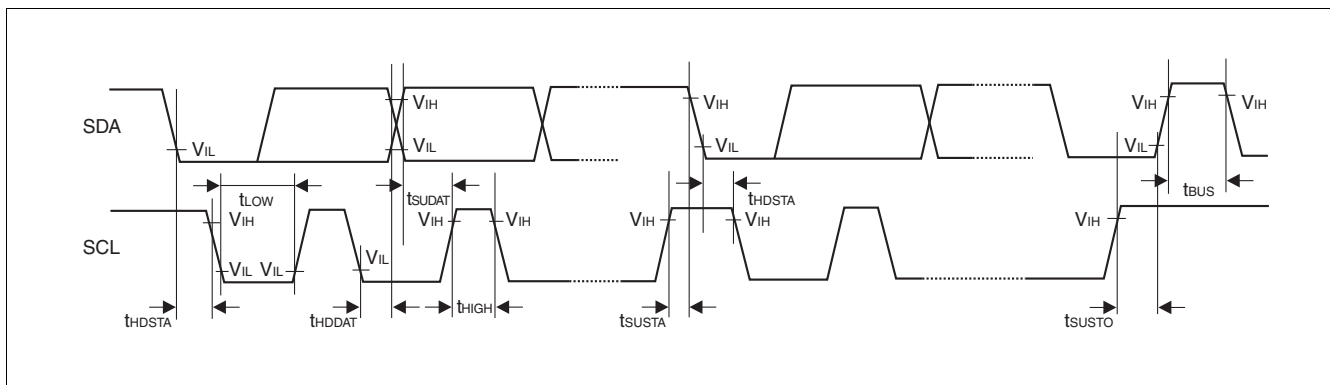
Parameter	Symbol	Condition	Standard-mode		Fast-mode*1		Unit
			Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>		0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t <sub>HDSTA</sub>	R = 1.7 kΩ <sub>2</sub> C = 50 pF*2	4.0	—	0.6	—	μs
"L" width of the SCL clock	t <sub>LOW</sub>		4.7	—	1.3	—	μs
"H" width of the SCL clock	t <sub>HIGH</sub>		4.0	—	0.6	—	μs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45*3	0	0.9*4	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t <sub>BUS</sub>		4.7	—	1.3	—	μs

\*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

\*2: R, C: Pull-up resistor and load capacitor of the SCL and SDA lines.

\*3: The maximum t<sub>HDDAT</sub> meets the requirement that it does not extend the "L" width (t<sub>LOW</sub>) of the SCL signal.

\*4: A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SUDAT</sub> ≥ 250 ns must then be met.



**11.5 A/D Converter**

( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$ ,  $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = \text{AV}_{SS} = 0\text{ V}$ )

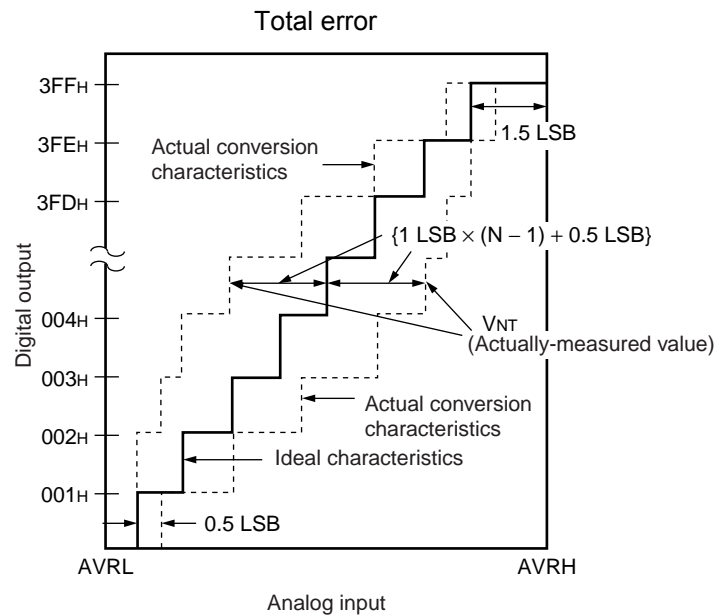
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	$\pm 3.0$	LSB	
Nonlinearity error	—	—	—	—	$\pm 2.5$	LSB	
Differential nonlinearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero reading voltage	$V_{OT}$	AN0 to AN23	$\text{AVRL} - 1.5 \times \text{LSB}$	$\text{AVRL} + 0.5 \times \text{LSB}$	$\text{AVRL} + 2.5 \times \text{LSB}$	V	
Full scale reading voltage	$V_{FST}$	AN0 to AN23	$\text{AVRH} - 3.5 \times \text{LSB}$	$\text{AVRH} - 1.5 \times \text{LSB}$	$\text{AVRH} + 0.5 \times \text{LSB}$	V	
Compare time	—	—	1.0	—	16500	$\mu\text{s}$	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	$\infty$	$\mu\text{s}$	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Analog port input current	$I_{AIN}$	AN0 to AN23	-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage range	$V_{AIN}$	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	$\text{AV}_{CC}$	V	
	—	AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	$I_A$	$\text{AV}_{CC}$	—	3.5	7.5	mA	
	$I_{AH}$	$\text{AV}_{CC}$	—	—	5	$\mu\text{A}$	*
Reference voltage current	$I_R$	AVRH	—	600	900	$\mu\text{A}$	
	$I_{RH}$	AVRH	—	—	5	$\mu\text{A}$	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

\*: If the A/D converter is not operating, a current when CPU is stopped is applicable ( $V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$ ).

**Note:** : The accuracy gets worse as  $|\text{AVRH} - \text{AVRL}|$  becomes smaller.

**11.6 Definition of A/D Converter Terms**

- Resolution : Analog variation that is recognized by the A/D converter.
- Non linearity error : The deviation between the actual conversion characteristics and a line that joins the zero-transition line ( “00 0000 0000” ← → “00 0000 0001” ) to the full-scale transition line ( “11 1111 1110” ← → “11 1111 1111” ).
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

N : Value of the digital output from the A/D converter

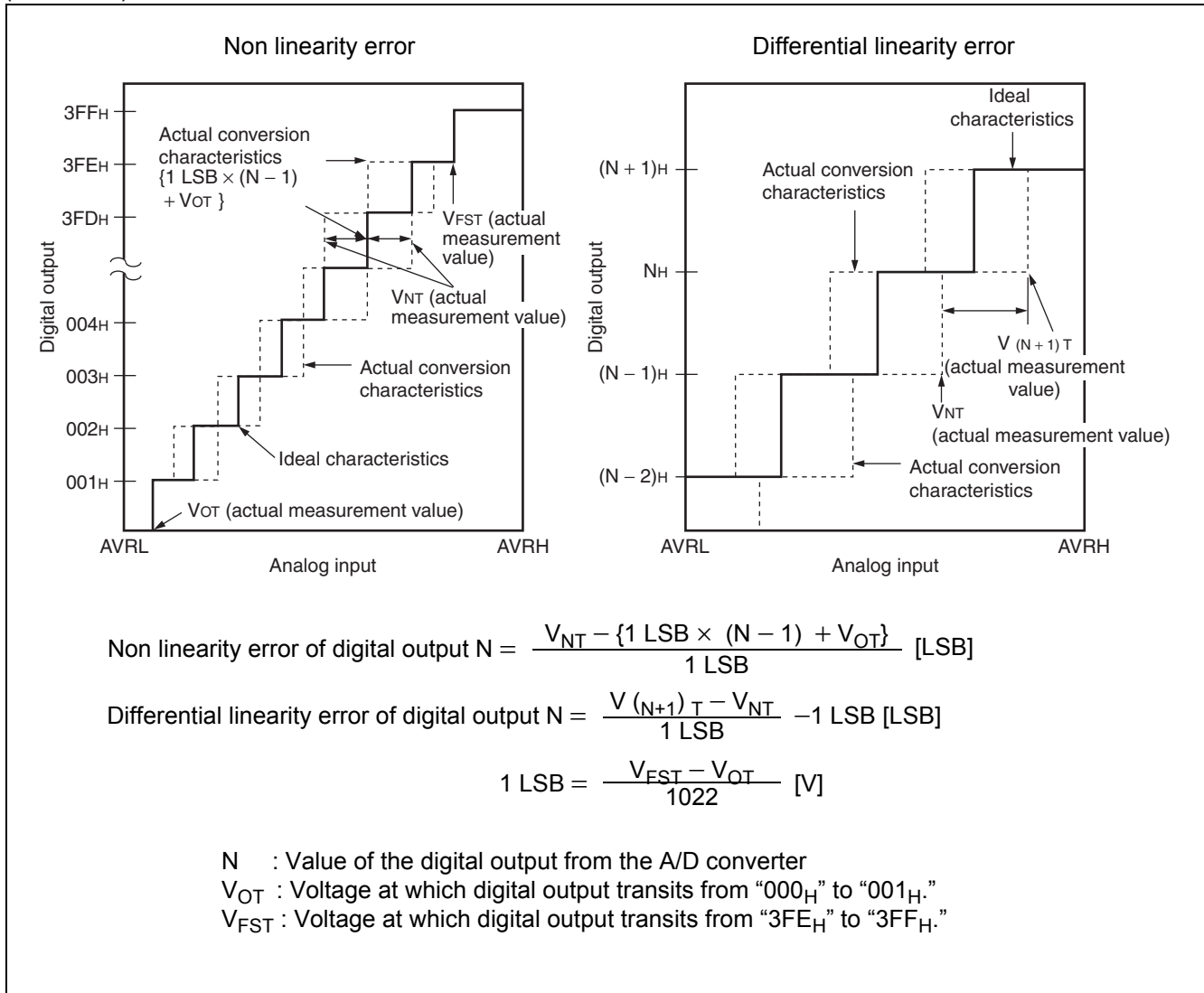
$V_{OT}$  (Ideal value) =  $AVRL + 0.5 \text{ LSB}$  [V]

$V_{FST}$  (Ideal value) =  $AVRH - 1.5 \text{ LSB}$  [V]

$V_{NT}$  : A voltage at which the digital output transitions from  $(N - 1)_H$  to  $N_H$ .

(Continued)

(Continued)



**11.7 Notes on A/D Converter Section**

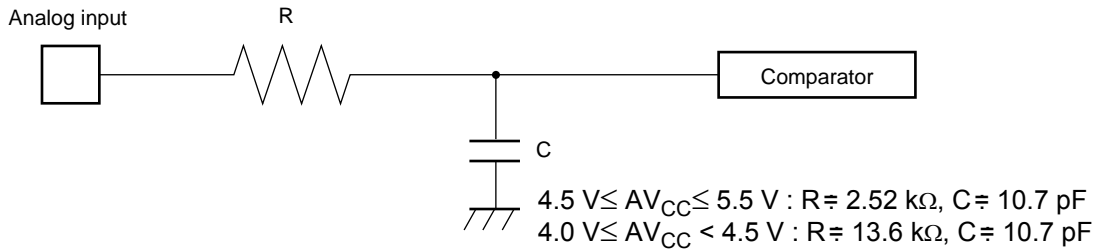
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower ( $4.0 \text{ V} \leq AV_{CC} \leq 5.5 \text{ V}$ ,  
 sampling period = 0.5 μs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

• Analog input circuit model



**Note:** : Use the values in the figure only as a guideline.

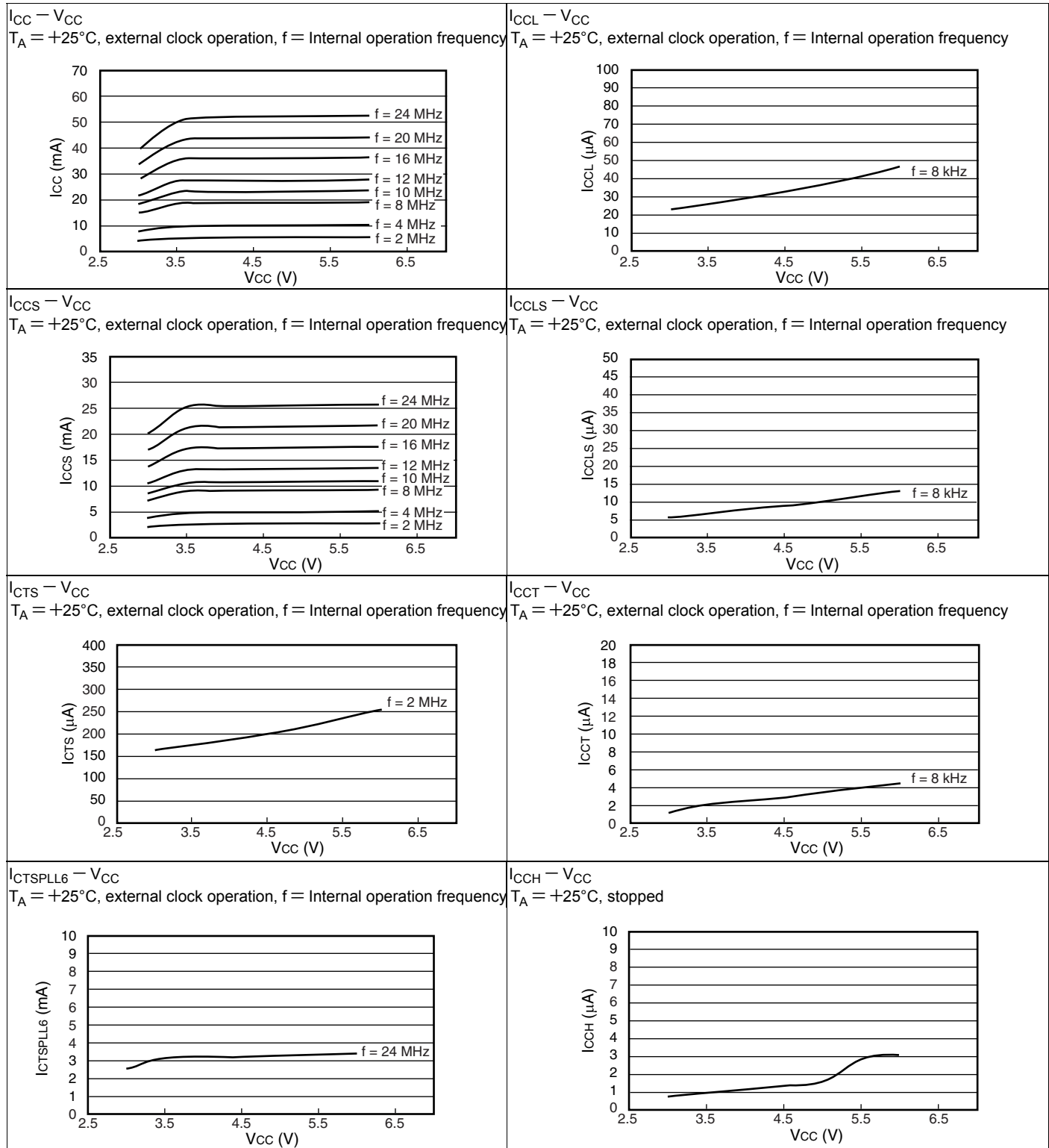
**11.8 Flash Memory Program/Erase Characteristics**

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T <sub>A</sub> = +25°C V <sub>CC</sub> = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	μs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average T <sub>A</sub> = +85°C	20	—	—	year	*

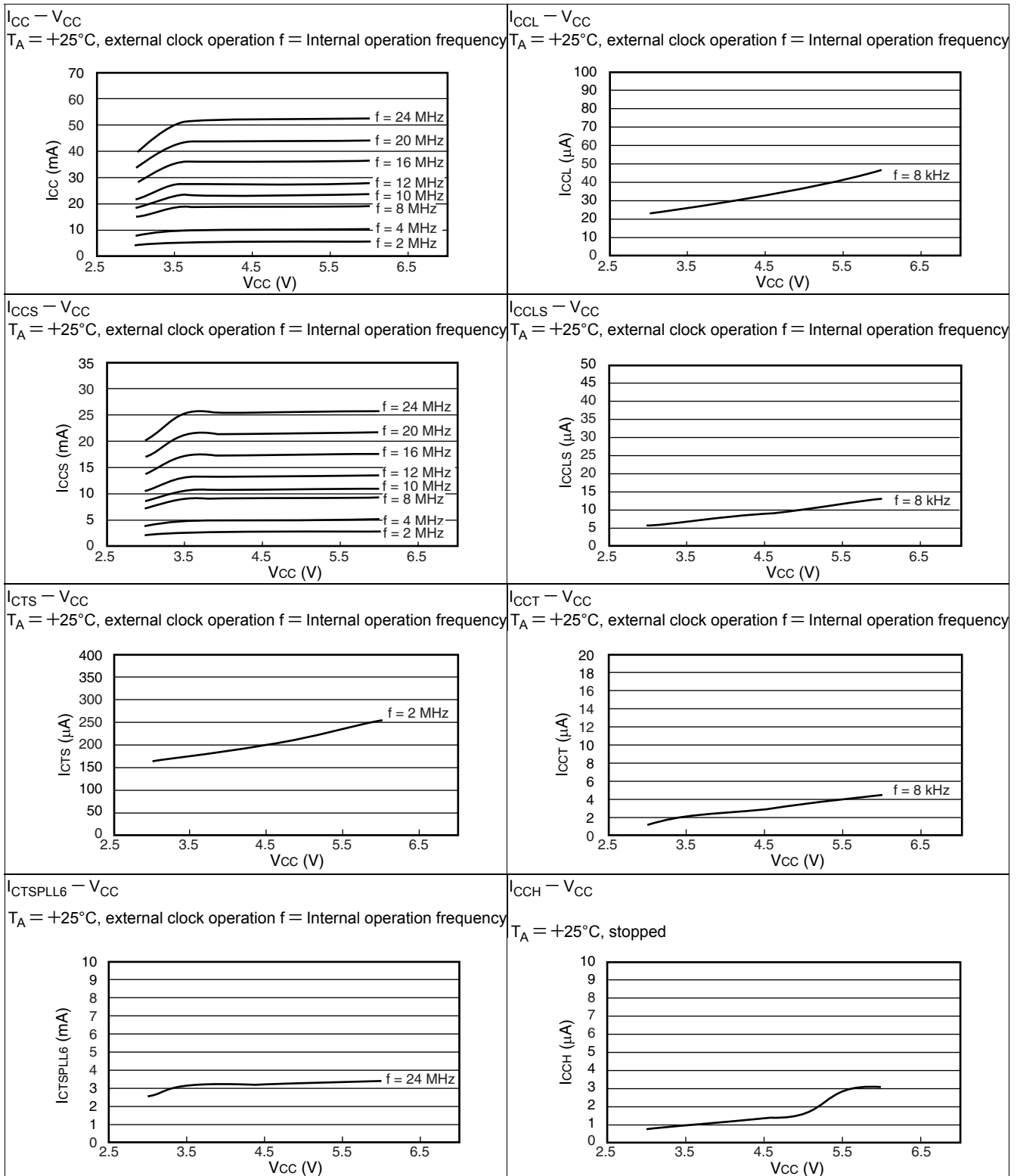
\* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C) .

**12. Example Characteristics**

- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES

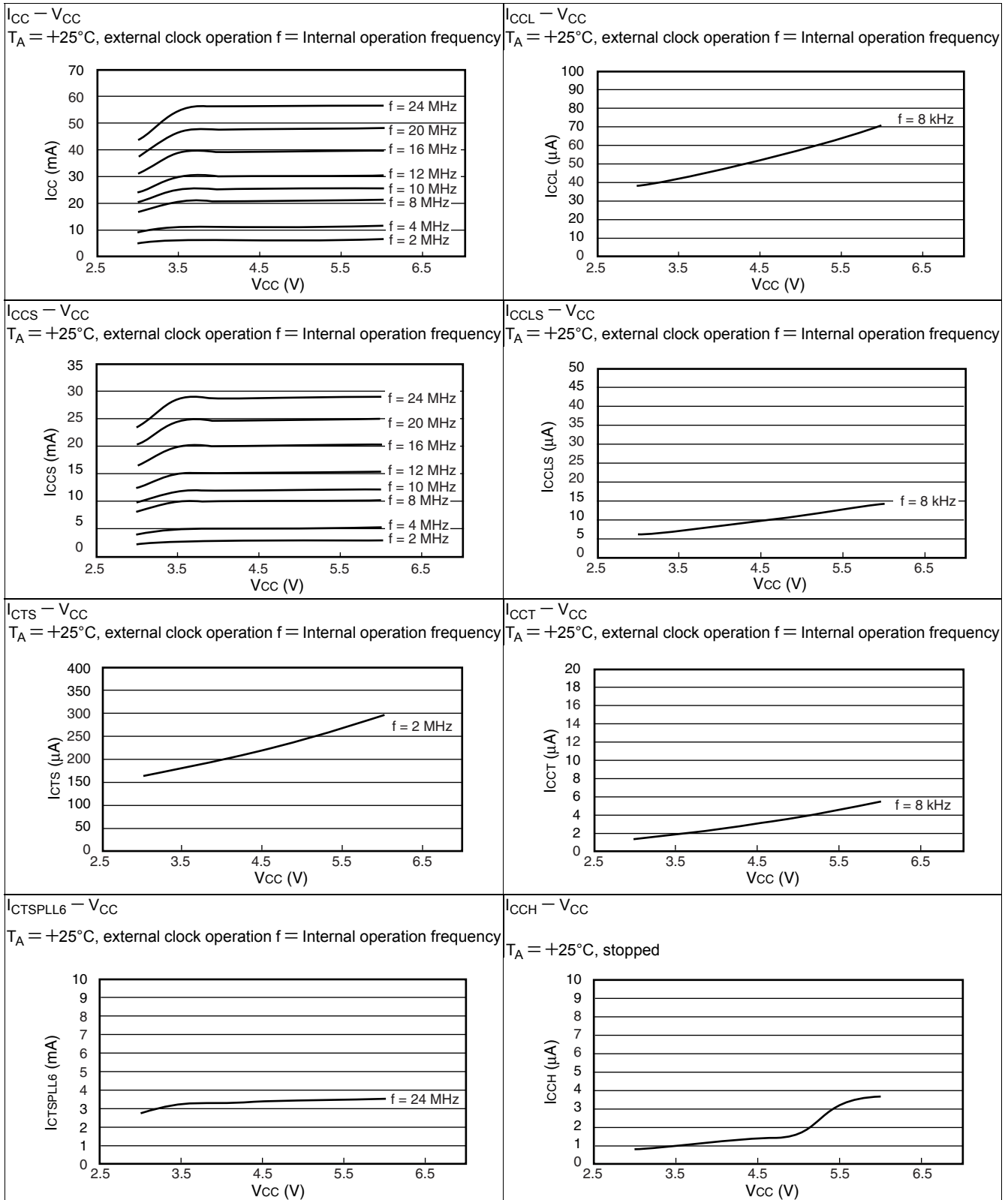


■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

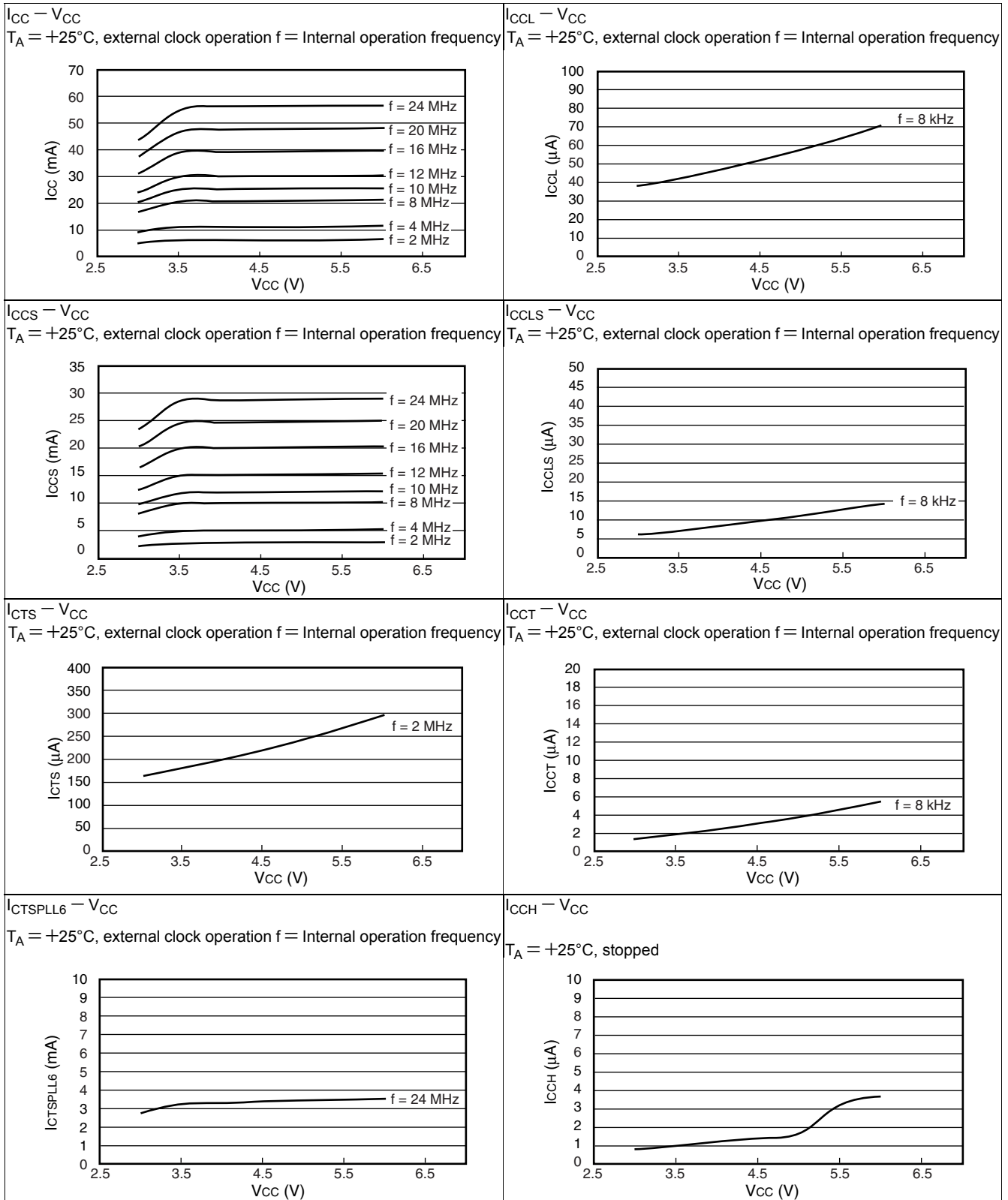




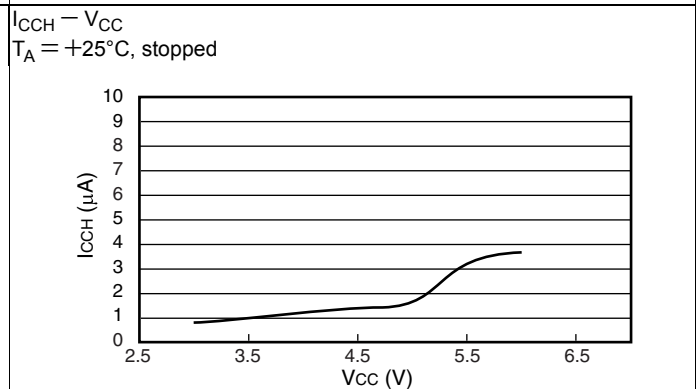
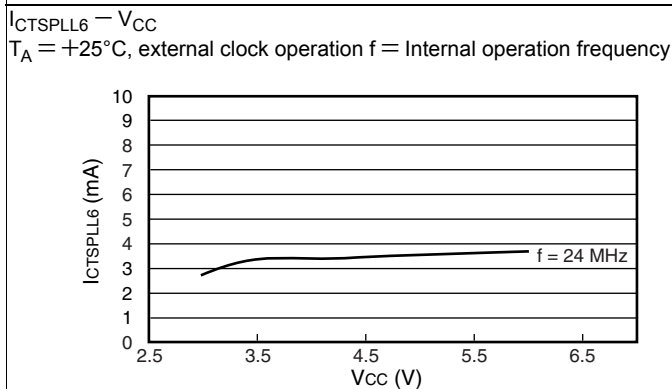
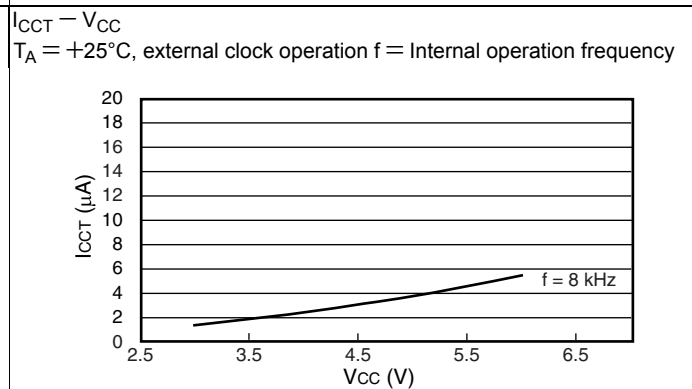
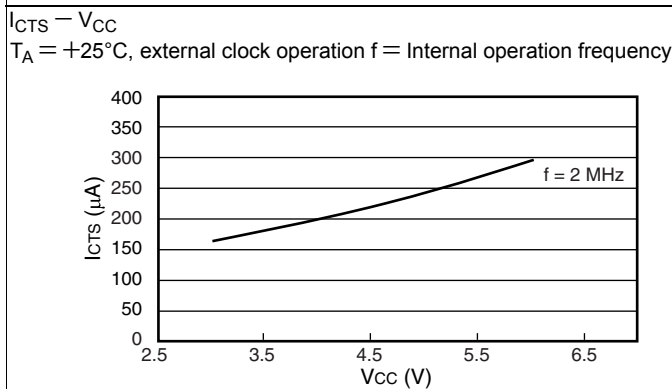
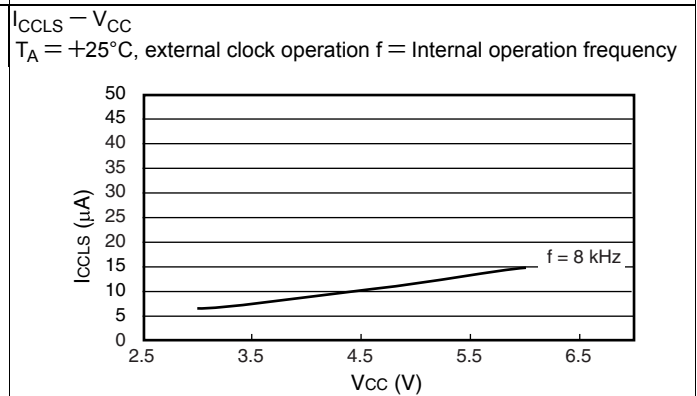
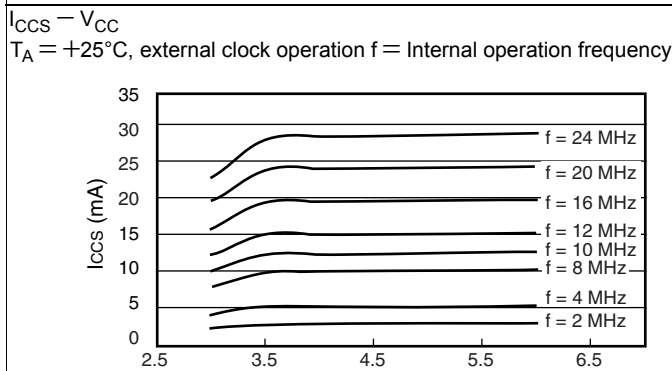
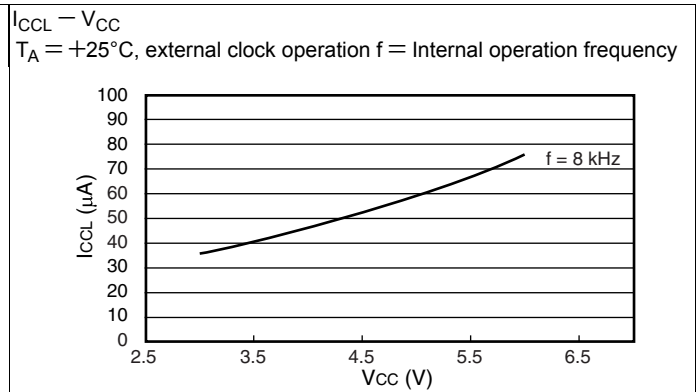
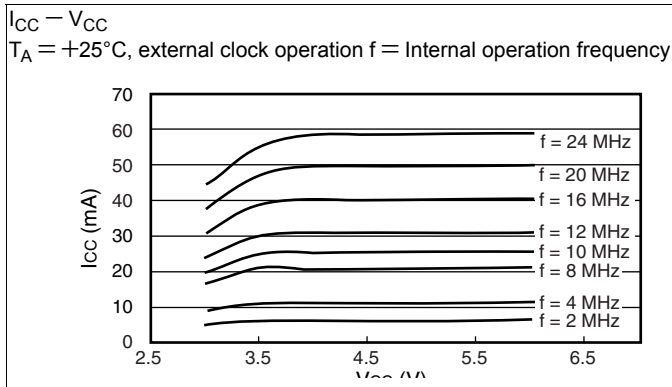
■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES



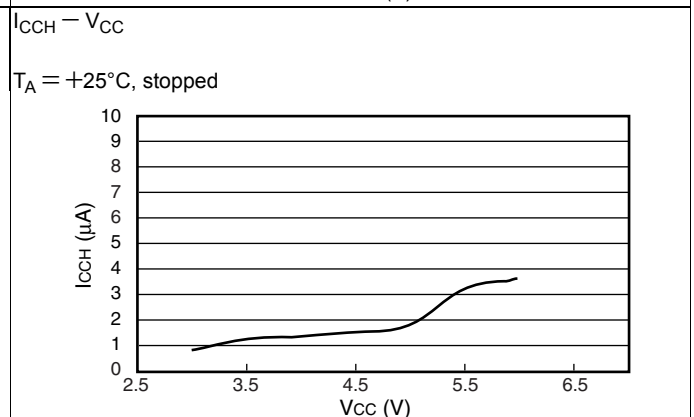
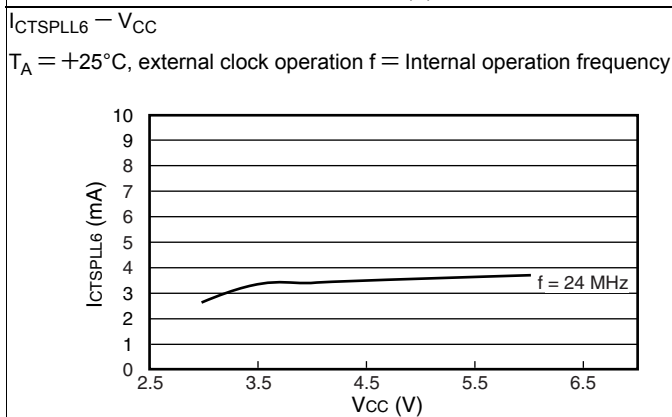
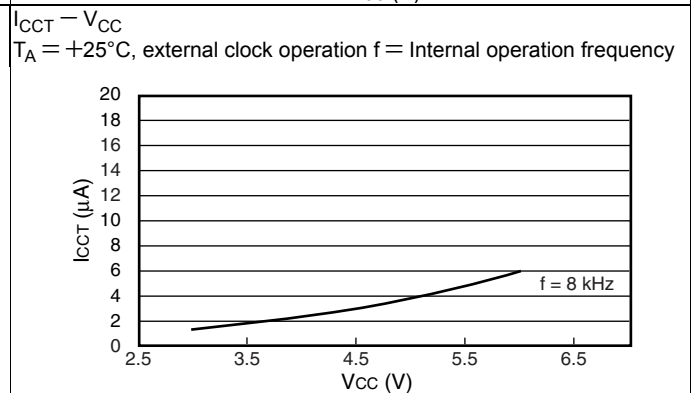
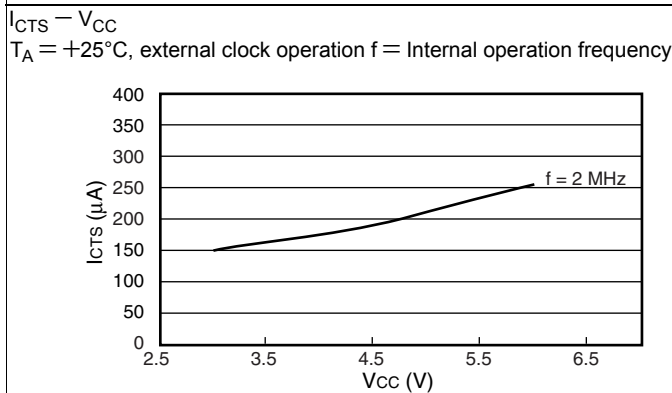
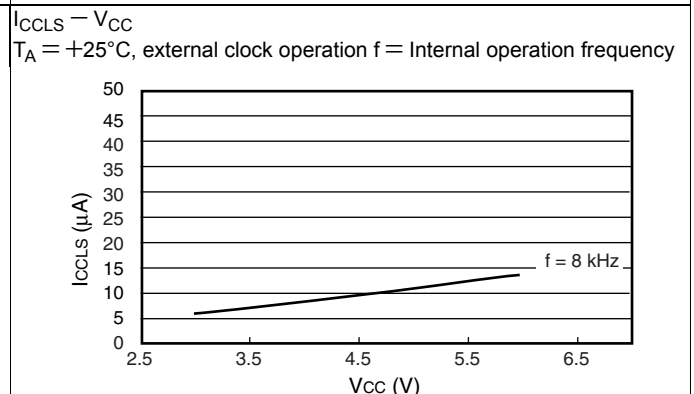
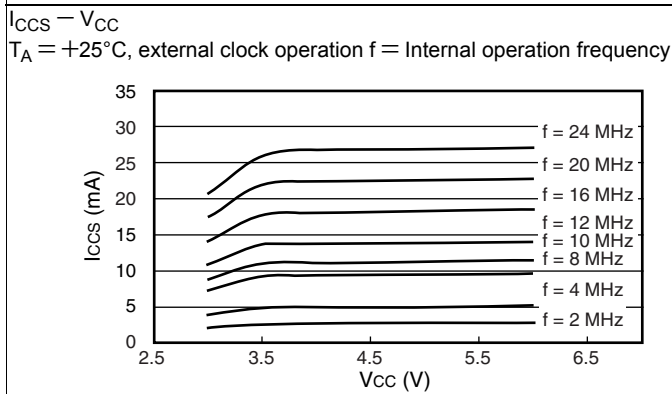
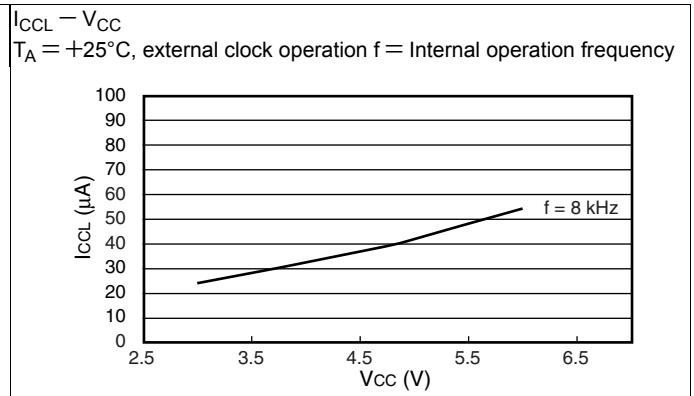
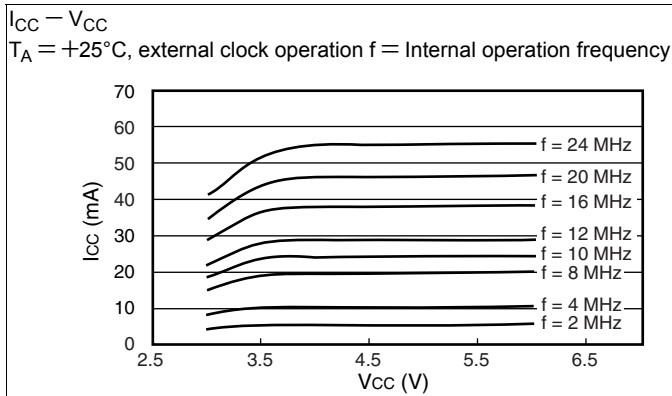
■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES



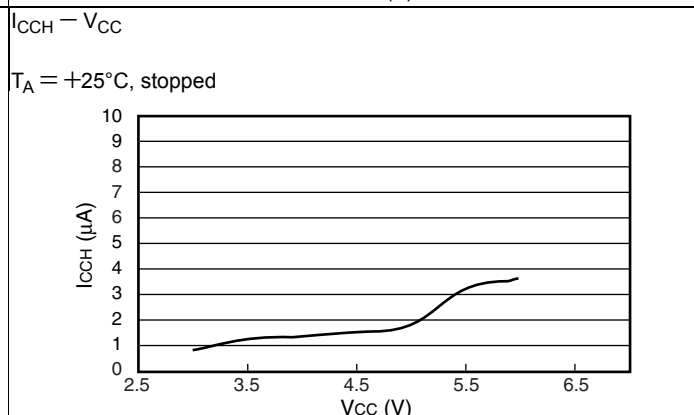
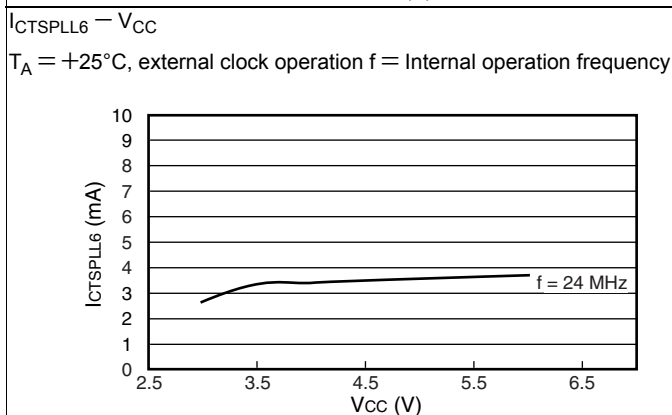
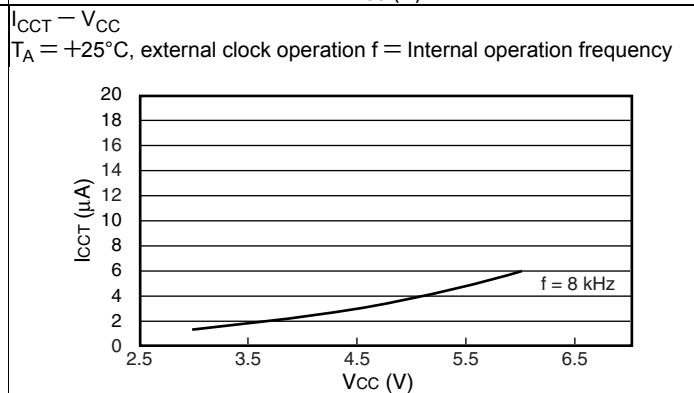
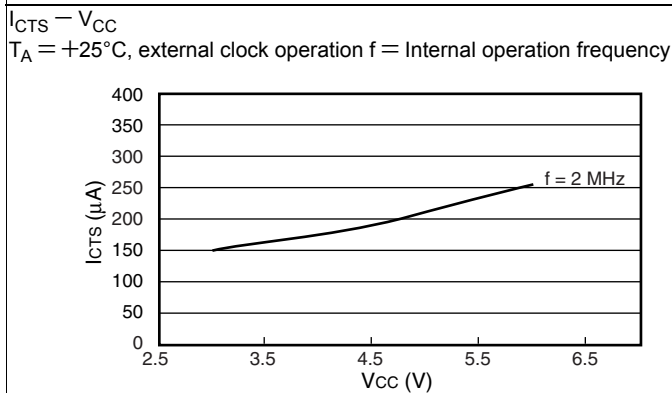
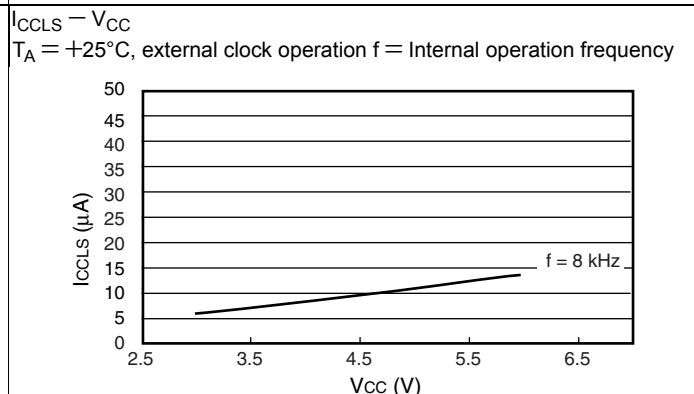
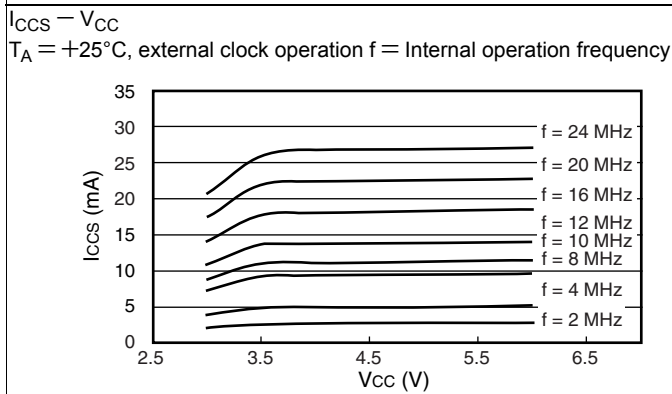
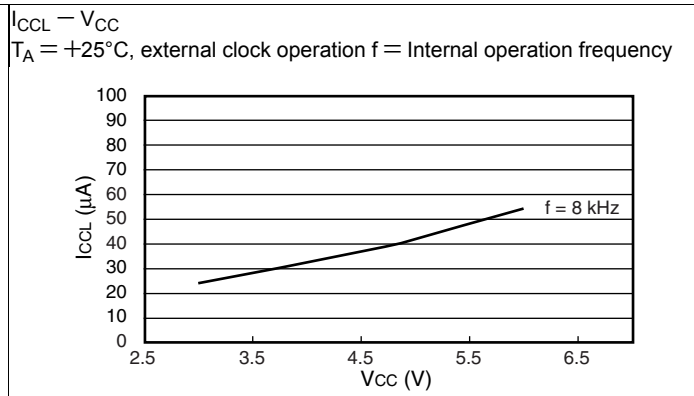
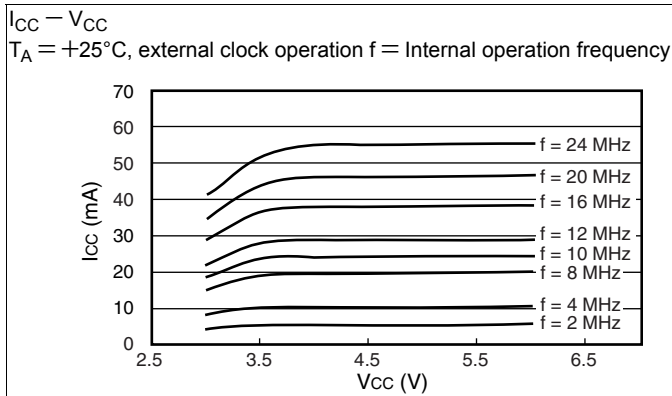
■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES



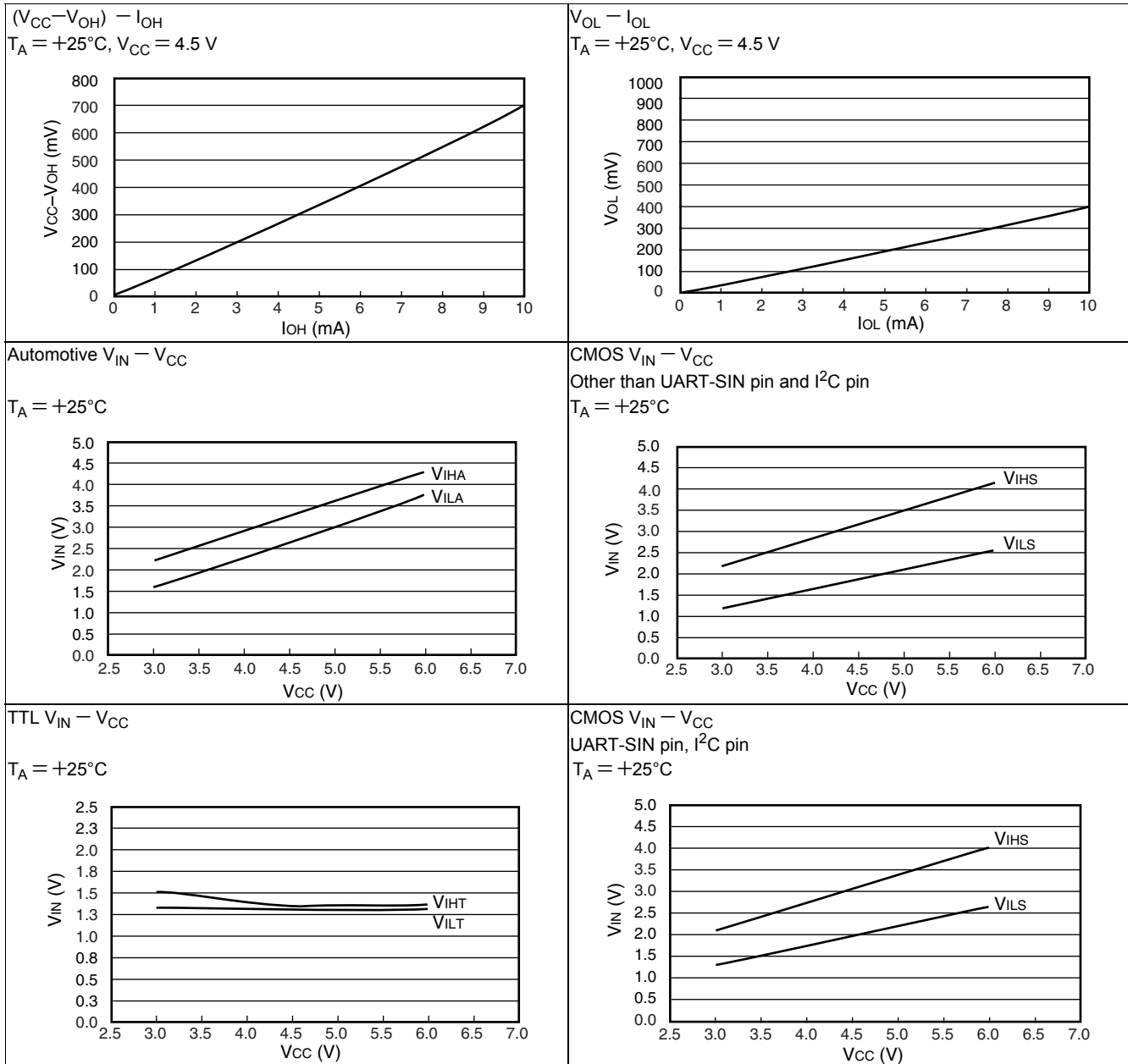
■ MB90346E, MB90346ES, MB90346CE, MB90346CES



■ MB90347E, MB90347ES, MB90347CE, MB90347CES



■ I/O characteristics



**13. Ordering Information**

Part number	Package	Remarks
MB90F342EPPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F342ESPF		
MB90F342CEPF		
MB90F342CESPF		
MB90F342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F342ESPMC		
MB90F342CEPMC		
MB90F342CESPMC		
MB90F345EPPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F345ESPF		
MB90F345CEPF		
MB90F345CESPF		
MB90F345EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F345ESPMC		
MB90F345CEPMC		
MB90F345CESPMC		
MB90F346EPPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F346ESPF		
MB90F346CEPF		
MB90F346CESPF		
MB90F346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F346ESPMC		
MB90F346CEPMC		
MB90F346CESPMC		

*(Continued)*

Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
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MB90342CEPMC		
MB90342CESPMC		

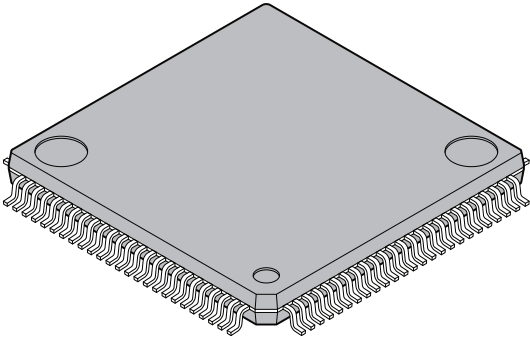
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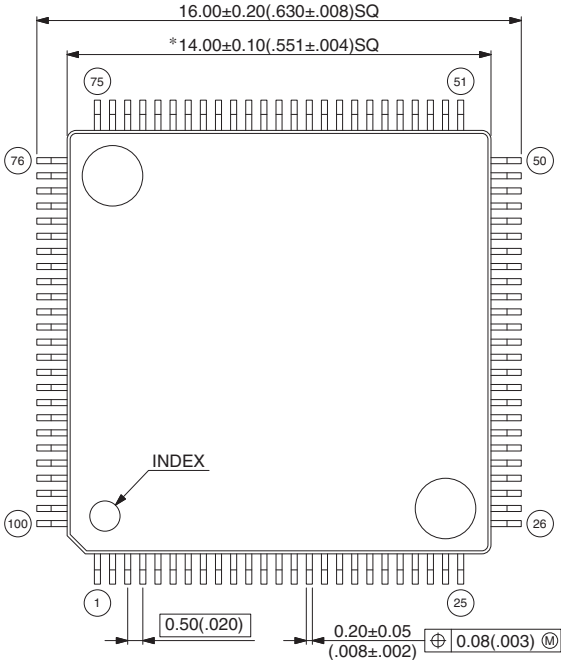
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Part number	Package	Remarks	
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90346ESPF			
MB90346CEPF			
MB90346CESPF			
MB90346EPMC	100-pin plastic LQFP (FPT-100P-M20)		
MB90346ESPMC			
MB90346CEPMC			
MB90346CESPMC			
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90347ESPF			
MB90347CEPF			
MB90347CESPF			
MB90347EPMC	100-pin plastic LQFP (FPT-100P-M20)		
MB90347ESPMC			
MB90347CEPMC			
MB90347CESPMC			
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90348ESPF			
MB90348CEPF			
MB90348CESPF			
MB90348EPMC	100-pin plastic LQFP (FPT-100P-M20)		
MB90348ESPMC			
MB90348CEPMC			
MB90348CESPMC			
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90349ESPF			
MB90349CEPF			
MB90349CESPF			
MB90349EPMC	100-pin plastic LQFP (FPT-100P-M20)		
MB90349ESPMC			
MB90349CEPMC			
MB90349CESPMC			
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation	
MB90V340E-102CR			

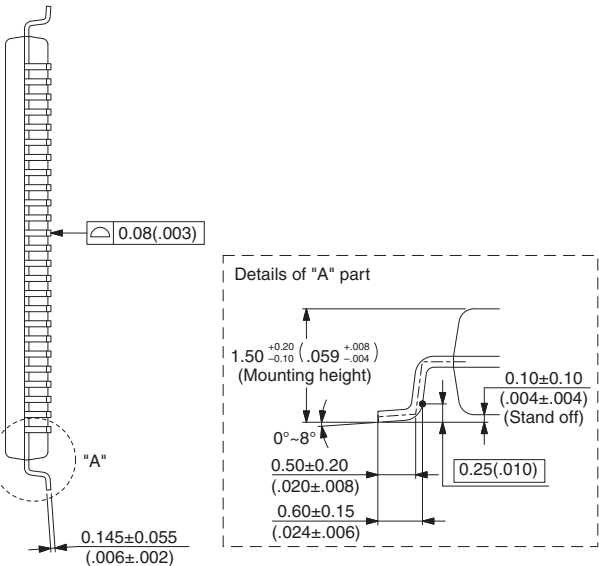
**14. Package Dimensions**

<p>100-pin plastic LQFP</p>  <p>(FPT-100P-M20)</p>	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP  
(FPT-100P-M20)



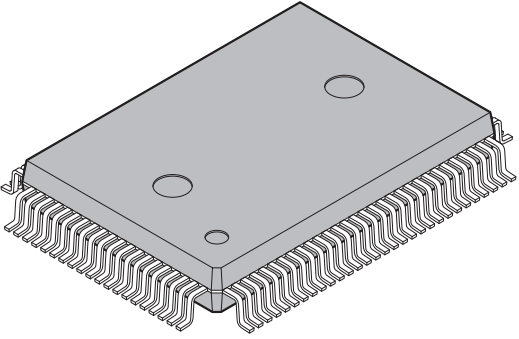
Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.

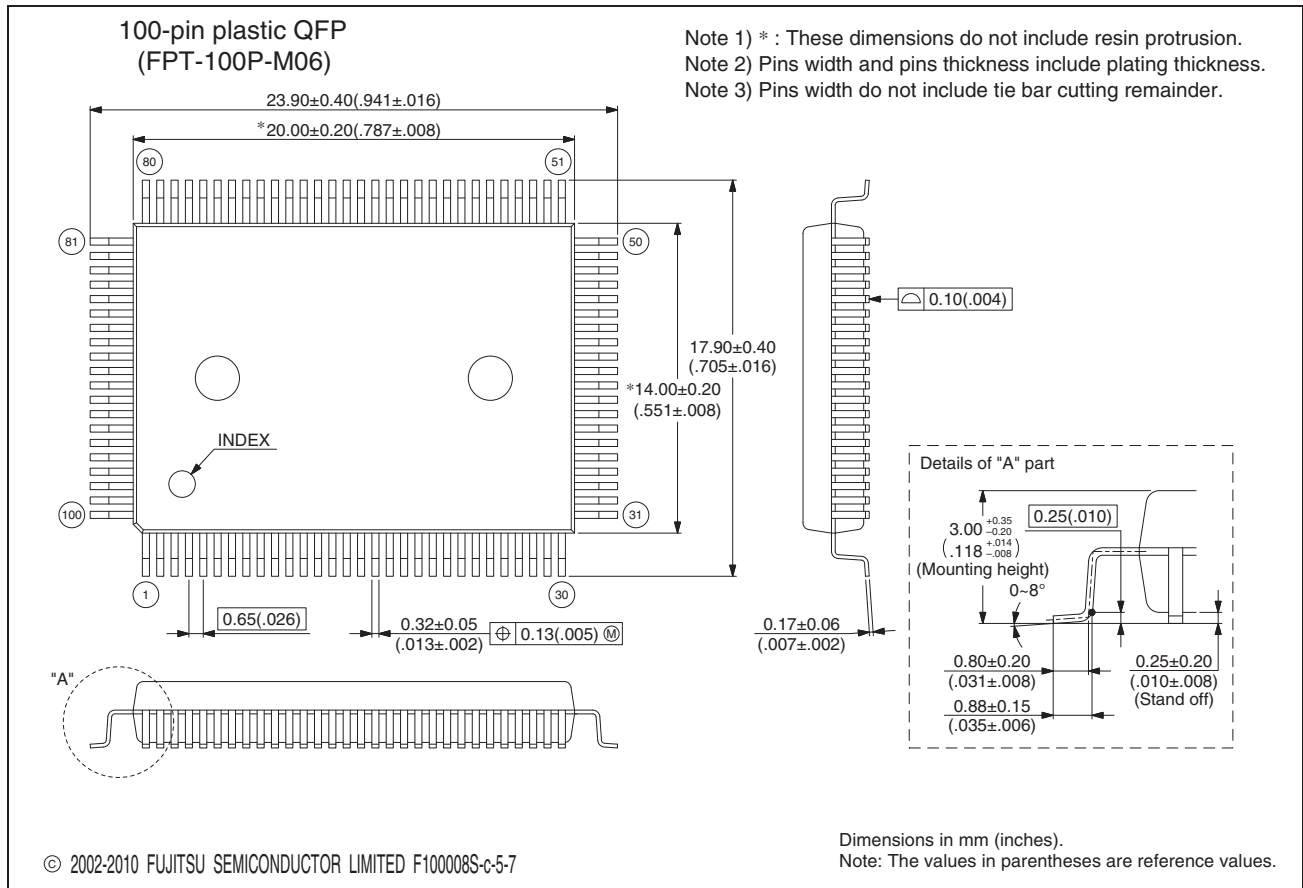


Dimensions in mm (inches).  
Note: The values in parentheses are reference values

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(Continued)

<p style="text-align: center;">100-pin plastic QFP</p>  <p style="text-align: center;">(FPT-100P-M06)</p>	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



**15. Major Changes**

**Spanсион Publication Number: DS07-13747-4E**

Page	Section	Change Results
—	—	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L” level maximum output current and “H” level maximum output current. Added “*7” in remark for “L” level average output current and “H” level average output current. Added “*8” in remark for “L” level average overall output current and “H” level average overall output current.
52		Added as follows. “*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

**NOTE:** Please see “Document History” about later revised information.

**Document History**

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template

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Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
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Wireless/RF	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

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