

16-bit Microcontroller

CMOS

F²MC-16LX MB90340E Series

MB90341E(S)/341CE(S)/342E(S)/342CE(S)/F342E(S)/F342CE(S)/F343E(S)/F343CE(S)/F345E(S)/
MB90F345CE(S)/346E(S)/346CE(S)/F346E(S)/F346CE(S)/347E(S)/347CE(S)/F347E(S)/F347CE(S)/
MB90348E(S)/348CE(S)/349E(S)/349CE(S)/F349E(S)/F349CE(S)/V340E-101/V340E-102

■ DESCRIPTION

The MB90340E series with up to 2 FULL-CAN* interfaces is especially designed for automotive and other industrial applications. Its main feature are the on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The power to the MCU core (3 V) is supplied by a built-in regulator circuit, giving these microcontrollers superior performance in terms of power consumption and tolerance to EMI.

* : Controller Area Network (CAN) - License of Robert Bosch GmbH

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page

URL : <http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

MB90340E Series

■ FEATURES

• CPU

- Instruction system best suited to controller
 - Wide choice of data types (bit, byte, word, and long word)
 - Wide choice of addressing modes (23 types)
 - Enhanced functionality with signed multiply and divide instructions and the RETI instruction
 - Enhanced high-precision computing with 32-bit accumulator
- Instruction system compatible with high-level language (C language) and multitask
 - Employing system stack pointer
 - Various enhanced pointer indirect instructions
 - Barrel shift instructions
- Increased processing speed
 - 4-byte instruction queue

• Serial interface

- UART (LIN/SCI) : up to 4 channels
 - Equipped with full-duplex double buffer
 - Clock-asynchronous or clock-synchronous serial transmission is available
- I²C interface* : up to 2 channels (only for devices with a C suffix in the part number)
 - Up to 400 kbps transfer rate

• Interrupt controller

- Powerful 8-level, 34-condition interrupt feature
- Up to 16 external interrupts are supported
- Automatic data transfer function independent of CPU
 - Expanded intelligent I/O service function (EI²OS) : up to 16 channels

• I/O ports

- General-purpose input/output port (CMOS output)
 - 80 ports (for devices without an S suffix in the part number - i.e. devices that support the sub clock)
 - 82 ports (for devices with an S suffix in the part number - i.e. devices that do not support the sub clock)

• 8/10-bit A/D converter

- 16 channels (only for devices without a C suffix in the part number)
- 24 channels (only for devices with a C suffix in the part number)
- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time : 3 μs (at 24 MHz machine clock, including sampling time)

• Program patch function

- Detects address matches against 6 address pointers

• Timer

- Time-base timer, watch timer, watchdog timer : 1 channel
- 8/16-bit PPG timer : 8-bit × 16 channels, or 16-bit × 8 channels
- 16-bit reload timer : 4 channels
- 16-bit input/output timer
 - 16-bit free-run timer : 2 channels
(FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
 - 16-bit input capture: (ICU): 8 channels
 - 16-bit output compare: (OCU): 8 channels

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- **Full-CAN controller**

- Up to 2 channels
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 16 built-in message buffers
- CAN wake-up function

- **Low power consumption (standby) mode**

- Sleep mode (a mode that halts CPU operating clock)
- Timebase timer mode (a mode where only the oscillation clock, sub clock, timebase timer and watch timer operate)
- Watch mode (a mode that operates sub clock and clock timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode

- **Clock modulation circuit**

- **Technology**

- CMOS technology

* : I²C license :

Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

MB90340E Series

■ PRODUCT LINEUP

Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F343E(S), MB90F343CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Parameter			
Type	Evaluation products	Flash memory products	MASK ROM products
CPU	F ² MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	External	512 Kbytes : MB90F345E(S), MB90F345CE(S) 384 Kbytes : MB90F343E(S), MB90F343CE(S) 256 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 128 Kbytes : MB90F347E(S), MB90F347CE(S) 64 Kbytes : MB90F346E(S), MB90F346CE(S)	256 Kbytes : MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S) 128 Kbytes : MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S) 64 Kbytes : MB90346E(S), MB90346CE(S)
RAM	30 Kbytes	20 Kbytes : MB90F343E(S), MB90F343CE(S), MB90F345E(S), MB90F345CE(S) 16 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 6 Kbytes : MB90F347E(S), MB90F347CE(S) 2 Kbytes : MB90F346E(S), MB90F346CE(S)	16 Kbytes : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) 6 Kbytes : MB90347E(S), MB90347CE(S) 2 Kbytes : MB90346E(S), MB90346CE(S)
Emulator-specific power supply*1	Yes	—	
Technology	0.35 μm CMOS with regulator for built-in power supply	0.35 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%	3.5 V to 5.5 V : When normal operating (not using A/D converter) 4.0 V to 5.5 V : When using the A/D converter/Flash programming 4.5 V to 5.5 V : When using the external bus	
Temperature range	—	-40 °C to +105 °C	
Package	PGA-299	QFP-100, LQFP-100	
UART	5 channels	4 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I ² C (400 kbps)	2 channels	Devices with a C suffix in the part number : 2 channels Devices without a C suffix in the part number : —	

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MB90340E Series

Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F343E(S), MB90F343CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
A/D Converter	24 input channels	Devices with a C suffix in the part number : 24 channels Devices without a C suffix in the part number : 16 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μ s include sample time (per one channel)		
16-bit Reload Timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = Machine clock frequency) Supports External Event Count function		
16-bit I/O Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$, $f_{sys}/2^5$, $f_{sys}/2^6$, $f_{sys}/2^7$ (f_{sys} = Machine clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit I/O timer matches the output compare register A pair of compare registers can be used to generate an output signal.		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width		
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or 128 μ s@ f_{osc} = 4 MHz (f_{sys} = Machine clock frequency, f_{osc} = Oscillation clock frequency)		
CAN Interface	3 channels	2 channels : MB90F342E(S), MB90F342CE(S), MB90F343E(S), MB90F343CE(S), MB90F345E(S), MB90F345CE(S) 1 channel : MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	2 channels : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S) 1 channel : MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		

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MB90340E Series

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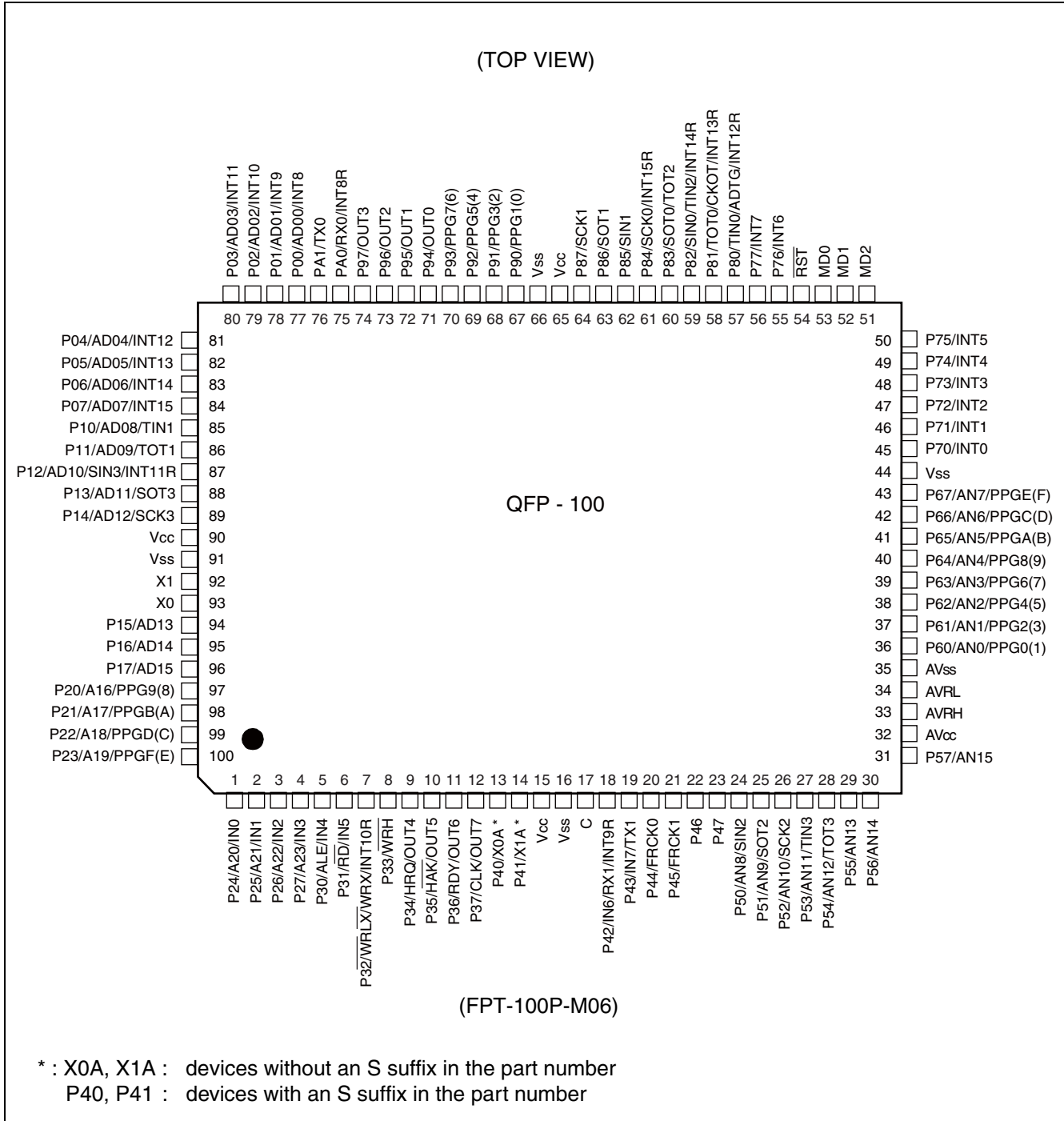
Part Number	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F343E(S), MB90F343CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Parameter			
External Interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI ² OS) and DMA		
D/A Converter	2 channels	—	
Sub clock (maximum 100 kHz)	Only for MB90V340E-102	Devices with sub clock : devices without an S suffix in the part number Devices without sub clock : devices with an S suffix in the part number	
I/O Ports	Virtually all external pins can be used as general purpose I/O port All ports are push-pull outputs Bit-wise settable as input/output or peripheral signal Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins) TTL input level settable for external bus (32-pin only for external bus)		
Flash Memory	—	Supports automatic programming, Embedded Algorithm ^{TM*2} Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 cycles Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (except for MB90F346E(S) and MB90F346CE (S))	

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual for details.

*2 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

PIN ASSIGNMENTS

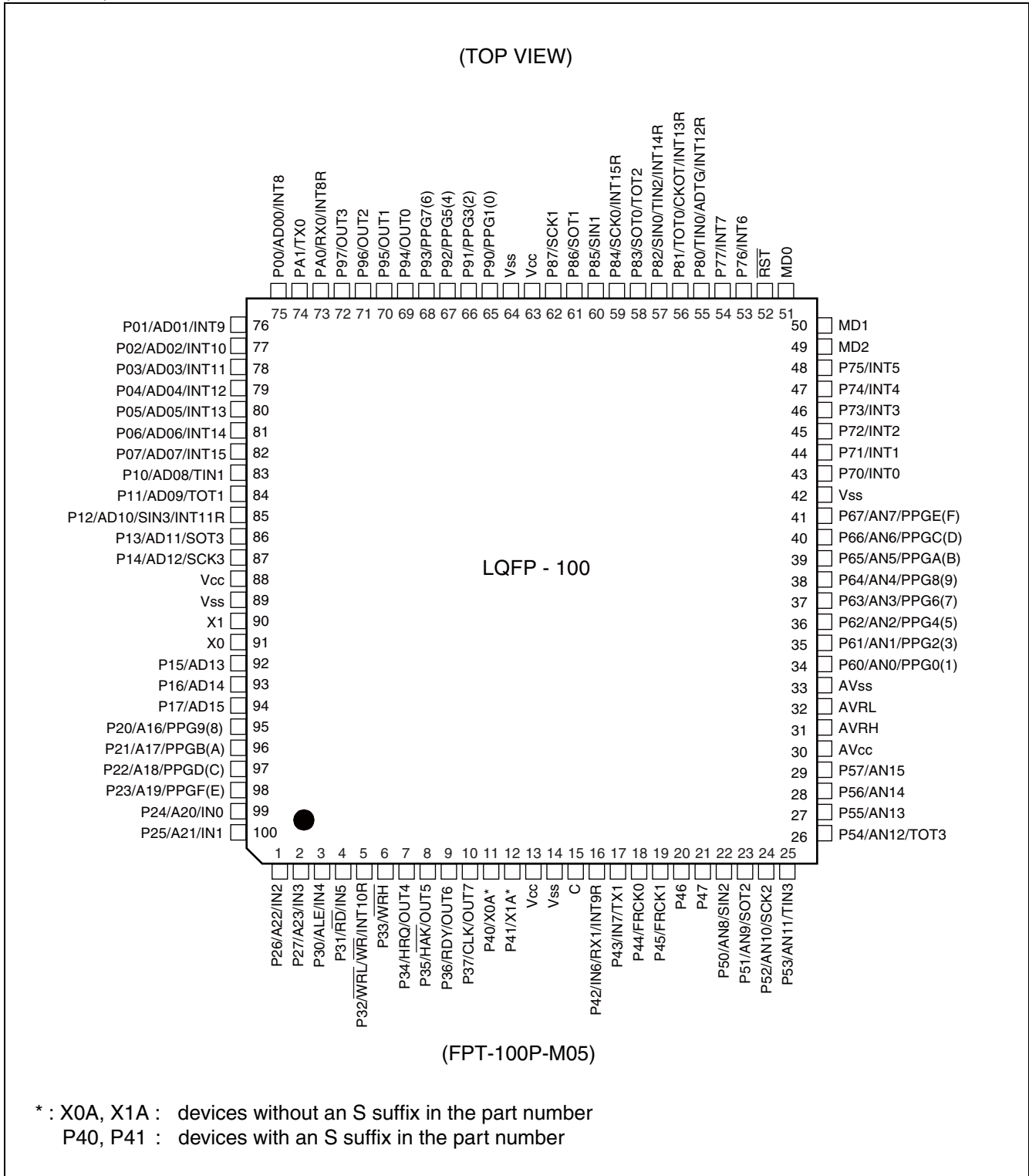
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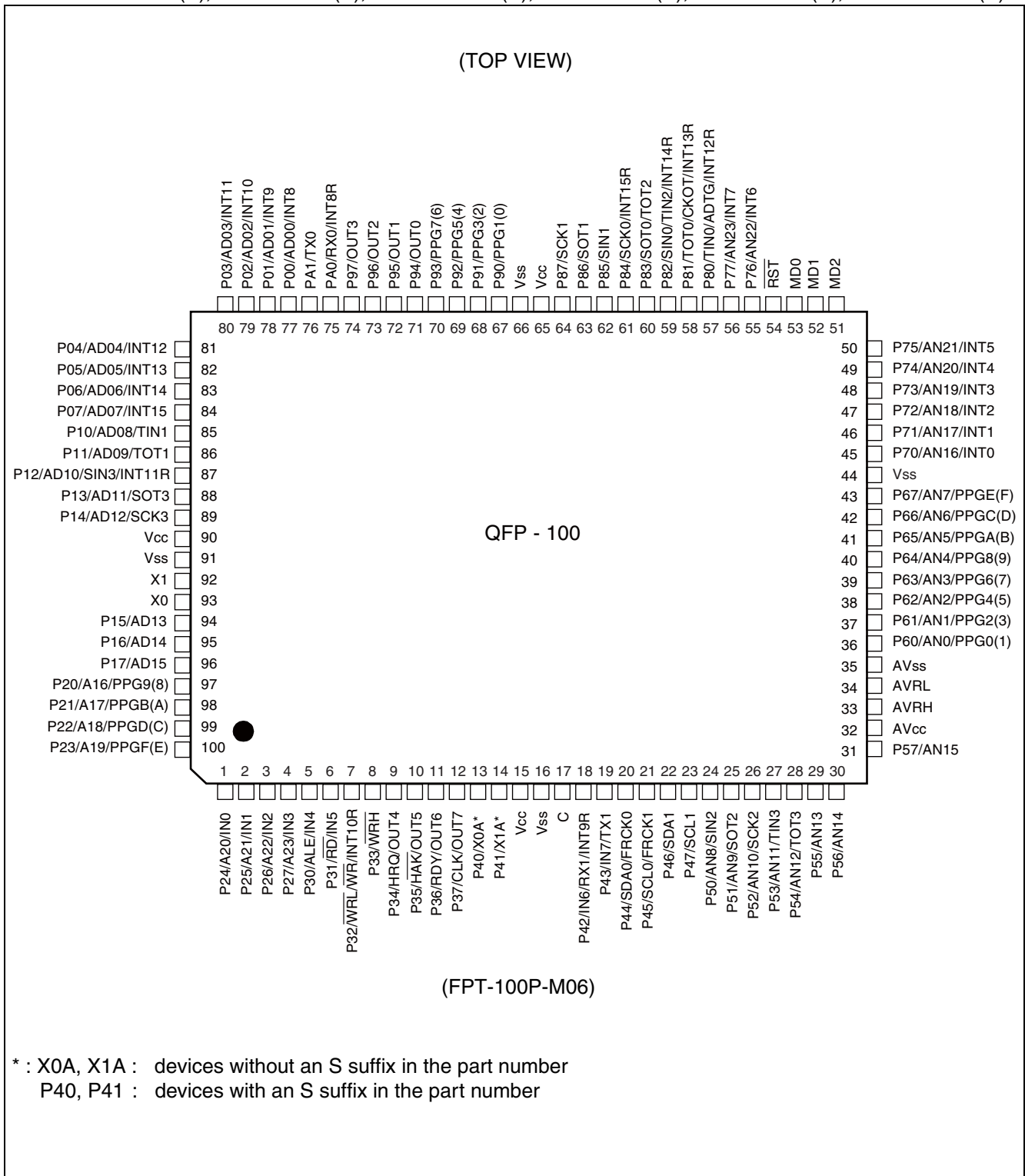
MB90340E Series

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MB90340E Series

- MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F343CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)



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■ PIN DESCRIPTION

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures.
5	3	P30	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture.
6	4	P31	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		\overline{RD}		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WR}/\overline{WRL}$ pin output is disabled.
		$\overline{WR} / \overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR}/\overline{WRL}$ pin output are enabled. \overline{WRL} is used to write-strobe 8 lower bits of the data bus in 16-bit access while \overline{WR} is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin.
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the \overline{WRH} pin output is disabled.
		\overline{WRH}		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the \overline{WRH} output pin is enabled.

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MB90340E Series

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare OCU7
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V _{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF .
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F343E/F345E only)
		INT9R		External interrupt request input pin

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MB90340E Series

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F343E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit I/O Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit I/O Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV _{cc}	K	Analog power input pin for the A/D Converter

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MB90340E Series

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV _{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V _{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	$\overline{\text{RST}}$	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

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MB90340E Series

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V _{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

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MB90340E Series

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
91	89	V _{SS}	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

(Continued)

MB90340E Series

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9,PPGB, PPGD,PPGF		Output pins for PPGs

*1 : FPT-100P-M06

*2 : FPT-100P-M05

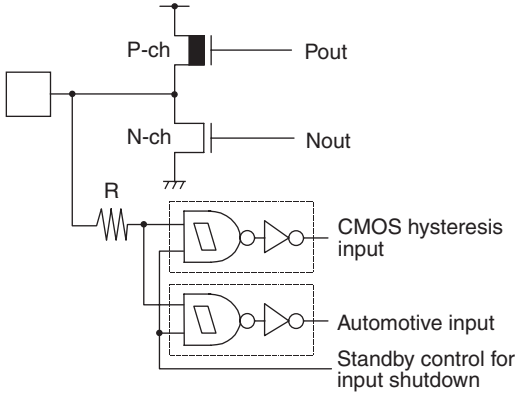
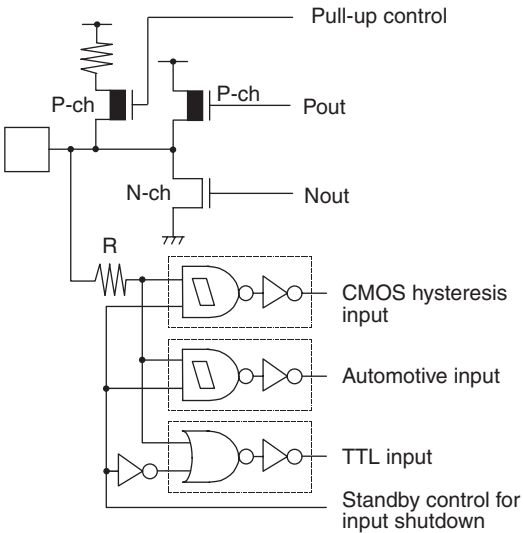
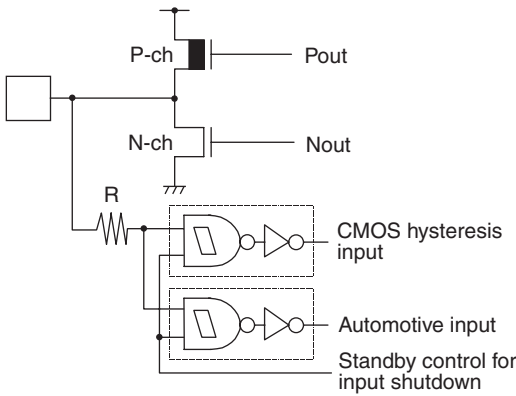
*3 : For I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

MB90340E Series

■ I/O CIRCUIT TYPE

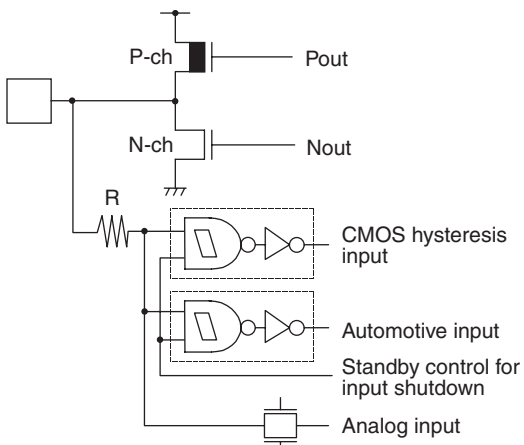
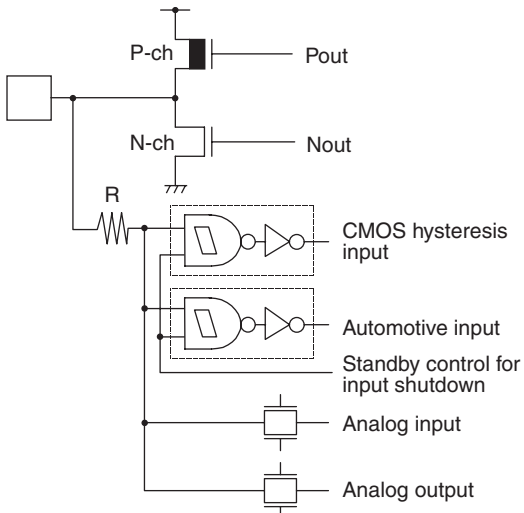
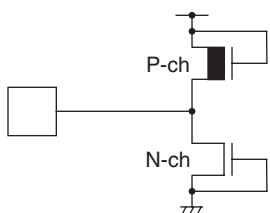
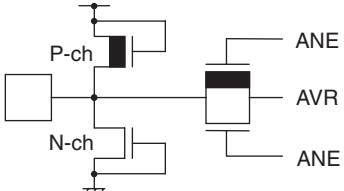
Type	Circuit	Remarks
A		<p>Oscillation circuit</p> <p>High-speed oscillation feedback resistor = approx. 1 MΩ</p>
B		<p>Oscillation circuit</p> <p>Low-speed oscillation feedback resistor = approx. 10 MΩ</p>
C		<ul style="list-style-type: none"> • MASK ROM and evaluation products: CMOS hysteresis input pin • Flash memory products: CMOS input pin
D		<p>MASK ROM and evaluation products:</p> <ul style="list-style-type: none"> • CMOS hysteresis input pin • Pull-down resistor value: approx. 50 kΩ <p>Flash memory products:</p> <ul style="list-style-type: none"> • CMOS input pin • No pull-down
E		<p>CMOS hysteresis input pin</p> <p>Pull-up resistor value: approx. 50 kΩ</p>

(Continued)

Type	Circuit	Remarks
F	 <p>The diagram shows a CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The gates of both are connected to a common input node. A pull-up resistor R is connected between the input node and the P-ch gate. The output of the P-ch is labeled Pout and the output of the N-ch is labeled Nout. The input node is connected to three input blocks: CMOS hysteresis input, Automotive input, and Standby control for input shutdown.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)
G	 <p>The diagram shows a CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The gates of both are connected to a common input node. A pull-up resistor R is connected between the input node and the P-ch gate. The output of the P-ch is labeled Pout and the output of the N-ch is labeled Nout. The input node is connected to four input blocks: CMOS hysteresis input, Automotive input, TTL input, and Standby control for input shutdown. A 'Pull-up control' signal is connected to the gate of the P-ch MOSFET.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) • Programmable pull-up resistor: $50 \text{ k}\Omega$ approx.
H	 <p>The diagram shows a CMOS output stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The gates of both are connected to a common input node. A pull-up resistor R is connected between the input node and the P-ch gate. The output of the P-ch is labeled Pout and the output of the N-ch is labeled Nout. The input node is connected to three input blocks: CMOS hysteresis input, Automotive input, and Standby control for input shutdown.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)

(Continued)

MB90340E Series

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input
J		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • D/A analog output • CMOS hysteresis input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input
K		<p>Power supply input protection circuit</p>
L		<ul style="list-style-type: none"> • A/D converter reference voltage power supply input pin, with the protection circuit • Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH

(Continued)

(Continued)

Type	Circuit	Remarks
M		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)
N		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) <p>Programmable pull-up resistor: 50 kΩ approx</p>
O		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS input (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input

MB90340E Series

■ HANDLING DEVICES

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC} , AV_{RH}) exceed the digital power-supply voltage.

2. Handling unused pins

Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k Ω or more.

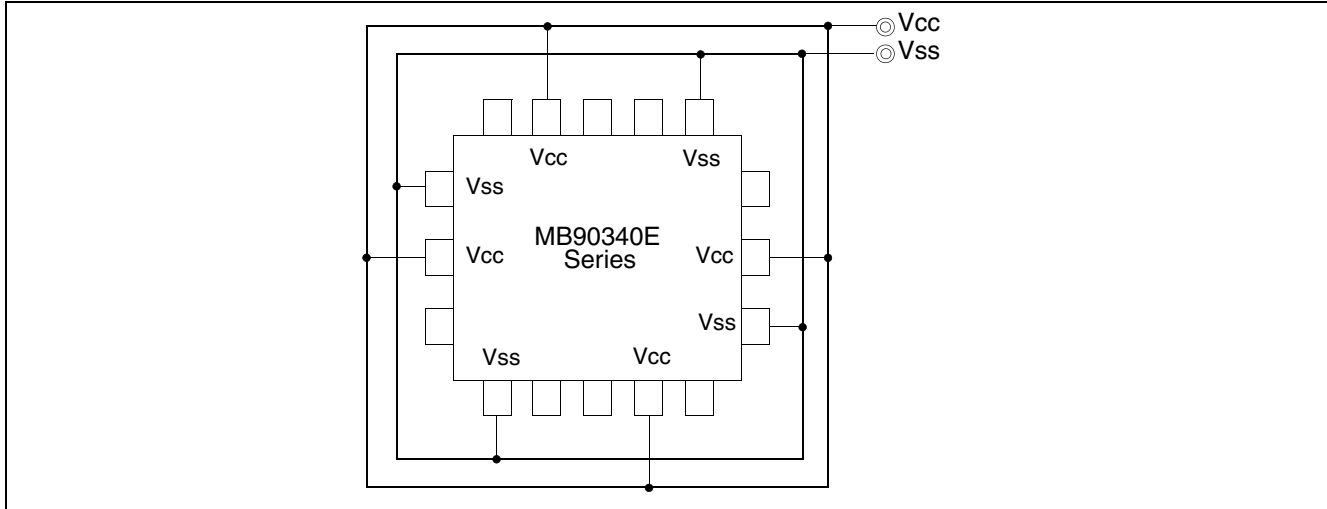
3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.

Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , AV_{RH} , AV_{RL}) and analog inputs (AN0 to AN23) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AV_{RH} or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$.

7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

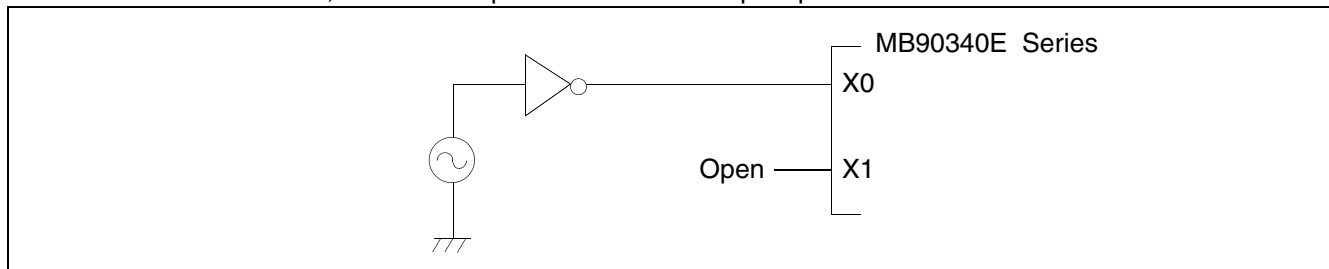
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.



10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

11. Notes on operation in PLL clock mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

12. Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 μ s or more (0.2 V to 2.7 V)

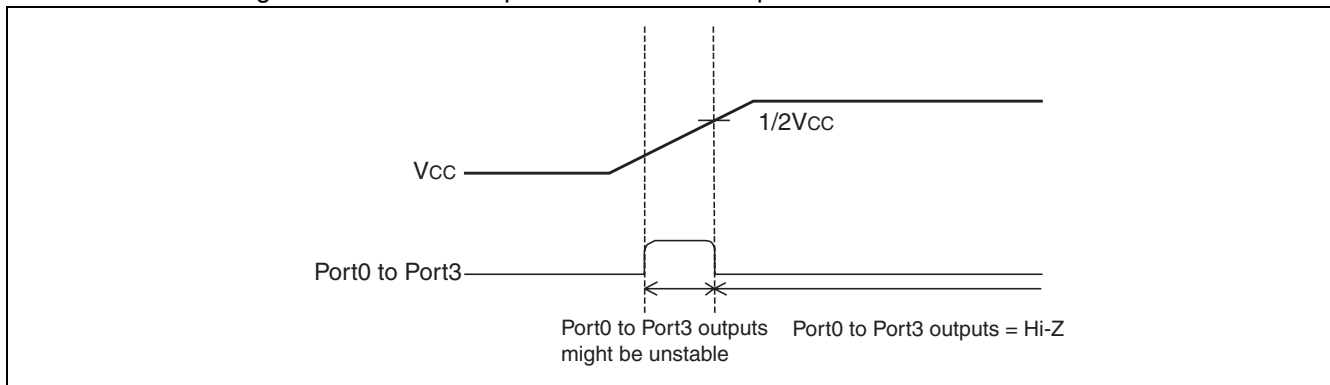
MB90340E Series

13. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

14. Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



15. Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

16. Flash Security Function (except for MB90F346E)

A security bit is located in the area of the flash memory.

If protection code 01_H is written in the security bit, the flash memory is in the protected state by security.

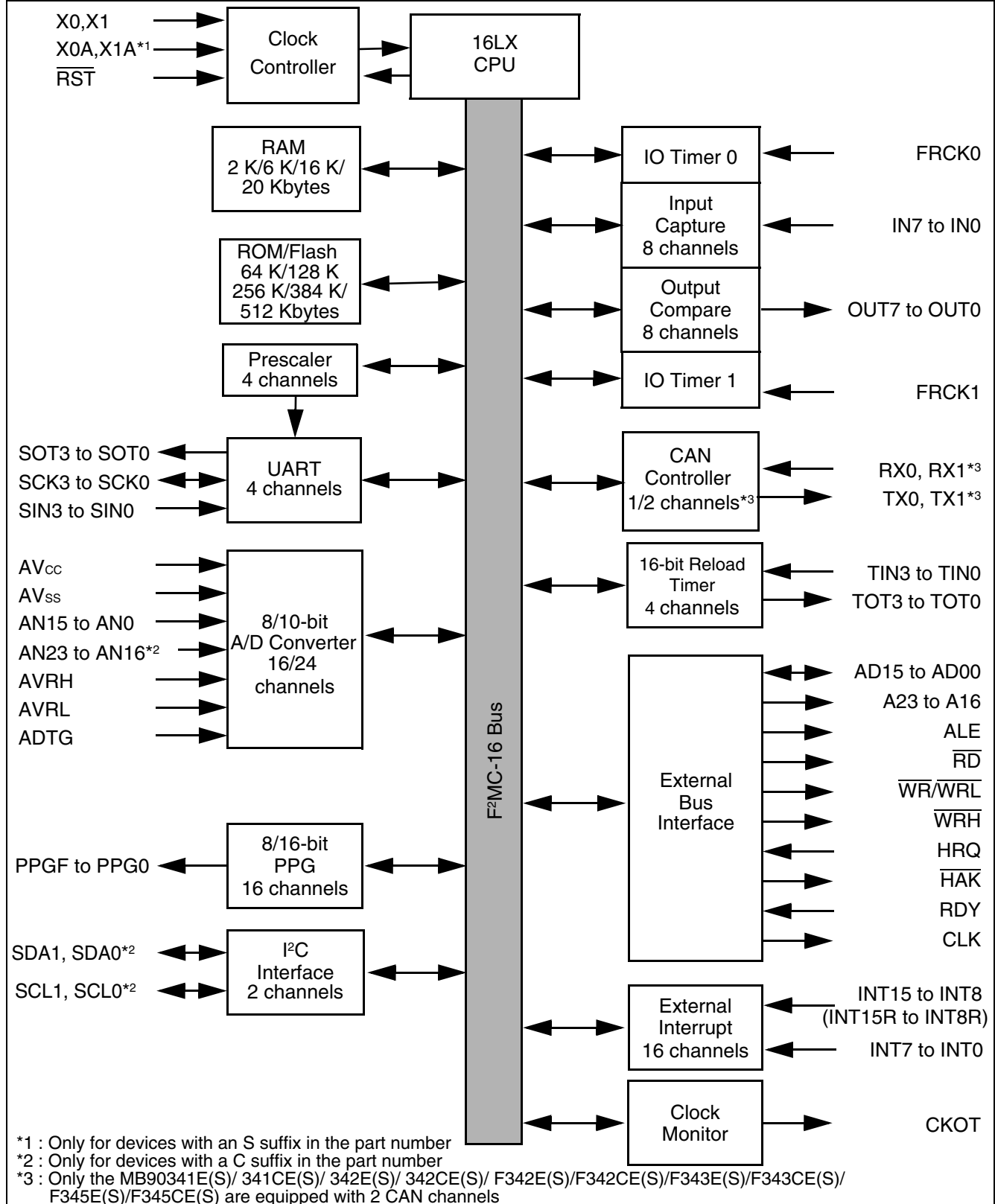
Therefore please do not write 01_H in this address if you do not use the security function.

Refer to following table for the address of the security bit.

	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	FE0001 _H
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	FC0001 _H
MB90F343E	Embedded 3 Mbits Flash Memory	F90001 _H
MB90F345E	Embedded 4 Mbits Flash Memory	F80001 _H

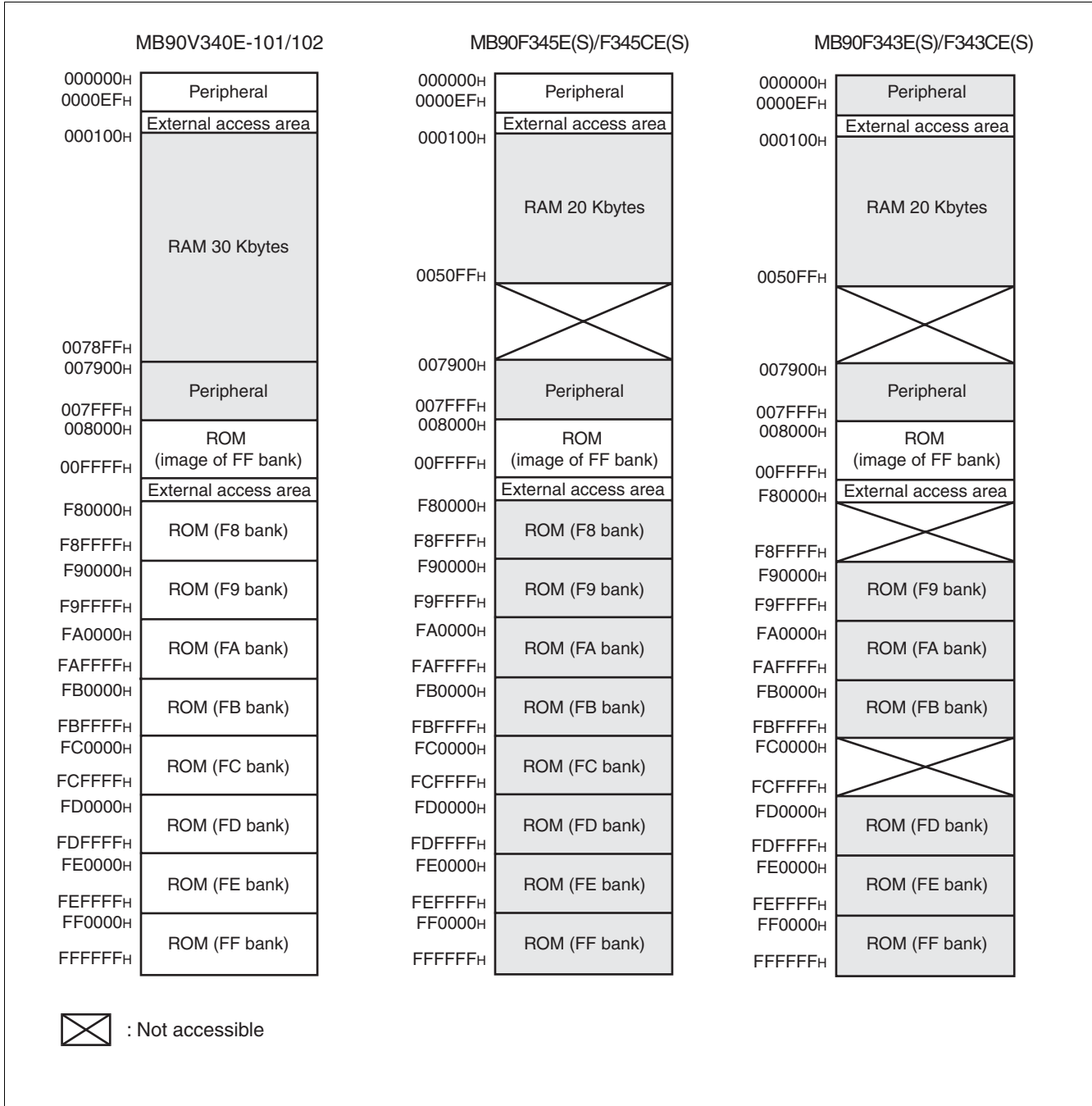
■ BLOCK DIAGRAMS

MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F343E(S), MB90F343CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)

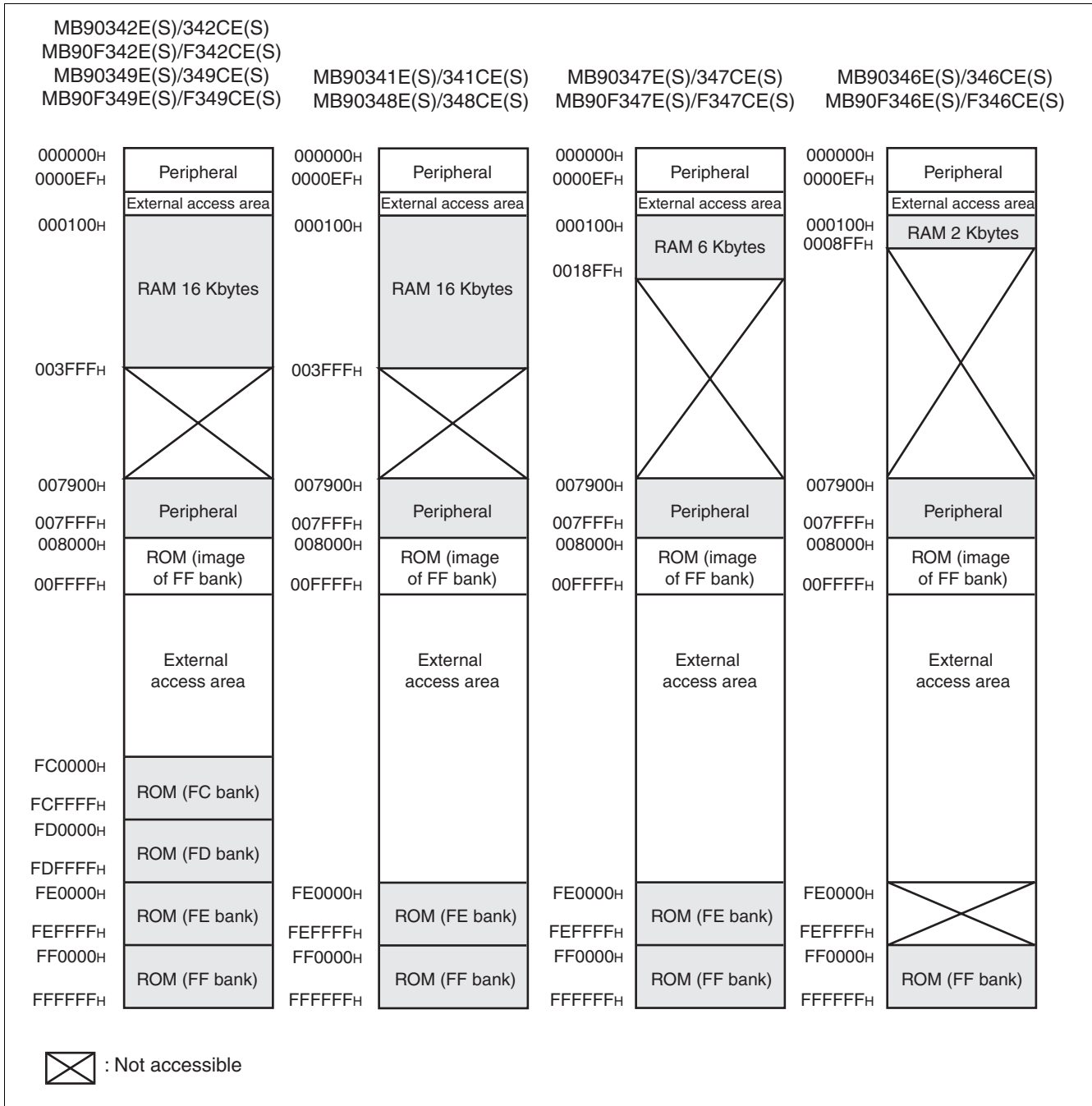


MB90340E Series

MEMORY MAP



MB90340E Series



Note: An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.

For example, when the address 00C000H is accessed, the data at FFC000H in ROM is actually accessed. The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

As a result, the image between FF8000H and FFFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

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■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
00000H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
00001H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
00002H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
00003H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
00004H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
00005H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
00006H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
00007H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
00008H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
00009H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX _B
0000AH	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX _B
0000BH	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	1111111 _B
0000CH	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	1111111 _B
0000DH	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	1111111 _B
0000EH	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXX _B
0000FH	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXX _B
00010H	Port 0 Direction Register	DDR0	R/W	Port 0	0000000 _B
00011H	Port 1 Direction Register	DDR1	R/W	Port 1	0000000 _B
00012H	Port 2 Direction Register	DDR2	R/W	Port 2	0000000 _B
00013H	Port 3 Direction Register	DDR3	R/W	Port 3	0000000 _B
00014H	Port 4 Direction Register	DDR4	R/W	Port 4	0000000 _B
00015H	Port 5 Direction Register	DDR5	R/W	Port 5	0000000 _B
00016H	Port 6 Direction Register	DDR6	R/W	Port 6	0000000 _B
00017H	Port 7 Direction Register	DDR7	R/W	Port 7	0000000 _B
00018H	Port 8 Direction Register	DDR8	R/W	Port 8	0000000 _B
00019H	Port 9 Direction Register	DDR9	R/W	Port 9	0000000 _B
0001AH	Port A Direction Register	DDRA	R/W	Port A	0000100 _B
0001BH	Reserved				
0001CH	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	0000000 _B
0001DH	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	0000000 _B
0001EH	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	0000000 _B
0001FH	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	0000000 _B

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
000020 _H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000 _B
000021 _H	Serial Control Register 0	SCR0	W,R/W		00000000 _B
000022 _H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000 _B
000023 _H	Serial Status Register 0	SSR0	R,R/W		00001000 _B
000024 _H	Extended Communication Control Register 0	ECCR0	R,W, R/W		000000XX _B
000025 _H	Extended Status/Control Register 0	ESCR0	R/W		00000100 _B
000026 _H	Baud Rate Generator Register 00	BGR00	R/W		00000000 _B
000027 _H	Baud Rate Generator Register 01	BGR01	R/W		00000000 _B
000028 _H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000 _B
000029 _H	Serial Control Register 1	SCR1	W,R/W		00000000 _B
00002A _H	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000 _B
00002B _H	Serial Status Register 1	SSR1	R,R/W		00001000 _B
00002C _H	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XX _B
00002D _H	Extended Status/Control Register 1	ESCR1	R/W		00000100 _B
00002E _H	Baud Rate Generator Register 10	BGR10	R/W		00000000 _B
00002F _H	Baud Rate Generator Register 11	BGR11	R/W		00000000 _B
000030 _H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1 _B
000031 _H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001 _B
000032 _H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0 _B
000033 _H	Reserved				
000034 _H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1 _B
000035 _H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001 _B
000036 _H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0 _B
000037 _H	Reserved				
000038 _H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1 _B
000039 _H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001 _B
00003A _H	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0 _B
00003B _H	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 _B
00003C _H	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1 _B
00003D _H	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001 _B
00003E _H	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0 _B
00003F _H	Reserved				

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
000040 _H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1 _B
000041 _H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001 _B
000042 _H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0 _B
000043 _H	Reserved				
000044 _H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1 _B
000045 _H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001 _B
000046 _H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0 _B
000047 _H	Reserved				
000048 _H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1 _B
000049 _H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 _B
00004A _H	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 _B
00004B _H	Reserved				
00004C _H	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1 _B
00004D _H	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 _B
00004E _H	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 _B
00004F _H	Reserved				
000050 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
000051 _H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX _B
000052 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
000053 _H	Input Capture Edge 2/3	ICE23	R		XXXXXXXX _B
000054 _H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B
000055 _H	Input Capture Edge 4/5	ICE45	R		XXXXXXXX _B
000056 _H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000 _B
000057 _H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX _B
000058 _H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 _B
000059 _H	Output Compare Control Status 1	OCS1	R/W		0XX00000 _B
00005A _H	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 _B
00005B _H	Output Compare Control Status 3	OCS3	R/W		0XX00000 _B
00005C _H	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
00005D _H	Output Compare Control Status 5	OCS5	R/W		0XX00000 _B
00005E _H	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status 7	OCS7	R/W		0XX00000 _B

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
000060 _H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 _B
000061 _H	Timer Control Status 0	TMCSR0	R/W		XXXX0000 _B
000062 _H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 _B
000063 _H	Timer Control Status 1	TMCSR1	R/W		XXXX0000 _B
000064 _H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000 _B
000065 _H	Timer Control Status 2	TMCSR2	R/W		XXXX0000 _B
000066 _H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000 _B
000067 _H	Timer Control Status 3	TMCSR3	R/W		XXXX0000 _B
000068 _H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0 _B
000069 _H	A/D Control Status 1	ADCS1	R/W		0000000X _B
00006A _H	A/D Data 0	ADCR0	R		00000000 _B
00006B _H	A/D Data 1	ADCR1	R		XXXXXXXX00 _B
00006C _H	ADC Setting 0	ADSR0	R/W		00000000 _B
00006D _H	ADC Setting 1	ADSR1	R/W		00000000 _B
00006E _H	Reserved				
00006F _H	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXXX1 _B
000070 _H to 00008F _H	Reserved for CAN Controller 0/1. Refer to "■ CAN CONTROLLERS"				
000090 _H to 00009A _H	Reserved				
00009B _H	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000 _B
00009C _H	DMA Status L Register	DSRL	R/W		00000000 _B
00009D _H	DMA Status H Register	DSRH	R/W		00000000 _B
00009E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
00009F _H	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXXX0 _B
0000A0 _H	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000 _B
0000A1 _H	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100 _B
0000A2 _H , 0000A3 _H	Reserved				
0000A4 _H	DMA Stop Status Register	DSSR	R/W	DMA	00000000 _B

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5 _H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXXX111 _B
0000A9 _H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B
0000B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W,R/W		00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
0000C0 _H	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX _B
0000C1 _H	D/A Converter Data 1	DAT1	R/W		XXXXXXXX _B
0000C2 _H	D/A Control 0	DACR0	R/W		XXXXXXXX0 _B
0000C3 _H	D/A Control 1	DACR1	R/W		XXXXXXXX0 _B

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
0000C4 _H , 0000C5 _H	Reserved				
0000C6 _H	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000 _B
0000C7 _H	External Interrupt Source 0	EIRR0	R/W		XXXXXXXX _B
0000C8 _H	External Interrupt Level Setting 0	ELVR0	R/W		00000000 _B
0000C9 _H	External Interrupt Level Setting 0	ELVR0	R/W		00000000 _B
0000CA _H	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000 _B
0000CB _H	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX _B
0000CC _H	External Interrupt Level Setting 1	ELVR1	R/W		00000000 _B
0000CD _H	External Interrupt Level Setting 1	ELVR1	R/W		00000000 _B
0000CE _H	External Interrupt Source Select	EISSR	R/W		00000000 _B
0000CF _H	PLL/Sub clock Control Register	PSCCR	W	PLL	XXXX0000 _B
0000D0 _H	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXX _B
0000D1 _H	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXX _B
0000D2 _H	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXX _B
0000D3 _H	DMA Control Register	DMACS	R/W		XXXXXXXX _B
0000D4 _H	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX _B
0000D5 _H	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX _B
0000D6 _H	Data Counter L Register	DCTL	R/W		XXXXXXXX _B
0000D7 _H	Data Counter H Register	DCTH	R/W		XXXXXXXX _B
0000D8 _H	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000 _B
0000D9 _H	Serial Control Register 2	SCR2	W,R/W		00000000 _B
0000DA _H	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000 _B
0000DB _H	Serial Status Register 2	SSR2	R,R/W		00001000 _B
0000DC _H	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX _B
0000DD _H	Extended Status Control Register 2	ESCR2	R/W		00000100 _B
0000DE _H	Baud Rate Generator Register 20	BGR20	R/W		00000000 _B
0000DF _H	Baud Rate Generator Register 21	BGR21	R/W		00000000 _B
0000E0 _H to 0000EF _H	Reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS”				
0000F0 _H to 0000FF _H	External				

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
007900 _H	Reload Register L0	PRLLO	R/W	16-bit PPG 0/1	XXXXXXXX _B
007901 _H	Reload Register H0	PRLH0	R/W		XXXXXXXX _B
007902 _H	Reload Register L1	PRLLO1	R/W		XXXXXXXX _B
007903 _H	Reload Register H1	PRLH1	R/W		XXXXXXXX _B
007904 _H	Reload Register L2	PRLLO2	R/W	16-bit PPG 2/3	XXXXXXXX _B
007905 _H	Reload Register H2	PRLH2	R/W		XXXXXXXX _B
007906 _H	Reload Register L3	PRLLO3	R/W		XXXXXXXX _B
007907 _H	Reload Register H3	PRLH3	R/W		XXXXXXXX _B
007908 _H	Reload Register L4	PRLLO4	R/W	16-bit PPG 4/5	XXXXXXXX _B
007909 _H	Reload Register H4	PRLH4	R/W		XXXXXXXX _B
00790A _H	Reload Register L5	PRLLO5	R/W		XXXXXXXX _B
00790B _H	Reload Register H5	PRLH5	R/W		XXXXXXXX _B
00790C _H	Reload Register L6	PRLLO6	R/W	16-bit PPG 6/7	XXXXXXXX _B
00790D _H	Reload Register H6	PRLH6	R/W		XXXXXXXX _B
00790E _H	Reload Register L7	PRLLO7	R/W		XXXXXXXX _B
00790F _H	Reload Register H7	PRLH7	R/W		XXXXXXXX _B
007910 _H	Reload Register L8	PRLLO8	R/W	16-bit PPG 8/9	XXXXXXXX _B
007911 _H	Reload Register H8	PRLH8	R/W		XXXXXXXX _B
007912 _H	Reload Register L9	PRLLO9	R/W		XXXXXXXX _B
007913 _H	Reload Register H9	PRLH9	R/W		XXXXXXXX _B
007914 _H	Reload Register LA	PRLLOA	R/W	16-bit PPG A/B	XXXXXXXX _B
007915 _H	Reload Register HA	PRLHA	R/W		XXXXXXXX _B
007916 _H	Reload Register LB	PRLLOB	R/W		XXXXXXXX _B
007917 _H	Reload Register HB	PRLHB	R/W		XXXXXXXX _B
007918 _H	Reload Register LC	PRLLOC	R/W	16-bit PPG C/D	XXXXXXXX _B
007919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
00791A _H	Reload Register LD	PRLLOD	R/W		XXXXXXXX _B
00791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
00791C _H	Reload Register LE	PRLLOE	R/W	16-bit PPG E/F	XXXXXXXX _B
00791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
00791E _H	Reload Register LF	PRLLOF	R/W		XXXXXXXX _B
00791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
007920 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
007921 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
007922 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007923 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
007924 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
007925 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
007926 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007927 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007928 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
007929 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
00792A _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792B _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792C _H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
00792D _H	Input Capture 6	IPCP6	R		XXXXXXXX _B
00792E _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
00792F _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
007930 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
007931 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
007932 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007933 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007934 _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
007935 _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
007936 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007937 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007938 _H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
007939 _H	Output Compare 4	OCCP4	R/W		XXXXXXXX _B
00793A _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793B _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793C _H	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX _B
00793D _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
00793E _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
00793F _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
007940 _H	Timer Data 0	TCDT0	R/W	I/O Timer 0	0000000 _B
007941 _H	Timer Data 0	TCDT0	R/W		0000000 _B
007942 _H	Timer Control Status 0	TCCSL0	R/W		0000000 _B
007943 _H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX _B
007944 _H	Timer Data 1	TCDT1	R/W	I/O Timer 1	0000000 _B
007945 _H	Timer Data 1	TCDT1	R/W		0000000 _B
007946 _H	Timer Control Status 1	TCCSL1	R/W		0000000 _B
007947 _H	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXX _B

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value	
007948 _H	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX _B	
007949 _H			R/W		XXXXXXXX _B	
00794A _H	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX _B	
00794B _H			R/W		XXXXXXXX _B	
00794C _H	Timer 2/Reload 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX _B	
00794D _H			R/W		XXXXXXXX _B	
00794E _H	Timer 3/Reload 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX _B	
00794F _H			R/W		XXXXXXXX _B	
007950 _H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000 _B	
007951 _H	Serial Control Register 3	SCR3	W,R/W		00000000 _B	
007952 _H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000 _B	
007953 _H	Serial Status Register 3	SSR3	R,R/W		00001000 _B	
007954 _H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX _B	
007955 _H	Extended Status Control Register	ESCR3	R/W		00000100 _B	
007956 _H	Baud Rate Generator Register 30	BGR30	R/W		00000000 _B	
007957 _H	Baud Rate Generator Register 31	BGR31	R/W		00000000 _B	
007958 _H	Serial Mode Register 4	SMR4	W,R/W		UART4	00000000 _B
007959 _H	Serial Control Register 4	SCR4	W,R/W			00000000 _B
00795A _H	Reception/Transmission Data Register 4	RDR4/TDR4	R/W	00000000 _B		
00795B _H	Serial Status Register 4	SSR4	R,R/W	00001000 _B		
00795C _H	Extended Communication Control Register 4	ECCR4	R,W, R/W	000000XX _B		
00795D _H	Extended Status Control Register	ESCR4	R/W	00000100 _B		
00795E _H	Baud Rate Generator Register 40	BGR40	R/W	00000000 _B		
00795F _H	Baud Rate Generator Register 41	BGR41	R/W	00000000 _B		
007960 _H to 00796B _H	Reserved					
00796C _H	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000 _B	
00796D _H	Reserved					
00796E _H	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	XXXXXXXX0 _B	
00796F _H	CAN Switch Register	CANSWR	R/W	CAN 0/1	XXXXXXXX0 _B	

(Continued)

MB90340E Series

Address	Register	Abbreviation	Access	Resource name	Initial value
007970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
007971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H		ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
007975 _H		ITMKH0	R/W		00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C Data Register 0	IDAR0	R/W		00000000 _B
007979 _H , 00797A _H	Reserved				
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 00797F _H	Reserved				
007980 _H	I ² C Bus Status Register 1	IBSR1	R	I ² C Interface 1	00000000 _B
007981 _H	I ² C Bus Control Register 1	IBCR1	W,R/W		00000000 _B
007982 _H	I ² C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000 _B
007983 _H		ITBAH1	R/W		00000000 _B
007984 _H	I ² C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111 _B
007985 _H		ITMKH1	R/W		00111111 _B
007986 _H	I ² C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 _B
007987 _H	I ² C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 _B
007988 _H	I ² C Data Register 1	IDAR1	R/W		00000000 _B
007989 _H , 00798A _H	Reserved				
00798B _H	I ² C Clock Control Register 1	ICCR1	R/W	I ² C Interface 1	00011111 _B
00798C _H to 0079C1 _H	Reserved				
0079C2 _H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B
0079C3 _H to 0079DF _H	Reserved				

(Continued)

MB90340E Series

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0079E0 _H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX _B
0079E1 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E2 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E3 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E4 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E5 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E6 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E7 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E8 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E9 _H to 0079EF _H	Reserved				
0079F0 _H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX _B
0079F1 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F2 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F3 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F4 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F5 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F6 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F7 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F8 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F9 _H to 0079FF _H	Reserved				
007A00 _H to 007AFF _H	Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
007B00 _H to 007BFF _H	Reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS”				
007C00 _H to 007CFF _H	Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
007D00 _H to 007DFF _H	Reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS”				
007E00 _H to 007FFF _H	Reserved				

Notes : • Initial value of “X” represents unknown value.

- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

■ CAN CONTROLLERS

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 _H	000080 _H	Message Buffer Valid Register	BVALR	R/W	00000000 _B 00000000 _B
000071 _H	000081 _H				
000072 _H	000082 _H	Transmit Request Register	TREQR	R/W	00000000 _B 00000000 _B
000073 _H	000083 _H				
000074 _H	000084 _H	Transmit Cancel Register	TCANR	W	00000000 _B 00000000 _B
000075 _H	000085 _H				
000076 _H	000086 _H	Transmission Complete Register	TCR	R/W	00000000 _B 00000000 _B
000077 _H	000087 _H				
000078 _H	000088 _H	Receive Complete Register	RCR	R/W	00000000 _B 00000000 _B
000079 _H	000089 _H				
00007A _H	00008A _H	Remote Request Receiving Register	RRTRR	R/W	00000000 _B 00000000 _B
00007B _H	00008B _H				
00007C _H	00008C _H	Receive Overrun Register	ROVRR	R/W	00000000 _B 00000000 _B
00007D _H	00008D _H				
00007E _H	00008E _H	Reception Interrupt Enable Register	RIER	R/W	00000000 _B 00000000 _B
00007F _H	00008F _H				

MB90340E Series

List of Control Registers (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007B00 _H	007D00 _H	Control Status Register	CSR	R/W, W R/W, R	0XXXX0X1 _B 00XXX000 _B
007B01 _H	007D01 _H				
007B02 _H	007D02 _H	Last Event Indicator Register	LEIR	R/W	000X0000 _B XXXXXXXX _B
007B03 _H	007D03 _H				
007B04 _H	007D04 _H	Receive And Transmit Error Counter	RTEC	R	00000000 _B 00000000 _B
007B05 _H	007D05 _H				
007B06 _H	007D06 _H	Bit Timing Register	BTR	R/W	11111111 _B X1111111 _B
007B07 _H	007D07 _H				
007B08 _H	007D08 _H	IDE Register	IDER	R/W	XXXXXXXX _B XXXXXXXX _B
007B09 _H	007D09 _H				
007B0A _H	007D0A _H	Transmit RTR Register	TRTRR	R/W	00000000 _B 00000000 _B
007B0B _H	007D0B _H				
007B0C _H	007D0C _H	Remote Frame Receive Waiting Register	RFWTR	R/W	XXXXXXXX _B XXXXXXXX _B
007B0D _H	007D0D _H				
007B0E _H	007D0E _H	Transmit Interrupt Enable Register	TIER	R/W	00000000 _B 00000000 _B
007B0F _H	007D0F _H				
007B10 _H	007D10 _H	Acceptance Mask Select Register	AMSR	R/W	XXXXXXXX _B XXXXXXXX _B
007B11 _H	007D11 _H				
007B12 _H	007D12 _H				XXXXXXXX _B XXXXXXXX _B
007B13 _H	007D13 _H				
007B14 _H	007D14 _H	Acceptance Mask Register 0	AMR0	R/W	XXXXXXXX _B XXXXXXXX _B
007B15 _H	007D15 _H				
007B16 _H	007D16 _H				XXXXXXXX _B XXXXXXXX _B
007B17 _H	007D17 _H				
007B18 _H	007D18 _H	Acceptance Mask Register 1	AMR1	R/W	XXXXXXXX _B XXXXXXXX _B
007B19 _H	007D19 _H				
007B1A _H	007D1A _H				XXXXXXXX _B XXXXXXXX _B
007B1B _H	007D1B _H				

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A00 _H to 007A1F _H	007C00 _H to 007C1F _H	General- Purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
007A20 _H	007C20 _H	ID Register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
007A21 _H	007C21 _H				XXXXXXXX _B XXXXXXXX _B
007A22 _H	007C22 _H				XXXXXXXX _B XXXXXXXX _B
007A23 _H	007C23 _H	ID Register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
007A24 _H	007C24 _H				XXXXXXXX _B XXXXXXXX _B
007A25 _H	007C25 _H				XXXXXXXX _B XXXXXXXX _B
007A26 _H	007C26 _H				XXXXXXXX _B XXXXXXXX _B
007A27 _H	007C27 _H	ID Register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
007A28 _H	007C28 _H				XXXXXXXX _B XXXXXXXX _B
007A29 _H	007C29 _H				XXXXXXXX _B XXXXXXXX _B
007A2A _H	007C2A _H				XXXXXXXX _B XXXXXXXX _B
007A2B _H	007C2B _H	ID Register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
007A2C _H	007C2C _H				XXXXXXXX _B XXXXXXXX _B
007A2D _H	007C2D _H				XXXXXXXX _B XXXXXXXX _B
007A2E _H	007C2E _H				XXXXXXXX _B XXXXXXXX _B
007A2F _H	007C2F _H	ID Register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
007A30 _H	007C30 _H				XXXXXXXX _B XXXXXXXX _B
007A31 _H	007C31 _H				XXXXXXXX _B XXXXXXXX _B
007A32 _H	007C32 _H				XXXXXXXX _B XXXXXXXX _B
007A33 _H	007C33 _H	ID Register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
007A34 _H	007C34 _H				XXXXXXXX _B XXXXXXXX _B
007A35 _H	007C35 _H				XXXXXXXX _B XXXXXXXX _B
007A36 _H	007C36 _H				XXXXXXXX _B XXXXXXXX _B
007A37 _H	007C37 _H	ID Register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
007A38 _H	007C38 _H				XXXXXXXX _B XXXXXXXX _B
007A39 _H	007C39 _H				XXXXXXXX _B XXXXXXXX _B
007A3A _H	007C3A _H				XXXXXXXX _B XXXXXXXX _B
007A3B _H	007C3B _H	ID Register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
007A3C _H	007C3C _H				XXXXXXXX _B XXXXXXXX _B
007A3D _H	007C3D _H				XXXXXXXX _B XXXXXXXX _B
007A3E _H	007C3E _H				XXXXXXXX _B XXXXXXXX _B
007A3F _H	007C3F _H				XXXXXXXX _B XXXXXXXX _B

MB90340E Series

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A40H	007C40H	ID Register 8	IDR8	R/W	XXXXXXXXXB
007A41H	007C41H				XXXXXXXXXB
007A42H	007C42H				XXXXXXXXXB
007A43H	007C43H				XXXXXXXXXB
007A44H	007C44H	ID Register 9	IDR9	R/W	XXXXXXXXXB
007A45H	007C45H				XXXXXXXXXB
007A46H	007C46H				XXXXXXXXXB
007A47H	007C47H				XXXXXXXXXB
007A48H	007C48H	ID Register 10	IDR10	R/W	XXXXXXXXXB
007A49H	007C49H				XXXXXXXXXB
007A4AH	007C4AH				XXXXXXXXXB
007A4BH	007C4BH				XXXXXXXXXB
007A4CH	007C4CH	ID Register 11	IDR11	R/W	XXXXXXXXXB
007A4DH	007C4DH				XXXXXXXXXB
007A4EH	007C4EH				XXXXXXXXXB
007A4FH	007C4FH				XXXXXXXXXB
007A50H	007C50H	ID Register 12	IDR12	R/W	XXXXXXXXXB
007A51H	007C51H				XXXXXXXXXB
007A52H	007C52H				XXXXXXXXXB
007A53H	007C53H				XXXXXXXXXB
007A54H	007C54H	ID Register 13	IDR13	R/W	XXXXXXXXXB
007A55H	007C55H				XXXXXXXXXB
007A56H	007C56H				XXXXXXXXXB
007A57H	007C57H				XXXXXXXXXB
007A58H	007C58H	ID Register 14	IDR14	R/W	XXXXXXXXXB
007A59H	007C59H				XXXXXXXXXB
007A5AH	007C5AH				XXXXXXXXXB
007A5BH	007C5BH				XXXXXXXXXB
007A5CH	007C5CH	ID Register 15	IDR15	R/W	XXXXXXXXXB
007A5DH	007C5DH				XXXXXXXXXB
007A5EH	007C5EH				XXXXXXXXXB
007A5FH	007C5FH				XXXXXXXXXB

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A60H	007C60H	DLC Register 0	DLCR0	R/W	XXXXXXXXXB
007A61H	007C61H				
007A62H	007C62H	DLC Register 1	DLCR1	R/W	XXXXXXXXXB
007A63H	007C63H				
007A64H	007C64H	DLC Register 2	DLCR2	R/W	XXXXXXXXXB
007A65H	007C65H				
007A66H	007C66H	DLC Register 3	DLCR3	R/W	XXXXXXXXXB
007A67H	007C67H				
007A68H	007C68H	DLC Register 4	DLCR4	R/W	XXXXXXXXXB
007A69H	007C69H				
007A6AH	007C6AH	DLC Register 5	DLCR5	R/W	XXXXXXXXXB
007A6BH	007C6BH				
007A6CH	007C6CH	DLC Register 6	DLCR6	R/W	XXXXXXXXXB
007A6DH	007C6DH				
007A6EH	007C6EH	DLC Register 7	DLCR7	R/W	XXXXXXXXXB
007A6FH	007C6FH				
007A70H	007C70H	DLC Register 8	DLCR8	R/W	XXXXXXXXXB
007A71H	007C71H				
007A72H	007C72H	DLC Register 9	DLCR9	R/W	XXXXXXXXXB
007A73H	007C73H				
007A74H	007C74H	DLC Register 10	DLCR10	R/W	XXXXXXXXXB
007A75H	007C75H				
007A76H	007C76H	DLC Register 11	DLCR11	R/W	XXXXXXXXXB
007A77H	007C77H				
007A78H	007C78H	DLC Register 12	DLCR12	R/W	XXXXXXXXXB
007A79H	007C79H				
007A7AH	007C7AH	DLC Register 13	DLCR13	R/W	XXXXXXXXXB
007A7BH	007C7BH				
007A7CH	007C7CH	DLC Register 14	DLCR14	R/W	XXXXXXXXXB
007A7DH	007C7DH				
007A7EH	007C7EH	DLC Register 15	DLCR15	R/W	XXXXXXXXXB
007A7FH	007C7FH				

MB90340E Series

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A80H to 007A87H	007C80H to 007C87H	Data Register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
007A88H to 007A8FH	007C88H to 007C8FH	Data Register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007A90H to 007A97H	007C90H to 007C97H	Data Register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007A98H to 007A9FH	007C98H to 007C9FH	Data Register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA0H to 007AA7H	007CA0H to 007CA7H	Data Register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA8H to 007AAFH	007CA8H to 007CAFH	Data Register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB0H to 007AB7H	007CB0H to 007CB7H	Data Register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB8H to 007ABFH	007CB8H to 007CBFH	Data Register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC0H to 007AC7H	007CC0H to 007CC7H	Data Register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC8H to 007ACFH	007CC8H to 007CCFH	Data Register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD0H to 007AD7H	007CD0H to 007CD7H	Data Register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD8H to 007ADFH	007CD8H to 007CDFH	Data Register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE0H to 007AE7H	007CE0H to 007CE7H	Data Register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE8H to 007AEFH	007CE8H to 007CEFH	Data Register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

MB90340E Series

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007AF0 _H to 007AF7 _H	007CF0 _H to 007CF7 _H	Data Register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
007AF8 _H to 007AFF _H	007CF8 _H to 007CFF _H	Data Register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

MB90340E Series

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
CAN 0 RX	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N	—	#12	FFFFCC _H		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 _H		
CAN 2 RX / I ² C0	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
CAN 2 TX/NS	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 0/1/4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 2/3/6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Time Base Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C _H		
A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
I/O Timer 0 / I/O Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5 / I ² C1	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0 to 3	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 _H		
UART 0 RX	Y2	10	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 TX	Y1	11	#36	FFFF6C _H		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 _H		

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Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	FFFF60H	ICR14	0000BEH
UART 2 TX / UART 4 TX	Y1	15	#40	FFFF5CH		
Flash Memory	N	—	#41	FFFF58H	ICR15	0000BFH
Delayed Interrupt	N	—	#42	FFFF54H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

- Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
 - When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
 - When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

MB90340E Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH, AV_{CC} \geq AVRL, AVRH \geq AVRL$
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma I_{CLAMP} $	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	-15	mA	*4
“H” level average output current	I_{OHAV}	—	-4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	-100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	-50	mA	*4
Power consumption	P_D	—	340	mW	MB90F347E
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

*5: • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

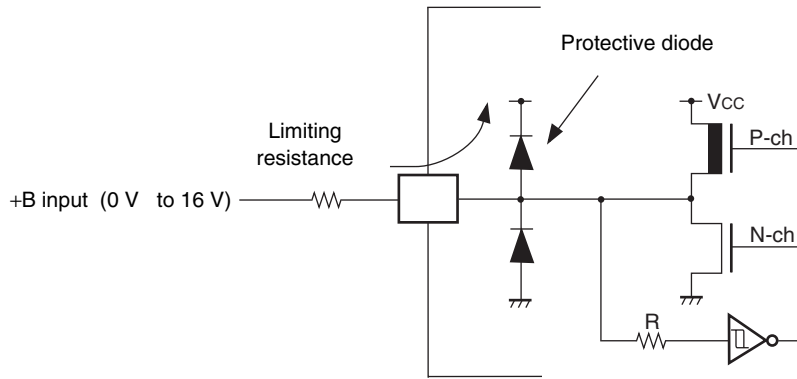
- Use within recommended operating conditions.
- Use with DC voltage (current)
- The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

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- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

- Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

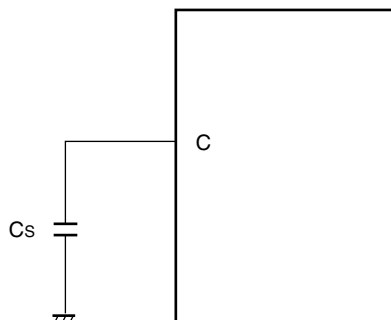
MB90340E Series

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	μF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	-40	—	+105	$^{\circ}\text{C}$	

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB90340E Series

3. DC Characteristics

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P83)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	\overline{RST} input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P83)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	\overline{RST} input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	V_{OHI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	V_{OLI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

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MB90340E Series

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($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-1	—	+1	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At writing Flash memory.	—	70	85	mA	Flash memory devices
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At erasing Flash memory.	—	75	90	mA	Flash memory devices
	I_{CCS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In Sleep mode.	—	25	35	mA	
	I_{CTS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 2 MHz, In Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub operation $T_A = +25\text{ }^\circ\text{C}$	—	70	140	μA	
	I_{CCLS}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub sleep $T_A = +25\text{ }^\circ\text{C}$	—	20	50	μA	
	I_{CCT}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In watch mode $T_A = +25\text{ }^\circ\text{C}$	—	10	35	μA	
	I_{CCH}		$V_{CC} = 5.0\text{ V}$, In Stop mode, $T_A = +25\text{ }^\circ\text{C}$	—	7	25	μA	
Input capacitance	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS}	—	5	15	pF		

* : The power supply current is measured with an external clock.

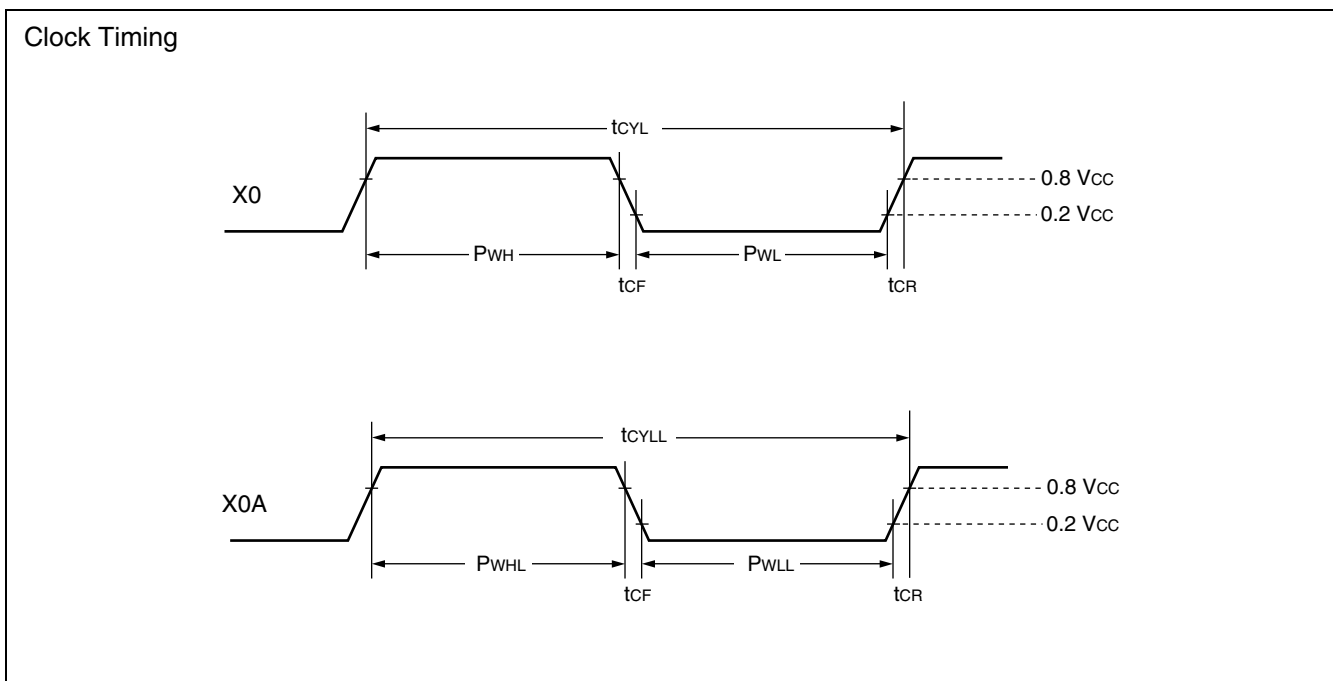
4. AC Characteristics

(1) Clock Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

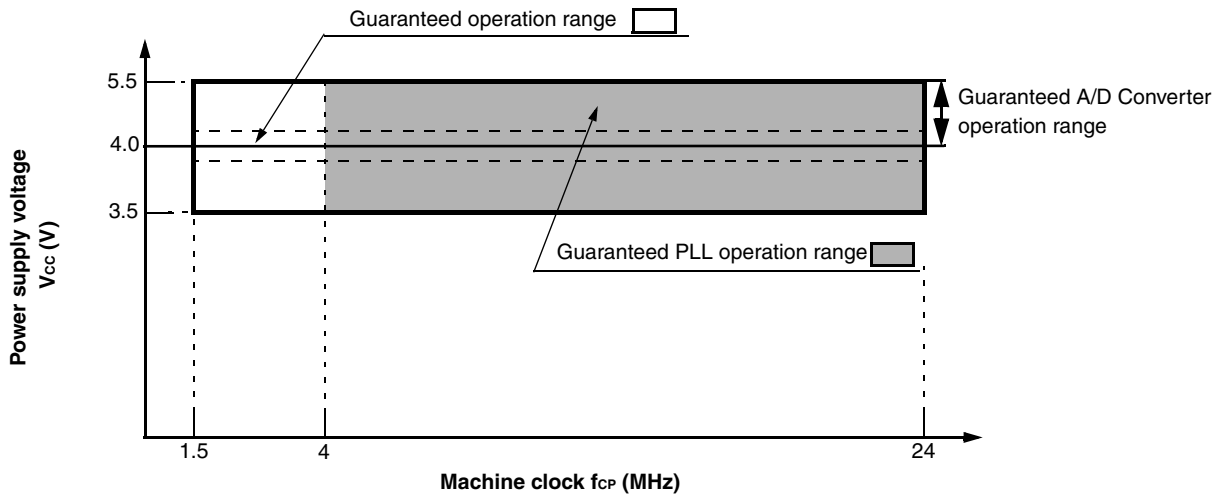
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_c	X0, X1	3	—	16	MHz	When using an oscillation circuit
		X0, X1	3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".

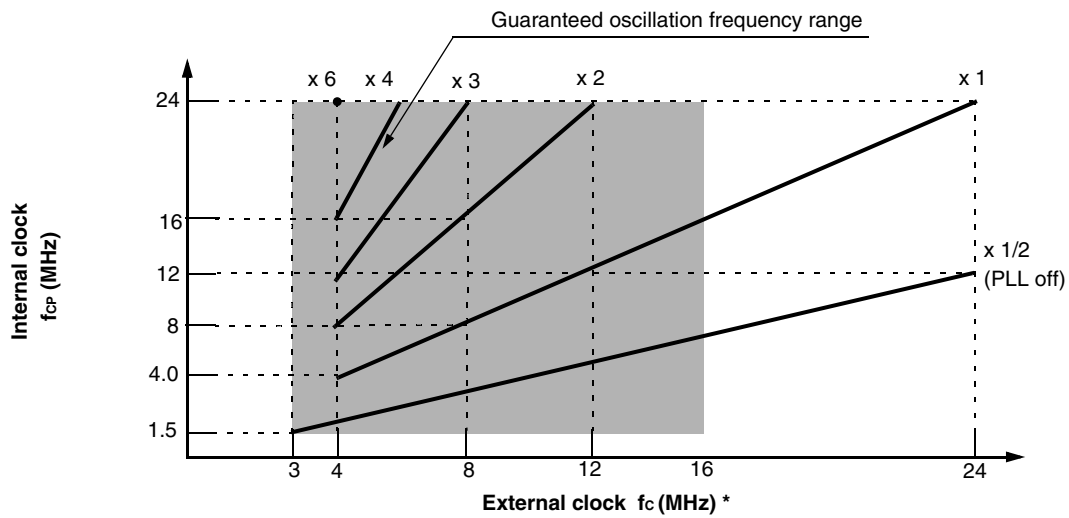


MB90340E Series

Guaranteed PLL operation range



Guaranteed operation range of MB90340E series



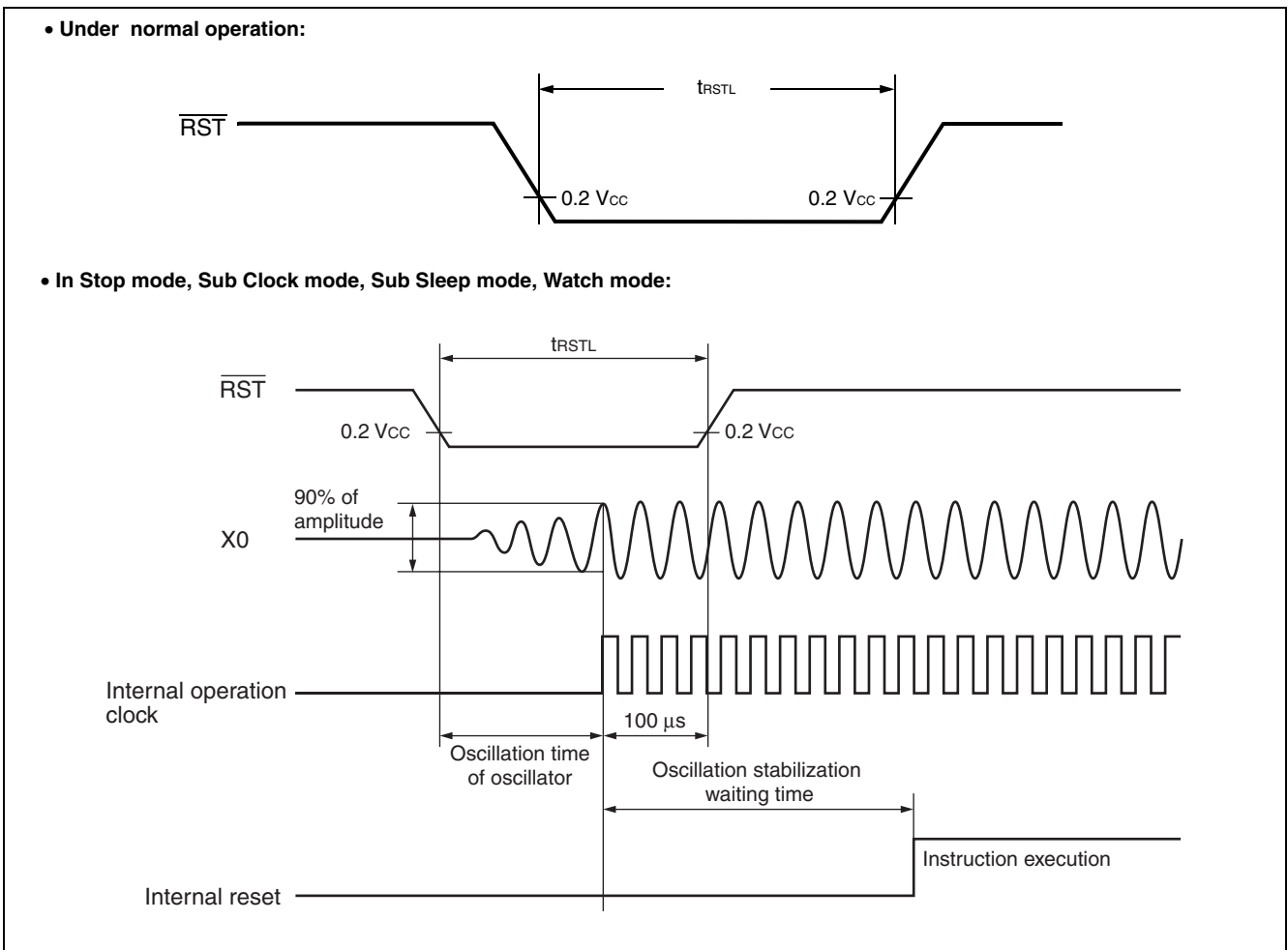
* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

(2) Reset Standby Input

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Value		Unit	Remarks	
			Min	Max			
Reset input time	t_{RSTL}	\overline{RST}	500	—	ns	Under normal operation	
			Oscillation time of oscillator* + 100 μs		—	ns	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	μs	In Time Timer mode	

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred μs and several ms, and for an external clock, the time is 0 ms.

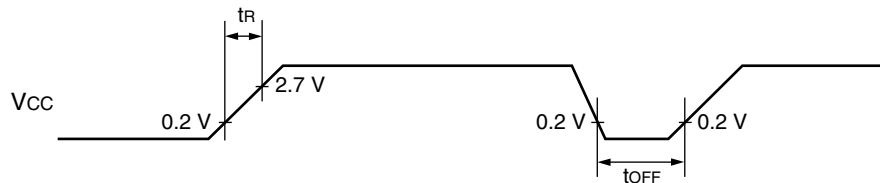


MB90340E Series

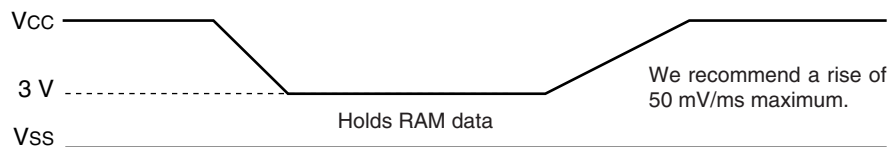
(3) Power On Reset

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}	—	1	—	ms	Due to repetitive operation



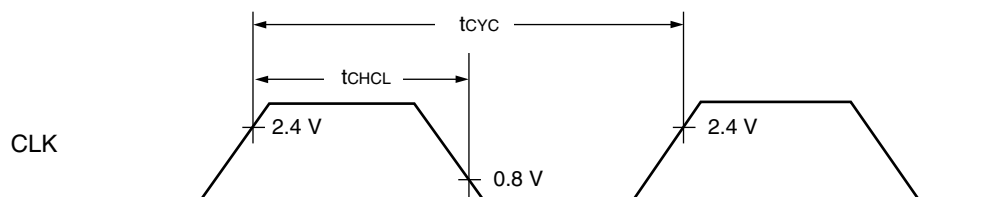
If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



(4) Clock Output Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

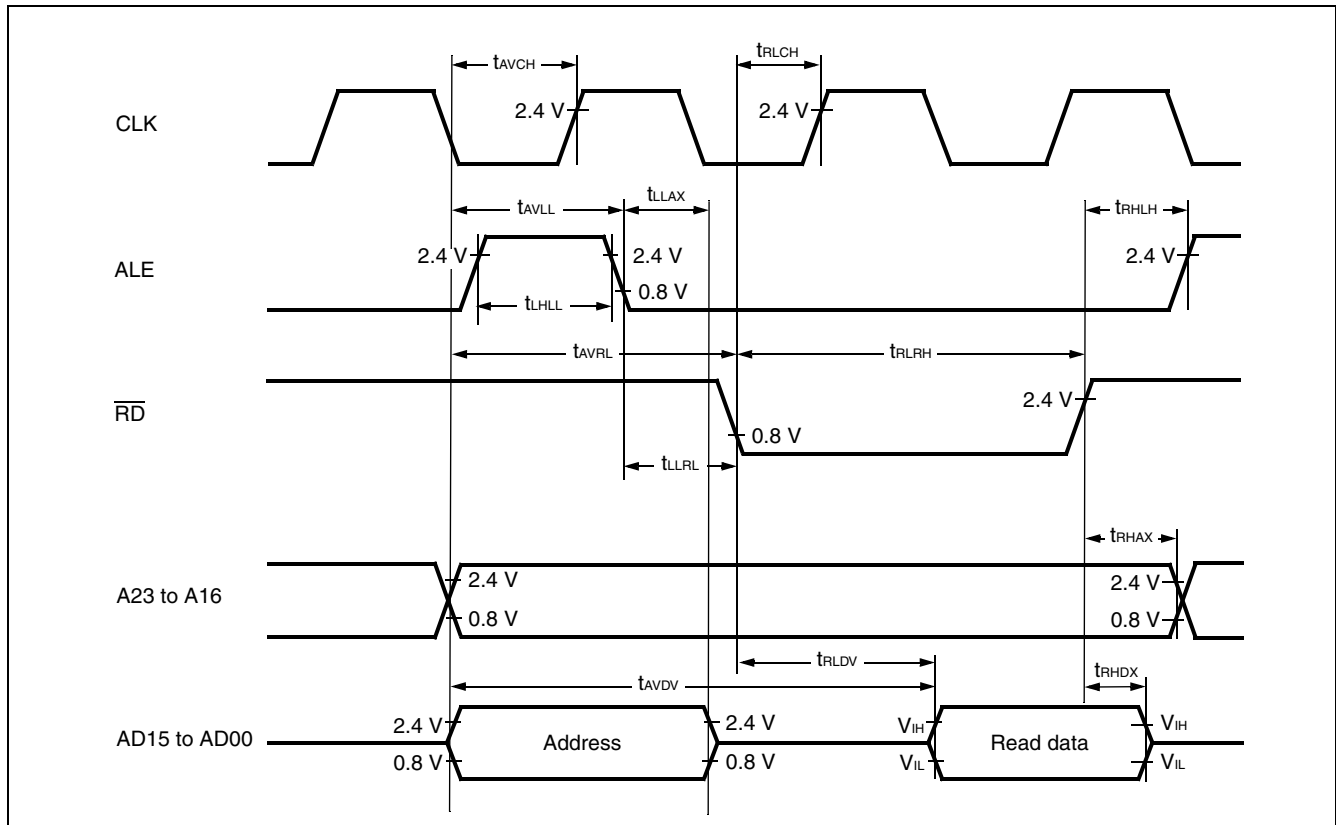
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.76	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK \downarrow	t_{CHCL}	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$



(5) Bus Timing (Read)

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns
Valid address → ALE ↓ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address → \overline{RD} ↓ time	t_{AVRL}	A23 to A16, AD15 to AD00, \overline{RD}		$t_{CP} - 15$	—	ns
Valid address → Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns
\overline{RD} pulse width	t_{RLRH}	\overline{RD}		$3 t_{CP}/2 - 20$	—	ns
\overline{RD} ↓ → Valid data input	t_{RLDV}	\overline{RD} , AD15 to AD00		—	$3 t_{CP}/2 - 50$	ns
\overline{RD} ↑ → Data hold time	t_{RHDX}	\overline{RD} , AD15 to AD00		0	—	ns
\overline{RD} ↓ → ALE ↑ time	t_{RHLH}	\overline{RD} , ALE		$t_{CP}/2 - 15$	—	ns
\overline{RD} ↑ → Address valid time	t_{RHAX}	\overline{RD} , A23 to A16		$t_{CP}/2 - 10$	—	ns
Valid address → CLK ↑ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
\overline{RD} ↓ → CLK ↑ time	t_{RLCH}	\overline{RD} , CLK		$t_{CP}/2 - 15$	—	ns
ALE ↓ → \overline{RD} ↓ time	t_{LLRL}	ALE, \overline{RD}		$t_{CP}/2 - 15$	—	ns

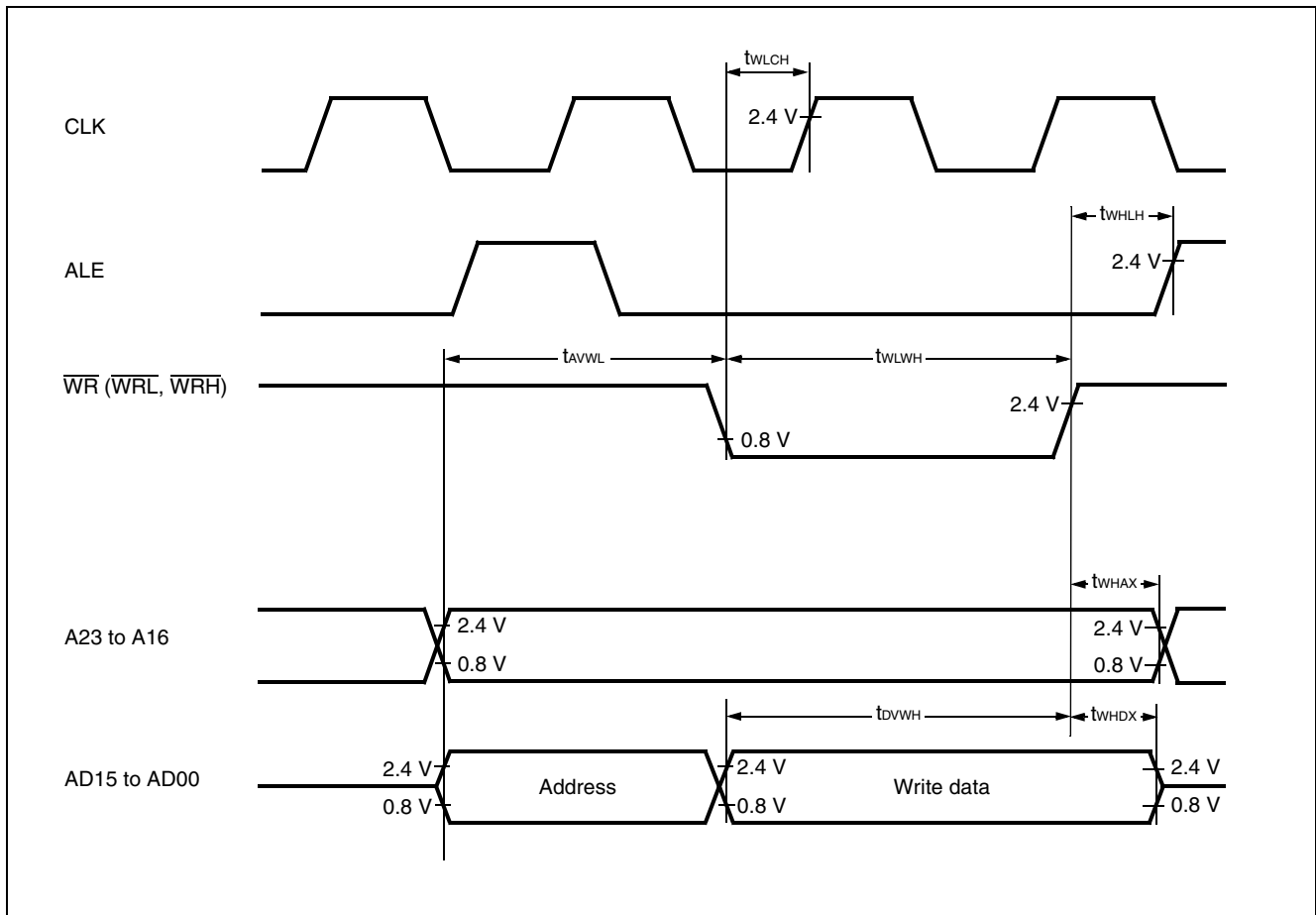


MB90340E Series

(6) Bus Timing (Write)

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\rightarrow \overline{WR} \downarrow$ time	t_{AVWL}	A23 to A16, AD15 to AD00, \overline{WR}	—	$t_{CP} - 15$	—	ns
\overline{WR} pulse width	t_{WLWH}	\overline{WR}		$3 t_{CP} / 2 - 20$	—	ns
Valid data output $\rightarrow \overline{WR} \uparrow$ time	t_{DVWH}	AD15 to AD00, \overline{WR}		$3 t_{CP} / 2 - 20$	—	ns
$\overline{WR} \uparrow \rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, \overline{WR}		15	—	ns
$\overline{WR} \uparrow \rightarrow$ Address valid time	t_{WHAX}	A23 to A16, \overline{WR}		$t_{CP} / 2 - 10$	—	ns
$\overline{WR} \uparrow \rightarrow$ ALE \uparrow time	t_{WHLH}	\overline{WR} , ALE		$t_{CP} / 2 - 15$	—	ns
$\overline{WR} \downarrow \rightarrow$ CLK \uparrow time	t_{WLCH}	\overline{WR} , CLK		$t_{CP} / 2 - 15$	—	ns

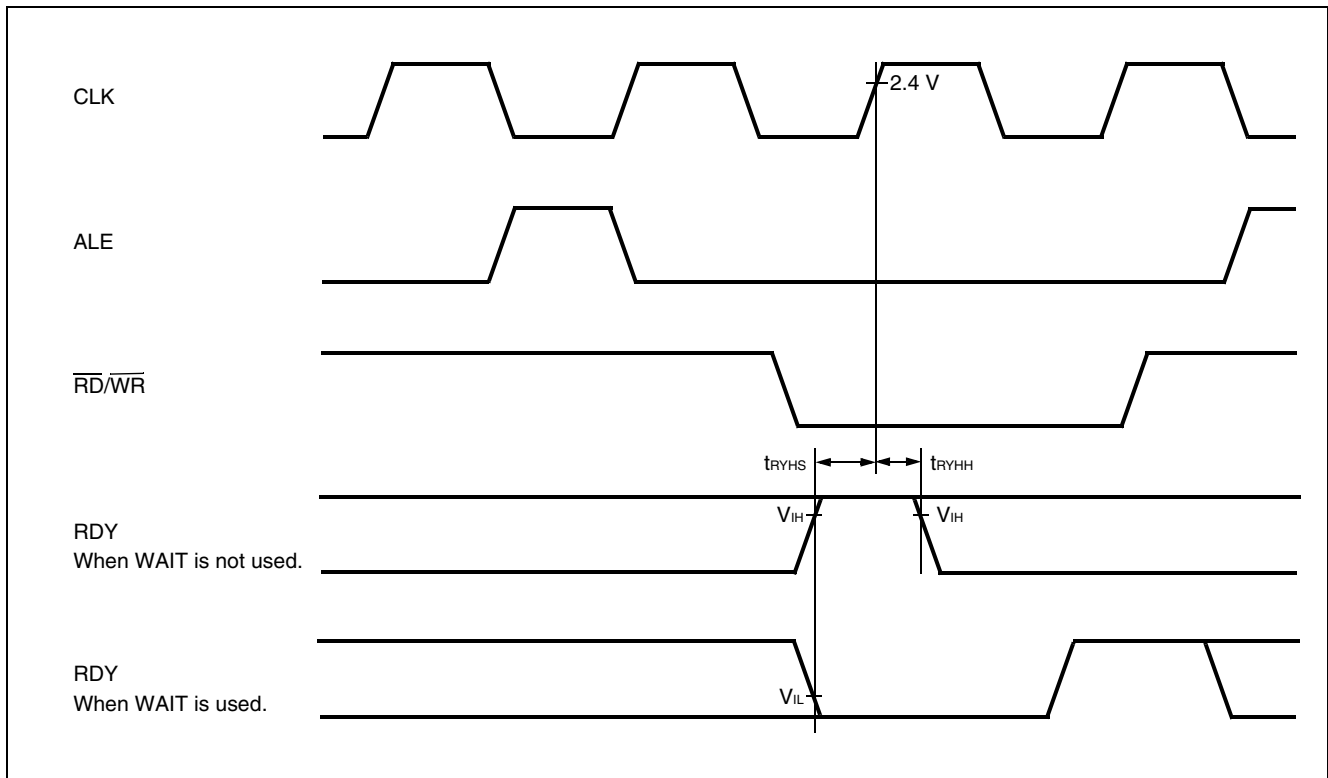


(7) Ready Input Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



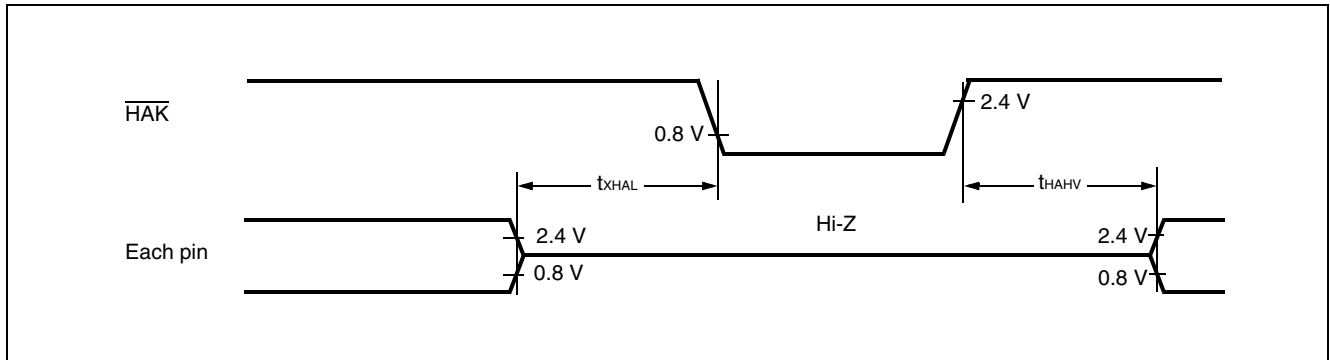
MB90340E Series

(8) Hold Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Pin floating $\rightarrow \overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns
$\overline{\text{HAK}} \uparrow$ time \rightarrow Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$		t_{CP}	$2 t_{CP}$	ns

Note : There is more than 1 cycle from when HRQ reads in until the $\overline{\text{HAK}}$ is changed.

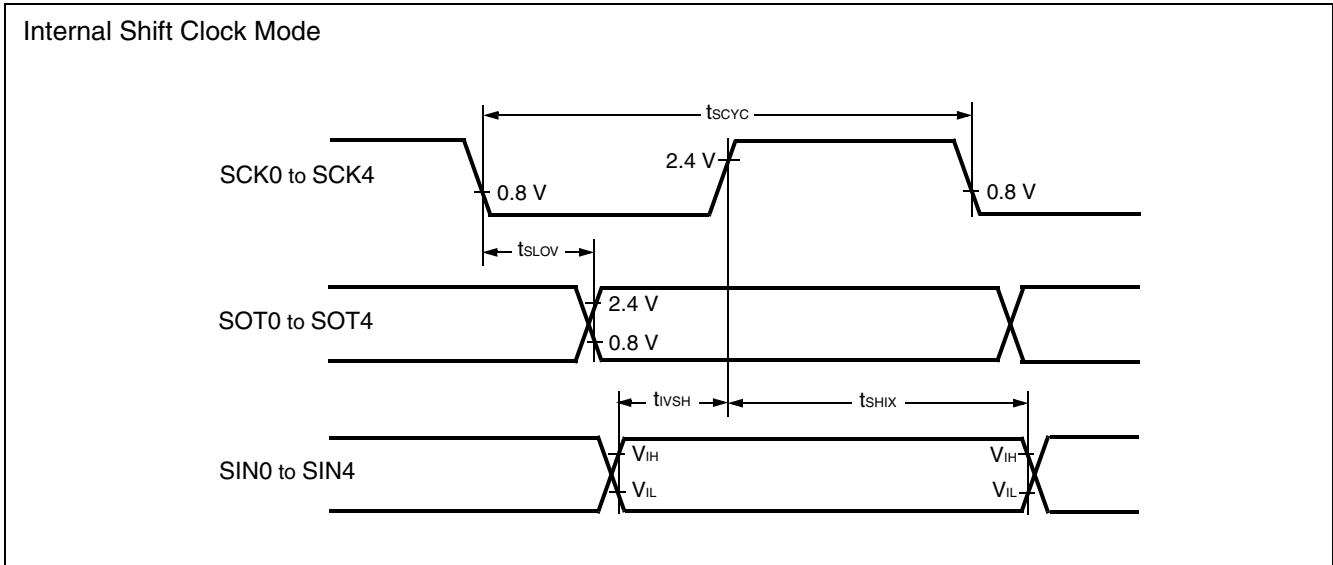


(9) UART0/1/2/3/4

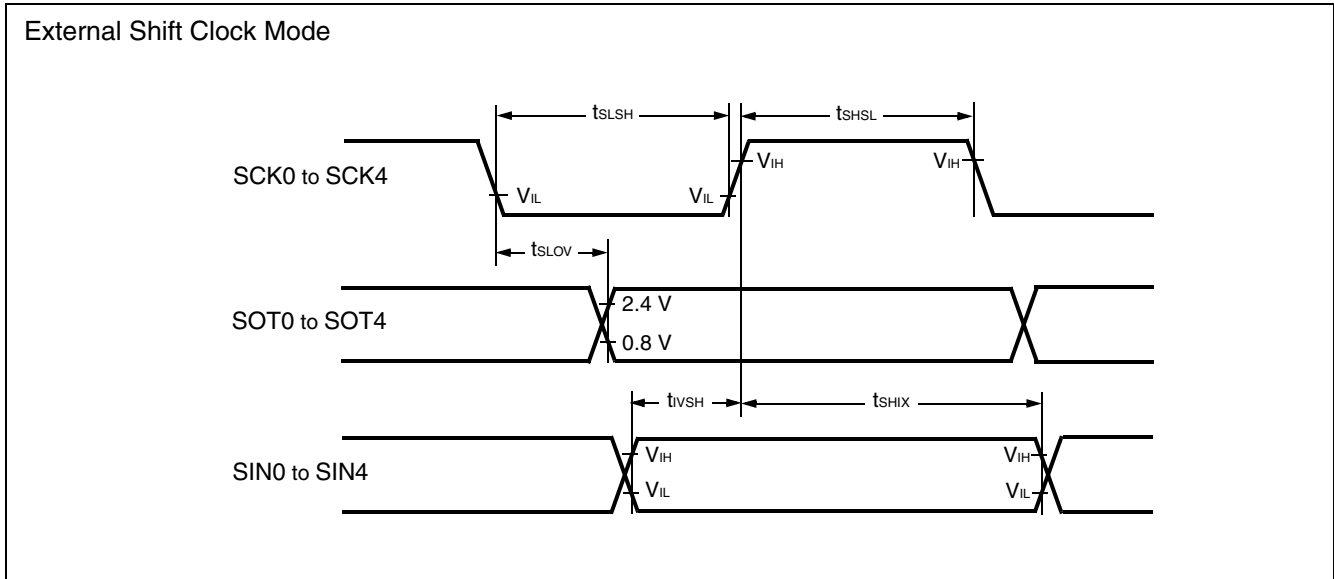
($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$8 t_{CP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		- 80	+ 80	ns
Valid SIN → SCK ↑	t_{VSH}	SCK0 to SCK4, SIN0 to SIN4		100	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$4 t_{CP}$	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4		$4 t_{CP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK4, SOT0 to SOT4		—	150	ns
Valid SIN → SCK ↑	t_{VSH}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK4, SIN0 to SIN4		60	—	ns

- Notes :
- AC characteristic CLK synchronized mode.
 - C_L is the value of the load capacitance applied to the pins during testing.



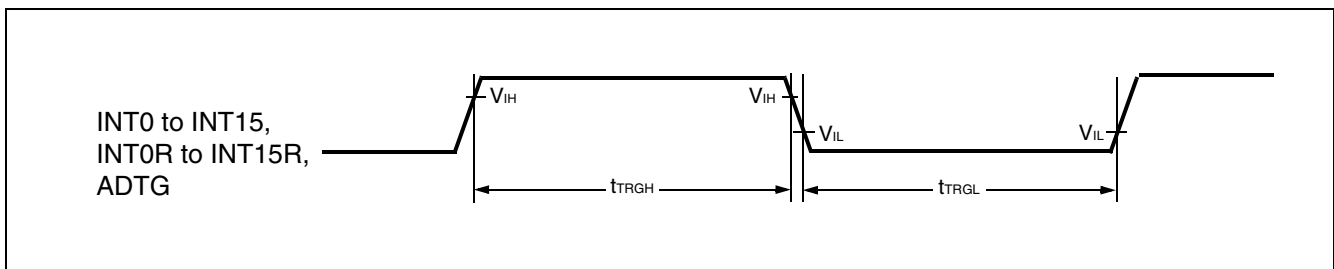
MB90340E Series



(10) Trigger Input Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0.0\text{ V}$)

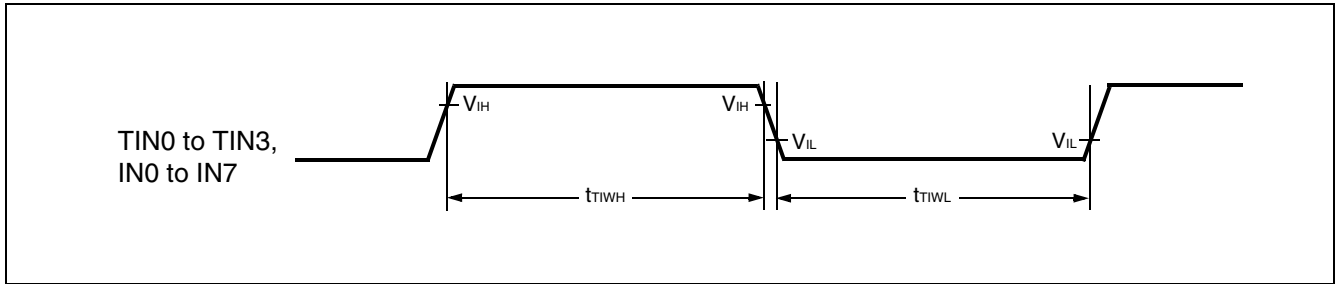
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT0R to INT15R, ADTG	—	$5 t_{CP}$	—	ns



(11) Timer Related Resource Input Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

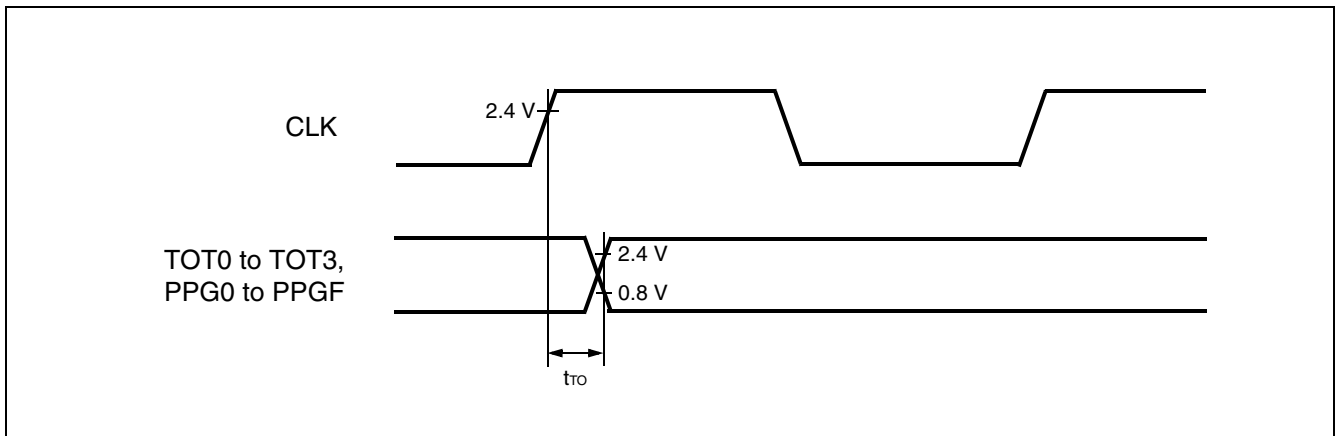
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns
	t_{TIWL}					



(12) Timer Related Resource Output Timing

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK \uparrow \rightarrow T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



MB90340E Series

(13) I²C Timing

(T_A = -40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V)

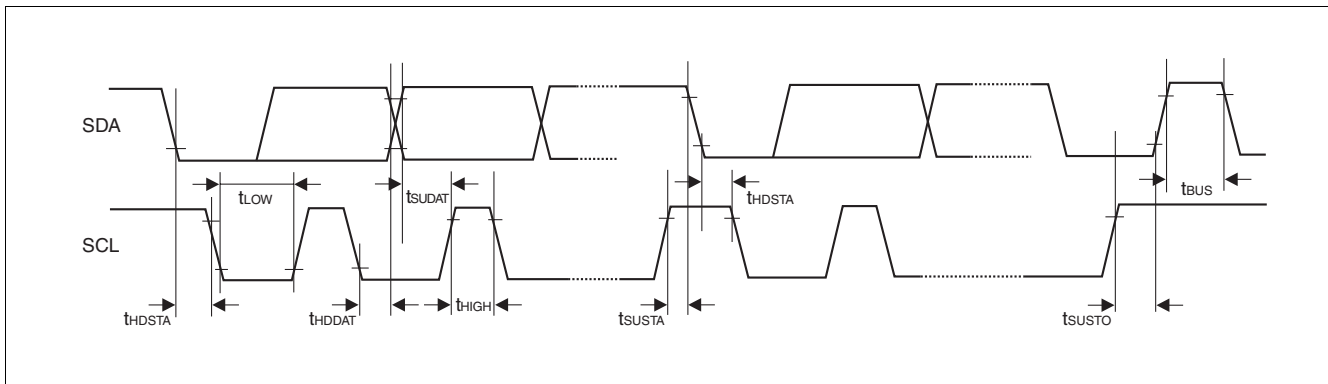
Parameter	Symbol	Condition	Standard-mode		Fast-mode* ¹		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ, C = 50 pF* ²	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs
“L” width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs
“H” width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ³	0	0.9* ⁴	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t _{BUS}	4.7	—	1.3	—	μs	

*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2: R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

*3: The maximum t_{HDDAT} meets the requirement that it does not extend the “L” width (t_{LOW}) of the SCL signal.

*4: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.



5. A/D Converter

($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $3.0\text{ V} \leq AVRH - AVRL$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	$AVRL - 1.5$	$AVRL + 0.5$	$AVRL + 2.5$	LSB	
Full scale reading voltage	V_{FST}	AN0 to AN23	$AVRH - 3.5$	$AVRH - 1.5$	$AVRH + 0.5$	LSB	
Compare time	—	—	1.0	—	16500	μs	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	∞	μs	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN23	-0.3	—	+0.3	μA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$AVRL + 2.7$	—	AV_{CC}	V	
	—	AVRL	0	—	$AVRH - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AVRH	—	600	900	μA	
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

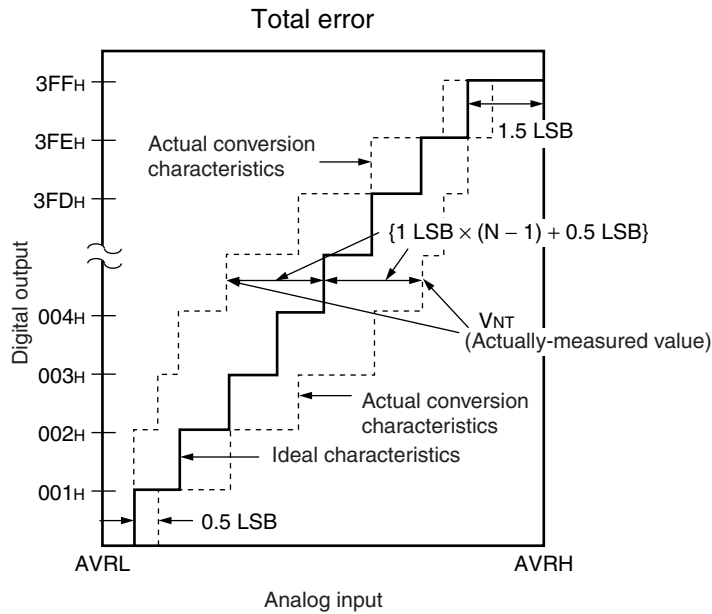
*: If the A/D convertor is not operating, a current when CPU is stopped is applicable ($V_{CC} = AV_{CC} = AVRH = 5.0\text{ V}$).

Note: The accuracy gets worse as $|AVRH - AVRL|$ becomes smaller.

MB90340E Series

6. Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by the A/D converter.
- Non linearity error : The deviation between the actual conversion characteristics and a line that joins the zero-transition line ("00 0000 0000" ← → "00 0000 0001") to the full-scale transition line ("11 1111 1110" ← → "11 1111 1111") .
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

N : Value of the digital output from the A/D converter

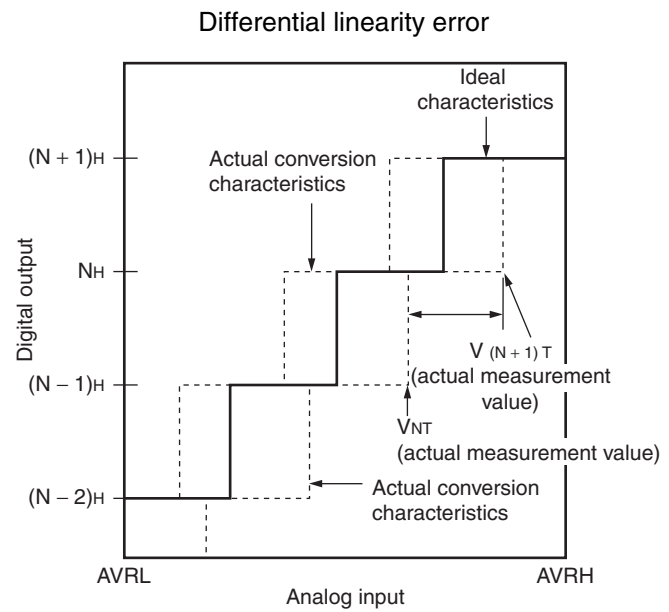
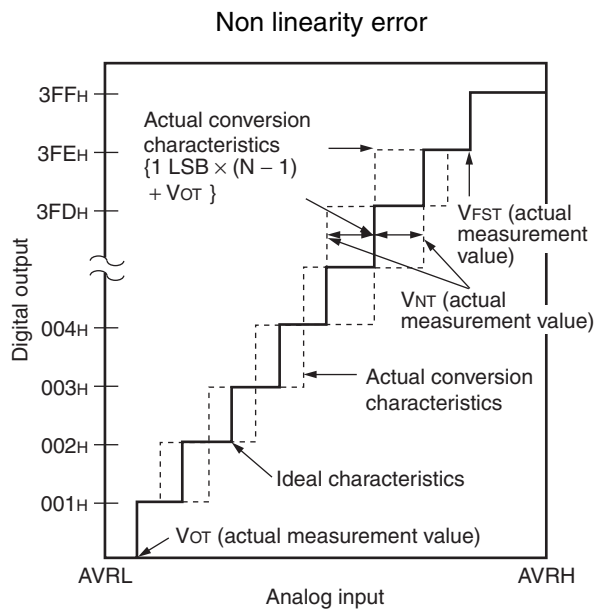
V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH - 1.5 LSB [V]

V_{NT} : A voltage at which the digital output transitions from (N - 1)_H to N_H.

(Continued)

(Continued)



$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : Value of the digital output from the A/D converter

V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”

V_{FST} : Voltage at which digital output transits from “3FE_H” to “3FF_H.”

MB90340E Series

7. Notes on A/D Converter Section

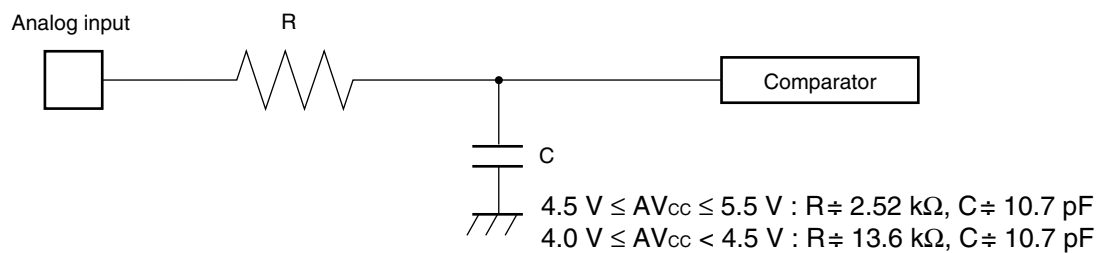
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 k Ω or lower ($4.0\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$,
sampling period = 0.5 μs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

• Analog input circuit model



Note : Use the values in the figure only as a guideline.

8. Flash Memory Program/Erase Characteristics

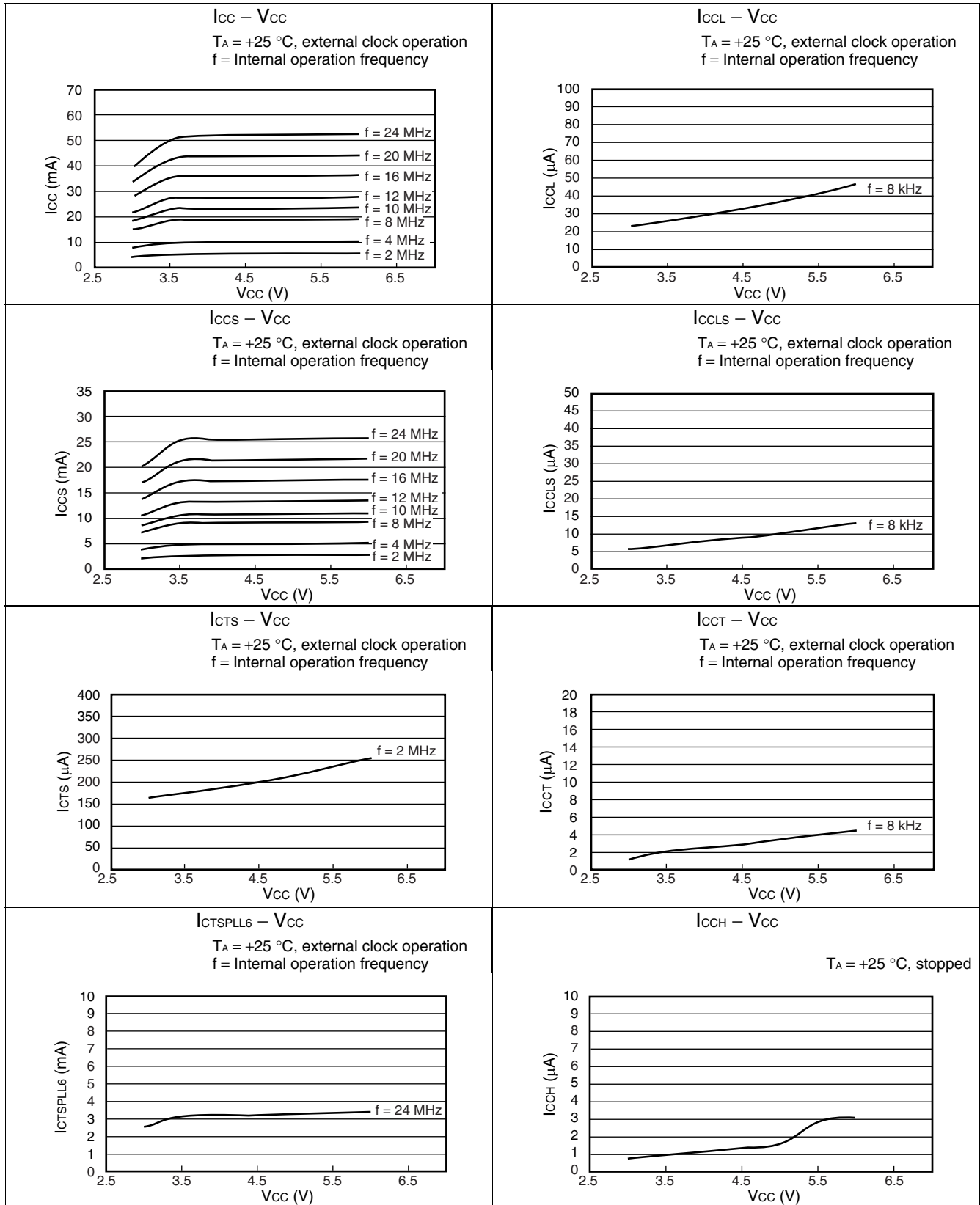
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T _A = +25 °C V _{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	μs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average T _A = +85 °C	20	—	—	year	*

* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

MB90340E Series

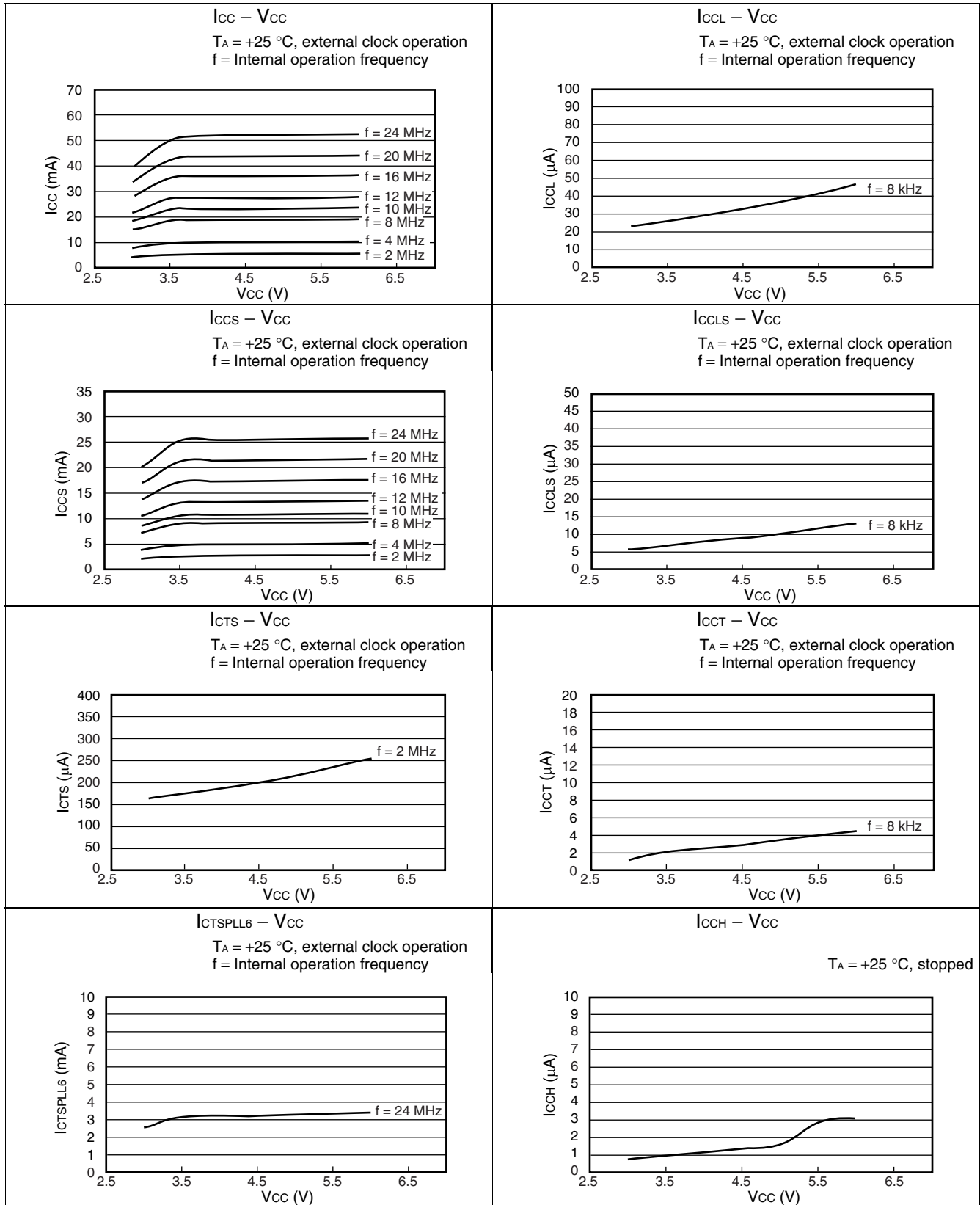
EXAMPLE CHARACTERISTICS

- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES



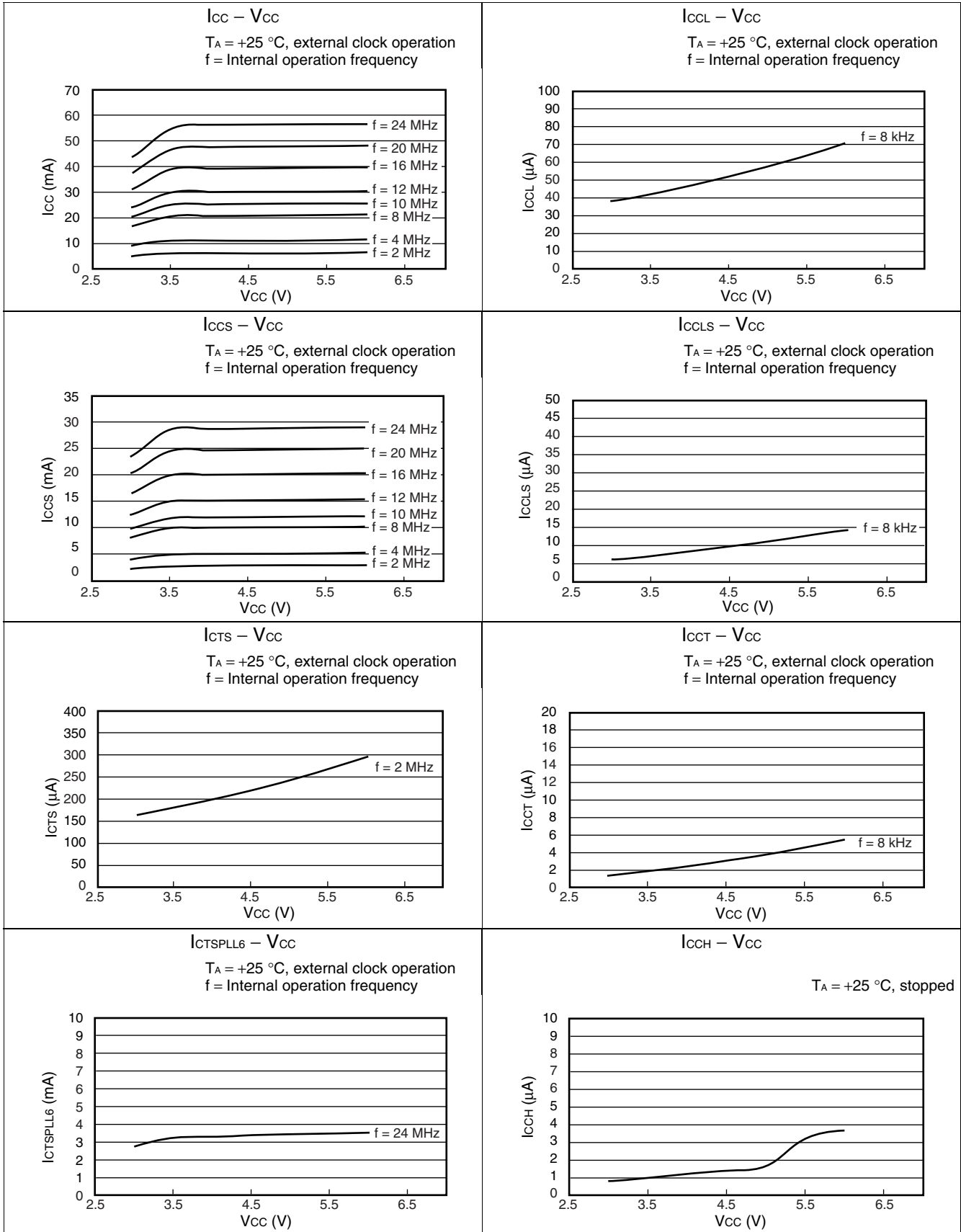
MB90340E Series

- MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES



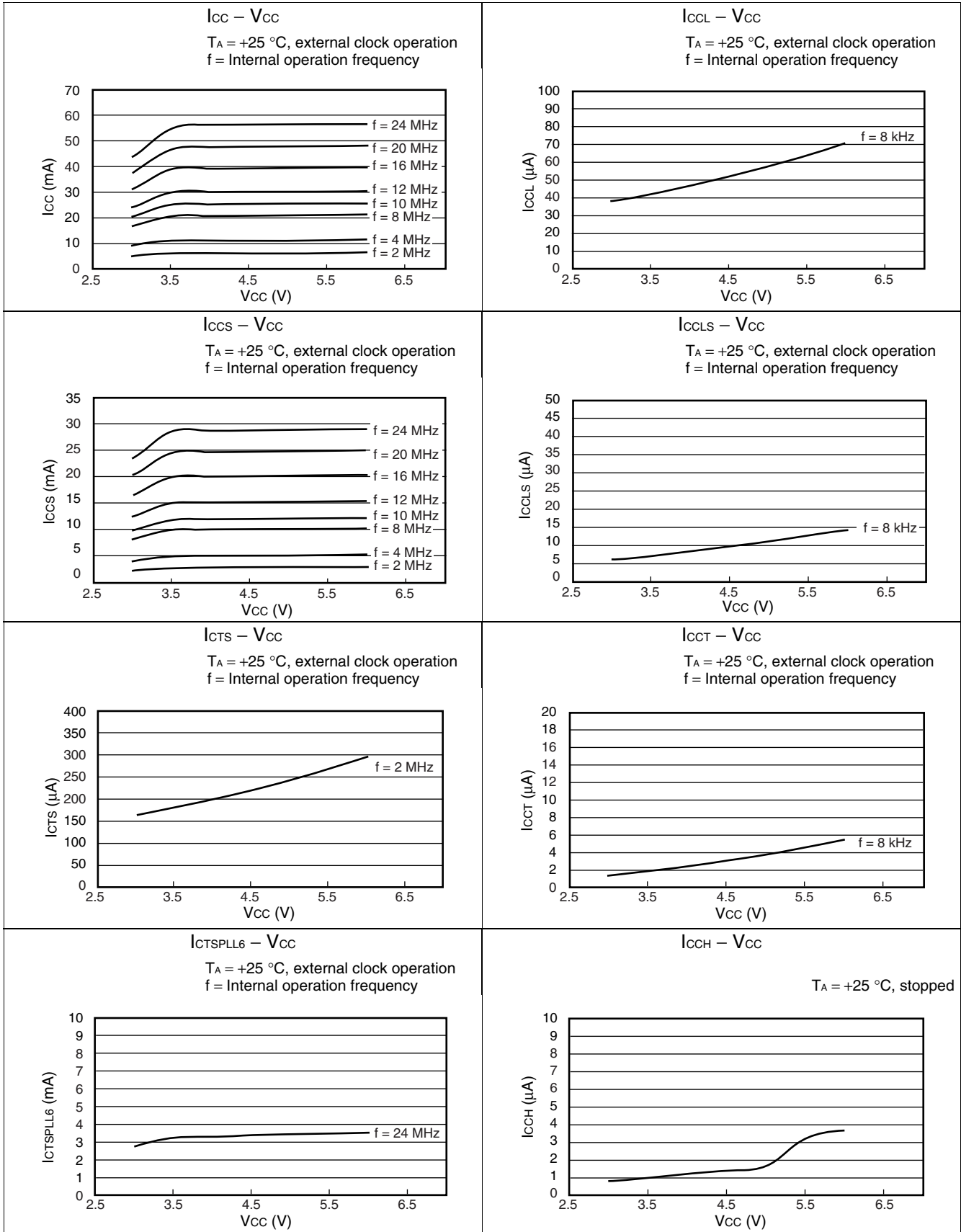
MB90340E Series

- MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES



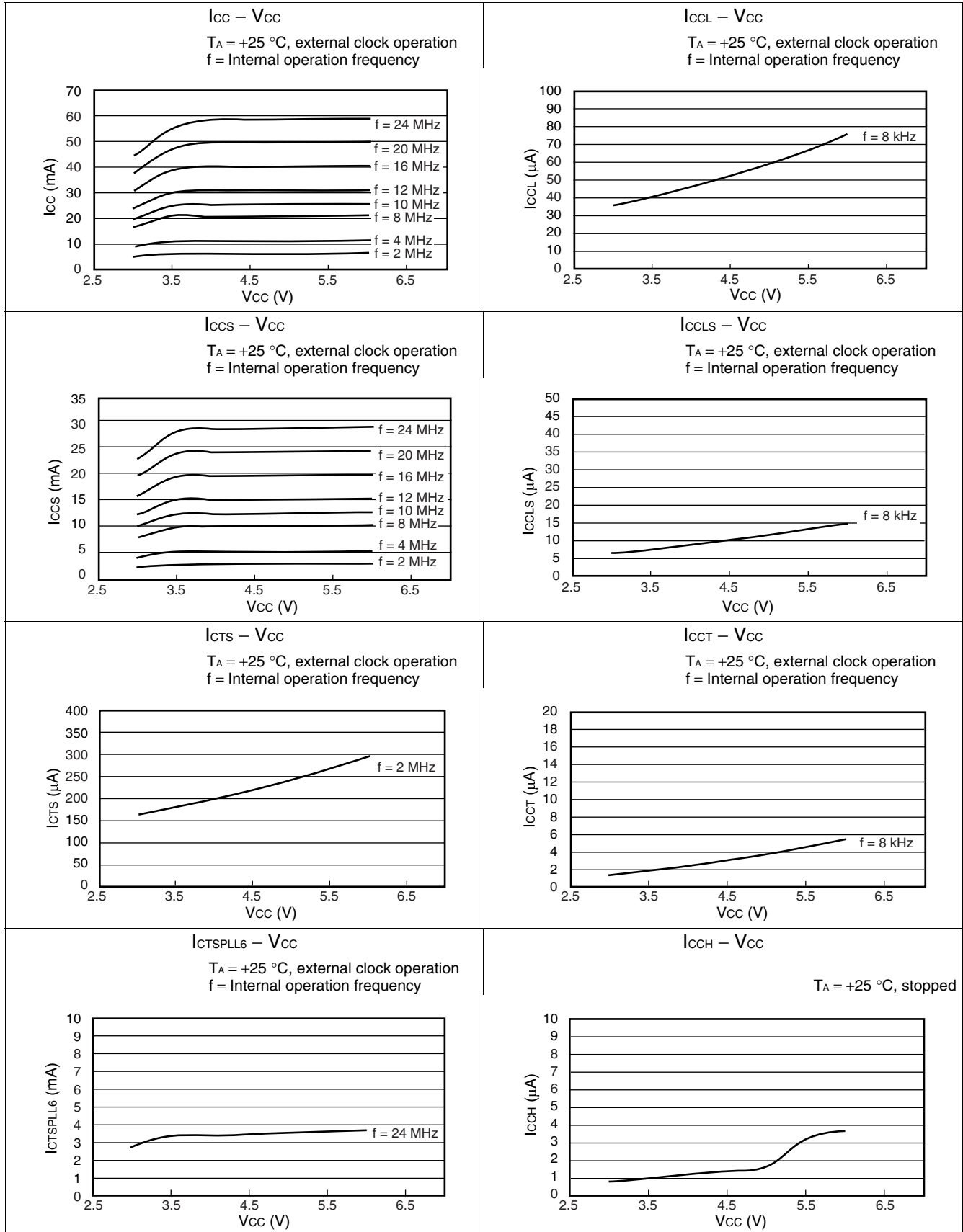
MB90340E Series

- MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES



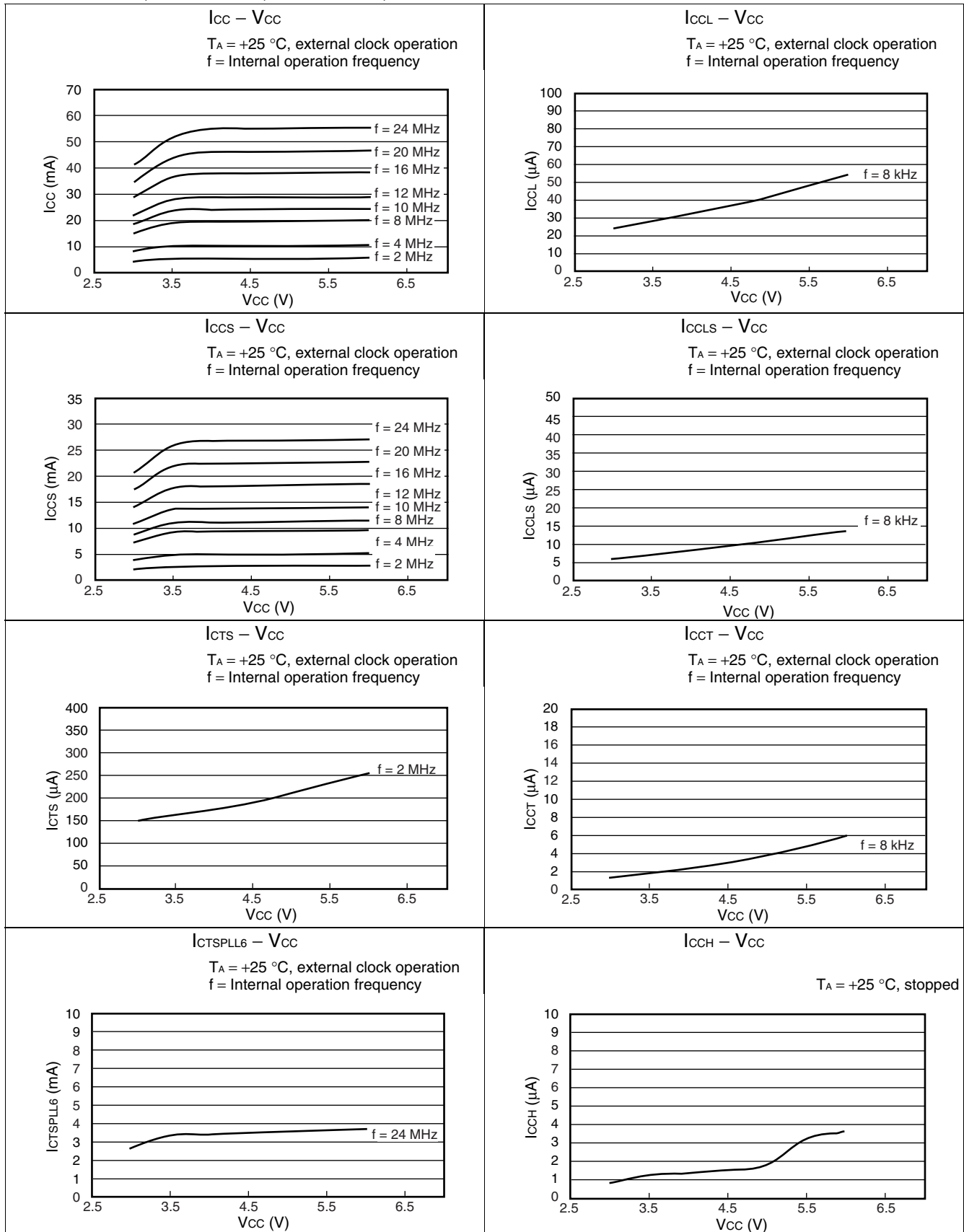
MB90340E Series

- MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES



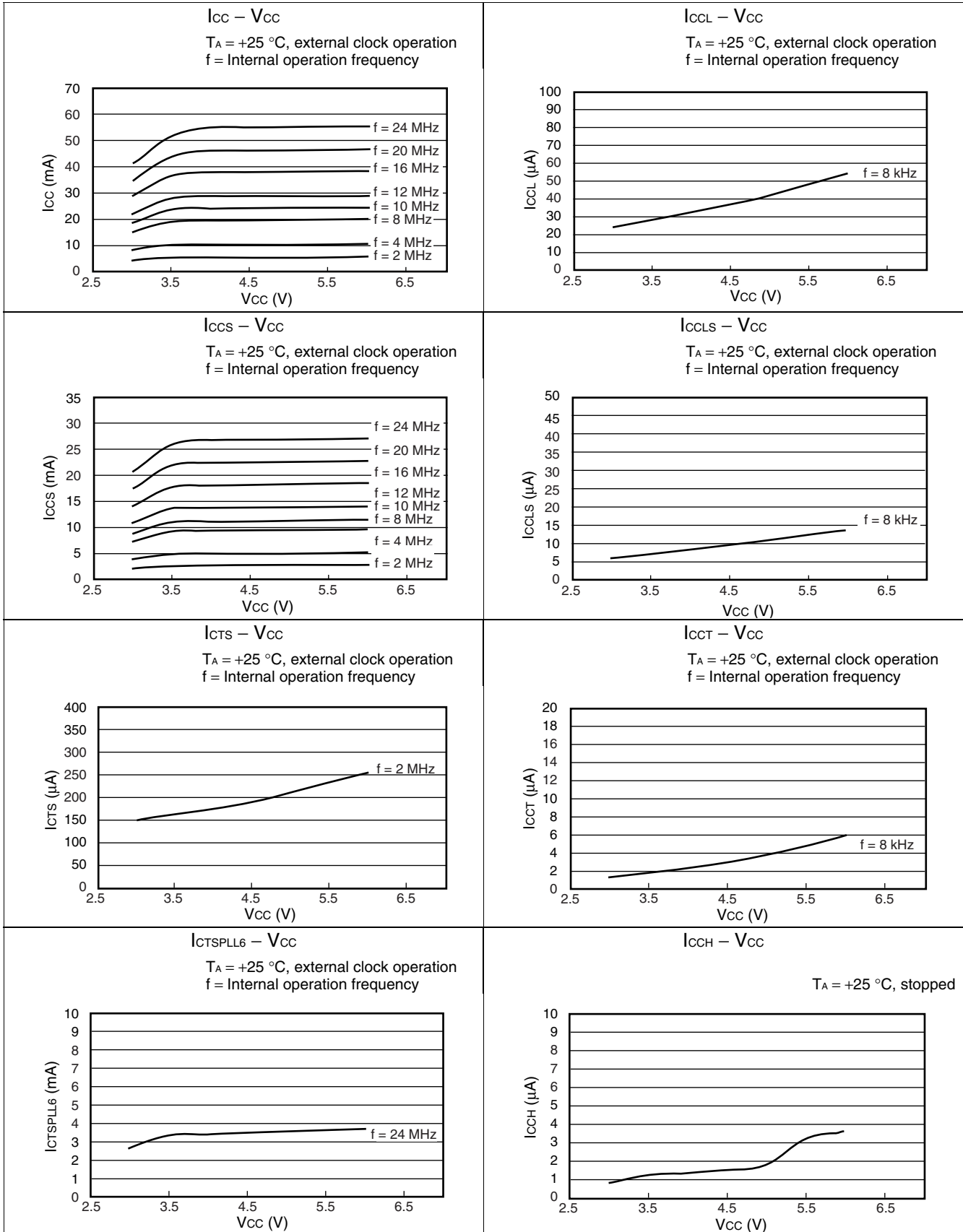
MB90340E Series

- MB90346E, MB90346ES, MB90346CE, MB90346CES



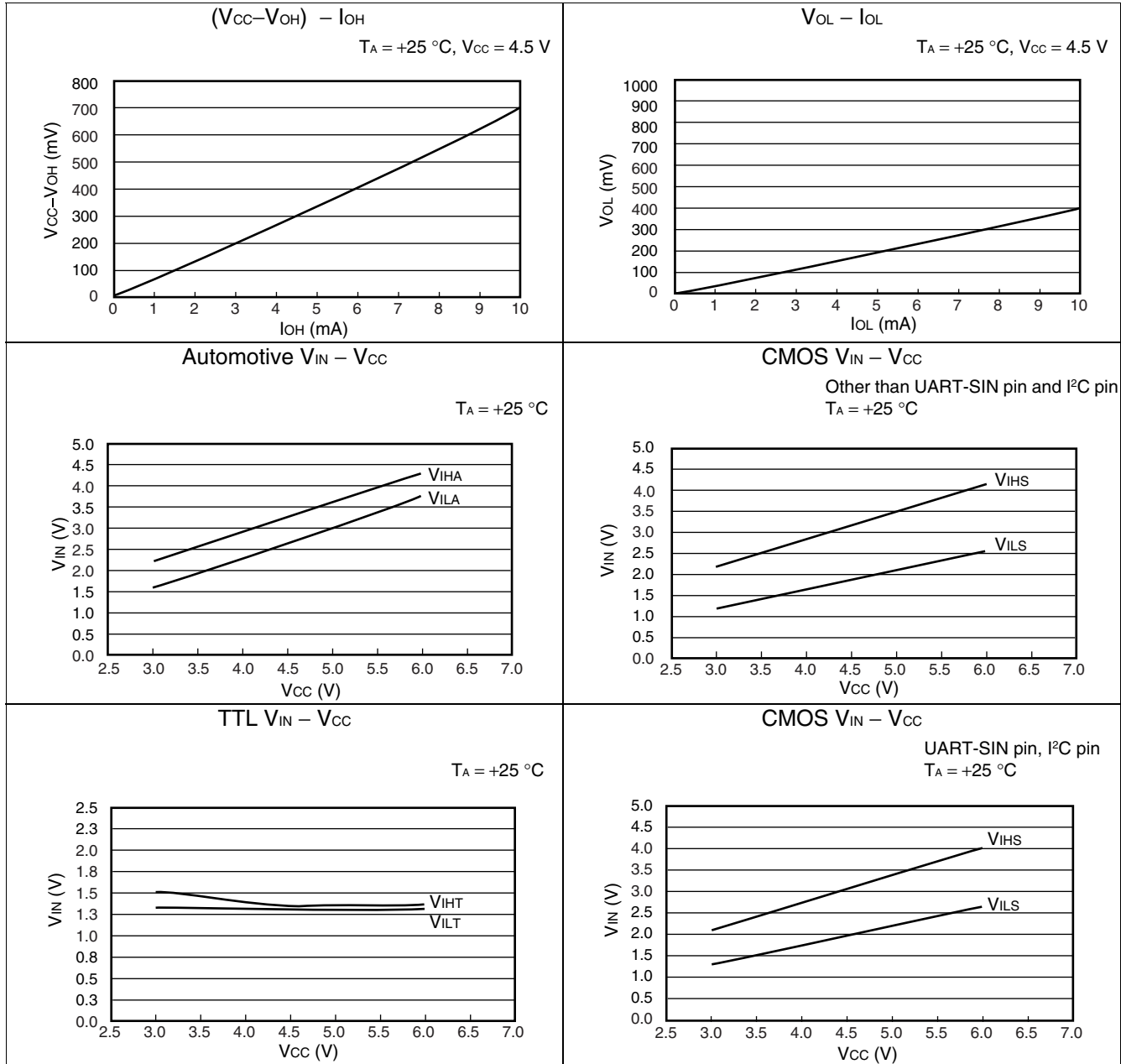
MB90340E Series

- MB90347E, MB90347ES, MB90347CE, MB90347CES



MB90340E Series

• I/O characteristics



MB90340E Series

■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F342ESPF		
MB90F342CEPF		
MB90F342CESPF		
MB90F342EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90F342ESPFV		
MB90F342CEPFV		
MB90F342CESPFV		
MB90F343EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F343ESPF		
MB90F343CEPF		
MB90F343CESPF		
MB90F343EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90F343ESPFV		
MB90F343CEPFV		
MB90F343CESPFV		
MB90F345EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F345ESPF		
MB90F345CEPF		
MB90F345CESPF		
MB90F345EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90F345ESPFV		
MB90F345CEPFV		
MB90F345CESPFV		
MB90F346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F346ESPF		
MB90F346CEPF		
MB90F346CESPF		
MB90F346EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90F346ESPFV		
MB90F346CEPFV		
MB90F346CESPFV		

(Continued)

MB90340E Series

Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90F347ESPFV		
MB90F347CEPFV		
MB90F347CESPFV		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90F349ESPFV		
MB90F349CEPFV		
MB90F349CESPFV		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90341ESPFV		
MB90341CEPFV		
MB90341CESPFV		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPFV	100-pin plastic LQFP (FPT-100P-M05)	
MB90342ESPFV		
MB90342CEPFV		
MB90342CESPFV		

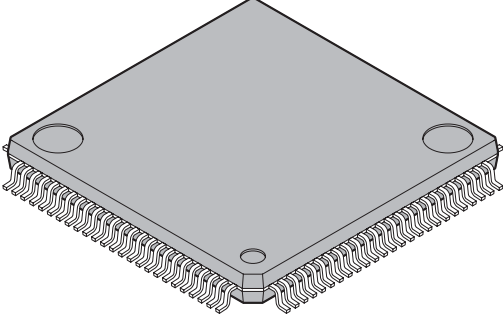
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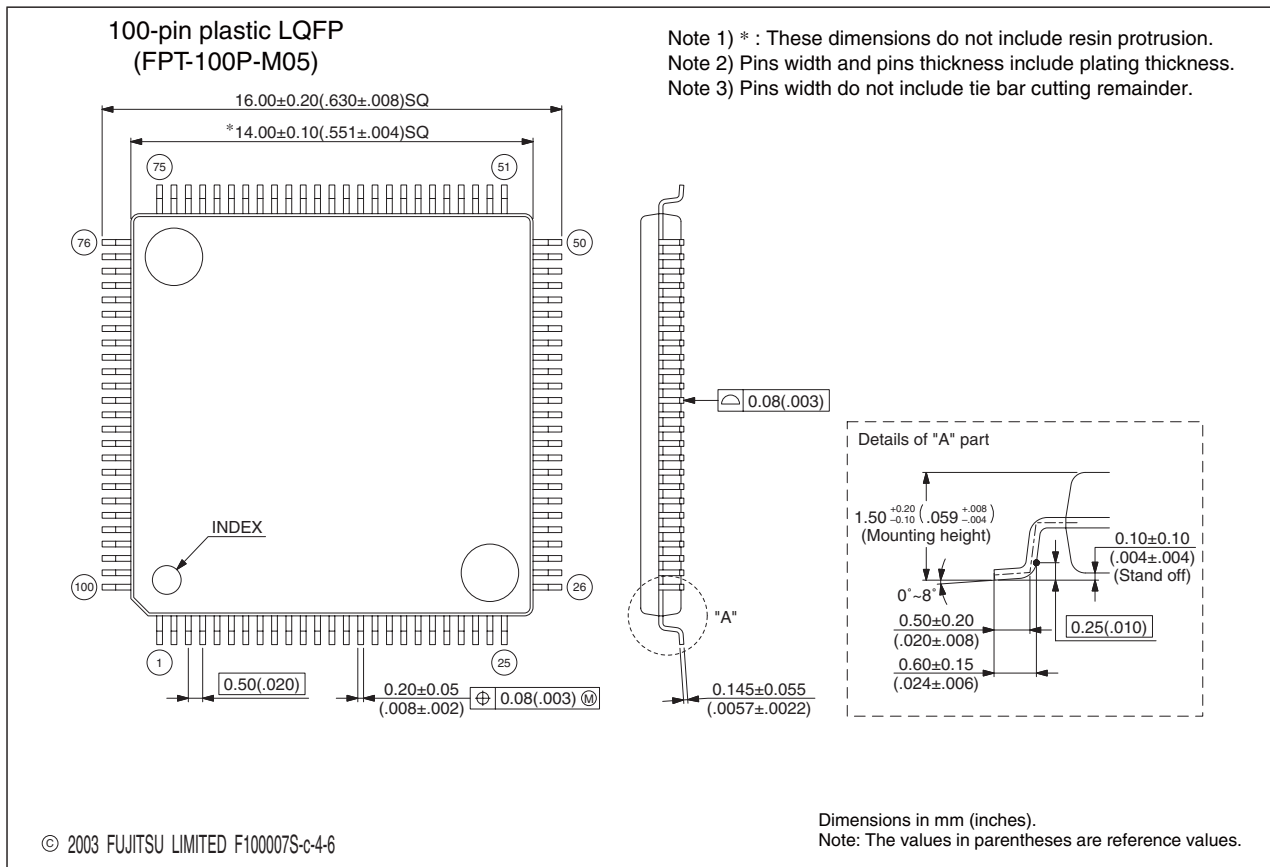
MB90340E Series

(Continued)

Part number	Package	Remarks	
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90346ESPF			
MB90346CEPF			
MB90346CESPF			
MB90346EPFV	100-pin plastic LQFP (FPT-100P-M05)		
MB90346ESPFV			
MB90346CEPFV			
MB90346CESPFV			
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90347ESPF			
MB90347CEPF			
MB90347CESPF			
MB90347EPFV	100-pin plastic LQFP (FPT-100P-M05)		
MB90347ESPFV			
MB90347CEPFV			
MB90347CESPFV			
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90348ESPF			
MB90348CEPF			
MB90348CESPF			
MB90348EPFV	100-pin plastic LQFP (FPT-100P-M05)		
MB90348ESPFV			
MB90348CEPFV			
MB90348CESPFV			
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)		
MB90349ESPF			
MB90349CEPF			
MB90349CESPF			
MB90349EPFV	100-pin plastic LQFP (FPT-100P-M05)		
MB90349ESPFV			
MB90349CEPFV			
MB90349CESPFV			
MB90V340E-101	299-pin ceramic PGA (PGA-299C-A01)		For evaluation
MB90V340E-102			

■ PACKAGE DIMENSIONS

<p>100-pin plastic LQFP</p>  <p>(FPT-100P-M05)</p>	Lead pitch	0.50 mm
	Package width × package length	14.0 × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.65g
	Code (Reference)	P-LFQFP100-14×14-0.50

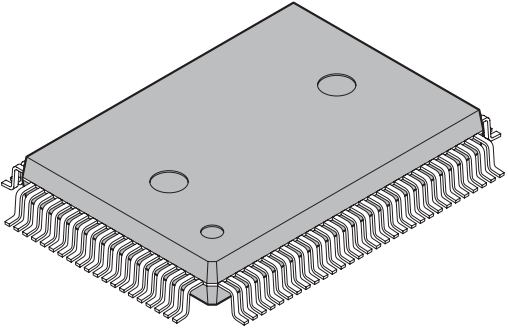


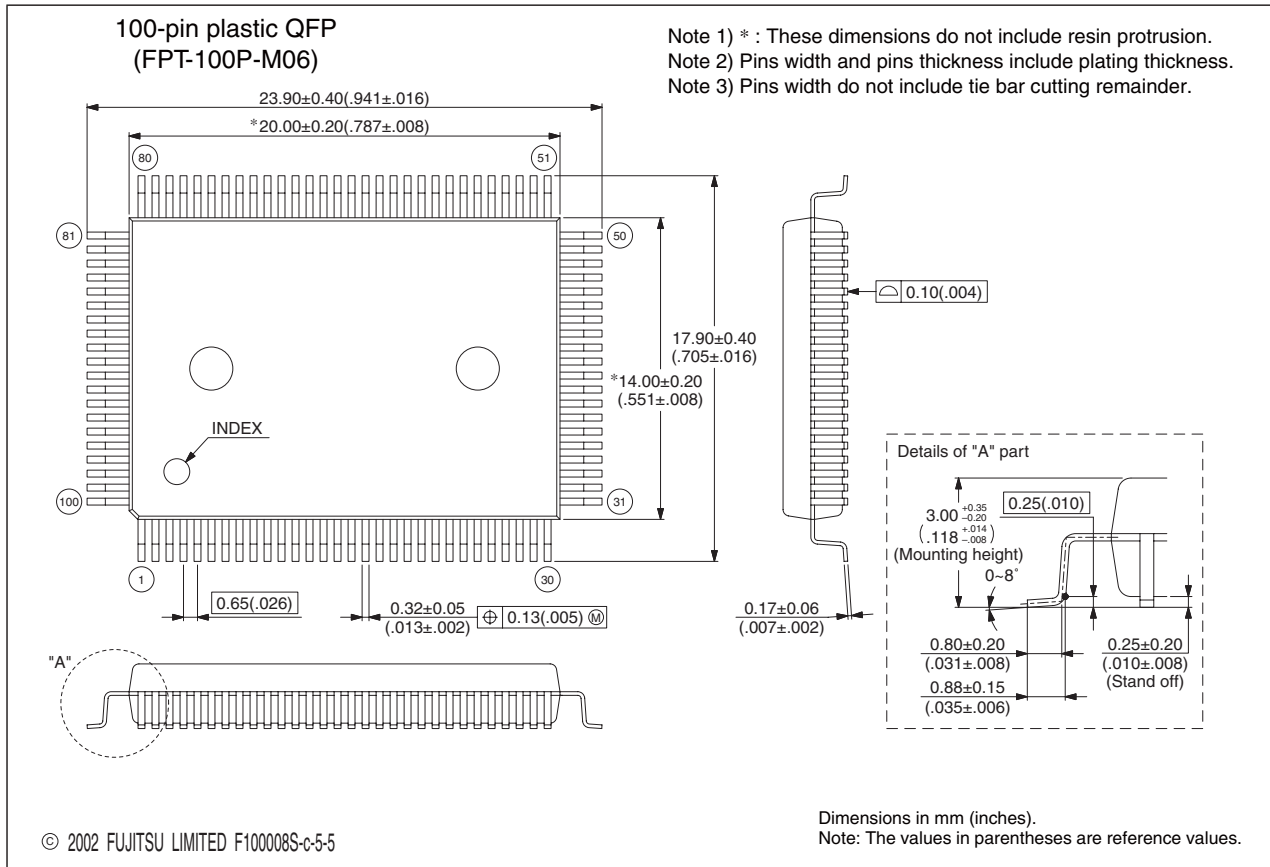
Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpkiv.html>

(Continued)

MB90340E Series

(Continued)

<p>100-pin plastic QFP</p>  <p>(FPT-100P-M06)</p>	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpklv.html>

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
3	■ FEATURES	Added a description of the "• Clock modulation circuit".
37	■ I/O MAP	Changed the row 0079C2 _H
38	Address 007E00 _H to 007FFF _H	Changed as follows; Reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS"→ Reserved
39 to 45	■ CAN CONTROLLERS	Deleted the address of CAN2

The vertical lines marked in the left side of the page show the changes.

MB90340E Series

The information for microcontroller supports is shown in the following homepage.
<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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