

16 M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE
REGISTERED TYPE

Description

The MC-4516DA726F, 4516DA726LF, 4516DA726LFB are 16,777,216 words by 72 bits synchronous dynamic RAM module on which 18 pieces of 64M SDRAM: μ PD4564441 are assembled, and the MC-4516DA726EFC is a 16,777,216 words by 72 bits synchronous dynamic RAM module on which 9 pieces of 128M SDRAM: μ PD45128841 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 16,777,216 words by 72 bits organization (ECC type)
- Clock frequency and access time from CLK

Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)	Module type
MC-4516DA726F-A80,	CL = 3	125 MHz	6 ns	PC100 Registered DIMM Rev. 1.0 Compliant
MC-4516DA726LF-A80	CL = 2	100 MHz	6 ns	
MC-4516DA726F-A10,	CL = 3	100 MHz	6 ns	
MC-4516DA726LF-A10	CL = 2	77 MHz	7 ns	
MC-4516DA726LFB-A80,	CL = 3	125 MHz	6 ns	PC100 Registered DIMM Rev. 1.2 Compliant
MC-4516DA726EFC-A80	CL = 2	100 MHz	6 ns	
MC-4516DA726LFB-A10,	CL = 3	100 MHz	6 ns	
MC-4516DA726EFC-A10	CL = 2	77 MHz	7 ns	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All DQs have $10\ \Omega \pm 10\%$ of series resistor
- Single 3.3 V ± 0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Registered type
- Serial PD

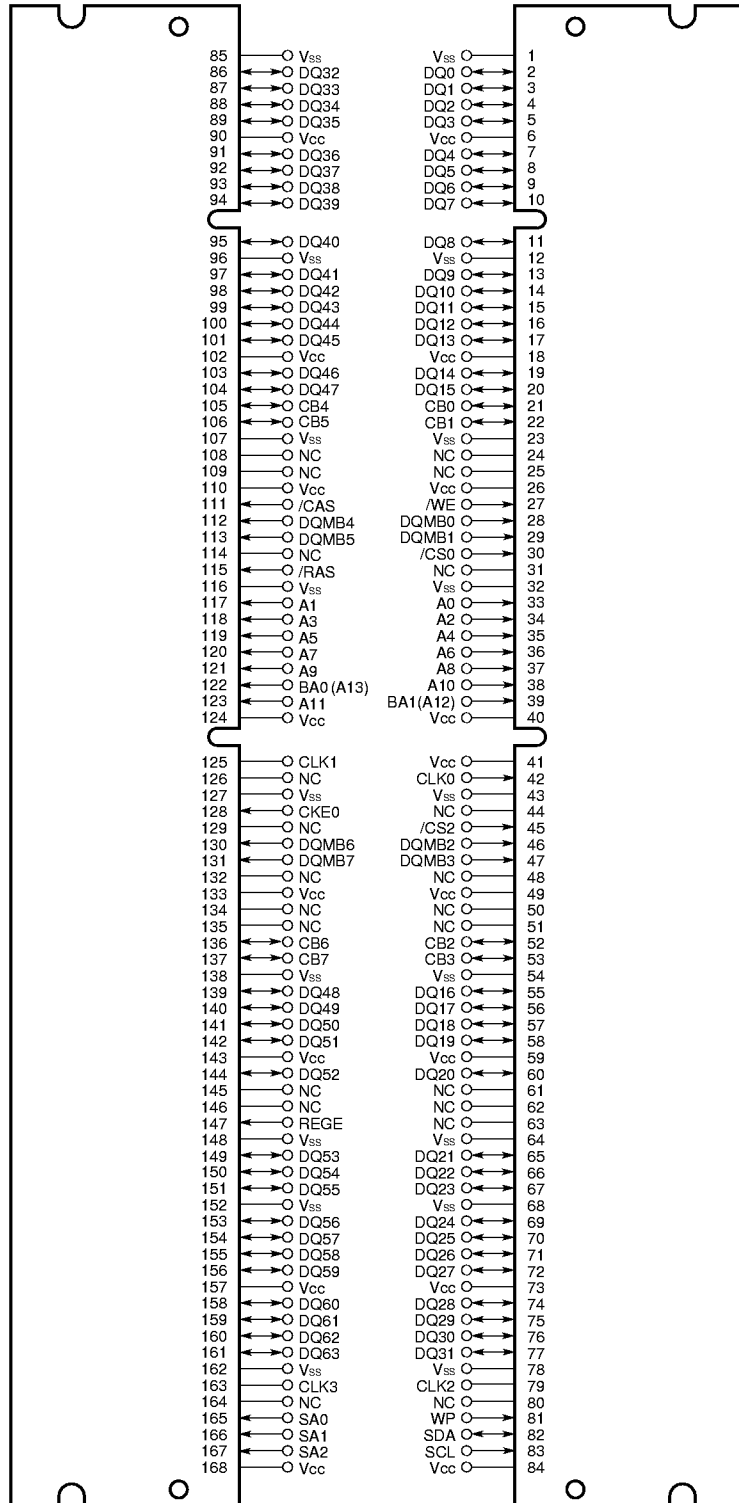
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-4516DA726F-A80	125 MHz	168-pin Dual In-line Memory Module	18 pieces of μ PD4564441G5 (Rev. E) (400 mil TSOP (II))
MC-4516DA726F-A10	100 MHz	(Socket Type)	
MC-4516DA726LF-A80	125 MHz	Edge connector: Gold plated	18 pieces of μ PD4564441G5 (Rev. L) (400 mil TSOP (II))
MC-4516DA726LF-A10	100 MHz	43.18 mm height	
MC-4516DA726LFB-A80	125 MHz		
MC-4516DA726LFB-A10	100 MHz		
MC-4516DA726EFC-A80	125 MHz	168-pin Dual In-line Memory Module (Socket Type)	9 pieces of μ PD45128841G5 (Rev. E) (400 mil TSOP (II))
MC-4516DA726EFC-A10	100 MHz	Edge connector: Gold plated 38.1 mm height	

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

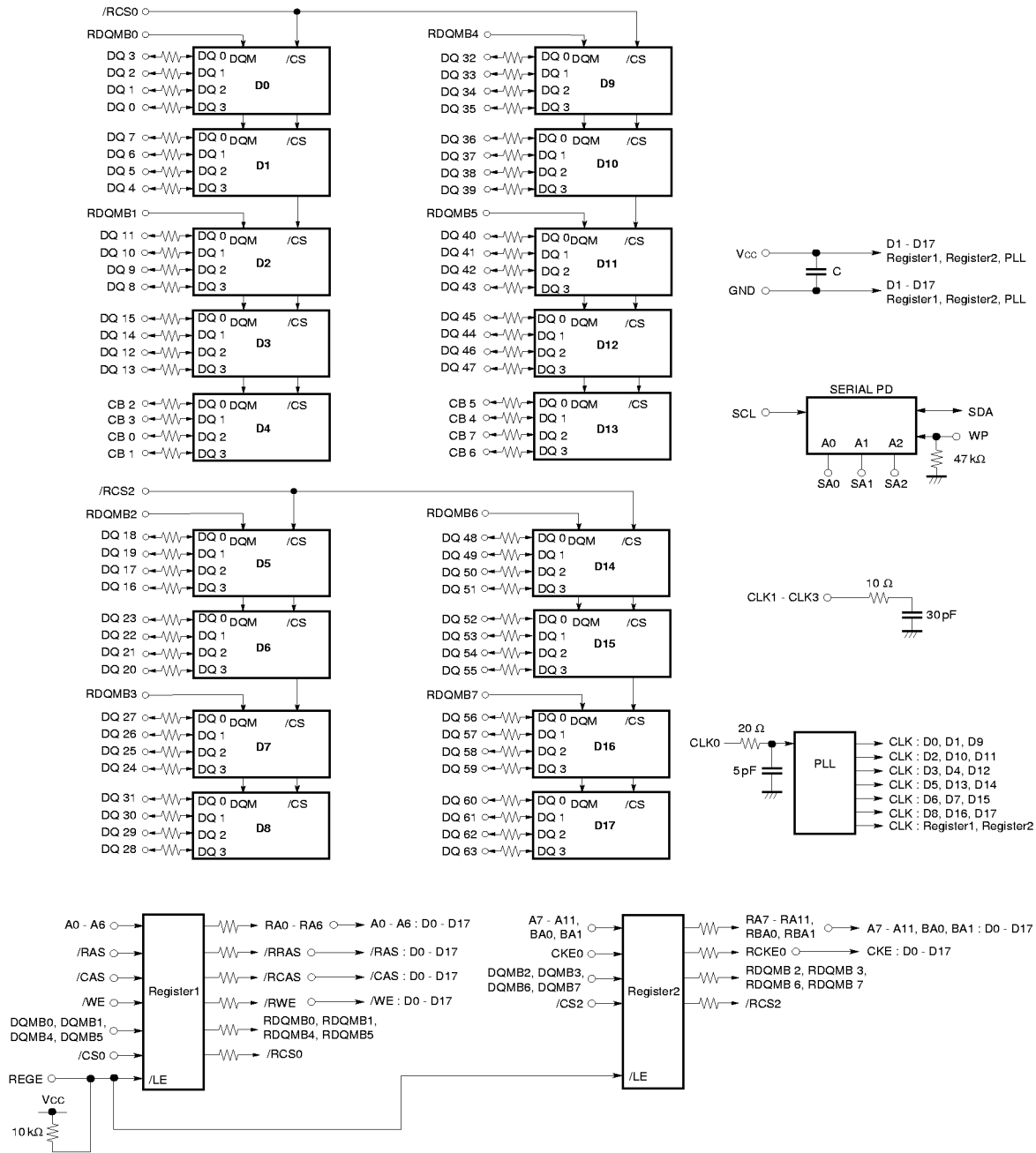


/xxx indicates active low signal.

- A0 - A11 : Address Inputs
[Row: A0 - A11, Column: A0 - A9]
- BA0 (A13), BA1 (A12) : SDRAM Bank Select
- DQ0 - DQ63, CB0 - CB7 : Data Inputs/Outputs
- CLK0 - CLK3 : Clock Input
- CKE0 : Clock Enable Input
- WP : Write Protect
- /CS0, /CS2 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SA0 - SA2 : Address Input for EEPROM
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- REGE : Register / Buffer Enable
- NC : No Connection

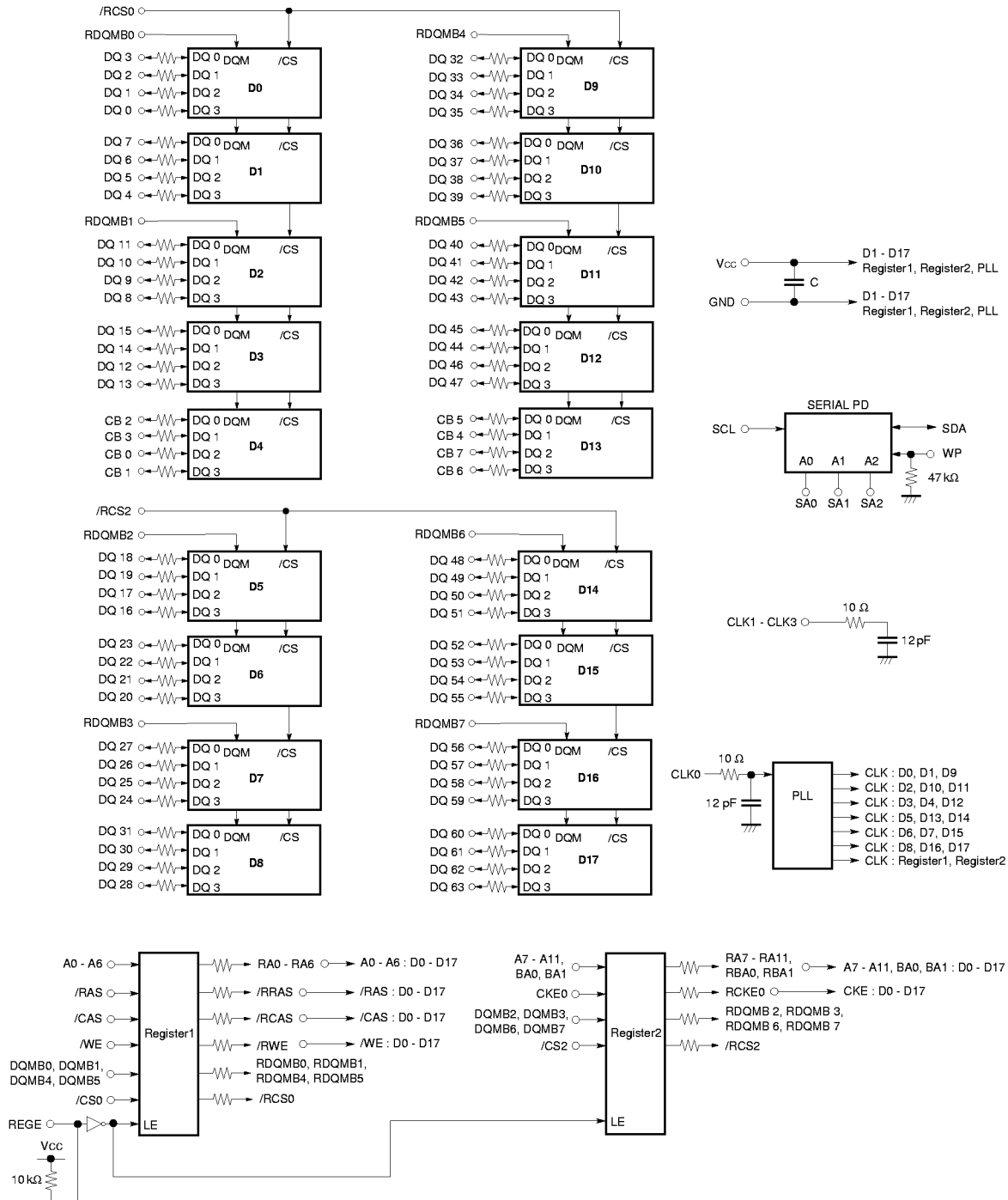
Block Diagrams

[MC-4516DA726F, 4516DA726LF]



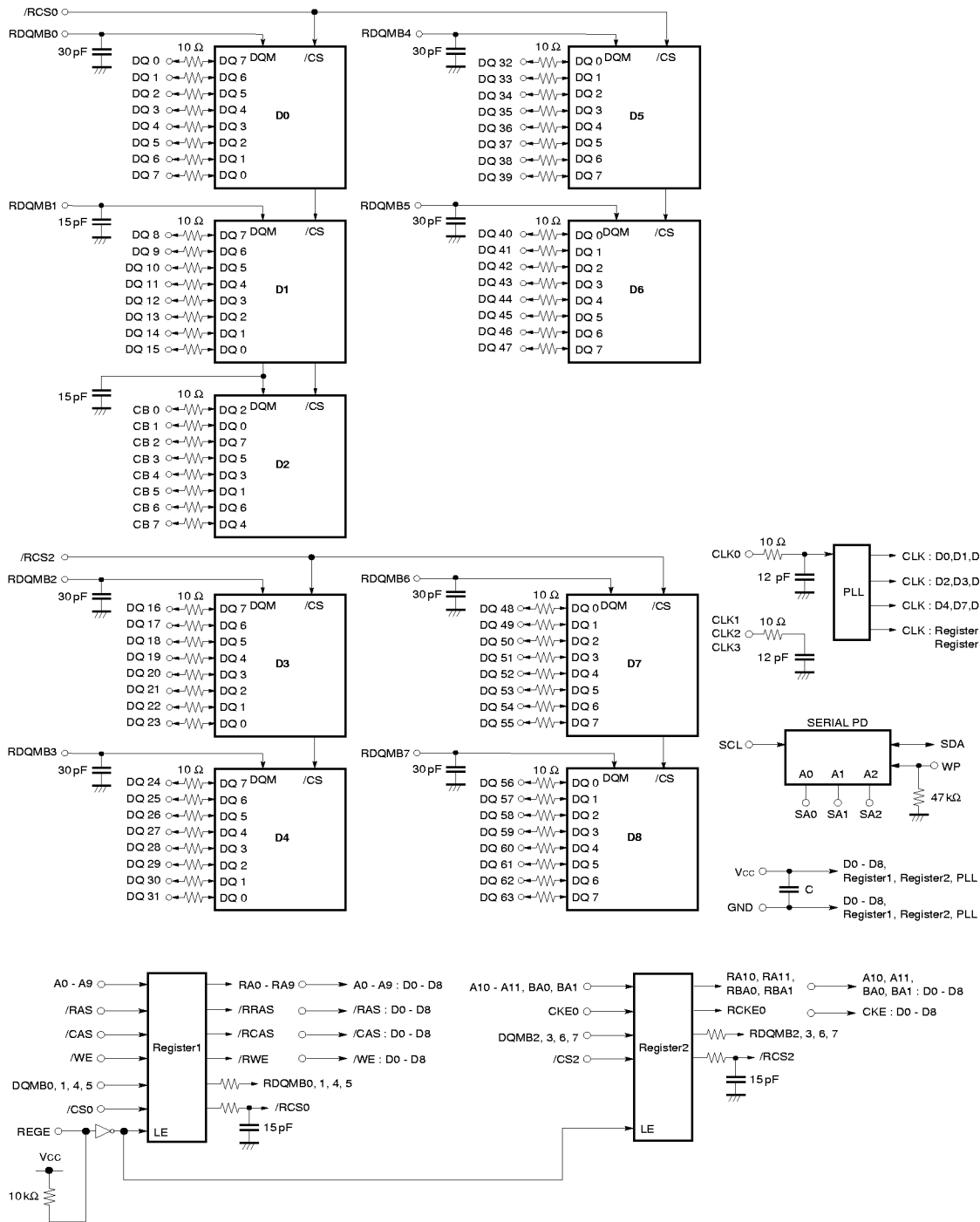
- Remarks**
1. The value of all resistors of DQs is 10 Ω.
 2. D0 - D17: μ PD4564441 (4M words \times 4 bits \times 4 banks)
 3. REGE \leq V_{IL}: Buffer mode
REGE \geq V_{IH}: Register mode
 4. Register: SN74ALVC16334DGG
PLL: CDC2509APW

[MC-4516DA726LFB]



- Remarks**
1. The value of all resistors of DQs is 10 Ω.
 2. D0 - D17: μ PD4564441 (4M words \times 4 bits \times 4 banks)
 3. REGE \leq V_{IL}: Buffer mode
REGE \geq V_{IH}: Register mode
 4. Register: HD74ALVC16835
PLL: HD74CDC2509B

[MC-4516DA726EFC]



- Remarks**
1. The value of all resistors of DQs is 10 Ω.
 2. D0 - D17: μPD45128841 (4M words × 8 bits × 4 banks)
 3. REGE ≤ V_{IL}: Buffer mode
REGE ≥ V_{IH}: Register mode
 4. Register: HD74ALVC162835
PLL: HD74CDC2509B

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 1 ms and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

[MC-4516DA726F, 4516DA726LF, 4516DA726LFB]

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC}		-0.5 to +4.6	V
Voltage on input pin relative to GND	V _T		-0.5 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		21	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

[MC-4516DA726EFC]

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC}		-0.5 to +4.6	V
Voltage on input pin relative to GND	V _T		-0.5 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		12	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		V _{CC} +0.3	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (TA = 25 °C, f = 1 MHz)

[MC-4516DA726F, 4516DA726LF]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	4		10	pF
	C _{I2}	CLK0	15		35	
	C _{I3}	CKE0	8		18	
	C _{I4}	/CS0, /CS2	4		10	
	C _{I5}	DQMB0 - DQMB7	4		10	
Data input/output capacitance	C _{I/O}	DQ0 - DQ63, CB0 - CB7	6		13	pF

★ [MC-4516DA726LFB]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	4		10	pF
	C _{I2}	CLK0	15		25	
	C _{I3}	CKE0	7		20	
	C _{I4}	/CS0, /CS2	4		10	
	C _{I5}	DQMB0 - DQMB7	4		10	
Data input/output capacitance	C _{I/O}	DQ0 - DQ63, CB0 - CB7	6		13	pF

★ [4516DA726EFC]

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	4		10	pF
	C _{I2}	CLK0	15		25	
	C _{I3}	CKE0	4		10	
	C _{I4}	/CS0, /CS2	4		10	
	C _{I5}	DQMB0 - DQMB7	4		10	
Data input/output capacitance	C _{I/O}	DQ0 - DQ63, CB0 - CB7	6		13	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-4516DA726F]

Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A80	1,650	mA	1
				-A10	1,470		
			/CAS latency = 3	-A80	1,740		
				-A10	1,560		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			268	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			19		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			610	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			108		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			340	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			72		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			700	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			180		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A80	1,920	mA	2
				-A10	1,560		
			/CAS latency = 3	-A80	2,190		
				-A10	1,920		
CBR (Auto) Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	/CAS latency = 2	-A80	2,640	mA	3
				-A10	2,640		
			/CAS latency = 3	-A80	2,730		
				-A10	2,730		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V			268	mA	
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V		-10	+10	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA			0.4	V	

- Notes**
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

[MC-4516DA726LF]

Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A80	1,650	mA	1
				-A10	1,470		
			/CAS latency = 3	-A80	1,740		
				-A10	1,560		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			268	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			26		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			610	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			108		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			340	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			72		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			700	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			270		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A80	1,920	mA	2
				-A10	1,560		
			/CAS latency = 3	-A80	2,190		
				-A10	1,920		
CBR (Auto) Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	/CAS latency = 2	-A80	2,640	mA	3
				-A10	2,640		
			/CAS latency = 3	-A80	2,730		
				-A10	2,730		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V			268	mA	
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V		-10	+10	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA			0.4	V	

- Notes**
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

[MC-4516DA726LFB]

Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC(MIN)} , I _O = 0 mA	/CAS latency = 2	-A80	1,650	mA	1
				-A10	1,470		
			/CAS latency = 3	-A80	1,740		
				-A10	1,560		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX)} , t _{CK} = 15 ns			268	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX)} , t _{CK} = ∞			86		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN)} , Input signals are changed one time during 30 ns.			610	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN)} , t _{CK} = ∞, Input signals are stable.			188		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX)} , t _{CK} = 15 ns			340	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX)} , t _{CK} = ∞			132		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN)} , Input signals are changed one time during 30 ns.			700	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN)} , t _{CK} = ∞, Input signals are stable.			350		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN)} , I _O = 0 mA	/CAS latency = 2	-A80	1,920	mA	2
				-A10	1,560		
			/CAS latency = 3	-A80	2,190		
				-A10	1,920		
CBR (Auto) Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN)}	/CAS latency = 2	-A80	2,640	mA	3
				-A10	2,640		
			/CAS latency = 3	-A80	2,730		
				-A10	2,730		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V			268	mA	
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V		-10	+10	μA	
Input leakage current (CKE0)				-20	+20		
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA			0.4	V	

- Notes**
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.
 - I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.

[MC-4516DA726EFC]

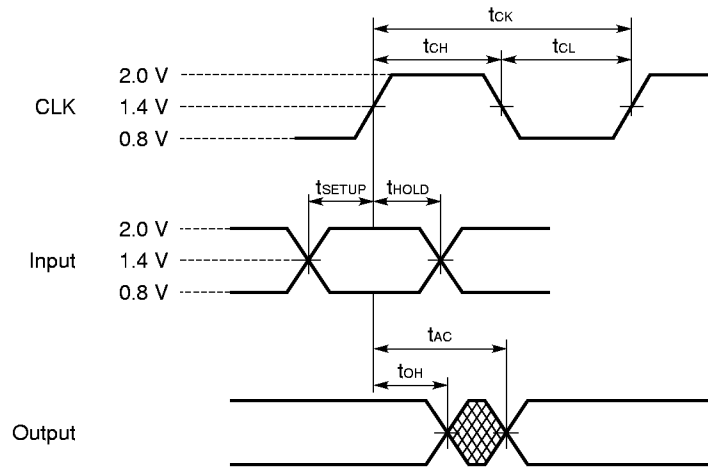
Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1 t _{RC} ≥ t _{RC(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A80	1,290	mA	1
				-A10	1,290		
			/CAS latency = 3	-A80	1,290		
				-A10	1,290		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			259	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			85		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			430	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			152		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			295	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			116		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			520	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			260		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A80	1,380	mA	2
				-A10	1,155		
			/CAS latency = 3	-A80	1,605		
				-A10	1,425		
CBR (Auto) Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	/CAS latency = 2	-A80	2,280	mA	3
				-A10	2,280		
			/CAS latency = 3	-A80	2,280		
				-A10	2,280		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V			268	mA	
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V		-10	+10	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA			0.4	V	

- Notes**
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

- AC measurements assume $t_r = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL} .
- If t_r is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.

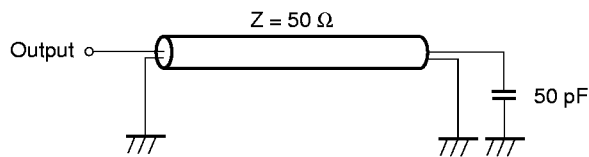


Synchronous Characteristics

[MC-4516DA726F, 4516DA726LF]

Parameter		Symbol	-A80		-A10		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	8	(125 MHz)	10	(100 MHz)	ns	
	/CAS latency = 2	t_{CK2}	10	(100 MHz)	13	(77 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		6		6	ns	1
	/CAS latency = 2	t_{AC2}		6		7	ns	1
Input CLK frequency			50	125	50	100	MHz	
Input CLK duty cycle			40	60	40	60	%	
Data-out hold time	/CAS latency = 3	t_{OH3}	3		3		ns	1
	/CAS latency = 2	t_{OH2}	3		3		ns	1
Data-out low-impedance time		t_{LZ}	0		0		ns	
Data-out high- impedance time	/CAS latency = 3	t_{HZ3}	3	6	3	6	ns	
	/CAS latency = 2	t_{HZ2}	3	6	3	7	ns	
Data-in setup time		t_{DS}	2		2		ns	
Data-in hold time		t_{DH}	1		1		ns	
Address setup time		t_{AS}	1.5		1.5		ns	
Address hold time		t_{AH}	0.9		0.9		ns	
CKE setup time		t_{CKS}	1.5		1.5		ns	
CKE hold time		t_{CKH}	0.9		0.9		ns	
CKE setup time (Power down exit)		t_{CKSP}	1.5		1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t_{CMS}	1.5		1.5		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t_{CMH}	0.9		0.9		ns	

Note 1. Output load

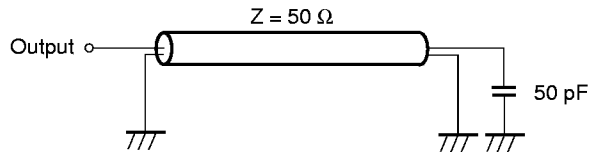


Remark These specifications are applied to the monolithic device.

[MC-4516DA726LFB, 4516DA726EFC]

Parameter		Symbol	-A80		-A10		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	8	(125 MHz)	10	(100 MHz)	ns	
	/CAS latency = 2	t_{CK2}	10	(100 MHz)	13	(77 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		6		6	ns	1
	/CAS latency = 2	t_{AC2}		6		7	ns	1
Input CLK frequency			50	125	50	100	MHz	
Input CLK duty cycle			40	60	40	60	%	
Data-out hold time	/CAS latency = 3	t_{OH3}	3		3		ns	1
	/CAS latency = 2	t_{OH2}	3		3		ns	1
Data-out low-impedance time		t_{LZ}	0		0		ns	
Data-out high- impedance time	/CAS latency = 3	t_{HZ3}	3	6	3	6	ns	
	/CAS latency = 2	t_{HZ2}	3	6	3	7	ns	
Data-in setup time		t_{DS}	2		2		ns	
Data-in hold time		t_{DH}	1		1		ns	
Address setup time		t_{AS}	2		2		ns	
Address hold time		t_{AH}	1		1		ns	
CKE setup time		t_{CKS}	2		2		ns	
CKE hold time		t_{CKH}	1		1		ns	
CKE setup time (Power down exit)		t_{CKSP}	2		2		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t_{CMS}	2		2		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t_{CMH}	1		1		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

Asynchronous Characteristics

Parameter	Symbol	-A80		-A10		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period	t _{RC}	70		70		ns	
ACT to PRE command period	t _{RAS}	48	120,000	50	120,000	ns	
PRE to ACT command period	t _{RP}	20		20		ns	
Delay time ACT to READ/WRITE command	t _{RCD}	20		20		ns	
ACT(0) to ACT(1) command period	t _{RRD}	16		20		ns	
Data-in to PRE command period	t _{DPL}	-1CLK+8		-1CLK+10		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t _{DAL3}	20	20		ns	
	/CAS latency = 2	t _{DAL2}	20	20		ns	
Mode register set cycle time	t _{RSC}	2		2		CLK	
Transition time	t _r	0.5	30	1	30	ns	
Refresh time (4,096 refresh cycles)	t _{REF}		64		64	ms	

Serial PD

[MC-4516DA726F, 4516DA726LF]

(1/2)

Byte No.	Function Described	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns	0AH	0	0	0	0	1	0	1	0	10 columns
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL
9	CL = 3 Cycle time	-A80	80H	1	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	10 ns
10	CL = 3 Access time	-A80	60H	0	1	1	0	0	0	0	6 ns
		-A10	60H	0	1	1	0	0	0	0	6 ns
11	DIMM configuration type	02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width	04H	0	0	0	0	0	1	0	0	x4
14	Error checking SDRAM width	04H	0	0	0	0	0	1	0	0	x4
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes	1FH	0	0	0	1	1	1	1	1	Registered
22	SDRAM device attributes: General	0EH	0	0	0	0	1	1	1	0	
23	CL = 2 Cycle time	-A80	A0H	1	0	1	0	0	0	0	10 ns
		-A10	D0H	1	1	0	1	0	0	0	13 ns
24	CL = 2 Access time	-A80	60H	0	1	1	0	0	0	0	6 ns
		-A10	70H	0	1	1	1	0	0	0	7 ns
25-26		00H	0	0	0	0	0	0	0	0	
27	t _{RP(MIN.)}	-A80	14H	0	0	0	1	0	1	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	20 ns
28	t _{RRD(MIN.)}	-A80	10H	0	0	0	1	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	20 ns
29	t _{RCD(MIN.)}	-A80	14H	0	0	0	1	0	1	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	20 ns
30	t _{RAS(MIN.)}	-A80	30H	0	0	1	1	0	0	0	48 ns
		-A10	32H	0	0	1	1	0	0	1	50 ns
31	Module bank density	20H	0	0	1	0	0	0	0	0	128M bytes

(2/2)

Byte No.	Function Described	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
32	Command and address signal input setup time	15H	0	0	0	1	0	1	0	1	1.5 ns	
33	Command and address signal input hold time	09H	0	0	0	0	1	0	0	1	0.9 ns	
34	Data signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
35	Data signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
36-61		00H	0	0	0	0	0	0	0	0		
62	SPD revision	12H	0	0	0	1	0	0	1	0	1.2A	
63	Checksum for bytes 0 - 62	-A80	07H	0	0	0	0	0	1	1	1	
		-A10	6DH	0	1	1	0	1	1	0	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency	64H	0	1	1	0	0	1	0	0	100 MHz	
127	Intel specification /CAS latency support	-A80	87H	1	0	0	0	0	1	1	1	
		-A10	85H	1	0	0	0	0	1	0	1	

[MC-4516DA726LFB]

(1/2)

Byte No.	Function Described	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM	
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows	
4	Number of columns	0AH	0	0	0	0	1	0	1	0	10 columns	
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank	
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	CL = 3 Cycle time	-A80	80H	1	0	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
10	CL = 3 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
11	DIMM configuration type	02H	0	0	0	0	0	0	1	0	ECC	
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	Normal	
13	SDRAM width	04H	0	0	0	0	0	1	0	0	x4	
14	Error checking SDRAM width	04H	0	0	0	0	0	1	0	0	x4	
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F	
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks	
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3	
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0	
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0	
21	SDRAM module attributes	1FH	0	0	0	1	1	1	1	1	Registered	
22	SDRAM device attributes: General	0EH	0	0	0	0	1	1	1	0		
23	CL = 2 Cycle time	-A80	A0H	1	0	1	0	0	0	0	0	10 ns
		-A10	D0H	1	1	0	1	0	0	0	0	13 ns
24	CL = 2 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	70H	0	1	1	1	0	0	0	0	7 ns
25-26		00H	0	0	0	0	0	0	0	0		
27	t _{RP(MIN.)}	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
28	t _{RRD(MIN.)}	-A80	10H	0	0	0	1	0	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
29	t _{RCD(MIN.)}	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
30	t _{RAS(MIN.)}	-A80	30H	0	0	1	1	0	0	0	0	48 ns
		-A10	32H	0	0	1	1	0	0	1	0	50 ns
31	Module bank density	20H	0	0	1	0	0	0	0	0	128M bytes	

(2/2)

Byte No.	Function Described	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
32	Command and address signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
33	Command and address signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
34	Data signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
35	Data signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
36-61		00H	0	0	0	0	0	0	0	0		
62	SPD revision	12H	0	0	0	1	0	0	1	0	1.2A	
63	Checksum for bytes 0 - 62	-A80	19H	0	0	0	1	1	0	0	1	
		-A10	7FH	0	1	1	1	1	1	1	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency	64H	0	1	1	0	0	1	0	0	100 MHz	
127	Intel specification /CAS latency support	-A80	87H	1	0	0	0	0	1	1	1	
		-A10	85H	1	0	0	0	0	1	0	1	

[4516DA726EFC]

(1/2)

Byte No.	Function Described	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM	
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows	
4	Number of columns	0AH	0	0	0	0	1	0	1	0	10 columns	
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank	
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	CL = 3 Cycle time	-A80	80H	1	0	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
10	CL = 3 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
11	DIMM configuration type	02H	0	0	0	0	0	0	1	0	ECC	
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	Normal	
13	SDRAM width	08H	0	0	0	0	1	0	0	0	x8	
14	Error checking SDRAM width	08H	0	0	0	0	1	0	0	0	x8	
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F	
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks	
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3	
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0	
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0	
21	SDRAM module attributes	1FH	0	0	0	1	1	1	1	1	Registered	
22	SDRAM device attributes: General	0EH	0	0	0	0	1	1	1	0		
23	CL = 2 Cycle time	-A80	A0H	1	0	1	0	0	0	0	0	10 ns
		-A10	D0H	1	1	0	1	0	0	0	0	13 ns
24	CL = 2 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	70H	0	1	1	1	0	0	0	0	7 ns
25-26		00H	0	0	0	0	0	0	0	0		
27	t _{RP(MIN.)}	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
28	t _{RRD(MIN.)}	-A80	10H	0	0	0	1	0	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
29	t _{RCD(MIN.)}	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
30	t _{RAS(MIN.)}	-A80	30H	0	0	1	1	0	0	0	0	48 ns
		-A10	32H	0	0	1	1	0	0	1	0	50 ns
31	Module bank density	20H	0	0	1	0	0	0	0	0	128M bytes	

(2/2)

Byte No.	Function Described	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
32	Command and address signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
33	Command and address signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
34	Data signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
35	Data signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
36-61		00H	0	0	0	0	0	0	0	0		
62	SPD revision	12H	0	0	0	1	0	0	1	0	1.2A	
63	Checksum for bytes 0 - 62	-A80	21H	0	0	1	0	0	0	0	1	
		-A10	87H	1	0	0	0	0	1	1	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency	64H	0	1	1	0	0	1	0	0	100 MHz	
127	Intel specification /CAS latency support	-A80	87H	1	0	0	0	0	1	1	1	
		-A10	85H	1	0	0	0	0	1	0	1	

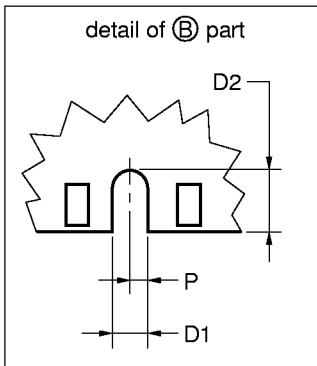
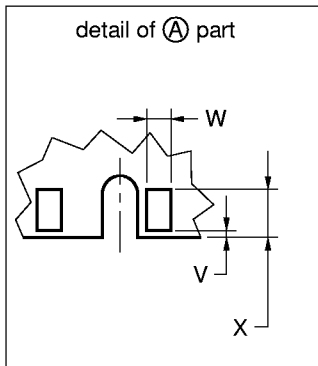
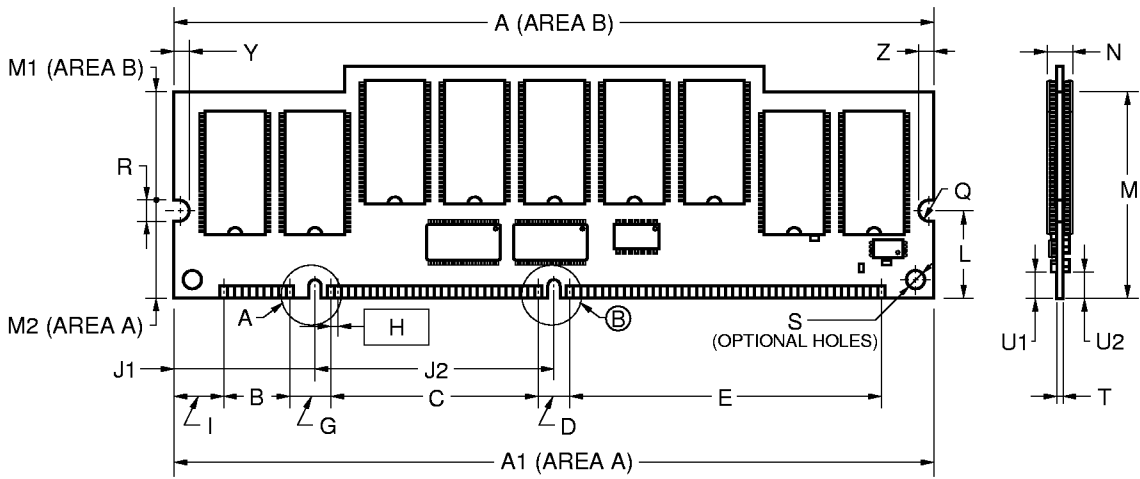
Timing Chart

Refer to the **SYNCHRONOUS DRAM MODULE TIMING CHART Information (M13348E)**.

Package Drawings

[MC-4516DA726F, 4516DA726LF]

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)

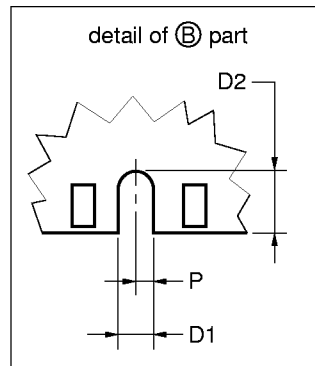
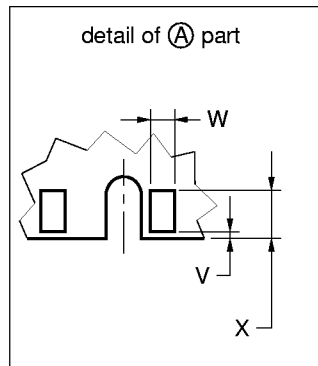
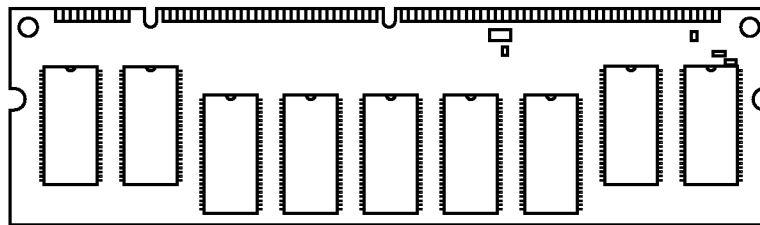
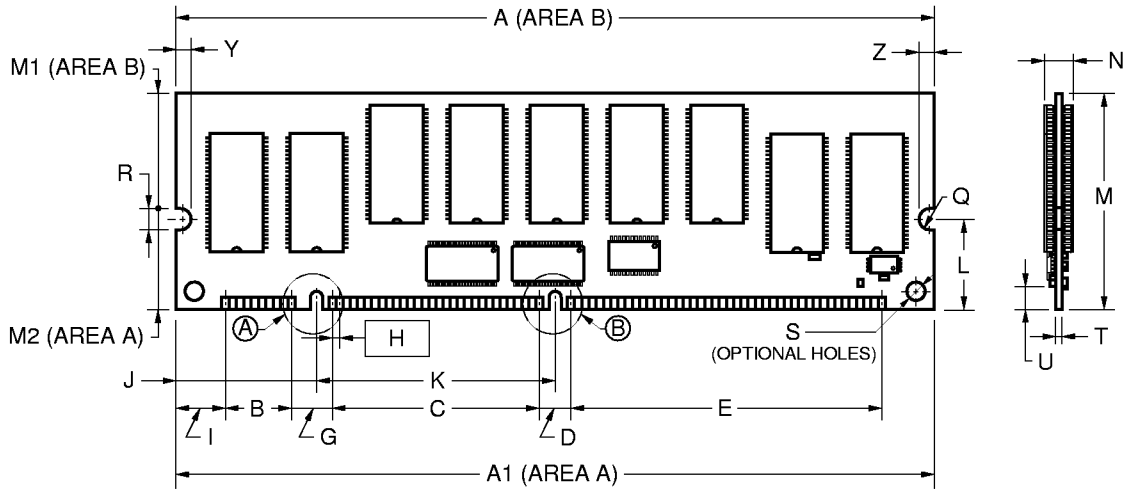


ITEM	MILLIMETERS
A	133.35
A1	133.35±0.13
B	11.43
C	36.83
D	6.35
D1	2.0
D2	3.125
E	54.61
F	5.08
G	6.35
H	1.27 (T.P.)
I	8.89
J1	24.495
J2	42.18
K1	29.97
K2	29.97
L	17.78
M	38.1±0.13
M1	18.32
M2	19.78
N	4.0 MAX.
P	1.0
Q	R2.0
R	4.0±0.10
S	φ 3.0
T	1.27±0.1
U1	4.0 MIN.
U2	4.0 MIN.
V	0.25 MAX.
W	1.0±0.05
X	2.54±0.10
Y	3.0 MIN.
Z	3.0 MIN.

M168S-50A93

[MC-4516DA726LFB]

168-PIN DUAL IN-LINE MODULE (SOCKET TYPE)

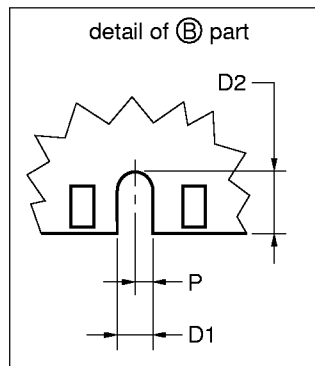
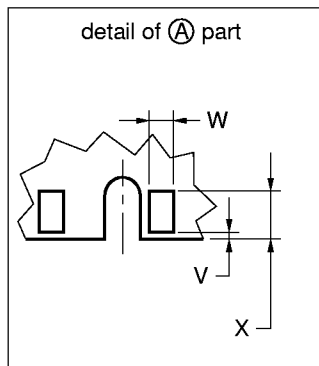
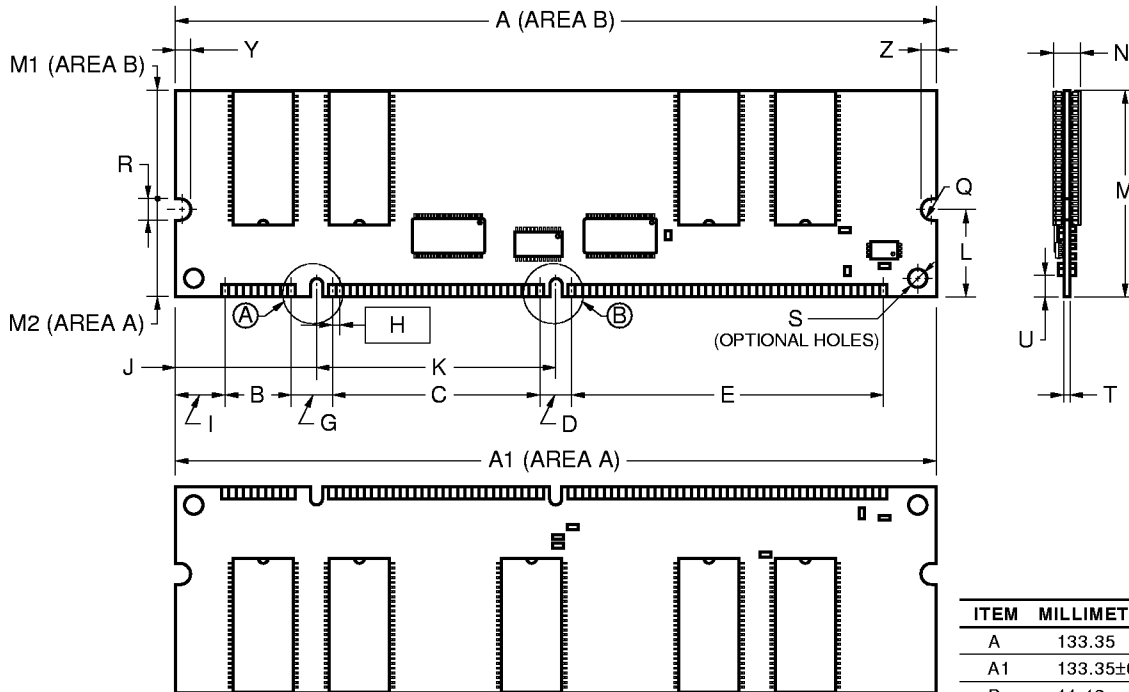


ITEM	MILLIMETERS
A	133.35
A1	133.35±0.13
B	11.43
C	36.83
D	6.35
D1	2.0
D2	3.125
E	54.61
G	6.35
H	1.27 (T.P.)
I	8.89
J	24.495
K	42.18
L	17.78
M	43.18±0.13
M1	23.40
M2	19.78
N	4.0 MAX.
P	1.0
Q	R2.0
R	4.0±0.10
S	φ 3.0
T	1.27±0.1
U	4.0 MIN.
V	0.2±0.15
W	1.0±0.05
X	2.54±0.10
Y	3.0 MIN.
Z	3.0 MIN.

M168S-50A107

★ [MC-4516DA726EFC]

168-PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	133.35
A1	133.35±0.13
B	11.43
C	36.83
D	6.35
D1	2.0
D2	3.125
E	54.61
G	6.35
H	1.27 (T.P.)
I	8.89
J	24.495
K	42.18
L	17.78
M	38.1±0.13
M1	18.32
M2	19.78
N	4.0 MAX.
P	1.0
Q	R2.0
R	4.0±0.10
S	φ 3.0
T	1.27±0.1
U	4.0 MIN.
V	0.2±0.15
W	1.0±0.05
X	2.54±0.10
Y	3.0 MIN.
Z	3.0 MIN.

M168S-50A106