

MC10E211, MC100E211

5V ECL 1:6 Differential Clock Distribution Chip

The MC10E/100E211 is a low skew 1:6 fanout device designed explicitly for low skew clock distribution applications.

The E211 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open in which case it will be pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

Both a common enable and individual output enables are provided. When asserted the positive output will go LOW on the next negative transition of the CLK (or SCLK) input. The enabling function is synchronous so that the outputs will only be enabled/disabled when the outputs are already in the LOW state. In this way the problem of runt pulse generation during the disable operation is avoided. Note that the internal flip flop is clocked on the falling edge of the input clock edge, therefore all associated specifications are referenced to the negative edge of the CLK input.

The output transitions of the E211 are faster than the standard ECLinPS edge rates. This feature provides a means of distributing higher frequency signals than capable with the E111 device. Because of these edge rates and the tight skew limits guaranteed in the specification, there are certain termination guidelines which must be followed. For more details on the recommended termination schemes please refer to the applications information section of this data sheet.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

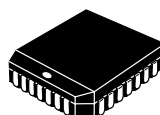
- Guaranteed Low Skew Specification
- Synchronous Enabling/Disabling
- Multiplexed Clock Inputs
- V_{BB} Output for Single-Ended Use
- Common and Individual Enable/Disable Control
- High Bandwidth Output Transistors
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",
Oxygen Index 28 to 34
- Transistor Count = 457 devices



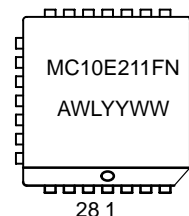
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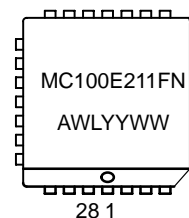
MARKING DIAGRAMS



PLCC-28
FN SUFFIX
CASE 776



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E211FN	PLCC-28	37 Units/Rail
MC10E211FNR2	PLCC-28	500 Units/Reel
MC100E211FN	PLCC-28	37 Units/Rail
MC100E211FNR2	PLCC-28	500 Units/Reel

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MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V _{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 -5.7 to -4.2	V V
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		119	160		119	160		119	160	mA
V _{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V _{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V _{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V _{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V _{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.4		4.6	2.4		4.6	2.4		4.6	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= -5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		119	160		119	160		119	160	mA
V _{OH}	Output HIGH Voltage (Note 2.)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
V _{OL}	Output LOW Voltage (Note 2.)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
V _{IH}	Input HIGH Voltage (Single Ended)	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
V _{IL}	Input LOW Voltage (Single Ended)	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
V _{BB}	Output Voltage Reference	-1.38		-1.37	-1.35		-1.25	-1.31		-1.19	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	-2.6		-0.4	-2.6		-0.4	-2.6		-0.4	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

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100E SERIES PECL DC CHARACTERISTICS $V_{CCx}=5.0\text{ V}; V_{EE}=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		119	160		119	160		137	164	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.4		4.6	2.4		4.6	2.4		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

100E SERIES NECL DC CHARACTERISTICS $V_{CCx}=0.0\text{ V}; V_{EE}=-5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		119	160		119	160		137	164	mA
V_{OH}	Output HIGH Voltage (Note 2.)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V_{OL}	Output LOW Voltage (Note 2.)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
V_{IL}	Input LOW Voltage (Single Ended)	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	-2.6		-0.4	-2.6		-0.4	-2.6		-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}-2$ volts.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

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AC CHARACTERISTICS $V_{CCx}= 5.0\text{ V}; V_{EE}= 0.0\text{ V}$ or $V_{CCx}= 0.0\text{ V}; V_{EE}= -5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q (Diff) CLK to Q (SE) SCLK to Q SEL to Q	795 745 650 745	930 930 900 970	1065 1115 1085 1195	805 755 650 755	940 940 910 980	1075 1125 1095 1205	825 775 650 775	960 960 930 1000	1095 1145 1115 1225	ps
t_{PHL}	Disable Time CLK or SCLK to Q (Note 3.)		600	800		600	800		600	800	ps
t_{skew}	Part-to-Part Skew CLK (Diff) to Q CLK (SE), SCLK to Q Within-Device Skew (Note 2.)		50	270 370 75		50	270 370 75			270 370 75	ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD		TBD			ps
t_s	Setup Time $\overline{EN}x$ to CLK \overline{CEN} to CLK (Note 3.)	200 200	-100 0		200 200	-100 0		200 200	-100 0		ps
t_h	Hold Time CLK to $\overline{EN}x$, \overline{CEN} (Note 3.)	900	600		900	160		900	600		ps
V_{PP}	Minimum Input Swing (CLK) (Note 4.)	0.25		1.0	0.25		1.0	0.25		1.0	V
t_r t_f	Rise/Fall Times (20 – 80%)	150		400	150		400	150		400	ps

- 10 Series: V_{EE} can vary +0.46 V / -0.06 V.
100 Series: V_{EE} can vary +0.46 V / -0.8 V.
- Within-Device skew is defined for identical transitions on similar paths through a device.
- Setup, Hold and Disable times are all relative to a falling edge on CLK or SCLK.
- Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.

APPLICATIONS INFORMATION

General Description

The MC10E/100E211 is a 1:6 fanout tree designed explicitly for low skew high speed clock distribution. The device was targeted to work in conjunction with the E111 device to provide another level of flexibility in the design and implementation of clock distribution trees. The individual synchronous enable controls and multiplexed clock inputs make the device ideal as the first level distribution unit in a distribution tree. The device provides the ability to distribute a lower speed scan or test clock along with the high speed system clock to ease the design of system diagnostics and self test procedures. The individual enables could be used to allow for the disabling of individual cards on a backplane in fault tolerant designs.

Because of lower fanout and larger skews the E211 will not likely be used as an alternative to the E111 for the bulk of the clock fanout generation. Figure 1 shows a typical application combining the two devices to take advantage of the strengths of each.

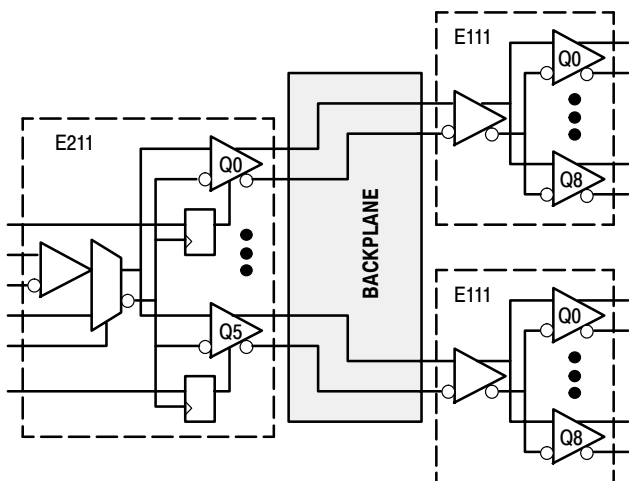


Figure 1. Standard E211 Application

Using the E211 in PECL Designs

The E211 device can be utilized very effectively in designs utilizing only a +5V power supply. Since the internal switching reference levels are biased off of the V_{CC} supply the input thresholds for the single-ended inputs will vary with V_{CC} . As a result the single-ended inputs should be driven by a device on the same board as the E211. Driving these inputs across a backplane where significant differences between the V_{CC} 's of the transmitter and receiver can occur can lead to AC performance and/or significant noise margin degradations. Because the differential I/O does not use a switching reference, and due to the CMR range of the E211, even under worst case V_{CC} situations between cards there will be no AC performance or noise margin loss for the differential CLK inputs.

For situations where TTL clocks are required the E211 can be interfaced with the H641 or H643 ECL to TTL Clock Distribution Chips. The H641 is a single supply 1:9 PECL to TTL device while the H643 is a 1:8 dual supply standard ECL to TTL device. By combining the superior skew performance of the E211, or E111, with the low skew translating capabilities of the H641 and H643 very low skew TTL clock distribution networks can be realized.

Handling Open Inputs and Outputs

All of the input pins of the E211 have a 50k Ω to 75k Ω pulldown resistor to pull the input to V_{EE} when left open. This feature can cause a problem if the differential clock inputs are left open as the input gate current source transistor will become saturated. Under these conditions the outputs of the CLK input buffer will go to an undefined state. It is recommended, if possible, that the SCLK input should be selected any time the differential CLK inputs are allowed to float. The SCLK buffer, under open input conditions, will maintain a defined output state and thus the Q outputs of the device will be in a defined state ($Q = \text{LOW}$). Note that if all of the inputs are left open the differential CLK input will be selected and the state of the Q outputs will be undefined.

With the simultaneous switching characteristics and the tight skew specifications of the E211 the handling of the unused outputs becomes critical. To minimize the noise generated on the die all outputs should be terminated in pairs, i.e. both the true and complement outputs should be terminated even if only one of the outputs will be used in the system. With both complimentary pairs terminated the current in the V_{CC} pins will remain essentially constant and thus inductance induced voltage glitches on V_{CC} will not occur. V_{CC} glitches will result in distorted output waveforms and degradations in the skew performance of the device.

The package parasitics of the 28-lead PLCC cause the signals on a given pin to be influenced by signals on adjacent pins. The E211 is characterized and tested with all of the outputs switching, therefore the numbers in the data book are guaranteed only for this situation. If all of the outputs of the E211 are not needed and there is a desire to save power the unused output pairs can be left unterminated. Unterminated outputs can influence the propagation delay on adjacent pins by 15ps - 20ps. Therefore under these conditions this 15ps - 20ps needs to be added to the overall skew of the device. Pins which are separated by a package corner are not considered adjacent pins in the context of propagation delay influence. Therefore as long as all of the outputs on a single side of the package are terminated the specification limits in the data sheet will apply.

APPLICATIONS INFORMATION

Differential versus Single-Ended Use

As can be seen from the data sheet, to minimize the skew of the E211 the device must be used in the differential mode. In the single-ended mode the propagation delays are dependent on the relative position of the V_{BB} switching reference. Any V_{BB} offset from the center of the input swing will add delay to either the T_{PLH} or T_{PHL} and subtract delay from the other. This increase and decrease in delay will lead to an increase in the duty cycle skew and thus part-to-part skew. The within-device skew will be independent of the V_{BB} and therefore will be the same regardless of whether the device is driven differentially or single-endedly.

For applications where part-to-part skew or duty cycle skew are not important the advantages of single-ended clock distribution may lead to its use. Using single-ended interconnect will reduce the number of signal traces to be routed, but remember that all of the complimentary outputs still need to be terminated therefore there will be no reduction in the termination components required. To use the E211 with a single-ended input the arrangement pictured in Figure 2b should be used. If the input to the differential CLK inputs are AC coupled as pictured in Figure 2a the dependence on a centered V_{BB} reference is removed. The situation pictured will ensure that the input is centered around the bias set by the V_{BB} . As a result when AC coupled the AC specification limits for a differential input can be used. For more information on AC coupling please refer to the interfacing section of the design guide in the ECLinPS data book.

Using the Enable Pins

Both the common enable (\overline{CEN}) and the individual enables (\overline{ENx}) are synchronous to the CLK or SCLK input depending on which is selected. The active low signals are clocked into the enable flip flops on the negative edges of the E211 clock inputs. In this way the devices will only be disabled when the outputs are already in the LOW state. The internal propagation delays are such that the delay to the output through the distribution buffers is less than that through the enable flip flops. This will ensure that the disabling of the device will not slice any time off the clock pulse. On initial power up the enable flip flops will randomly

attain a stable state, therefore precautions should be taken on initial power up to ensure the E211 is in the desired state.

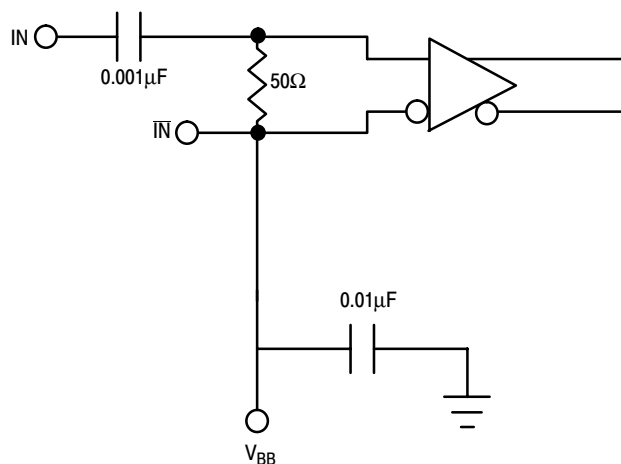


Figure 2a. AC Coupled Input

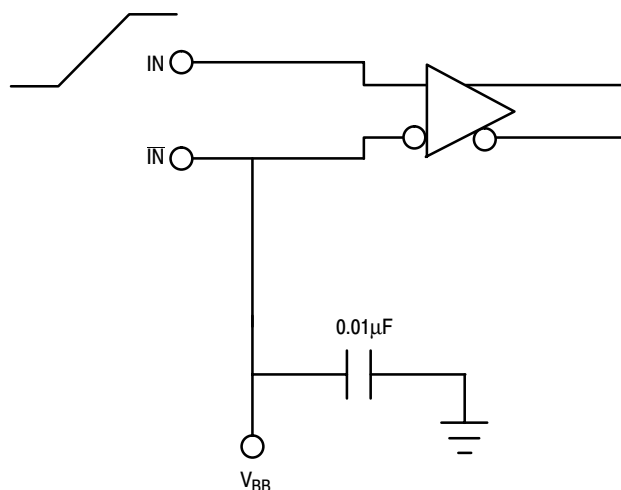


Figure 2b. Single-Ended Input

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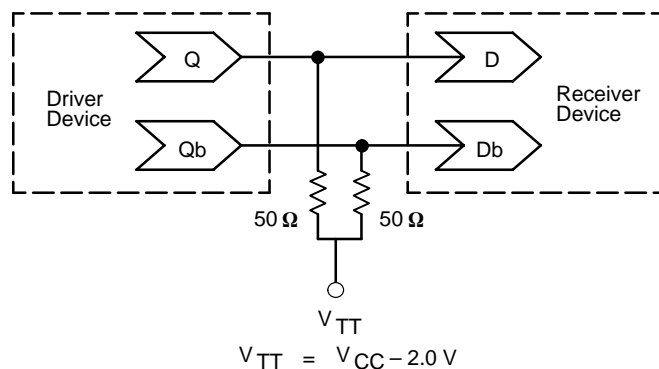


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

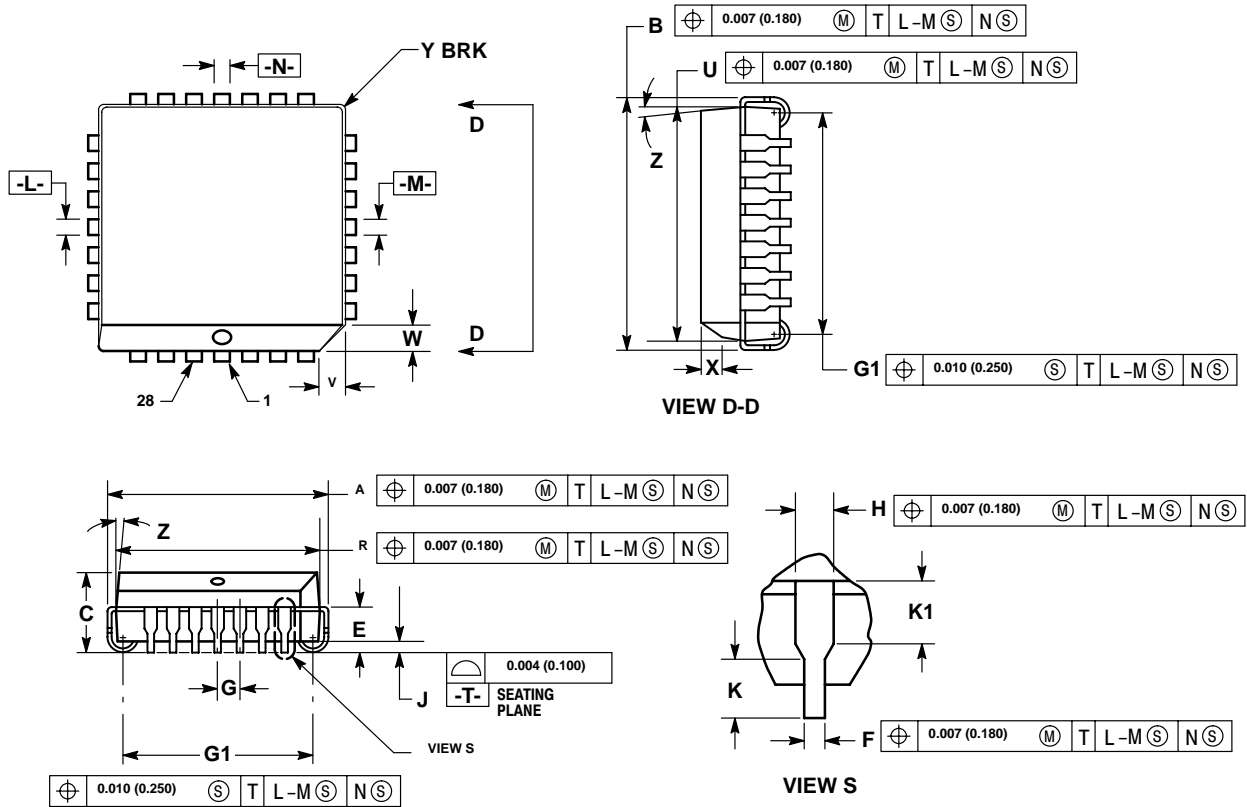
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

Notes

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