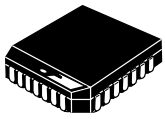
1:6 Differential Clock Distribution Chip

MC10E211
MC100E211

1:6 DIFFERENTIAL CLOCK DISTRIBUTION CHIP



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E/100E211 is a low skew 1:6 fanout device designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal (PECL is an acronym for Positive ECL, PECL levels are ECL levels referenced to +5V rather than ground). If a single-ended input is to be used the V_{BB} pin should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. The V_{BB} supply is designed to act as the switching reference for the input of the E211 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

- Guaranteed Low Skew Specification
- Synchronous Enabling/Disabling
- Multiplexed Clock Inputs
- V_{BB} Output for Single-Ended Use
- Internal 75kΩ Input Pulldown Resistors
- Common and Individual Enable/Disable Control
- High Bandwidth Output Transistors
- Extended 100E V_{EE} Range of –4.2V to –5.46V

The E211 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open in which case it will be pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

Both a common enable and individual output enables are provided. When asserted the positive output will go LOW on the next negative transition of the CLK (or SCLK) input. The enabling function is synchronous so that the outputs will only be enabled/disabled when the outputs are already in the LOW state. In this way the problem of runt pulse generation during the disable operation is avoided. Note that the internal flip flop is clocked on the falling edge of the input clock edge, therefore all associated specifications are referenced to the negative edge of the CLK input.

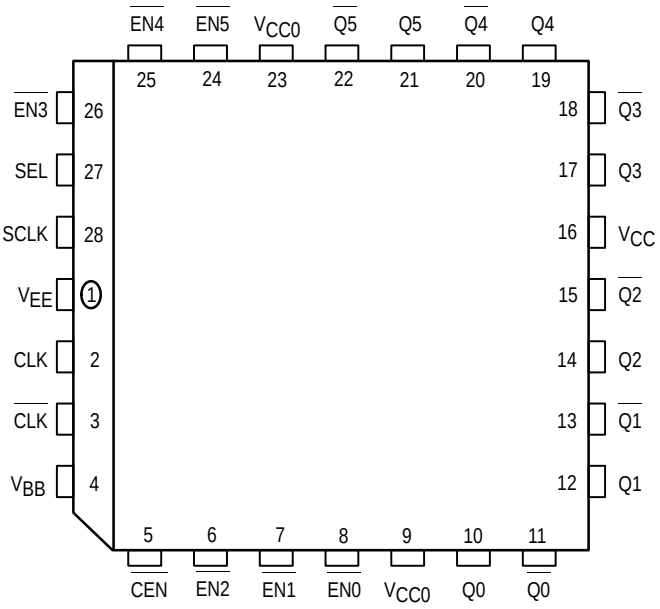
The output transitions of the E211 are faster than the standard ECLinPS™ edge rates. This feature provides a means of distributing higher frequency signals than capable with the E111 device. Because of these edge rates and the tight skew limits guaranteed in the specification, there are certain termination guidelines which must be followed. For more details on the recommended termination schemes please refer to the applications information section of this data sheet.

FUNCTION TABLE

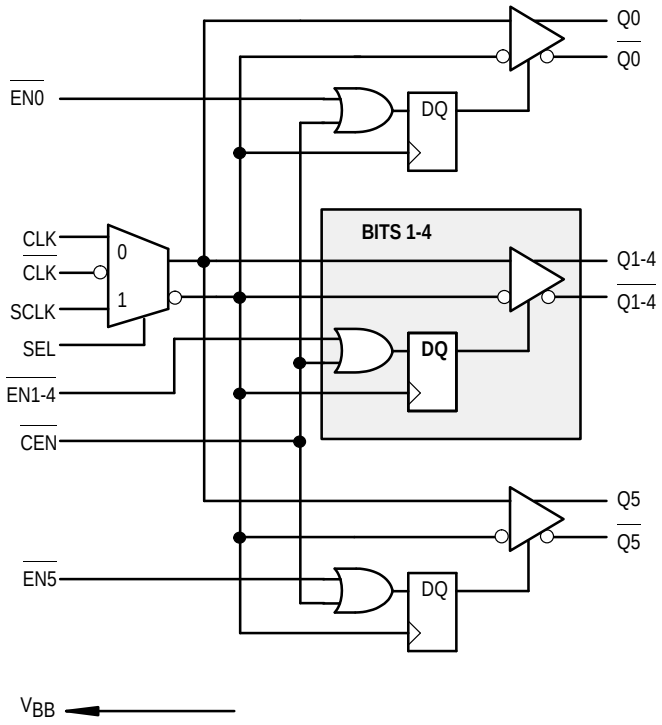
CLK	SCLK	SEL	$\overline{ENx}$	Q
H/L	X	L	L	CLK
X	H/L	H	L	SCLK
Z*	Z*	X	H	L

* Z = Negative transition of CLK or SCLK

ECLinPS is a trademark of Motorola Inc.



Pinout: 28-Lead PLCC (Top View)



Logic Diagram

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Output Reference Voltage	V_{BB}										V	
10E		–1.38		–1.27	–1.35		–1.25	–1.31		–1.19		
100E		–1.38		–1.26	–1.38		–1.26	–1.38		–1.26		
Input High Current	I_{IH}			150			150			150	μA	
Power Supply Current	I_{EE}										mA	
10E			119	160		119	160		119	160		
100E			119	160		119	160		137	164		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Propagation Delay to Output	t_{PLH}										ps	
CLK to Q (Diff)	t_{PHL}	795	930	1065	805	940	1075	825	960	1095		
CLK to Q (SE)		745	930	1115	755	940	1125	775	960	1145		
SCLK to Q		650	900	1085	650	910	1095	650	930	1115		
SEL to Q		745	970	1195	755	980	1205	775	1000	1225		
Disable Time	t_{PHL}										ps	
CLK or SCLK to Q			600	800		600	800		600	800		2
Part–to–Part Skew	t_{skew}										ps	
CLK (Diff) to Q				270			270			270		
CLK (SE), SCLK to Q				370			370			370		
Within-Device Skew			50	75		50	75			75		1
Setup Time	t_s										ps	
ENx to CLK		200	–100		200	–100		200	–100			
CEN to CLK		200	0		200	0		200	0			2
Hold Time	t_h										ps	
CLK to ENx, CEN		900	600		900	160		900	600			2
Minimum Input Swing (CLK)	V_{PP}	0.25		1.0	0.25		1.0	0.25		1.0	V	3
Com. Mode Range (CLK)	V_{CMR}	–0.4		Note	–0.4		Note	–0.4		Note	V	4
Rise/Fall Times	t_r										ps	
20 – 80%	t_f	150		400	150		400	150		400		

1. Within-Device skew is defined for identical transitions on similar paths through a device.
2. Setup, Hold and Disable times are all relative to a falling edge on CLK or SCLK.
3. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.
4. The range in which the high level of the input swing must fall while meeting the V_{PP} spec. The lower end of the range is V_{EE} dependent and can be calculated as V_{EE} + 2.4V.

APPLICATIONS INFORMATION

General Description

The MC10E/100E211 is a 1:6 fanout tree designed explicitly for low skew high speed clock distribution. The device was targeted to work in conjunction with the E111 device to provide another level of flexibility in the design and implementation of clock distribution trees. The individual synchronous enable controls and multiplexed clock inputs make the device ideal as the first level distribution unit in a distribution tree. The device provides the ability to distribute a lower speed scan or test clock along with the high speed system clock to ease the design of system diagnostics and self test procedures. The individual enables could be used to allow for the disabling of individual cards on a backplane in fault tolerant designs.

Because of lower fanout and larger skews the E211 will not likely be used as an alternative to the E111 for the bulk of the clock fanout generation. Figure 1 shows a typical application combining the two devices to take advantage of the strengths of each.

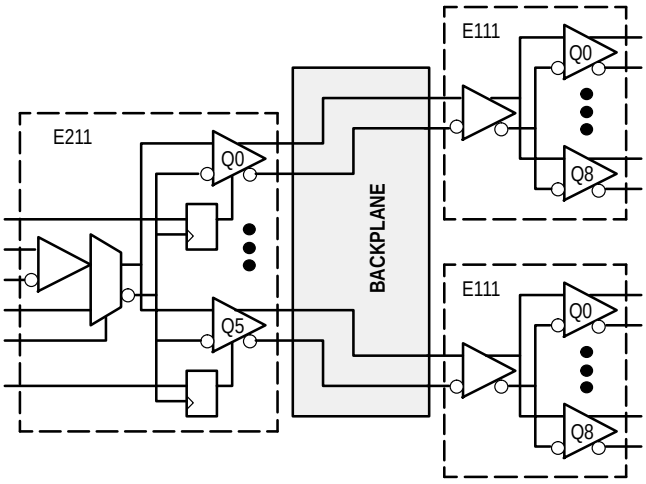


Figure 1. Standard E211 Application

Using the E211 in PECL Designs

The E211 device can be utilized very effectively in designs utilizing only a +5V power supply. Since the internal switching reference levels are biased off of the V_{CC} supply the input thresholds for the single-ended inputs will vary with V_{CC}. As a result the single-ended inputs should be driven by a device on the same board as the E211. Driving these inputs across a backplane where significant differences between the V_{CC}'s of the transmitter and receiver can occur can lead to AC performance and/or significant noise margin degradations. Because the differential I/O does not use a switching reference, and due to the CMR range of the E211, even under worst case V_{CC} situations between cards there will be no AC performance or noise margin loss for the differential CLK inputs.

For situations where TTL clocks are required the E211 can be interfaced with the H641 or H643 ECL to TTL Clock Distribution Chips from Motorola. The H641 is a single supply 1:9 PECL to TTL device while the H643 is a 1:8 dual supply standard ECL to TTL device. By combining the superior skew performance of the E211, or E111, with the low skew translating capabilities of the H641 and H643 very low skew TTL clock distribution networks can be realized.

Handling Open Inputs and Outputs

All of the input pins of the E211 have a 50kΩ to 75kΩ pulldown resistor to pull the input to V_{EE} when left open. This feature can cause a problem if the differential clock inputs are left open as the input gate current source transistor will become saturated. Under these conditions the outputs of the CLK input buffer will go to an undefined state. It is recommended, if possible,that the SCLK input should be selected any time the differential CLK inputs are allowed to float. The SCLK buffer, under open input conditions, will maintain a defined output state and thus the Q outputs of the device will be in a defined state (Q = LOW). Note that if all of the inputs are left open the differential CLK input will be selected and the state of the Q outputs will be undefined.

With the simultaneous switching characteristics and the tight skew specifications of the E211 the handling of the unused outputs becomes critical. To minimize the noise generated on the die all outputs should be terminated in pairs, ie. both the true and compliment outputs should be terminated even if only one of the outputs will be used in the system. With both complimentary pairs terminated the current in the V_{CC} pins will remain essentially constant and thus inductance induced voltage glitches on V_{CC} will not occur. V_{CC} glitches will result in distorted output waveforms and degradations in the skew performance of the device.

The package parasitics of the 28-lead PLCC cause the signals on a given pin to be influenced by signals on adjacent pins. The E211 is characterized and tested with all of the outputs switching, therefore the numbers in the data book are guaranteed only for this situation. If all of the outputs of the E211 are not needed and there is a desire to save power the unused output pairs can be left unterminated. Unterminated outputs can influence the propagation delay on adjacent pins by 15ps - 20ps. Therefore under these conditions this 15ps - 20ps needs to be added to the overall skew of the device. Pins which are separated by a package corner are not considered adjacent pins in the context of propagation delay influence. Therefore as long as all of the outputs on a single side of the package are terminated the specification limits in the data sheet will apply.

APPLICATIONS INFORMATION

Differential versus Single-Ended Use

As can be seen from the data sheet, to minimize the skew of the E211 the device must be used in the differential mode. In the single-ended mode the propagation delays are dependent on the relative position of the V_{BB} switching reference. Any V_{BB} offset from the center of the input swing will add delay to either the T_{PLH} or T_{PHL} and subtract delay from the other. This increase and decrease in delay will lead to an increase in the duty cycle skew and thus part-to-part skew. The within-device skew will be independent of the V_{BB} and therefore will be the same regardless of whether the device is driven differentially or single-endedly.

For applications where part-to-part skew or duty cycle skew are not important the advantages of single-ended clock distribution may lead to its use. Using single-ended interconnect will reduce the number of signal traces to be routed, but remember that all of the complimentary outputs still need to be terminated therefore there will be no reduction in the termination components required. To use the E211 with a single-ended input the arrangement pictured in Figure 2b should be used. If the input to the differential CLK inputs are AC coupled as pictured in Figure 2a the dependence on a centered V_{BB} reference is removed. The situation pictured will ensure that the input is centered around the bias set by the V_{BB}. As a result when AC coupled the AC specification limits for a differential input can be used. For more information on AC coupling please refer to the interfacing section of the design guide in the ECLinPS data book.

Using the Enable Pins

Both the common enable ($\overline{CEN}$) and the individual enables (ENx) are synchronous to the CLK or SCLK input depending on which is selected. The active low signals are clocked into the enable flip flops on the negative edges of the E211 clock inputs. In this way the devices will only be disabled when the outputs are already in the LOW state. The internal propagation delays are such that the delay to the output through the distribution buffers is less than that through the enable flip flops. This will ensure that the disabling of the device will not slice any time off the clock pulse. On initial power up the enable flip flops will randomly attain a stable state, therefore precautions should be taken on initial power up to ensure the E211 is in the desired state.

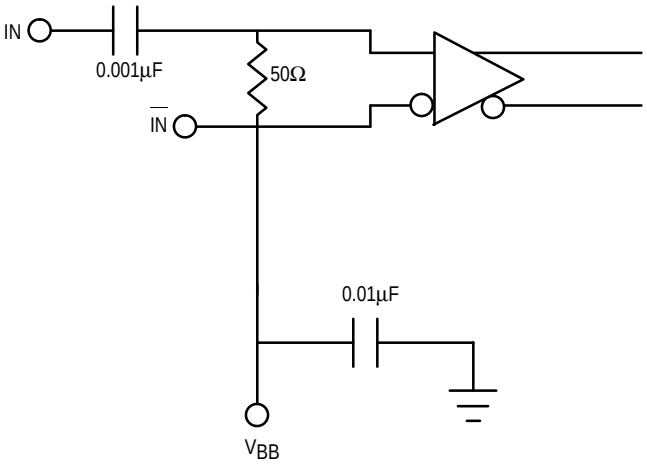


Figure 2a. AC Coupled Input

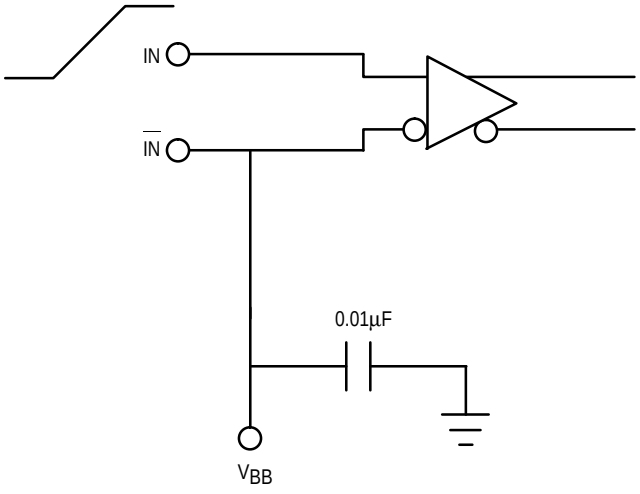
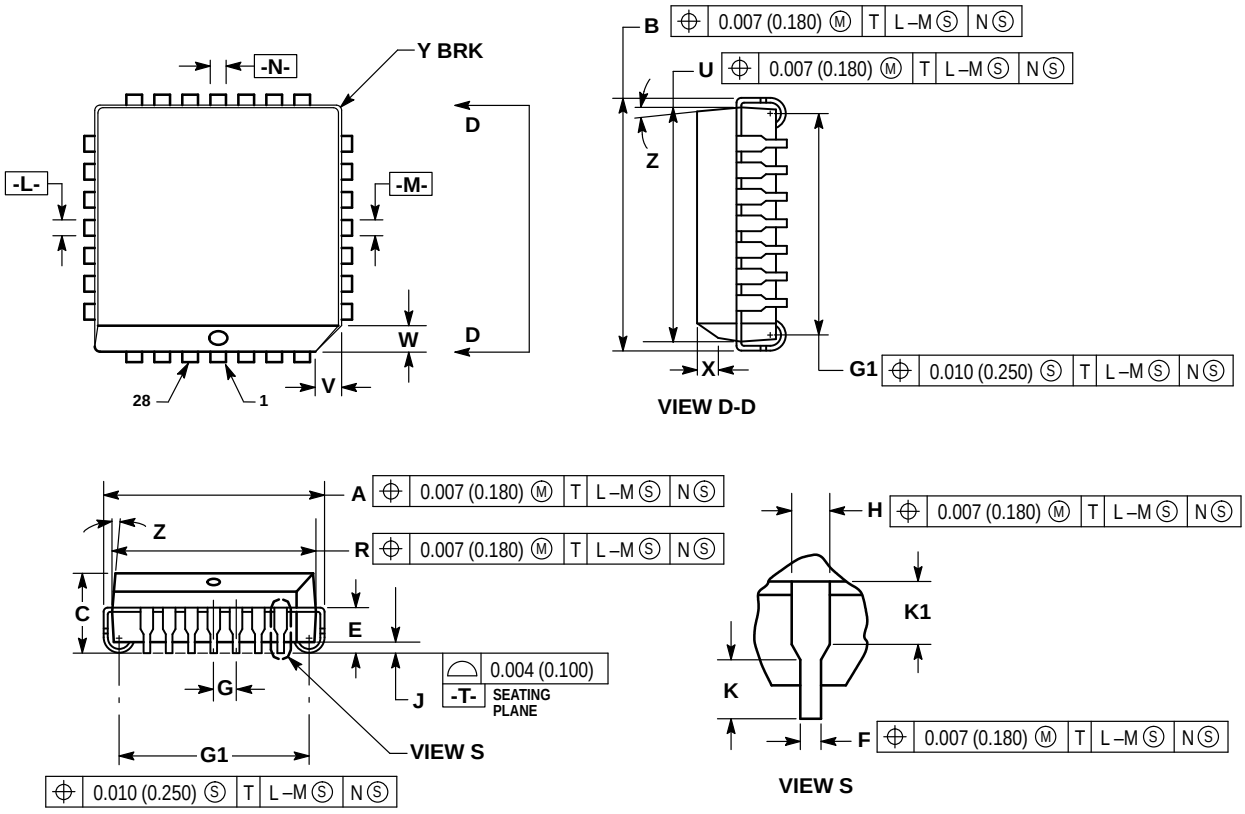


Figure 2b. Single-Ended Input

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298