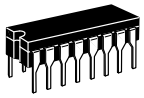
Hex D Master-Slave Flip-Flop With Reset

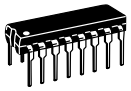
MC10186

The MC10186 contains six high–speed, master slave type “D” flip–flops. Clocking is common to all six flip–flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive–going Clock transition. Thus, outputs may change only on a positive–going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master–slave construction of this device. **A COMMON RESET IS INCLUDED IN THIS CIRCUIT. RESET ONLY FUNCTIONS WHEN CLOCK IS LOW**.

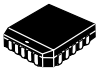
P_D = 460 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_r, t_f = 2.0 ns typ (20%–80%)



L SUFFIX
CERAMIC PACKAGE
CASE 620–10

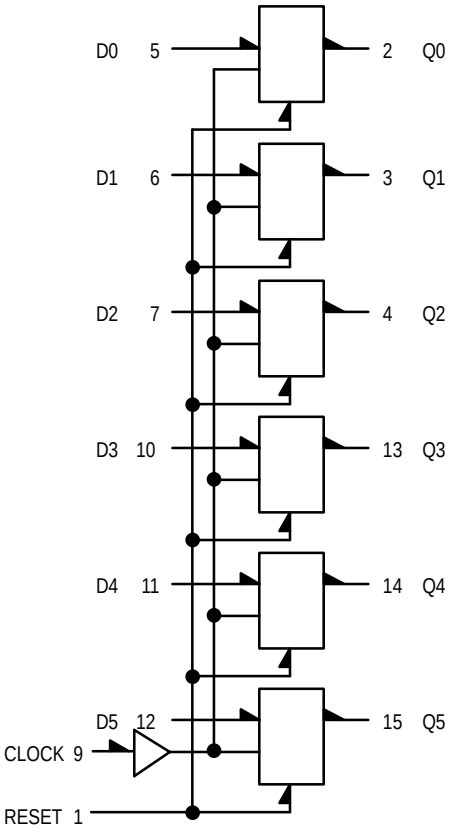


P SUFFIX
PLASTIC PACKAGE
CASE 648–08



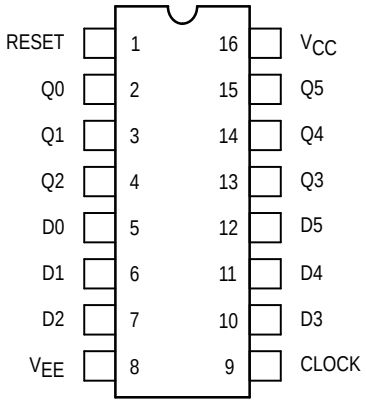
FN SUFFIX
PLCC
CASE 775–02

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

CLOCKED TRUTH TABLE

R	C	D	Qn + 1
L	L	X	Q_n
L	H*	L	L
L	H*	H	H
H	L	X	L

*A clock H is a clock transition from a low to a high state.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		121		88	110		121	mAdc
Input Current	I_{inH}	5 9 1		350 495 920			220 310 575		220 310 575	µAdc
	I_{inL}	5	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2† 15†	–1.060 –1.060	–0.890 –0.890	–0.960 –0.960		–0.810 –0.810	–0.890 –0.890	–0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2† 15†	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2† 15†	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2† 15†		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{1+3-} t_{1+4-} t_{9+2+} t_{9+2-}	3 4 2 2	1.6 1.6 1.6 1.6	4.6 4.6 4.6 4.6	1.6 1.6 1.6 1.6	2.5 2.5 3.5 3.5	4.5 4.5 4.5 4.5	1.6 1.6 1.6 1.6	5.0 5.0 5.0 5.0	
Rise Time (20 to 80%)	t_{2+}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4	
Fall Time (20 to 80%)	t_{2-}	2	1.0	4.1	1.1	1.8	4.0	1.1	4.4	
Setup Time	t_{setup}	2	2.5		2.5	2.5		2.5		ns
Hold Time	t_{hold}	2	1.5		1.5	–1.5		1.5		ns
Toggle Frequency (Max)	f_{tog}	2	125		125	150		125		MHz

† Output level to be measured after clock pulse. V_{IL} ⟋ V_{IH} appears at clock input (Pin 9).

ELECTRICAL CHARACTERISTICS (continued)

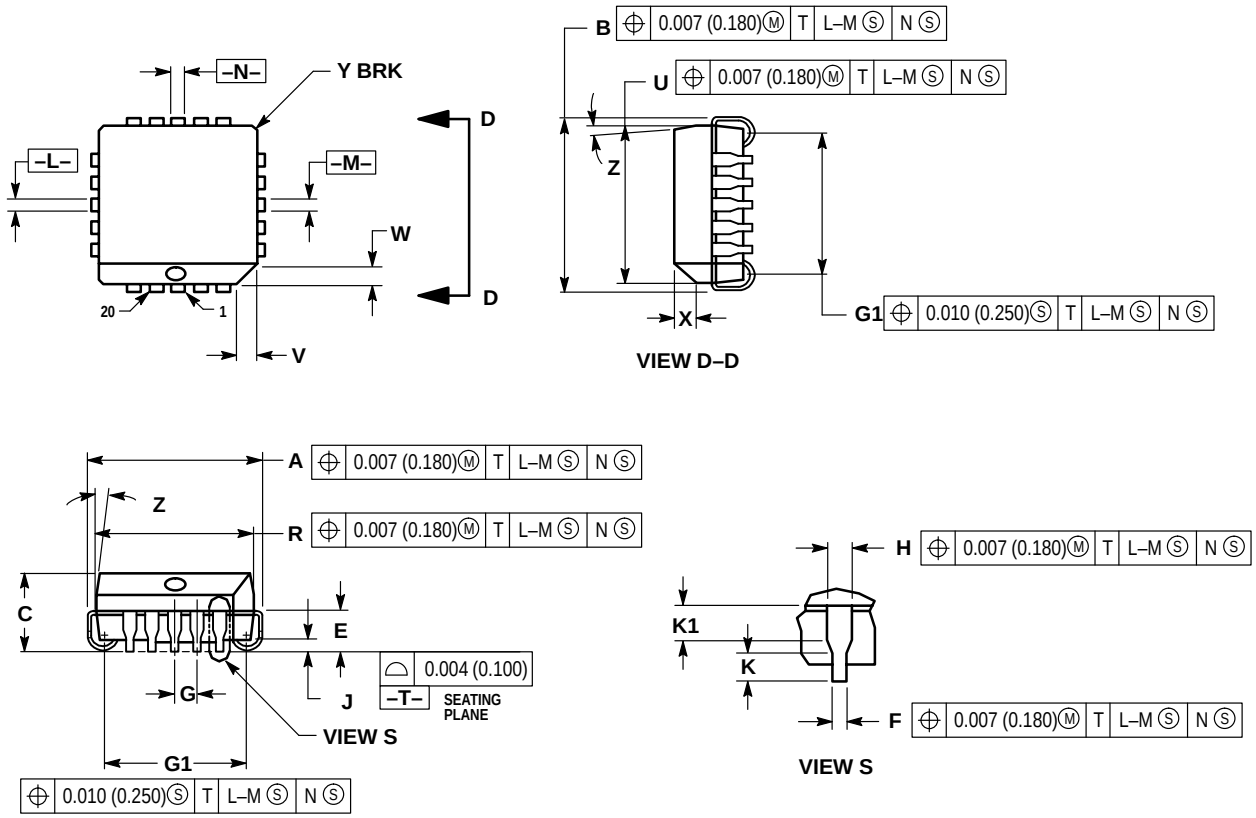
				TEST VOLTAGE VALUES (Volts)					
			@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
			–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
			+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
			+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	16
Input Current		I_{inH}	5 9 1	5 9 1				8 8 8	16 16 16
		I_{inL}	5		5			8	16
Output Voltage	Logic 1	V_{OH}	2† 15†	5 12				8 8	16 16
Output Voltage	Logic 0	V_{OL}	2† 15†		5 12			8 8	16 16
Threshold Voltage	Logic 1	V_{OHA}	2† 15†			5 12		8 8	16 16
Threshold Voltage	Logic 0	V_{OLA}	2† 15†				5 12	8 8	16 16
Switching Times	(50Ω Load)			**+1.11Vdc**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay		t_{1+3-} t_{1+4-} t_{9+2+} t_{9+2-}	3 4 2 2	6 7		1, 9 1, 9 5, 9 5, 9	3 4 2 2	8 8 8 8	16 16 16 16
Rise Time	(20 to 80%)	t_{2+}	2			5, 9	2	8	16
Fall Time	(20 to 80%)	t_{2-}	2			5, 9	2	8	16
Setup Time		t_{setup}	2			5, 9	2	8	16
Hold Time		t_{hold}	2			5, 9	2	8	16
Toggle Frequency (Max)		f_{tog}	2					8	16

† Output level to be measured after clock pulse. V_{IL} ⟋ V_{IH} appears at clock input (Pin 9).

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

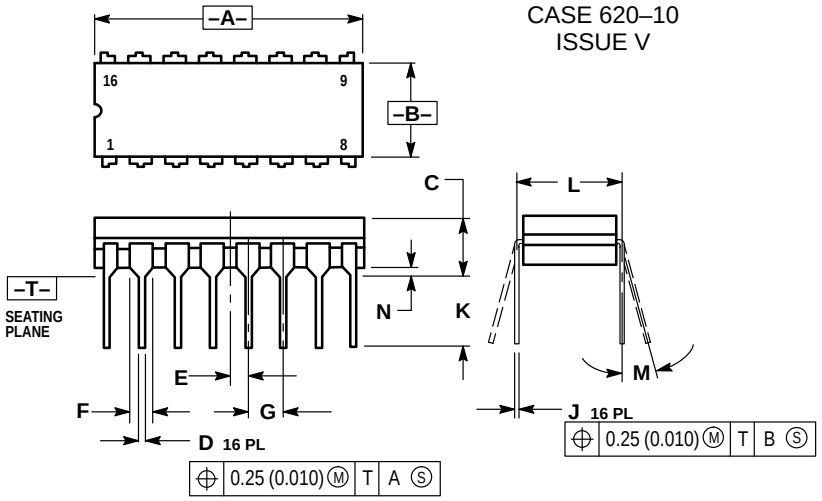


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS

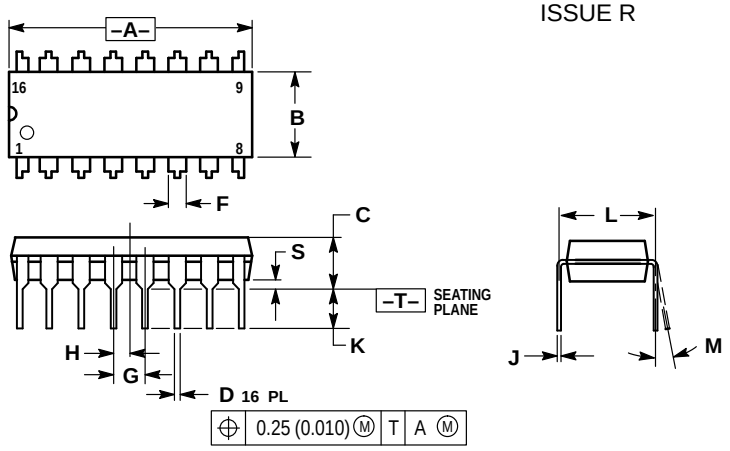
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298