Hex D Master-Slave Flip-Flop

Description

The MC10H176 contains six master slave type D flip-flops with a common clock. This MECL $10H^{\text{TM}}$ part is a functional/pinout duplication of the standard MECL $10K^{\text{TM}}$ family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

Features

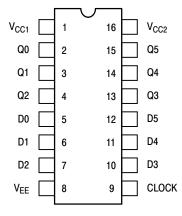
- Propagation Delay, 1.7 ns Typical
- Power Dissipation, 460 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

CLOCKED TRUTH TABLE

С	Q	Q _{n+1}
L	Х	Q _n
H *	L	L
H *	Н	Н

* A clock H is a clock transition from a low to a high state.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



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PDIP-16 P SUFFIX CASE 648-02

MARKING DIAGRAMS*



A = Assembly Location

WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G = Pb-Free Package

*For additional marking information, refer to Application Note <u>AND8002/D</u>.

ORDERING INFORMATION

Device	Package	Shipping
MC10H176PG	PDIP-16 (Pb-Free)	25 Units/Tube

Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V _{CC} = 0)	-8.0 to 0	Vdc
VI	Input Voltage (V _{CC} = 0)	0 to V _{EE}	Vdc
l _{out}	Output Current Continuous Surge	50 100	mA
T _A	Operating Temperature Range	0 to +75	°C
T _{stg}	Storage Temperature Range Plastic Ceramic	-55 to +150 -55 to +165	°C

Table 2. ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V \pm 5%) (Note 1)

		C	0	25	5°	7	75°	
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
Ι _Ε	Power Supply Current	_	123	-	112	-	123	mA
I _{inH}	Input Current High Pins 5,6,7,10,11,12 Pin 9	- -	425 670	- -	265 420	-	265 420	μΑ
I _{inL}	Input Current Low	0.5	-	0.5	-	0.3	-	μΑ
V _{OH}	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V _{OL}	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V _{IL}	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

^{1.} Each MECL 10H™ series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

Table 3. AC PARAMETERS

t _{pd}	Propagation Delay	0.9	2.1	0.9	2.2	1.0	2.4	ns
t _{set}	Set-up Time	1.5	-	1.5	-	1.5	-	ns
t _{hold}	Hold Time	0.9	-	0.9	-	1.0	-	ns
t _r	Rise Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
t _f	Fall Time	0.5	1.8	0.5	1.9	0.5	2.0	ns
f _{tog}	Toggle Frequency	250	-	250	-	250	-	MHz

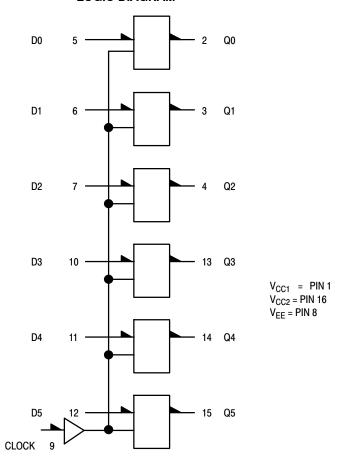
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

APPLICATION INFORMATION

The MC10H176 contains six high-speed, master slave type "D" flip-flops. Data is entered into the master when the clock is low. Master-to-slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change

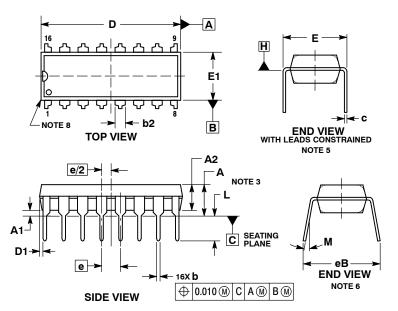
only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

LOGIC DIAGRAM



PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 **ISSUE V**



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
- DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
 DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
- PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C
- DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
 DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
- LEADS, WHERE THE LEADS EXIT THE BODY.
 PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
- CORNERS)

	INC	HES	MILLIMETER		
DIM	MIN	MAX	MIN	MAX	
Α		0.210		5.33	
A1	0.015		0.38		
A2	0.115	0.195	2.92	4.95	
b	0.014	0.022	0.35	0.56	
b2	0.060 TYP		1.52 TYP		
С	0.008	0.014	0.20	0.36	
D	0.735	0.775	18.67	19.69	
D1	0.005		0.13		
E	0.300	0.325	7.62	8.26	
E1	0.240	0.280	6.10	7.11	
е	0.100 BSC		2.54	BSC	
eB		0.430		10.92	
L	0.115	0.150	2.92	3.81	
М		10°		10°	

STYLE 1:		STYLE 2	:
PIN 1.	CATHODE	PIN 1.	COMMON DRAIN
2.	CATHODE	2.	COMMON DRAIN
3.	CATHODE	3.	COMMON DRAIN
4.	CATHODE	4.	COMMON DRAIN
5.	CATHODE	5.	COMMON DRAIN
6.	CATHODE	6.	COMMON DRAIN
7.	CATHODE	7.	COMMON DRAIN
8.	CATHODE	8.	COMMON DRAIN
9.	ANODE	9.	GATE
10.	ANODE	10.	SOURCE
11.	ANODE	11.	GATE
12.	ANODE	12.	SOURCE
13.	ANODE	13.	GATE
14.	ANODE	14.	SOURCE
15.	ANODE	15.	GATE
16.	ANODE	16.	SOURCE

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