

MC10H181

4-Bit Arithmetic Logic Unit/ Function Generator

The MC10H181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (PG) and carry generate (GG) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10H179, full-carry look-ahead, as a second order look-ahead block, the MC10H181 provides high-speed arithmetic operations on very long words.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and no increase in power supply current.

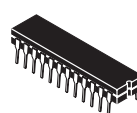
- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K – Compatible



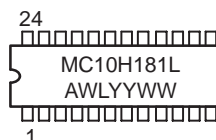
ON Semiconductor

<http://onsemi.com>

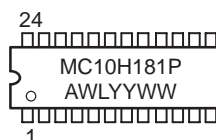
MARKING DIAGRAMS



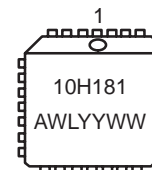
CDIP-24
L SUFFIX
CASE 758



PDIP-24
P SUFFIX
CASE 724



PLCC-28
FN SUFFIX
CASE 776



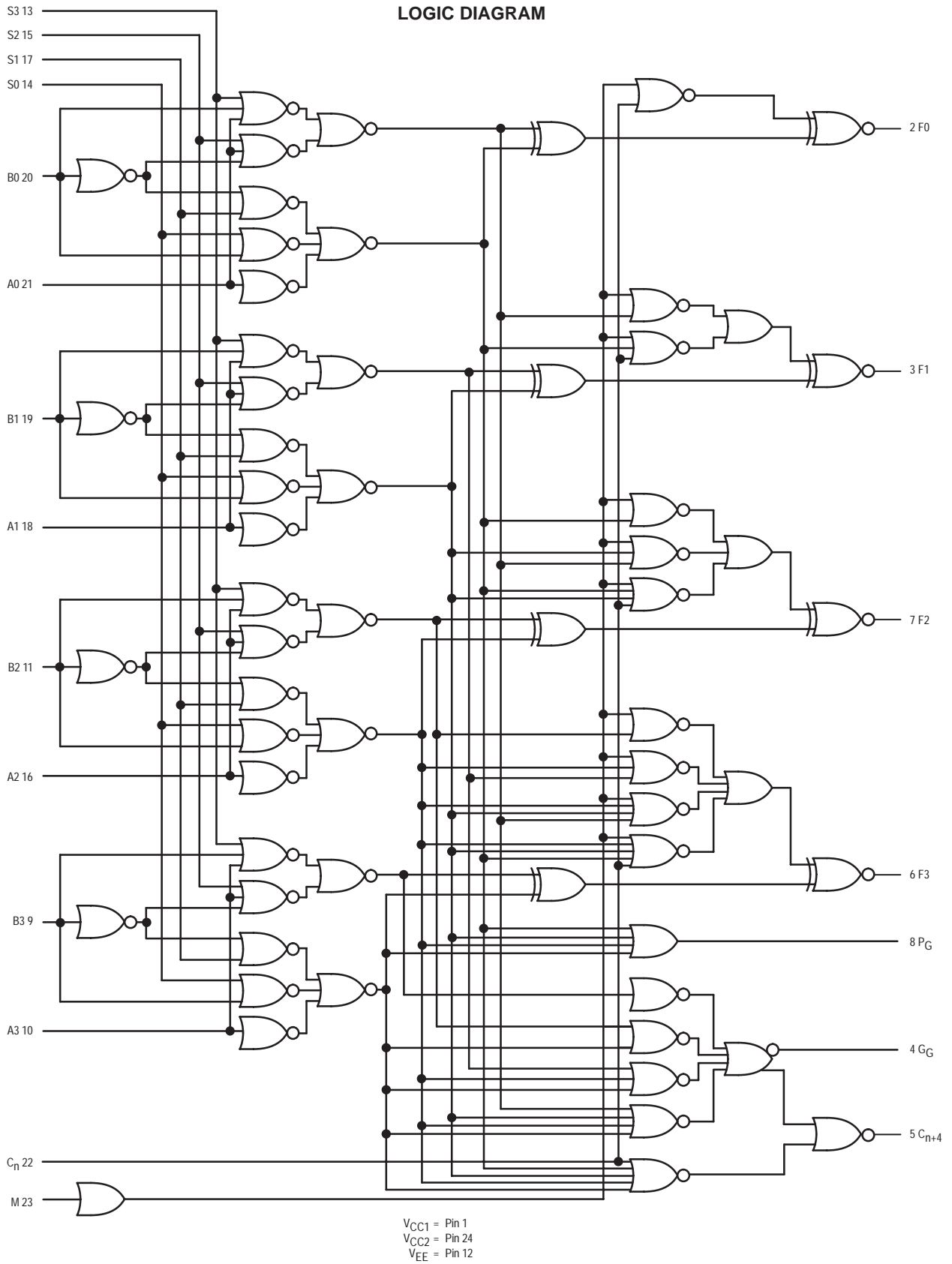
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H181L	CDIP-24	15 Units/Rail
MC10H181P	PDIP-24	15 Units/Rail
MC10H181FN	PLCC-28	37 Units/Rail

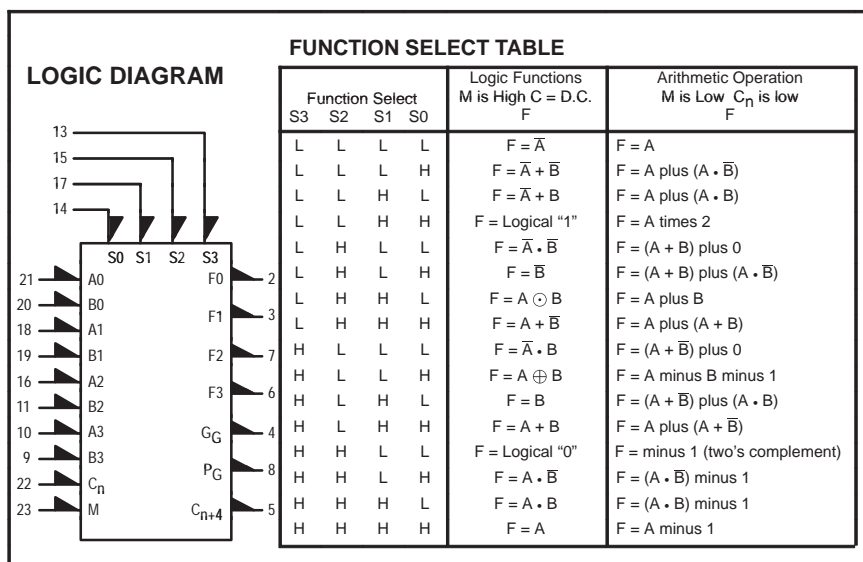
MC10H181

LOGIC DIAGRAM

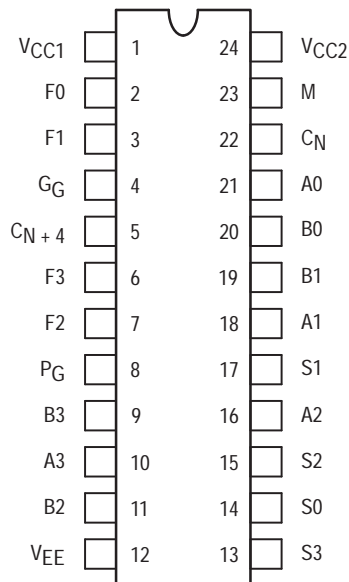


V_{CC1} = Pin 1
V_{CC2} = Pin 24
V_{EE} = Pin 12

MC10H181



DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18
of the ON Semiconductor MECL Data Book (DL122/D).

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply ($V_{CC} = 0$)	-8.0 to 0	Vdc
V_I	Input Voltage ($V_{CC} = 0$)	0 to V_{EE}	Vdc
I_{out}	Output Current - Continuous - Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range - Plastic - Ceramic	-55 to +150 -55 to +165	°C

MC10H181

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2\text{ V} \pm 5.0\%$) (See Note 1.)

Characteristic	Symbol	0°		+25°		+75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	–	159	–	145	–	159	mA
Input Current High Pin 22 Pins 14,23 Pins 13,15,17 Pins 10,16,18,21 Pins 9,11,19,20	I_{inH}	–	720	–	450	–	450	μA
Input Current Low Pins 9–11, 13–22	I_{inL}	0.5	–	0.5	–	0.3	–	μA
High Output Voltage	V_{OH}	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
Low Output Voltage	V_{OL}	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
High Input Voltage	V_{IH}	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
Low Input Voltage	V_{IL}	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts.

AC PARAMETERS

Characteristic	Symbol	Input	Output	Conditions †	AC Switching Characteristics						Unit
					0°C		+25°C		+75°C		
					Min	Max	Min	Max	Min	Max	
Propagation Delay Rise Time, Fall Time	t_{+}, t_{-} t_{+}, t_{-}	C_n C_n	C_{n+4} C_{n+4}	A0,A1,A2,A3 A0,A1,A2,A3	0.7 0.6	2.0 2.0	0.7 0.6	2.0 2.0	0.7 0.7	2.2 2.2	ns ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{-} t_{-}, t_{-} t_{+}, t_{-}	C_n C_n C_n	F1 F1 F1	A0	1.0 0.7	3.0 2.2	1.0 0.7	3.0 2.2	1.2 0.7	3.3 2.4	ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{-} t_{-}, t_{-} t_{+}, t_{-}	A1 A1 A1	F1 F1 F1		1.5 0.7	3.7 2.0	1.5 0.7	3.7 2.0	1.6 0.7	4.0 2.2	ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{-} t_{+}, t_{-}	A1 A1	P_G P_G	S0,S3 S0,S3	1.5 0.9	3.7 2.4	1.5 0.9	3.7 2.4	1.6 0.9	4.0 2.6	ns ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{-} t_{+}, t_{-}	A1 A1	G_G G_G	A0,A2,A3, C_n A0,A2,A3, C_n	1.5 0.7	3.7 2.2	1.5 0.7	3.7 2.2	1.6 0.7	3.9 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t_{-}, t_{+} t_{+}, t_{-}	A1 A1	C_{n+4} C_{n+4}	A0,A2,A3, C_n A0,A2,A3, C_n	1.5 0.5	3.6 2.0	1.5 0.5	3.6 2.0	1.6 0.5	3.9 2.2	ns ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{+} t_{+}, t_{-}	B1 B1	F1 F	S3, C_n S3, C_n	2.0 0.7	4.5 2.3	2.0 0.7	4.5 2.3	2.1 0.7	4.8 2.5	ns ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{-} t_{+}, t_{-}	B1 B1	P_G P_G	S0,A1 S0,A1	1.5 0.7	3.8 2.2	1.5 0.7	3.8 2.2	1.6 0.7	4.0 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{-} t_{+}, t_{-}	B1 B1	G_G G_G	S3, C_n S3, C_n	1.5 0.7	3.7 2.2	1.5 0.7	3.7 2.2	1.6 0.7	4.0 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t_{-}, t_{+} t_{+}, t_{-}	B1 B1	C_{n+4} C_{n+4}	S3, C_n S3, C_n	2.0 0.5	4.0 2.0	2.0 0.5	4.0 2.2	2.1 0.5	4.3 2.2	ns ns
Propagation Delay Rise Time, Fall Time	t_{+}, t_{+} t_{+}, t_{-}	M M	F1 F1	– –	1.5 0.8	4.2 2.3	1.5 0.8	4.2 2.3	1.6 0.8	4.5 2.5	ns ns
Propagation Delay Rise Time, Fall Time	t_{-}, t_{+} t_{+}, t_{-}	S1 S1	F1 F1	A1,B1 A1,B1	1.5 0.7	4.5 2.0	1.5 0.7	4.5 2.0	1.6 0.7	4.8 2.2	ns ns
Propagation Delay Rise Time, Fall Time	t_{-}, t_{-} t_{+}, t_{-}	S1 S1	P_G P_G	A3,B3 A3,B3	1.5 0.7	4.0 2.0	1.5 0.7	4.0 2.2	1.6 0.7	4.3 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t_{-}, t_{+} t_{+}, t_{-}	S1 S1	C_{n+4} C_{n+4}	A3,B3 A3,B3	1.5 0.7	4.1 2.2	1.5 0.7	4.1 2.2	1.6 0.7	4.4 2.4	ns ns
Propagation Delay Rise Time, Fall Time	t_{-}, t_{+} t_{+}, t_{-}	S1 S1	G_G G_G	A3,B3 A3,B3	1.3 0.5	4.5 3.2	1.3 0.5	4.5 3.2	1.4 0.5	4.8 3.4	ns ns

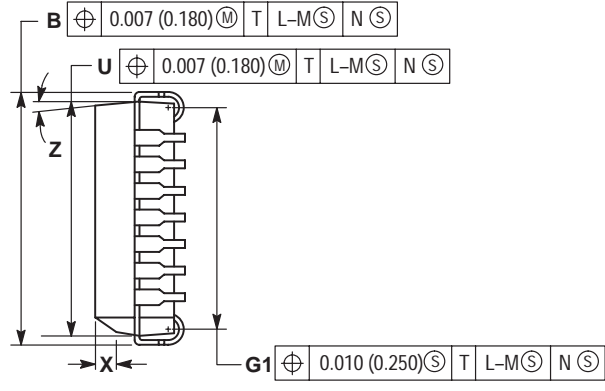
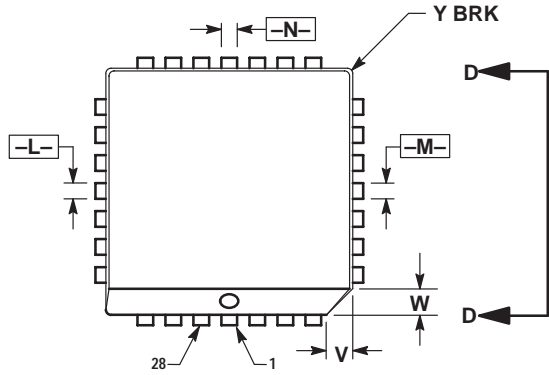
† Logic high level (+1.11 Vdc) applied to pins listed. All other input pins are left floating or tied to +0.31 Vdc.

$V_{CC1} = V_{CC2} = +2.0\text{ Vdc}$, $V_{EE} = -3.2\text{ Vdc}$

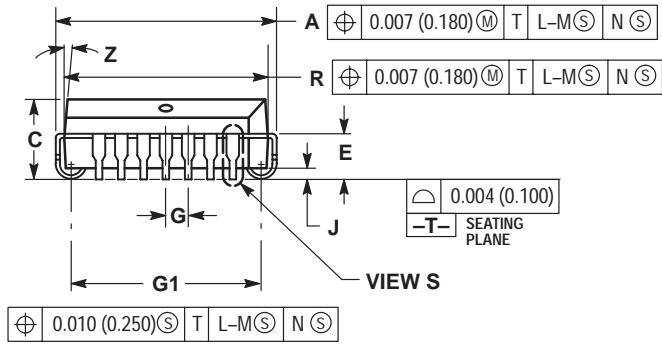
MC10H181

PACKAGE DIMENSIONS

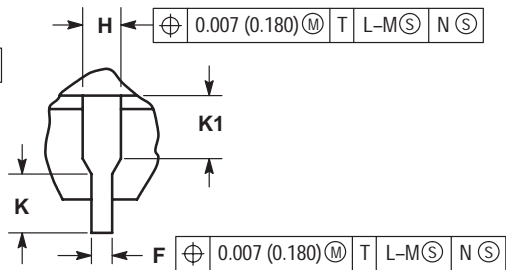
PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE D



VIEW D-D



VIEW S



VIEW S

NOTES:

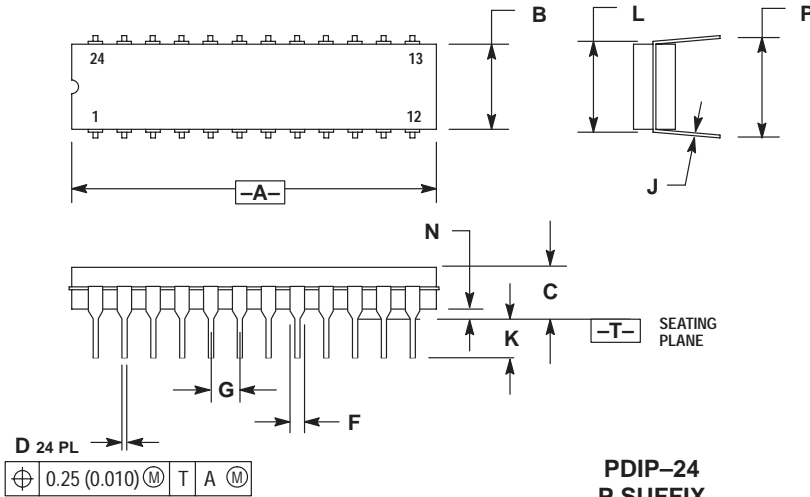
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

MC10H181

PACKAGE DIMENSIONS

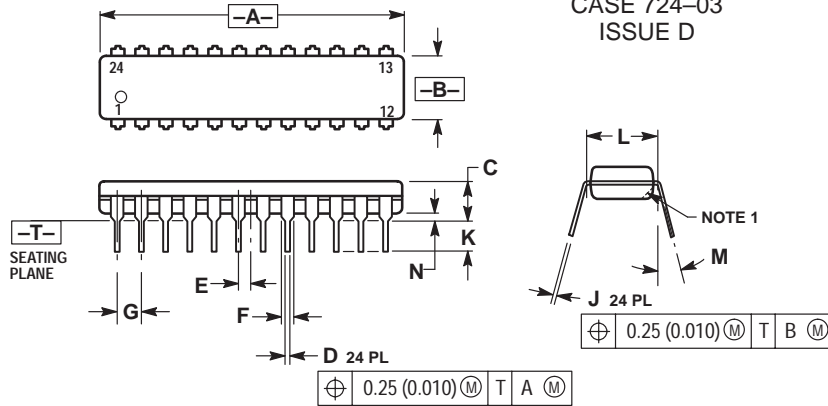
CDIP-24 L SUFFIX CERAMIC DIP PACKAGE CASE 758-02 ISSUE A



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.240	1.285	31.50	32.64
B	0.285	0.305	7.24	7.75
C	0.160	0.200	4.07	5.08
D	0.015	0.021	0.38	0.53
F	0.045	0.062	1.14	1.57
G	0.100 BSC		2.54 BSC	
J	0.008	0.013	0.20	0.33
K	0.100	0.165	2.54	4.19
L	0.300	0.310	7.62	7.87
N	0.020	0.050	0.51	1.27
P	0.360	0.400	9.14	10.16


PDIP-24 P SUFFIX PLASTIC DIP PACKAGE CASE 724-03 ISSUE D



- NOTES:
 1. CHAMFERED CONTOUR OPTIONAL.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

North America Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 2:30pm to 5:00pm Munich Time)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (M-F 2:30pm to 5:00pm Toulouse Time)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (M-F 1:30pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong 800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

Phone: 81-3-5740-2745
Email: r14525@onsemi.com

Fax Response Line: 303-675-2167
800-344-3810 Toll Free USA/Canada

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local
Sales Representative.