



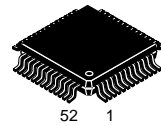
# MC13109

## Universal Cordless Telephone Subsystem IC

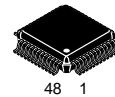
The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compaander
  - Expander Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT-1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14-Bit Programmable Counter and 2nd LO with 12-Bit Counter
  - Transmit Section Contains Phase Detector and 14-Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One-Third the Power Consumption of Competing Devices
- AN1575: Refer to Application Note for a List of “Worldwide Cordless Telephone Frequencies” (Chapter 8 Addendum of DL128 Data Book)

### UNIVERSAL CT-1 SUBSYSTEM INTEGRATED CIRCUIT



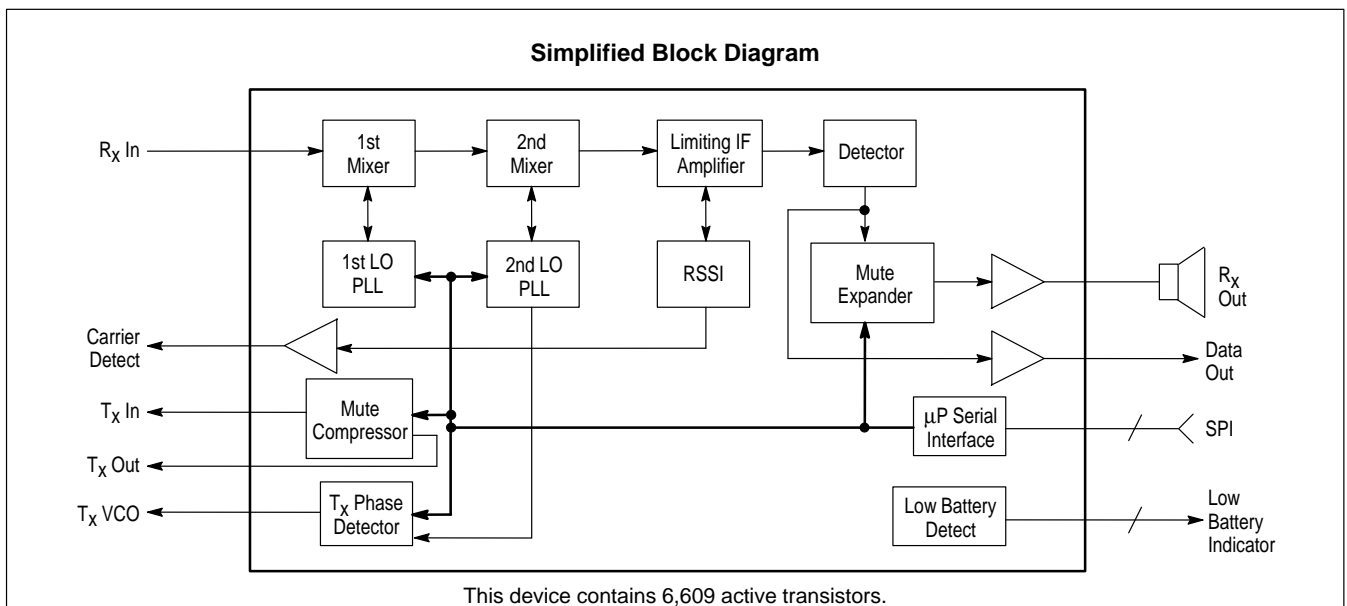
**FB SUFFIX**  
PLASTIC PACKAGE  
CASE 848B  
(QFP-52)



**FTA SUFFIX**  
PLASTIC PACKAGE  
CASE 932  
(Thin QFP)

#### ORDERING INFORMATION

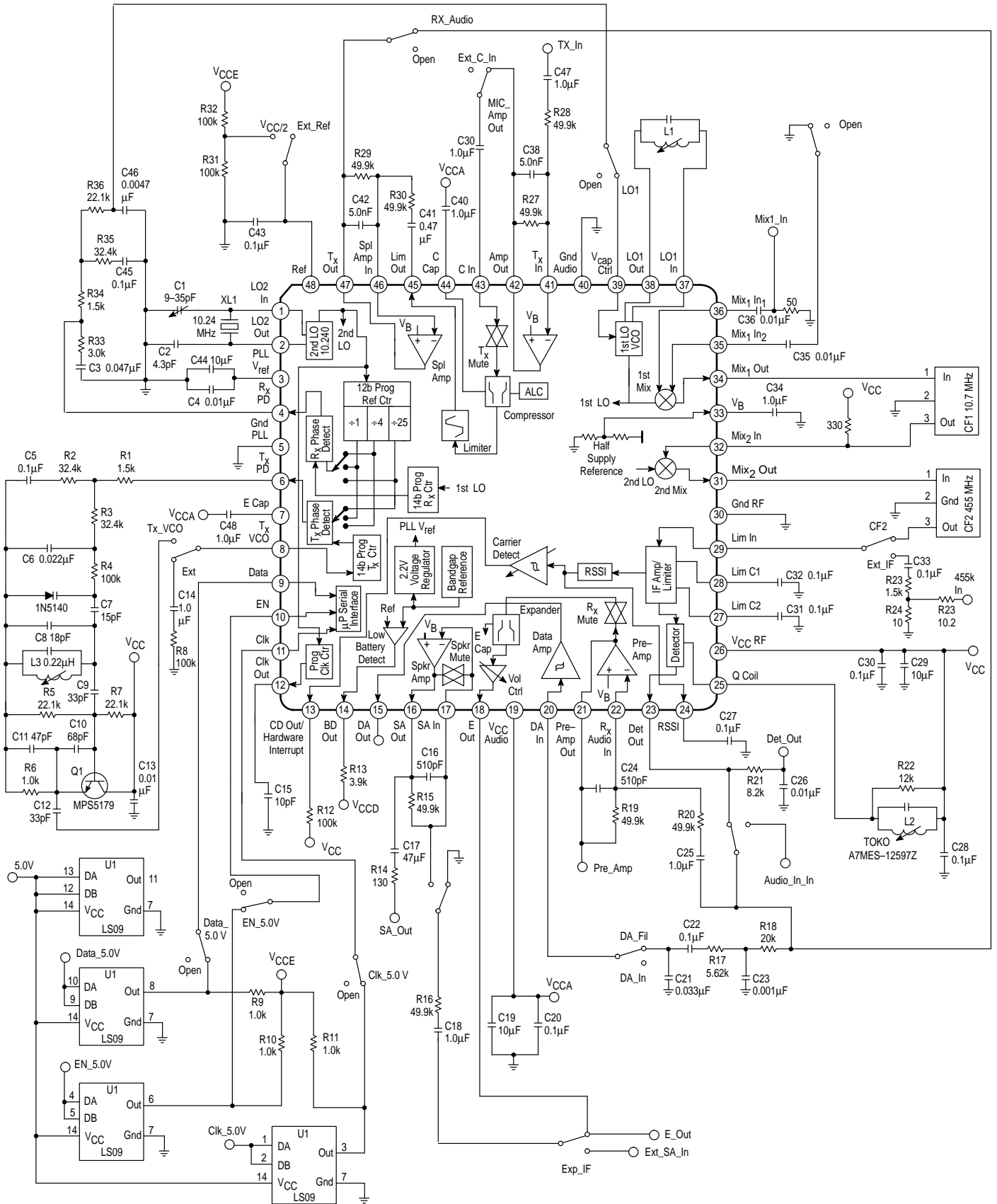
Device	Tested Operating Temperature Range	Package
MC13109FB	T <sub>A</sub> = -20° to +85°C	QFP-52
MC13109FTA		TQFP-48





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Figure 2. MC13109FTA Test Circuit



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## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	-0.5 to +5.5	Vdc
Junction Temperature	$T_J$	-65 to +150	°C

**NOTE:** 1. Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.  
2. ESD data available upon request.

## RECOMMENDED OPERATING CONDITIONS

Characteristic	Min	Typ	Max	Unit
$V_{CC}$	2.0	-	5.5	Vdc
Operating Ambient Temperature	-20	-	85	°C

**NOTE:** All limits are not necessarily functional concurrently.

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.6$  V,  $T_A = 25^\circ\text{C}$ , RF In = 46.61 MHz,  $f_{DEV} = \pm 3.0$  kHz,  $f_{mod} = 1.0$  kHz; Test Circuit Figure 1.)

Characteristic	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>				
Static Current				
Active Mode ( $V_{CC} = 2.6$ V)	-	6.7	12	mA
Active Mode ( $V_{CC} = 3.6$ V)	-	7.1	-	mA
Receive Mode ( $V_{CC} = 2.6$ V)	-	4.3	7.0	mA
Receive Mode ( $V_{CC} = 3.6$ V)	-	4.5	-	mA
Standby Mode ( $V_{CC} = 2.6$ V)	-	300	600	$\mu\text{A}$
Standby Mode ( $V_{CC} = 3.6$ V)	-	600	-	$\mu\text{A}$
Inactive Mode ( $V_{CC} = 2.6$ V)	-	40	80	$\mu\text{A}$
Inactive Mode ( $V_{CC} = 3.6$ V)	-	56	-	$\mu\text{A}$

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### ELECTRICAL CHARACTERISTICS (continued)

#### FM Receiver

The FM receivers can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25

channel U.S., without the need for any external switching circuitry (see Figure 29).

(Test Conditions:  $V_{CC} = 2.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $f_O = 46.61\text{ MHz}$ ,  $f_{DEV} = \pm 3.0\text{ kHz}$ ,  $f_{mod} = 1.0\text{ kHz}$ .)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Sensitivity (Input for 12 dB SINAD)	Matched Impedance Differential Input	Mix <sub>1</sub> In <sub>1/2</sub>	Det Out	V <sub>SIN</sub>	–	0.7	–	μVrms
1st Mixer Conversion Gain	V <sub>in</sub> = 1.0 mVrms, with CF <sub>1</sub> Load	Mix <sub>1</sub> In <sub>1/2</sub>	CF <sub>1</sub>	MX <sub>gain1</sub>	–	10	–	dB
2nd Mixer Conversion Gain	V <sub>in</sub> = 3.0 mVrms, with CF <sub>2</sub> Load	Mix <sub>2</sub> In	CF <sub>2</sub>	MX <sub>gain2</sub>	–	20	–	dB
1st and 2nd Mixer Gain Total	V <sub>in</sub> = 1.0 mVrms, with CF <sub>1</sub> and CF <sub>2</sub> Load	Mix <sub>1</sub> In <sub>1/2</sub>	CF <sub>2</sub>	MX <sub>gainT</sub>	24	30	–	dB
1st Mixer Input Impedance	–	–	Mix <sub>1</sub> In <sub>1</sub> Mix <sub>1</sub> In <sub>2</sub>	Z <sub>in1</sub>	–	1.0	–	kΩ
2nd Mixer Input Impedance	–	–	Mix <sub>2</sub> In	Z <sub>in2</sub>	–	3.0	–	kΩ
1st Mixer Output Impedance	–	–	Mix <sub>1</sub> Out	Z <sub>out1</sub>	–	330	–	Ω
2nd Mixer Output Impedance	–	–	Mix <sub>2</sub> Out	Z <sub>out2</sub>	–	1.5	–	kΩ
IF –3.0 dB Limiting Sensitivity	f <sub>in</sub> = 455 kHz	Lim In	Det Out	IF Sens	–	55	–	μVrms
Total Harmonic Distortion (CCITT Filter)	With R <sub>C</sub> = 8.2 kΩ/ 0.01 μF Filter at Det Out	Mix <sub>1</sub> In <sub>1/2</sub>	Det Out	THD	–	0.7	–	%
Recovered Audio	With R <sub>C</sub> = 8.2 kΩ/ 0.01 μF Filter at Det Out	Mix <sub>1</sub> In <sub>1/2</sub>	Det Out	AFO	80	100	154	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V <sub>in</sub> = 10 mVrms, R <sub>C</sub> = 8.2 kΩ/0.01 μF	Mix <sub>1</sub> In <sub>1/2</sub>	Det Out	SN	–	49	–	dB
AM Rejection Ratio	30% AM, V <sub>in</sub> = 10 mVrms, R <sub>C</sub> = 8.2 kΩ/0.001 μF	Mix <sub>1</sub> In <sub>1/2</sub>	Det Out	AMR	–	37	–	dB
First Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix <sub>1</sub> In <sub>1/2</sub>	Mix <sub>1</sub> Out	TOI <sub>mix1</sub>	–	–10	–	dBm
Second Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix <sub>2</sub> In	Mix <sub>2</sub> Out	TOI <sub>mix2</sub>	–	–27	–	dBm
Detector Output Impedance	–	–	Det Out	Z <sub>O</sub>	–	870	–	Ω

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### ELECTRICAL CHARACTERISTICS (continued)

#### RSSI/Carrier Detect

Connect 0.01  $\mu\text{F}$  to Gnd from “RSSI” output pin to form the carrier detect filter. “CD Out” is an open collector output which requires an external 100 k $\Omega$  pull-up resistor to  $V_{\text{CC}}$ .

The carrier detect threshold is programmable through the MPU interface.

( $R_{\text{L}} = 100 \text{ k}\Omega$ ,  $V_{\text{CC}} = 2.6 \text{ V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$ .)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI Output Current Dynamic Range	–	Mix <sub>1</sub> In	RSSI	RSSI	–	65	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix <sub>1</sub> In	CD Out	$V_{\text{T}}$	–	22.5	–	$\mu\text{Vrms}$
Hysteresis	–	Mix <sub>1</sub> In	CD Out	Hys	–	2.0	–	dB
Output High Voltage	$V_{\text{in}} = 0 \mu\text{Vrms}$ , $R_{\text{L}} = 100 \text{ k}\Omega$ , CD = (10100)	Mix <sub>1</sub> In	CD Out	$V_{\text{OH}}$	$V_{\text{CC}} - 0.1$	2.6	–	V
Output Low Voltage	$V_{\text{in}} = 100 \mu\text{Vrms}$ , $R_{\text{L}} = 100 \text{ k}\Omega$ , CD = (10100)	Mix <sub>1</sub> In	CD Out	$V_{\text{OL}}$	–	0.01	0.4	V
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	$V_{\text{Trange}}$	–20	–	11	dB
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	$V_{\text{Tn}}$	–	32	–	–

#### Data Amp Comparator (see Figure 4)

Inverting hysteresis comparator. Open collector output with internal 100 k $\Omega$  pull-up resistor. A band pass filter is connected between the “Det Out” pin and the “DA In” pin with

component values as shown in the attached block diagram. The “DA In” input signal is ac coupled.

( $V_{\text{CC}} = 2.6 \text{ V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$ )

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	$V_{\text{T}}$	$V_{\text{CC}} - 0.9$	$V_{\text{CC}} - 0.7$	$V_{\text{CC}} - 0.5$	V
Input Impedance	–	–	DA In	$Z_{\text{I}}$	–	11	–	k $\Omega$
Output Impedance	–	–	DA Out	$Z_{\text{O}}$	–	100	–	k $\Omega$
Output High Voltage	$V_{\text{in}} = V_{\text{CC}} - 1.0 \text{ V}$ , $I_{\text{OH}} = 0 \text{ mA}$	DA In	DA Out	$V_{\text{OH}}$	$V_{\text{CC}} - 0.1$	2.6	–	V
Output Low Voltage	$V_{\text{in}} = V_{\text{CC}} - 0.4 \text{ V}$ , $I_{\text{OL}} = 0 \text{ mA}$	DA In	DA Out	$V_{\text{OL}}$	–	0.03	0.4	V

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### ELECTRICAL CHARACTERISTICS (continued)

#### Pre-Amplifier/Expander/R<sub>x</sub> Mute/Volume Control (See Figure 4)

The Pre-Amplifier is an inverting rail-to-rail output swing operational amplifier with the non-inverting input terminal connected to the internal V<sub>B</sub> half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The expander analog ground is set to

the half supply reference so the input and output swing capability will increase as the supply voltage increases. The volume control can be adjusted through the MPU interface. The "R<sub>x</sub> Audio In" input signal is ac coupled.

(Test Conditions: V<sub>CC</sub> = 2.6 V, T<sub>A</sub> = 25°C, f<sub>in</sub> = 1.0 kHz, Set External Pre-Amplifier R's for Gain of 1, Volume Control = (0111).)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Pre-Amp Open Loop Gain	–	R <sub>x</sub> Audio In	Pre-Amp	A <sub>VOL</sub>	–	60	–	dB
Pre-Amp Gain Bandwidth	–	R <sub>x</sub> Audio In	Pre-Amp	GBW	–	100	–	kHz
Pre-Amp Maximum Output Swing	R <sub>L</sub> = 10 kΩ	R <sub>x</sub> Audio In	Pre-Amp	V <sub>Omax</sub>	–	V <sub>CC</sub> – 0.3	–	V <sub>pp</sub>
Expander 0 dB Gain Level	V <sub>in</sub> = –10 dBV	R <sub>x</sub> Audio In	E Out	G	–3.0	–0.11	3.0	dB
Expander Gain Tracking	V <sub>in</sub> = –20 dBV, Output Relative to G V <sub>in</sub> = –30 dBV, Output Relative to G	R <sub>x</sub> Audio In	E Out	G <sub>t</sub>	–21 –42	–19.65 –39.42	–19 –37	dB
Total Harmonic Distortion	V <sub>in</sub> = –10 dBV	R <sub>x</sub> Audio In	E Out	THD	–	0.5	–	%
Maximum Output Voltage	Increase input voltage until output voltage THD = 5%, then measure output voltage. R <sub>L</sub> = 10 kΩ	R <sub>x</sub> Audio In	E Out	V <sub>Omax</sub>	–	–5.0	–	dBV
Attack Time	E <sub>cap</sub> = 1.0 μF, R <sub>filt</sub> = 20 kΩ (See Appendix B)	R <sub>x</sub> Audio In	E Out	t <sub>a</sub>	–	3.0	–	ms
Release Time	E <sub>cap</sub> = 1.0 μF, R <sub>filt</sub> = 20 kΩ (See Appendix B)	R <sub>x</sub> Audio In	E Out	t <sub>r</sub>	–	13.5	–	ms
Compressor to Expander Crosstalk	V (R <sub>x</sub> Audio In) = 0 V <sub>rms</sub> , V <sub>in</sub> = –10 dBV	C In	E Out	C <sub>T</sub>	–	–	–70	dB
R <sub>x</sub> Mute	V <sub>in</sub> = –10 dBV No popping detectable during R <sub>x</sub> Mute transitions	R <sub>x</sub> Audio In	E Out	M <sub>e</sub>	–	–70	–	dB
Volume Control Range	Programmable through MPU Interface	–	–	V <sub>Crange</sub>	–14	–	16	dB
Volume Control Steps	Programmable through MPU Interface	–	–	V <sub>Cn</sub>	–	16	–	–

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### ELECTRICAL CHARACTERISTICS (continued)

#### Speaker Amplifier/SP Mute

The Speaker Amplifier is an inverting rail-to-rail operational amplifier. The non-inverting input terminal is connected to the internal  $V_B$  half supply reference. External

resistors and capacitors are used to set the gain and frequency response. The "SA In" input is ac coupled.

(Test Conditions:  $V_{CC} = 2.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $f_{in} = 1.0\text{ kHz}$ , External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Maximum Output Swing	$V_{CC} = 2.3\text{ V}$ , $R_L = 130\ \Omega$	SA In	SA Out	$V_{Omax}$	–	0.8	–	$V_{pp}$
	$V_{CC} = 2.3\text{ V}$ , $R_L = 600\ \Omega$				–	2.0	–	
	$V_{CC} = 3.4\text{ V}$ , $R_L = 600\ \Omega$				–	3.0	–	
SP Mute	$V_{in} = -20\text{ dBV}$ $R_L = 130\ \Omega$ No popping detectable during SP Mute transitions	SA In	SA Out	$M_{sp}$	–	–70	–	dB

#### Mic Amplifier (See Figure 6)

The Mic Amplifier is an inverting rail-to-rail output operational amplifier with the non-inverting input terminal connected to the internal  $V_B$  half supply reference. External

resistors and capacitors are connected to set the gain and frequency response. The "T<sub>x</sub> In" input is ac coupled.

(Test Conditions:  $V_{CC} = 2.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $f_{in} = 1.0\text{ kHz}$ , External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	T <sub>x</sub> In	Amp Out	$A_{VOL}$	–	60	–	dB
Gain Bandwidth	–	T <sub>x</sub> In	Amp Out	GBW	–	100	–	kHz
Maximum Output Swing	$R_L = 10\text{ k}\Omega$	T <sub>x</sub> In	Amp Out	$V_{Omax}$	–	$V_{CC} - 0.3$	–	$V_{pp}$



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### ELECTRICAL CHARACTERISTICS (continued)

#### Compressor/ALC/T<sub>x</sub> Mute/Limiter (See Figure 5)

The compressor analog ground is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The “C In” input is ac coupled. The ALC (Automatic Level Control) provides a soft limit to the output signal swing as the input voltage

increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface.

(Test Conditions:  $V_{CC} = 2.6\text{ V}$ ,  $f_{in} = 1.0\text{ kHz}$ ,  $T_A = 25^\circ\text{C}$ .)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Compressor 0 dB Gain Level	$V_{in} = -10\text{ dBV}$ , ALC disabled, Limiter disabled	C In	Lim Out	G	-3.0	-0.17	3.0	dB
Compressor Gain Tracking	$V_{in} = -30\text{ dBV}$ , Output Relative to G	C In	Lim Out	$G_t$	-11	-10.23	-9.0	dB
	$V_{in} = -50\text{ dBV}$ , Output Relative to G				-23	-20.23	-17	
Maximum Compressor Gain	$V_{in} = -70\text{ dBV}$	C In	Lim Out	$A_{Vmax}$	-	30	-	dB
Total Harmonic Distortion	$V_{in} = -10\text{ dBV}$ , ALC disabled, Limiter disabled	C In	Lim Out	THD	-	0.5	-	%
Input Impedance	-	C In	Lim Out	$Z_{in}$	-	16	-	k $\Omega$
Attack Time	$C_{cap} = 1.0\text{ }\mu\text{F}$ , $R_{filt} = 20\text{ k}\Omega$ (see Appendix B)	C In	Lim Out	$t_a$	-	3.0	-	ms
Release Time	$C_{cap} = 1.0\text{ }\mu\text{F}$ , $R_{filt} = 20\text{ k}\Omega$ (see Appendix B)	C In	Lim Out	$t_r$	-	13.5	-	ms
Expander to Compressor Crosstalk	$V(\text{C In}) = 0\text{ V}_{rms}$ , $V_{in} = -10\text{ dBV}$	R <sub>x</sub> Audio In	Lim Out	$C_T$	-	-	-40	dB
T <sub>x</sub> Data Mute	$V_{in} = -10\text{ dBV}$ , ALC disabled No popping detectable during R <sub>x</sub> Mute transitions	C In	Lim Out	$M_e$	-	-70	-	dB
ALC Dynamic Range	-	C In	Lim Out	DR	-24	-	-2.5	dBV
ALC Output Level	$V_{in} = -18\text{ dBV}$	C In	Lim Out	ALC <sub>out</sub>	-	-16	-	dBV
	$V_{in} = -2.5\text{ dBV}$				-	-12	-	
Limiter Output Level	ALC disabled	C In	T <sub>x</sub> Out	$V_{lim}$	-	0.8	-	V <sub>pp</sub>

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## ELECTRICAL CHARACTERISTICS (continued)

### Splatter Amplifier (see Figure 7)

The Splatter Amplifier is an inverting rail-to-rail output operational amplifier with the non-inverting input terminal connected to the internal  $V_B$  half supply reference. External

resistors and capacitors can be connected to set the gain and frequency response. The “Spl Amp In” input is ac coupled.

(Test Conditions:  $V_{CC} = 2.6$  V,  $T_A = 25^\circ\text{C}$ ,  $f_{in} = 1.0$  kHz, External resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	Spl Amp In	$T_X$ Out	$A_{VOL}$	–	60	–	dB
Gain Bandwidth	–	Spl Amp In	$T_X$ Out	GBW	–	100	–	kHz
Maximum Output Swing	$R_L = 10$ k $\Omega$	Spl Amp In	$T_X$ Out	$V_{Omax}$	–	$V_{CC} - 0.3$	–	$V_{pp}$

### $T_X$ Audio Path Recommendation

The recommended configuration for the  $T_X$  Audio path includes setting the Microphone Amplifier gain to 16 dB using the external gain setting resistors and setting the Splatter

Amplifier gain to 9.0 dB using the external gain setting resistors. With these gain values, the total  $T_X$  Path transfer characteristic is shown in Figure 7.

### PLL Voltage Regulator

The PLL supply voltage is regulated to a nominal of 2.2 V. The “ $V_{CC}$  Audio” pin is the supply voltage for the internal voltage regulator. The “PLL  $V_{ref}$ ” pin is the 2.2 V regulated output voltage. Two capacitors with 10  $\mu\text{F}$  and 0.01  $\mu\text{F}$  values must be connected to the “PLL  $V_{ref}$ ” pin to filter and stabilize this regulated voltage. The voltage regulator provides power for the 2nd LO,  $R_X$  and  $T_X$  PLL's, and MPU Interface. The voltage regulator can also be used to provide a regulated supply voltage for external IC's.  $R_X$  and  $T_X$  PLL loop performance are independent of the power supply voltage when the voltage regulator is used. The voltage regulator requires about 200 mV of “headroom”. When the power supply decreases to within about 200 mV of the output

voltage, the regulator will go out of regulation but the output voltage will not turn off. Instead, the output voltage will maintain about a 200 mV delta to the power supply voltage as the power supply voltage continues to decrease. The “PLL  $V_{ref}$ ” pin can be connected to “ $V_{CC}$  Audio” by the external wiring if voltage higher than 2.2 V is required. But it should not be connected to other supply except “ $V_{CC}$  Audio”. The voltage regulator is “on” in the Active and  $R_X$  modes. In the Standby and Inactive modes, the voltage regulator is turned off to reduce current drain and the “PLL  $V_{ref}$ ” pin is internally connected to “ $V_{CC}$  Audio” (i.e., the supply voltage is maintained but is now unregulated).

(Test Conditions:  $V_{CC} = 2.6$  V,  $T_A = 25^\circ\text{C}$ .)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Output Voltage Level	$V_{CC} = 2.6$ V, $I_L = 0$ mA	–	$V_{CC}$ PLL	$V_{out}$	1.9	2.2	2.5	V
Line Regulation	$I_L = 0$ mA, $V_{CC} = 2.6$ to 5.5 V	$V_{CC}$	$V_{CC}$ PLL	Regline	–	1.43	40	mV
Load Regulation	$V_{CC} = 2.6$ V, $I_L = 0$ to 1.0 mA	$V_{CC}$	$V_{CC}$ PLL	Regload	–	–1.86	40	mV
Drop-Out Voltage	$I_L = 0$ mA	–	–	DO	–	–	$V_{out} + 200$	mV

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## ELECTRICAL CHARACTERISTICS (continued)

### Low Battery Detect

An external resistor divider is connected to the “Ref” input pin to set the threshold for the low battery detect. The voltage at the “Ref” input pin is compared to an internal 1.23 V

Bandgap reference voltage. The “BD Out” pin is open collector and requires an external pull-up resistor to  $V_{CC}$ .

(Test Conditions:  $V_{CC} = 2.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Average Threshold Voltage	Take average of rising and falling threshold	Ref	Ref/BD Out	Threshold	–	1.23	–	V
Hysteresis	–	Ref	Ref/BD Out	Hys	–	4.0	–	mV
Input Current	$V_{in} = 1.6\text{ V}$	–	Ref	$I_{in}$	–50	5.71	+50	nA
Output High Voltage	$V_{ref} = 1.6$ , $R_L = 3.9\text{ k}\Omega$	Ref	BD Out	$V_{OH}$	$V_{CC} - 0.1$	2.6	–	V
Output Low Voltage	$V_{ref} = 0.9$ , $R_L = 3.9\text{ k}\Omega$	Ref	BD Out	$V_{OL}$	–	0.12	0.4	V

Figure 3. Data Amp Operation

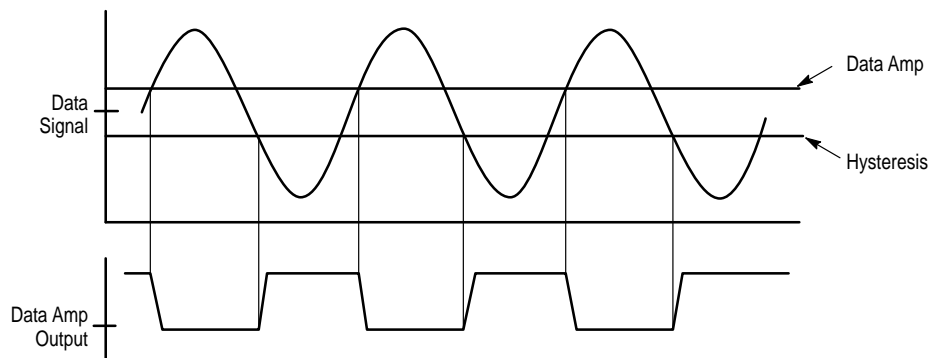
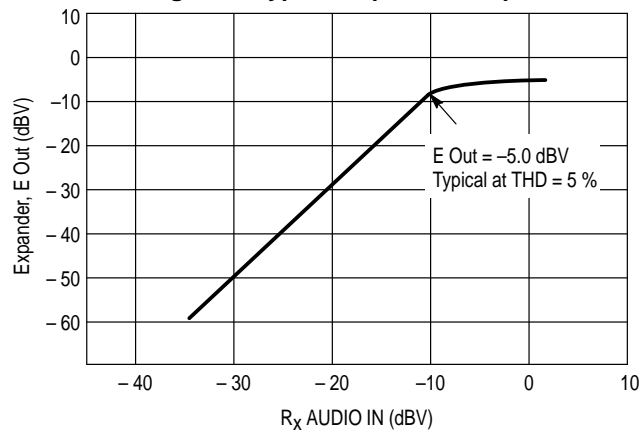
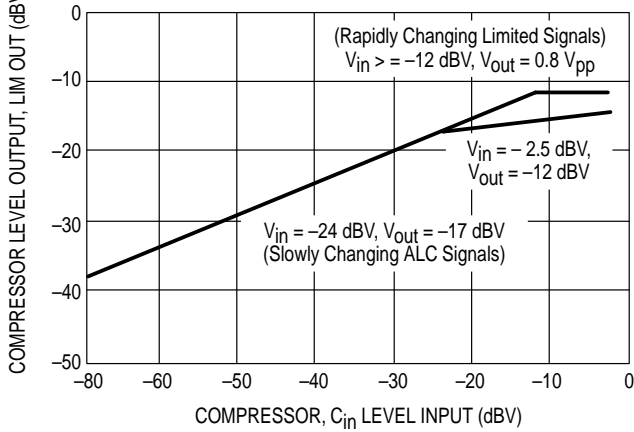


Figure 4. Typical Expander Response

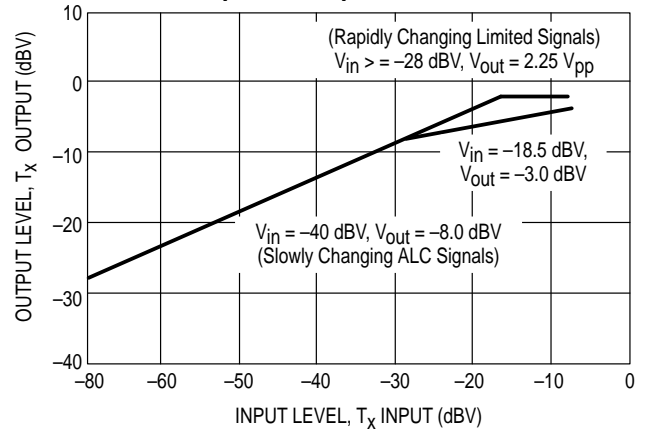


# MC13109

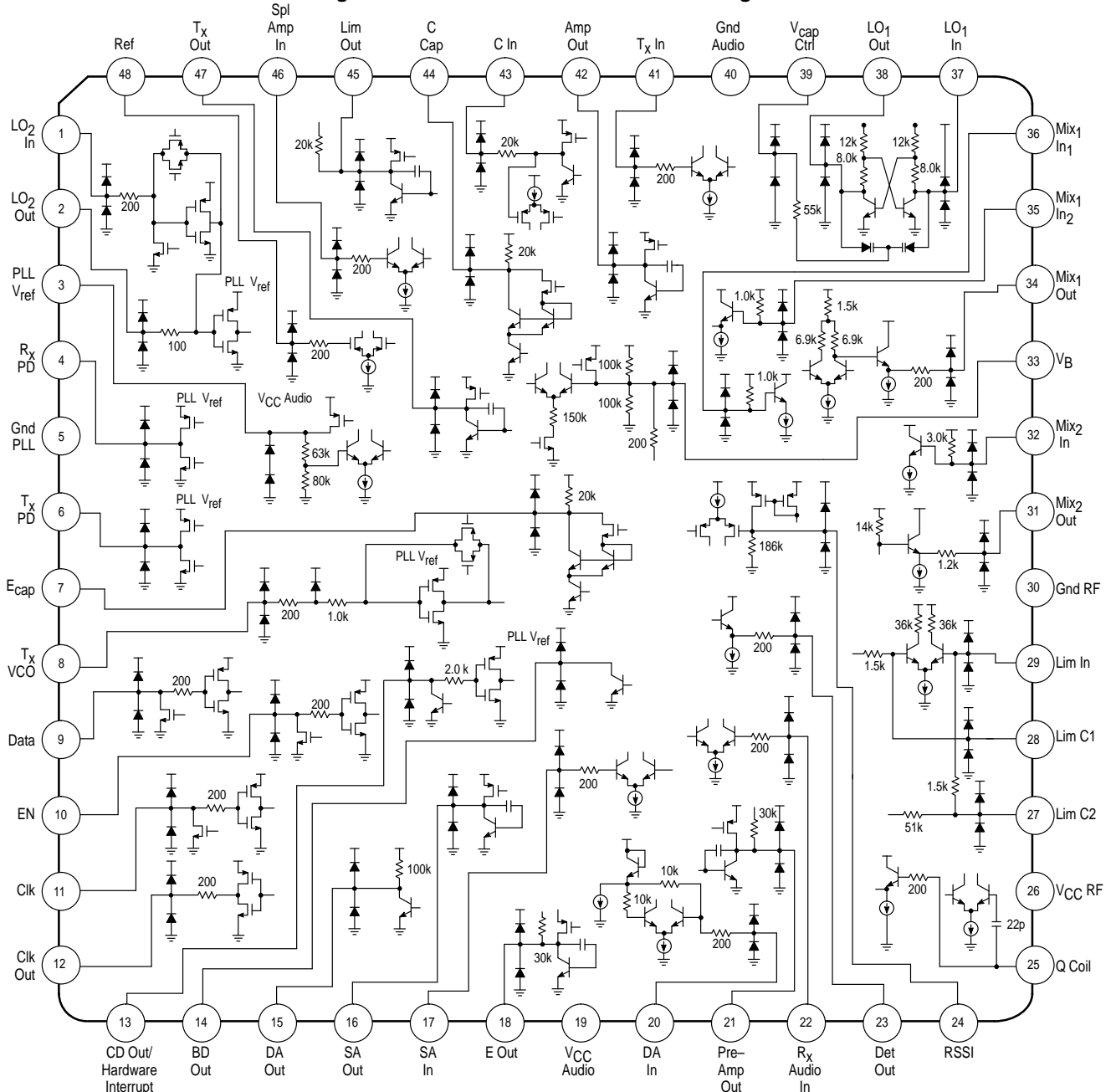
**Figure 5. Typical Compressor/ALC/Limiter Response**



**Figure 6. Total Tx Path, Mic Amp Gain = 16 dB, Splatter Amp Gain = 9.0 dB**



**Figure 7. MC13109FTA Internal I/O Block Diagram**



# MC13109

## PIN FUNCTION DESCRIPTION

48-TQFP Pin	52-QFP Pin	Symbol	Type	Description
1 2	1 2	LO <sub>2</sub> In LO <sub>2</sub> Out	–	These pins form the PLL reference oscillator when connected to an external parallel-resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO <sub>2</sub> ) for the RF receiver.
3	3	PLL V <sub>ref</sub>	Supply	Voltage Regulator output pin. The internal voltage regulator provides a stable power supply voltage for the R <sub>X</sub> and T <sub>X</sub> PLL's and can also be used as a regulated supply voltage for the other IC's.
4	4	R <sub>X</sub> PD	Output	Three state voltage output of the R <sub>X</sub> Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R <sub>X</sub> PLL loop filter. It is important to minimize the line length and capacitance of this pin.
5	5	Gnd PLL	Gnd	Ground pin for PLL section of IC.
6	6	T <sub>X</sub> PD	Output	Three state voltage output of the T <sub>X</sub> Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T <sub>X</sub> PLL loop filter. It is important to minimize the line length and capacitance on this pin.
7	7	E Cap	–	Expander rectifier filter capacitor pin. Connect capacitor to V <sub>CC</sub> .
8	8	T <sub>X</sub> VCO	Input	Transmit divide counter input which is driven by an ac coupled external transmit loop VCO. The minimum signal level is 200 mV <sub>pp</sub> @ 80.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	12	Clk Out	Output	Microprocessor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
N/A	14	Status Out	Output	This pin indicates when the internal latches may have lost memory due to a power glitch.
13	15	CD Out/ Hardware Interrupt	Output/ Input	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull-up resistor. 2) Hardware interrupt input which can be used to "wake-up" from Inactive Mode.
14	16	BD Out	Output	Low battery detect output (open collector with external pull-up resistor).
15	17	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull-up resistor).
16	18	SA Out	Output	Speaker amplifier output.
17	19	SA In	Input	Speaker amplifier input (ac coupled).
18	20	E Out	Output	Expander output.
19	21	V <sub>CC</sub> Audio	Supply	V <sub>CC</sub> supply for audio section.
20	22	DA In	Input	Data amplifier input (ac coupled).
21	23	Pre-Amp Out	Output	Pre-amplifier output for connection of pre-amplifier feedback resistor.
22	24	R <sub>X</sub> Audio In	Input	R <sub>X</sub> audio input to pre-amplifier (ac coupled).
23	25	Det Out	Output	Audio output from FM detector.
24	26	RSSI	–	Receive signal strength indicator filter capacitor.
N/A	27	N/A	–	Note used.
25	28	Q Coil	–	A quad coil or ceramic discriminator are connected to this pin.
26	29	V <sub>CC</sub> RF	Supply	V <sub>CC</sub> supply for RF receiver section.
27 28	30 31	Lim C2 Lim C1	–	IF amplifier/limiter capacitor pins.

## MC13109

### PIN FUNCTION DESCRIPTION (continued)

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
29	32	Lim In	Input	Signal input for IF amplifier/limiter.
30	33	Gnd RF	Gnd	Ground pin for RF section of the IC.
31	34	Mix <sub>2</sub> Out	Output	Second mixer output.
32	35	Mix <sub>2</sub> In	Input	Second mixer input.
33	36	V <sub>B</sub>	–	Internal half supply analog ground reference.
34	37	Mix <sub>1</sub> Out	Output	First mixer output.
35	38	Mix <sub>1</sub> In <sub>2</sub>	Input	Negative polarity first mixer input.
36	39	Mix <sub>1</sub> In <sub>1</sub>	Input	Positive polarity first mixer input.
37 38	40 41	LO <sub>1</sub> In LO <sub>1</sub> Out	–	Tank elements for 1st LO multivibrator oscillator are connected to these pins.
39	42	V <sub>cap</sub> Ctrl	–	1st LO varactor control pin.
40	43	Gnd Audio	Gnd	Ground for audio section of the IC.
41	44	T <sub>X</sub> In	Input	T <sub>X</sub> path input to Microphone Amplifier (ac coupled).
42	45	Amp Out	Output	Microphone amplifier output.
43	46	C In	Input	Compressor input (ac coupled).
44	47	C Cap	–	Compressor rectifier filter capacitor pin. Connect capacitor to V <sub>CC</sub> .
45	48	Lim Out	Output	T <sub>X</sub> path limiter output.
46	49	Spl Amp In	Input	Splatter amplifier input (ac coupled).
47	50	T <sub>X</sub> Out	Output	T <sub>X</sub> path audio output.
48	51	Ref	Input	Reference voltage input for low battery detect.
N/A	52	N/A	–	Not used.

#### Power Supply Voltage

This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on two or three NiCad cells or on 5.0 V power.

#### PLL Frequency Synthesizer General Description

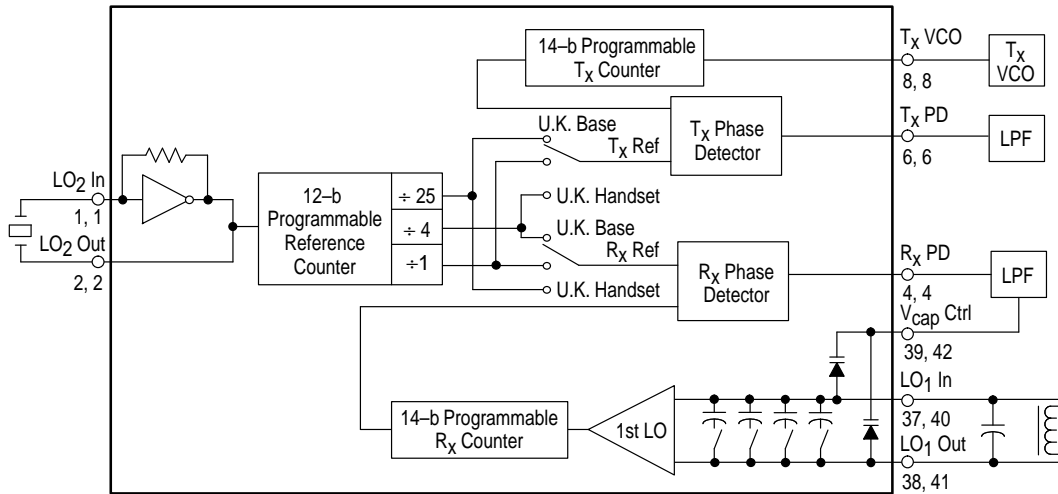
Figure 8 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), France, Spain, Australia, Korea, New Zealand, U.K., Netherlands and China (see channel frequency tables in Appendix A).

The 2nd local oscillator and reference divider provide the reference frequency for the R<sub>X</sub> and T<sub>X</sub> PLL loops. The

programmed divider value for the reference divider is selected based on the crystal frequency and the desired R<sub>X</sub> and T<sub>X</sub> reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U.K. The 14-bit T<sub>X</sub> counter is programmed for the desired transmit channel frequency. The 14-bit R<sub>X</sub> counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #6 and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

# MC13109

Figure 8. Dual PLL Simplified Block Diagram



## ELECTRICAL CHARACTERISTICS ( $V_{CC} = 2.6\text{ V}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
<b>PLL PIN DC</b>						
Input Voltage Low	–	Data Clk EN Hardware Int.	$V_{IL}$	–	0.3	V
Input Voltage High	–	Data Clk EN	$V_{IH}$	"PLL $V_{ref}$ " – 0.3	" $V_{CC}$ Audio"	V
Input Current Low	$V_{in} = 0.3\text{ V}$	Data Clk EN	$I_{IL}$	–5.0	–	$\mu\text{A}$
Input Current High	$V_{in} = (V_{CC}\text{ Audio}) - 0.3$	Data Clk EN	$I_{IH}$	–	5.0	$\mu\text{A}$
Hysteresis Voltage	–	Data Clk EN	$V_{hys}$	1.0	–	V
Output Current High	–	R <sub>x</sub> PD T <sub>x</sub> PD	$I_{OH}$	–	–0.7	mA
Output Current Low	–	R <sub>x</sub> PD T <sub>x</sub> PD	$I_{OL}$	0.7	–	mA
Output Voltage Low	$I_{IL} = 0.7\text{ mA}$	R <sub>x</sub> PD T <sub>x</sub> PD	$V_{OL}$	–	(PLL $V_{ref}$ ) * 0.2	V
Output Voltage High	$I_{IH} = -0.7\text{ mA}$	R <sub>x</sub> PD T <sub>x</sub> PD	$V_{OH}$	(PLL $V_{ref}$ ) * 0.8	–	V
Tri-State Leakage Current	$V = 1.2\text{ V}$	R <sub>x</sub> PD T <sub>x</sub> PD	$I_{OZ}$	–50	50	nA
Input Capacitance	–	Data Clk EN	$C_{in}$	–	8.0	pF
Output Capacitance	–	R <sub>x</sub> PD T <sub>x</sub> PD	$C_{out}$	–	8.0	pF

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## ELECTRICAL CHARACTERISTICS (continued) ( $V_{CC} = 2.6\text{ V}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
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### PLL PIN INTERFACE

EN to Clk Setup Time	–	EN, Clk	$t_{suEC}$	200	–	ns
Data to Clk Setup Time	–	Data, Clk	$t_{suDC}$	100	–	ns
Hold Time	–	Data, Clk	$t_h$	90	–	ns
Recovery Time	–	EN, Clk	$t_{rec}$	90	–	ns
Input Pulse Width	–	EN, Clk	$t_w$	100	–	ns
Input Rise and Fall Time	–	Data Clk EN	$t_r$ , $t_f$	– – –	9.0	$\mu\text{s}$
MPU Interface Power-Up Delay	90% of PLL $V_{ref}$ to Data, Clk, EN	–	$t_{puMPU}$	–	100	$\mu\text{s}$

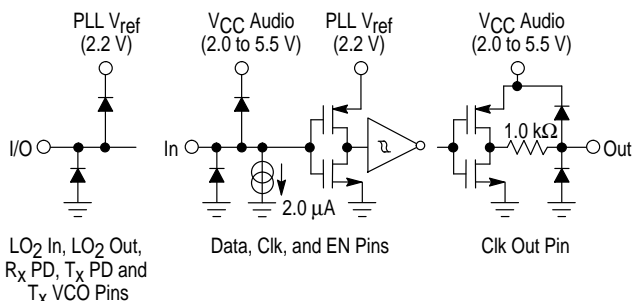
### PLL LOOP

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
2nd LO Frequency	–	LO <sub>2</sub> In LO <sub>2</sub> Out	$f_{LO}$	–	12	MHz
“T <sub>X</sub> VCO” Input Frequency	$V_{in} = 200\text{ mV}_{pp}$	T <sub>X</sub> VCO	$f_{txmax}$	–	80	MHz

### PLL I/O Pin Specifications

The 2nd LO, R<sub>X</sub> and T<sub>X</sub> PLL's and MPU serial interface are normally powered by the internal voltage regulator at the “PLL  $V_{ref}$ ” pin. The “PLL  $V_{ref}$ ” pin is the output of a voltage regulator which is powered from the “V<sub>CC Audio</sub>” power supply pin. Therefore, the maximum input and output levels for most PLL I/O pins (LO<sub>2</sub> In, LO<sub>2</sub> Out, R<sub>X</sub> PD, T<sub>X</sub> PD, T<sub>X</sub> VCO) is the regulated voltage at the “PLL  $V_{ref}$ ” pin. The ESD protection diodes on these pins are also connected to “PLL  $V_{ref}$ ”. Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is  $V_{CC}$ . Figure 9 shows a simplified schematic of the PLL I/O pins.

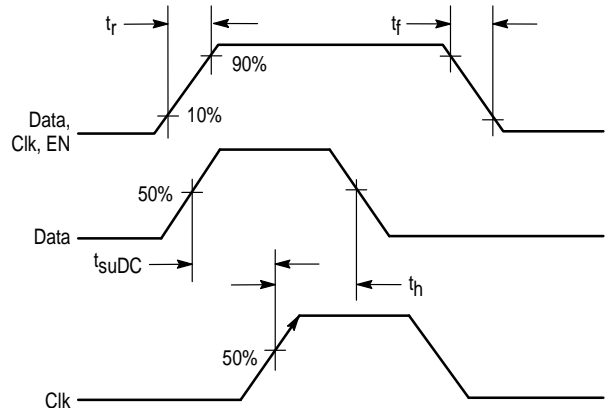
Figure 9. PLL I/O Pin Simplified Schematics



### Microprocessor Serial Interface

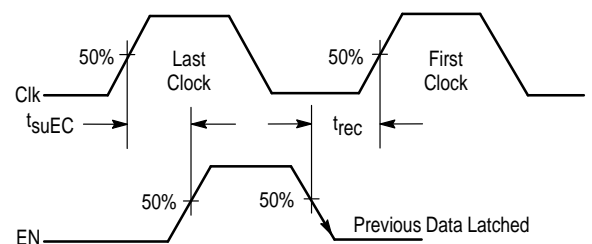
The “Data”, “Clk”, and “EN” pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counter and various control functions. The “Data” and “Clk” pins are used to load data into the shift register. Figure 10 shows “Data” and “Clk” pin timing. Data is clocked on positive clock transitions.

Figure 10. Data and Clock Timing Requirement



After data is loaded into the shift register, the data is latched into the appropriate latch register using the “EN” pin. This is done in two steps. First, an 8-bit address is loaded into the shift register and latched into the 8-bit address latch register. Then, up to 16-bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 11 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 11. Enable Timing Requirement

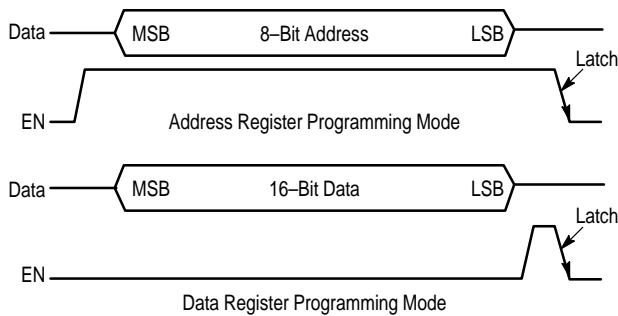




## MC13109

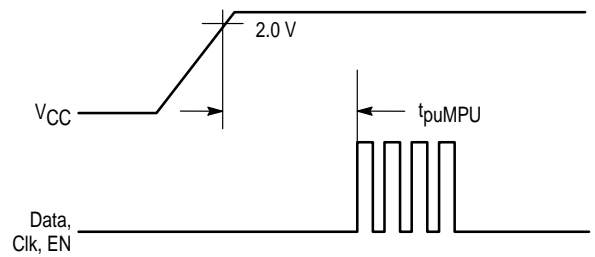
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 12 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when "EN" is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the "EN" high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

**Figure 12. Microprocessor Interface Programming Mode Diagrams**



The MPU serial interface is fully operational within 100  $\mu$ s after the power supply has reached its minimum level during power-up (See Figure 13). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby,  $R_x$ , and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

**Figure 13. Microprocessor Serial Interface Power-Up Delay**



### Status Out

This is a digital output which indicates whether the latch registers have been reset to their power-up default values. Latch power-up default values are given in Figure 32. If there is a power glitch or ESD event which causes the latch registers to be reset to their default values, the "Status Out" pin will indicate this to the MPU so it can reload the correct information into the latch registers.

**Figure 14. Status Out Operation**

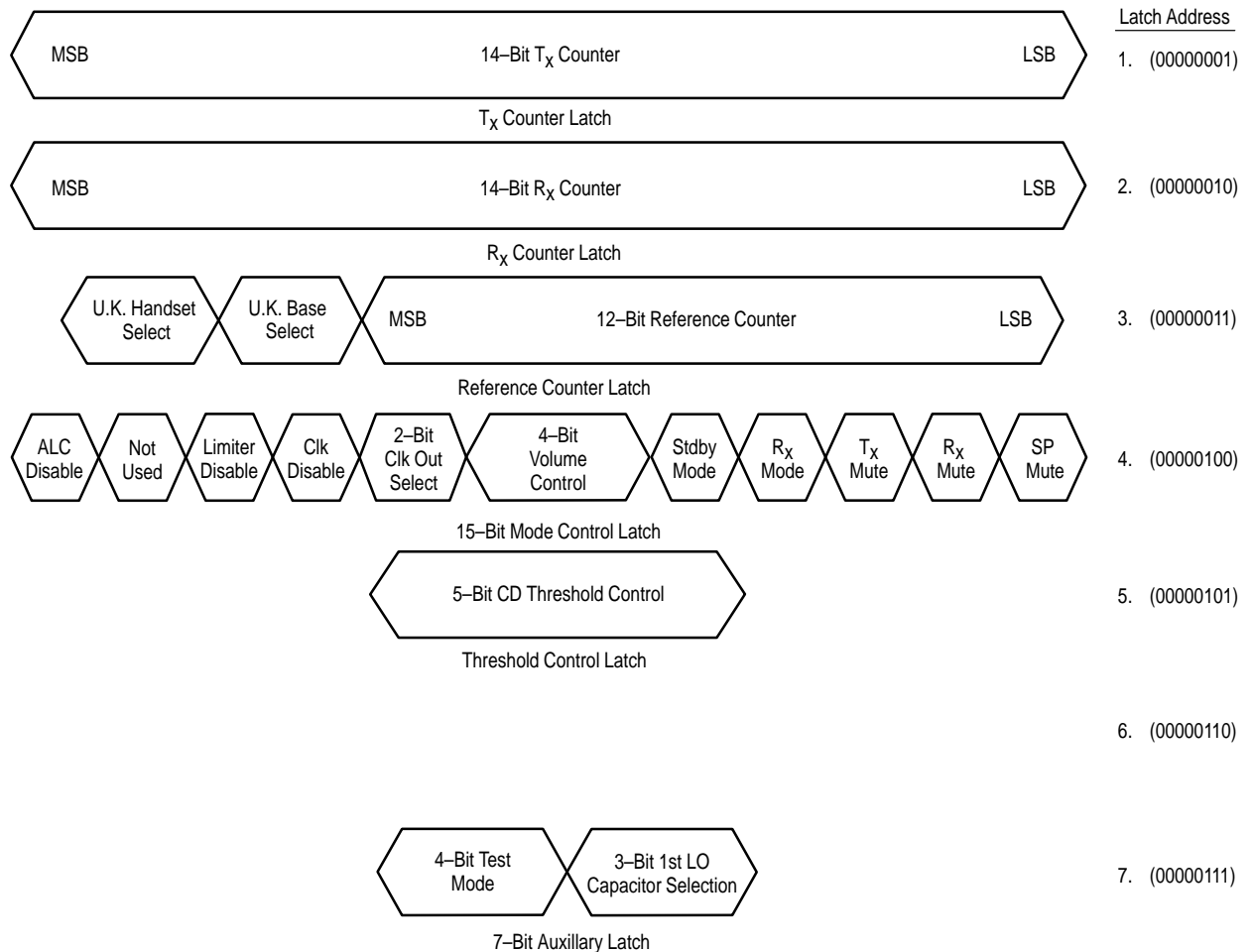
Status Latch Register Bits	Status Out Logic Level
Latch bits not at power-up default value	0
Latch bits at power-up default value	1

### Data Registers

Figure 15 shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. "Don't care" bits can be loaded into the shift register first if 8-bit bytes of data are loaded.

# MC13109

**Figure 15. Microprocessor Interface Data Latch Registers**



### Reference Frequency Selection

The “LO<sub>2</sub> In” and “LO<sub>2</sub> Out” pins form a reference oscillator when connected to an external parallel-resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 16 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries.

**Figure 16. Reference Frequency and Reference Divider Values**

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency
10.24 MHz	2048	1	5.0 kHz
10.24 MHz	1024	4	2.5 kHz
11.15 MHz	2230	1	5.0 kHz
12.00 MHz	2400	1	5.0 kHz
11.15 MHz	1784	1	6.25 kHz
11.15 MHz	446	4	6.25 kHz
11.15 MHz	446	25	1.0 kHz

### Reference Counter

Figure 17 shows how the reference frequencies for the R<sub>x</sub> and T<sub>x</sub> loops are generated. All countries except U.K. require that the T<sub>x</sub> and R<sub>x</sub> reference frequencies be identical. In this case, set “U.K. Base Select” and “U.K. Handset Select” bits to “0”. Then the fixed divider is set to “1” and the T<sub>x</sub> and R<sub>x</sub> reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value for T<sub>x</sub> and R<sub>x</sub>.

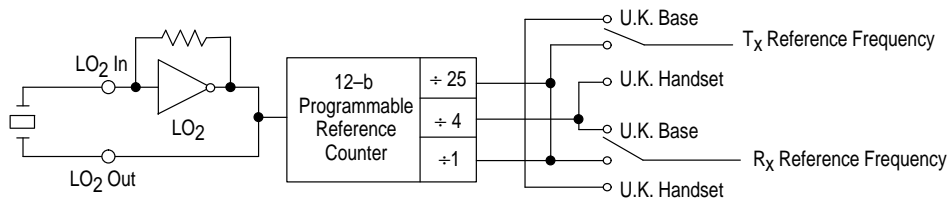
For U.K. base operation, set “U.K. Base Select” to “1”. For U.K. handset operation, set “U.K. Handset Select” to “1”. The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T<sub>x</sub> and R<sub>x</sub> reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12-bit reference divider (4095). In this case, set “U.K. Base Select” to “1” and set “U.K. Handset Select” to “1”. This will give a fixed divide by 4 for both the T<sub>x</sub> and R<sub>x</sub> reference. Then set the reference divider to 1024 to get a total divider of 4096.

### Mode Control Register

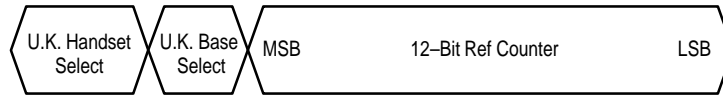
Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Control Register. Operation of the Control Register is explained in Figures 18 through 25.

# MC13109

**Figure 17. Reference Register Programming Mode**

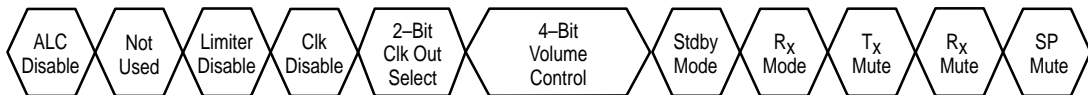


U.K. Handset Select	U.K. Base Select	T <sub>x</sub> Divider Value	R <sub>x</sub> Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Base Set
1	0	4	25	U.K. Hand Set
1	1	4	4	Netherlands Base and Hand Set



14-Bit Reference Counter Latch

**Figure 18. Control Register Bits**



**Figure 19. Mute and Disable Control Bit Descriptions**

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T <sub>x</sub> Mute	1 0	Transmit Channel Muted Normal Operation
R <sub>x</sub> Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

### Power Saving Operating Modes

When the MC13109 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R<sub>x</sub>, Standby, Interrupt and Inactive. In Active Mode, all circuit blocks are powered. In R<sub>x</sub> mode, all circuitry is powered down except for those circuit

sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 20 shows the control register bit values for selection of each power saving mode and Figure 21 show the circuit blocks which are powered in each of these operating mode.

**Figure 20. Power Saving Mode Selection**

Stdby Mode Bit	R <sub>x</sub> Mode Bit	"CD Out/Hardware Interrupt" Pin	Power Saving Mode
0	0	X	Active
0	1	X	R <sub>x</sub>
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Inactive

# MC13109

**Figure 21. Circuit Blocks Powered During Power Saving Modes**

Circuit Blocks	Active	R <sub>X</sub>	Standby	Inactive
"PLL V <sub>ref</sub> " Regulated Voltage	X	X	X <sup>1</sup>	X <sup>1</sup>
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver	X	X		
1st LO VCO	X	X		
R <sub>X</sub> PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T <sub>X</sub> PLL	X			
R <sub>X</sub> Audio Path	X			
T <sub>X</sub> Audio Path	X			

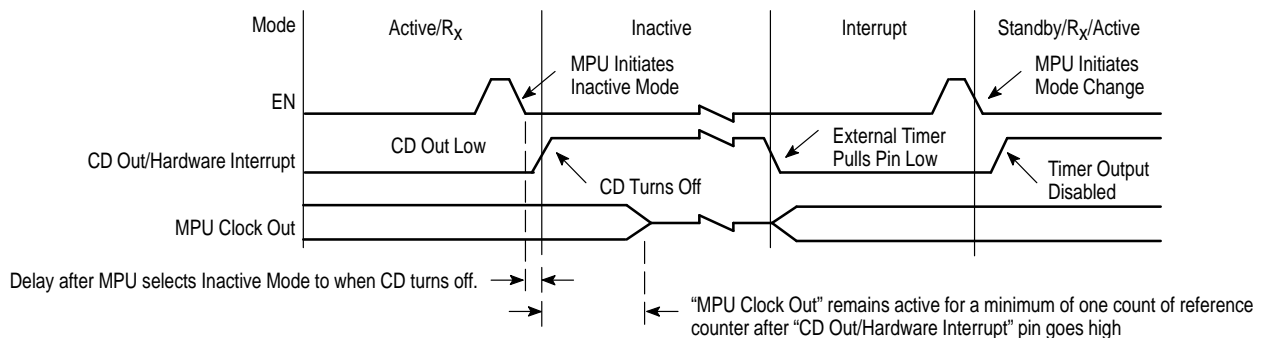
**NOTE:** 1. In Standby and Inactive Modes, "PLL V<sub>ref</sub>" remains powered but is not regulated. It will fluctuate with V<sub>CC</sub>.

## Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13109 into the Inactive mode, which turns off the MPU Clock Output (see Figure 22), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 μs) after the command is given to switch into the "Inactive" mode. An external timing circuit should be used to initiate the turn-on sequence. The "CD Out" pin has a dual function. In the Active and R<sub>X</sub> modes it performs the carrier detect function. In the

Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state due to the external pull-up resistor. In the Inactive mode the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low" by the external timing circuit, the MC13109 switches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R<sub>X</sub> modes.

**Figure 22. Hardware Interrupt Operation**



## MC13109

### “Clk Out” Divider Programming

The “Clk Out” pin is derived from the 2nd local oscillator and can be used to drive a microprocessor, thereby reducing the number of crystals required. Figure 23 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 24 shows the “Clk Out” register bit values.

**Figure 23. Clock Output Values**

Crystal Frequency	Clock Output Divider			
	2	3	5	10
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

**Figure 24. Clock Output Divider**

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	5
1	1	10

### MPU “Clk Out” Power-Up Default Divider Value

The power-up default divider value is “divide by 10”. This provides an MPU clock of about 1.0 MHz after initial power-up. The reason for choosing this relatively low clock frequency after initial power-up is that some microprocessors that operate down to a 2.0 V power supply have a maximum clock frequency of 1.0 MHz. After initial power-up, the MPU can change the clock divider value to set the clock to the desired operating frequency. Special care has been taken in the design of the clock divider to ensure that the transition between one clock divider value and another is “smooth” (i.e., there will be no narrow clock pulses to disturb the MPU).

### MPU “Clk Out” Radiated Noise on Circuit Board

The clock line running between the MC13109 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on-chip in-series with the “Clk Out” output driver. A small capacitor can be connected to the “Clk Out” line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the “Clk Out” line.

### Volume Control

The volume control can be programmed in 2.0 dB gain steps from -14 dB to +16 dB. The power-up default value is 0 dB.

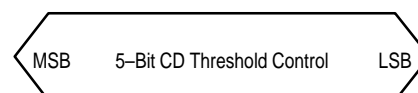
**Figure 25. Volume Control**

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	-14 dB
0	0	0	1	1	-12 dB
0	0	1	0	2	-10 dB
0	0	1	1	3	-8.0 dB
0	1	0	0	4	-6.0 dB
0	1	0	1	5	-4.0 dB
0	1	1	0	6	-2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

### Gain Control Register

The gain control register contains bits which control the Carrier Detect threshold. Operation of these latch bits are explained in Figures 26 and 27.

**Figure 26. Gain Control Latch Bits**



## MC13109

### Carrier Detect Threshold Programming

The "CD Out" pin will give an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification

section of this document. If a different carrier detect threshold value is desired, it can be set through the MPU interface as shown in Figure 27 below.

Figure 27. Carrier Detect Threshold Control

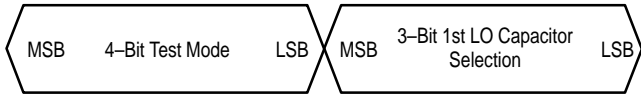
CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	-20 dB
0	0	0	0	1	1	-19 dB
0	0	0	1	0	2	-18 dB
0	0	0	1	1	3	-17 dB
0	0	1	0	0	4	-16 dB
0	0	1	0	1	5	-15 dB
0	0	1	1	0	6	-14 dB
0	0	1	1	1	7	-13 dB
0	1	0	0	0	8	-12 dB
0	1	0	0	1	9	-11 dB
0	1	0	1	0	10	-10 dB
0	1	0	1	1	11	-9.0 dB
0	1	1	0	0	12	-8.0 dB
0	1	1	0	1	13	-7.0 dB
0	1	1	1	0	14	-6.0 dB
0	1	1	1	1	15	-5.0 dB
1	0	0	0	0	16	-4.0 dB
1	0	0	0	1	17	-3.0 dB
1	0	0	1	0	18	-2.0 dB
1	0	0	1	1	19	-1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

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## Auxiliary Register

The auxiliary register contains a 3-bit 1st LO Capacitor Selection latch and a 4-bit Test Mode latch. Operation of these latch bits are explained in Figures 28, 29 and 30.

**Figure 28. Auxiliary Register Latch Bits**



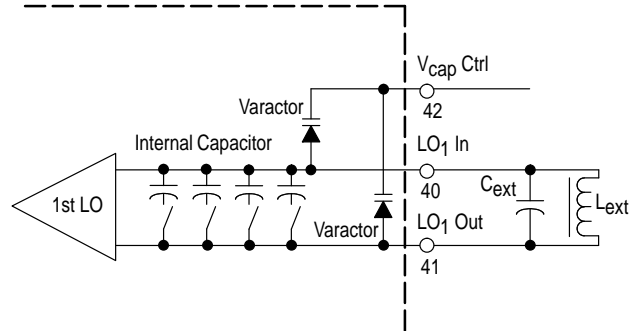
## First Local Oscillator Capacitor Selection for 25 Channel U.S. Operation

There is a very large frequency difference between the minimum and maximum channel frequencies in the proposed 25 Channel U.S. standard. The sensitivity of the 1st LO is not large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figure 29 shows the

schematic of the 1st LO tank circuit. Figure 30 shows the latch control bit values.

The internal varactor temperature coefficient is 1800 ppm/°C ( $C_0 = 8.9 \text{ pF}$  at  $25^\circ\text{C}$ ,  $V_{\text{cap}}$  control voltage = 1.2 V,  $F_{\text{req}} = 36 \text{ MHz}$ ). Customer is suggested to use a negative temperature coefficient capacitor in 1st LO tank circuit when the whole operating temperature range of  $-40$  to  $+85^\circ\text{C}$  is considered.

**Figure 29. 1st LO Schematic**



**Figure 30. 1st LO Capacitor Select for U.S. 25 Channels**

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap. Bit 0	1st LO Cap. Select	U.S. Base Channels	U.S. Handset Channels	Internal Cap. Value (Excluding Varactor)	Varactor Value over 0.5 to 2.2 V Range	External Capacitor Value	External Inductor Value
0	0	0	0	16 – 25	–	0.92 pF	10 – 6.4 pF	27 pF	0.47 $\mu\text{H}$
0	0	0	0	–	16 – 25	0.92 pF	10 – 6.4 pF	33 pF	0.47 $\mu\text{H}$
0	0	1	1	1 – 6	–	2.61 pF	10 – 6.4 pF	27 pF	0.47 $\mu\text{H}$
0	1	0	2	7 – 15	–	1.82 pF	10 – 6.4 pF	27 pF	0.47 $\mu\text{H}$
0	1	1	3	–	1 – 6	8.69 pF	10 – 6.4 pF	33 pF	0.47 $\mu\text{H}$
1	0	0	4	–	7 – 15	7.19 pF	10 – 6.4 pF	33 pF	0.47 $\mu\text{H}$

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Figure 31. Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T <sub>X</sub> VCO" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mV <sub>pp</sub>	–
1	0	0	0	1	R <sub>X</sub> Counter, upper 6	0 to 2.2 V	Input Frequency/64
2	0	0	1	0	R <sub>X</sub> Counter, lower 8	0 to 2.2 V	See Note Below
3	0	0	1	1	R <sub>X</sub> Prescaler	0 to 2.2 V	Input Frequency/4
4	0	1	0	0	T <sub>X</sub> Counter, upper 6	0 to 2.2 V	Input Frequency/64
5	0	1	0	1	T <sub>X</sub> Counter, lower 8	0 to 2.2 V	See Note Below
6	0	1	1	0	T <sub>X</sub> Prescaler	>200 mV <sub>pp</sub>	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.2 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.2 V	Input Frequency/100
9	1	0	0	1	AGC Gain = 10 Option	N/A	–
10	1	0	1	0	AGC Gain = 25 Option	N/A	–

**NOTE:** To determine the correct output, look at the lower 8 bits in the R<sub>X</sub> or T<sub>X</sub> register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6 bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) >= 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

## Test Modes

Test Mode Control latch bits enable independent testing of internal counters and set AGC Gain Options. In test mode, the "T<sub>X</sub> VCO" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0" for normal operation. Test mode operation is described in Figure 31. During normal operation and when testing the T<sub>X</sub> Prescaler, the "T<sub>X</sub> VCO" input can be a minimum of 200 mV<sub>pp</sub> at 80 MHz and should be ac coupled. For other test modes, input signals should be standard logic levels of 0 to 2.2 V and a maximum frequency of 16 MHz.

## Power-Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The MC13109 is initially placed in the Rx mode with all mutes active and nothing disabled. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The MPU clock output divider is set to 10 to give the minimum clock output frequency. The T<sub>X</sub> and R<sub>X</sub> latch registers are set for USA Channel Frequency #21. Figure 32 shows the initial power-up states for all latch registers.

Figure 32. Latch Register Power-Up Defaults

Register	Count	MSB								LSB							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T <sub>X</sub>	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R <sub>X</sub>	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	–	–	–	–	–	–	–	–	–	–	1	0	1	0	0
TM	N/A	–	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0



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Figure 33.  $I_{CC}$  versus  $V_{CC}$  at Active Mode

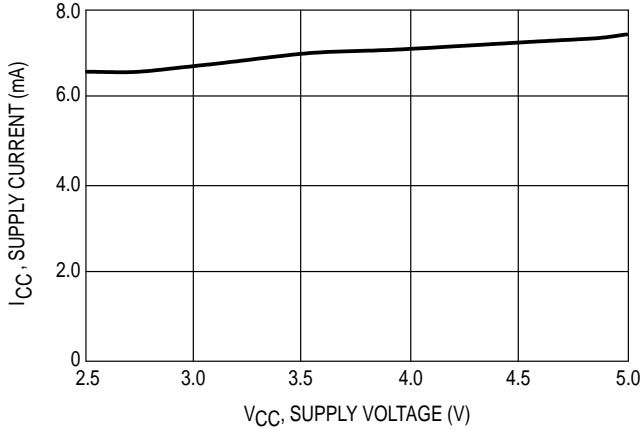


Figure 34.  $I_{CC}$  versus  $V_{CC}$  at Receive Mode

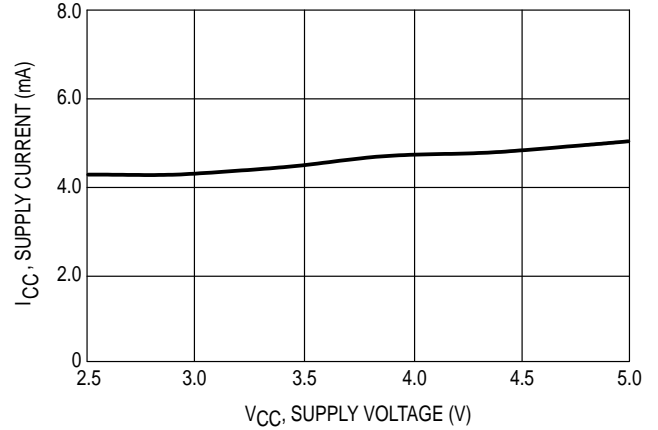


Figure 35.  $I_{CC}$  versus  $V_{CC}$  at Standby Mode

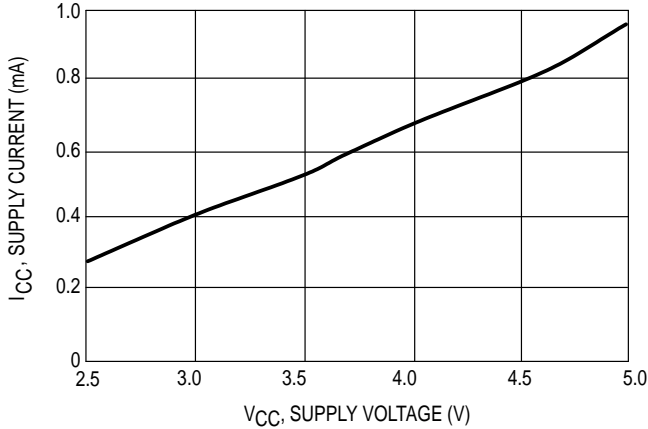


Figure 36.  $I_{CC}$  versus  $V_{CC}$  at Inactive Mode

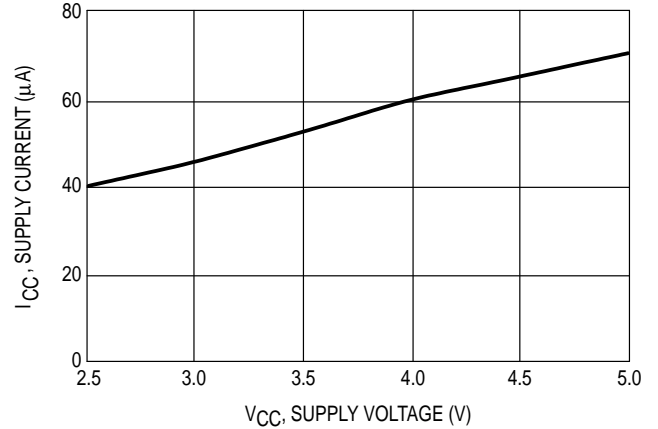


Figure 37.  $RF_{in}$  versus  $AF_{out}$ , N+D, N, AMR

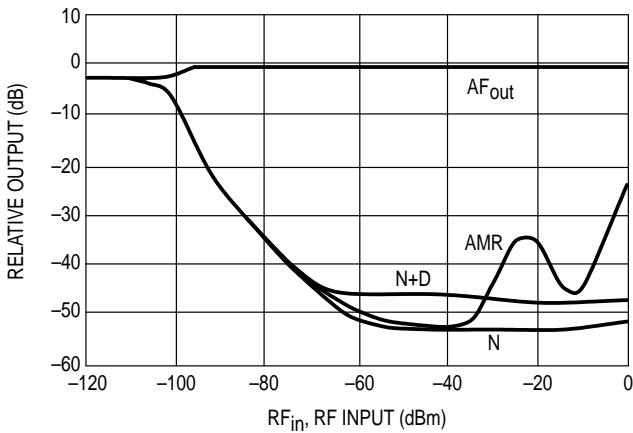


Figure 38. Recovered Audio/THD versus  $f_{DEV}$

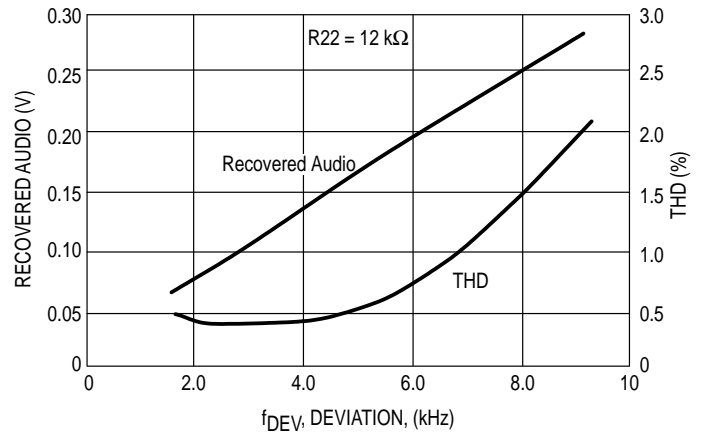


Figure 39. RSSI Output versus  $RF_{in}$

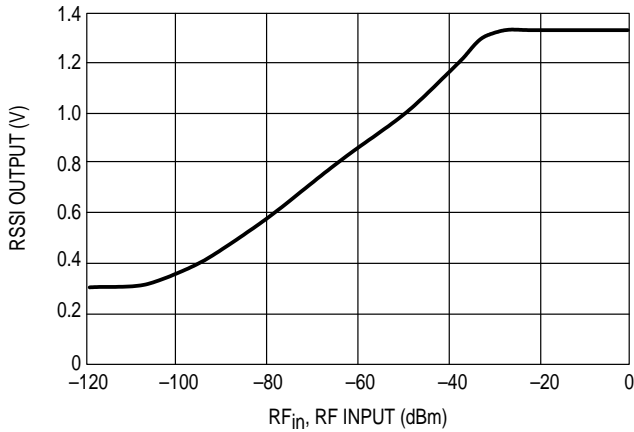
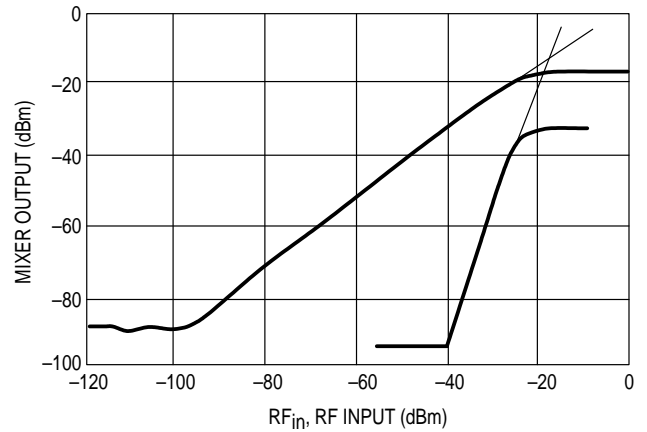


Figure 40. First Mixer Third Order Intercept Performance



**APPENDIX A – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME**

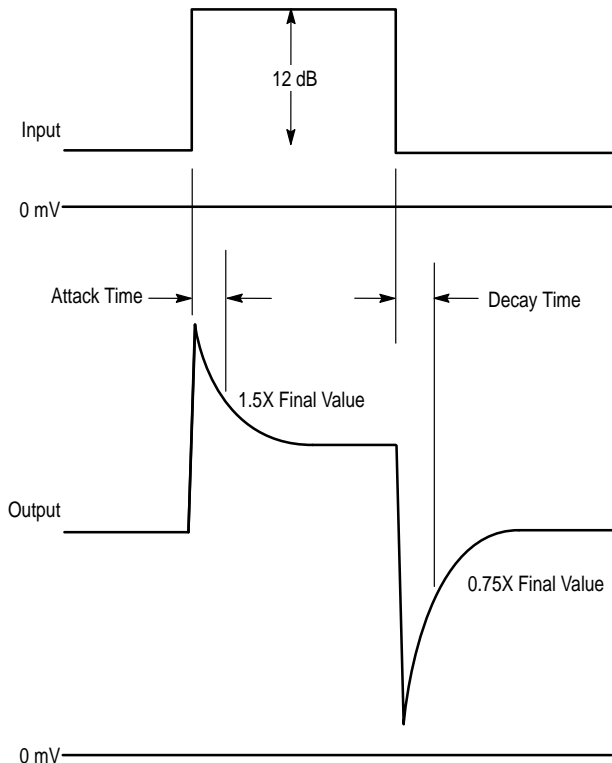
This measurement definition is based on EIA/CCITT recommendations.

**Compressor Attack Time**

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

**Compressor Decay Time**

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

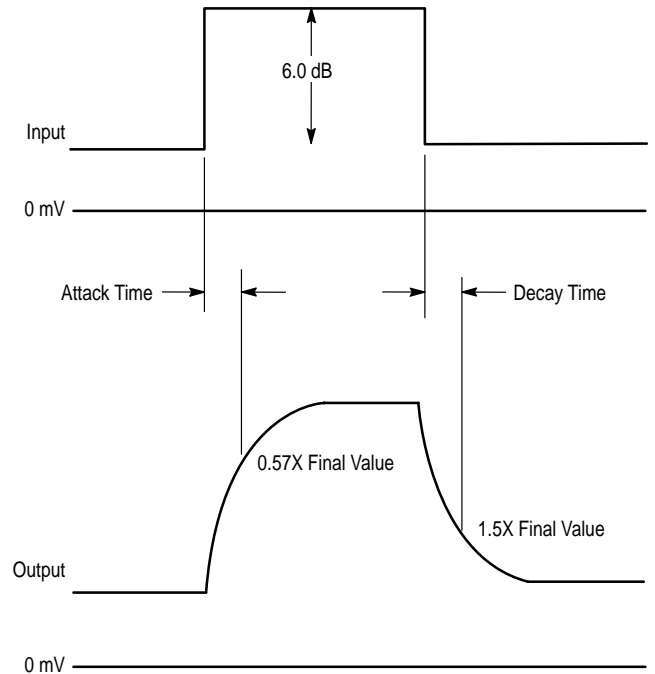


**Expander Attack**

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

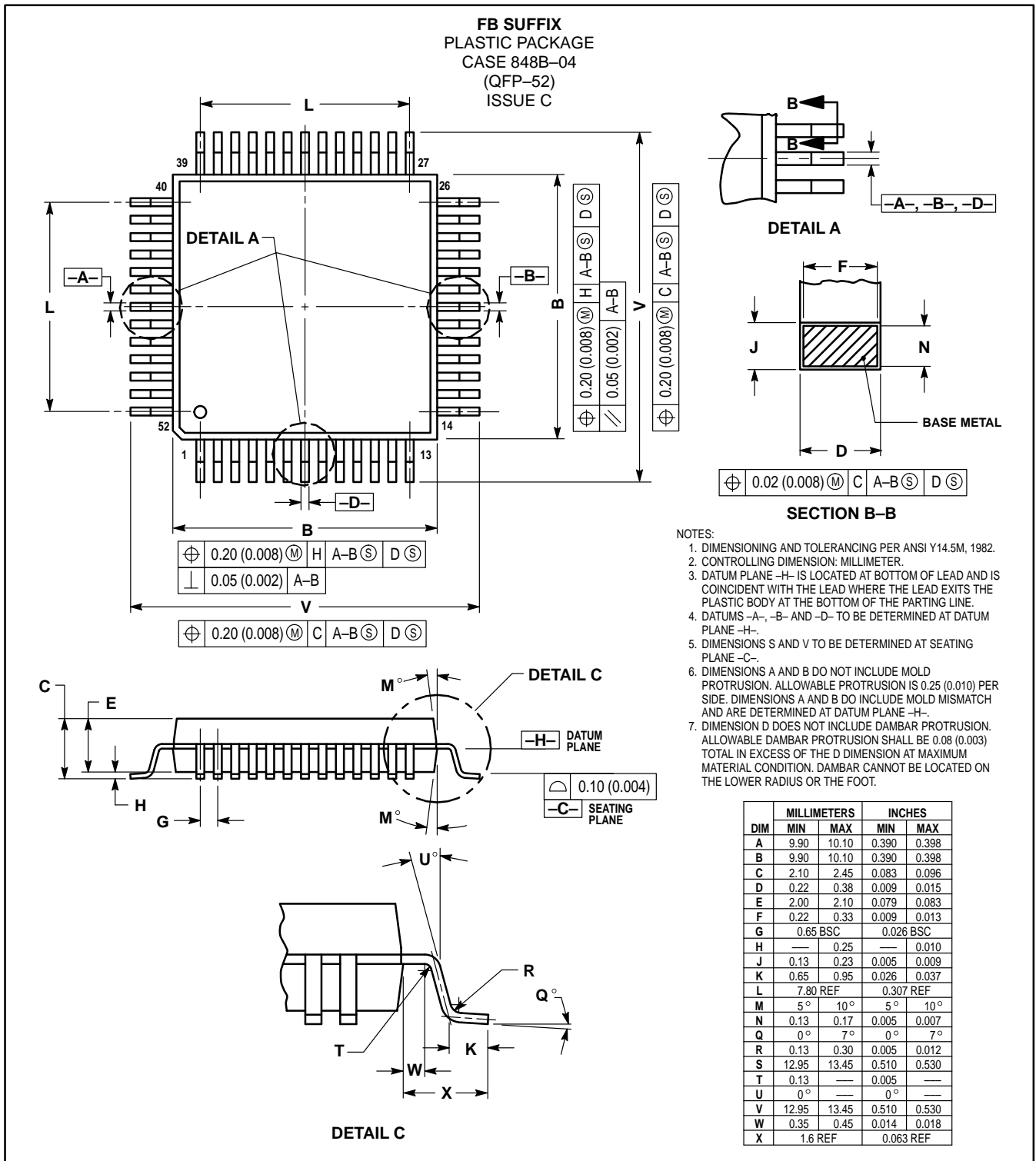
**Expander Decay**

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



# MC13109

## OUTLINE DIMENSIONS

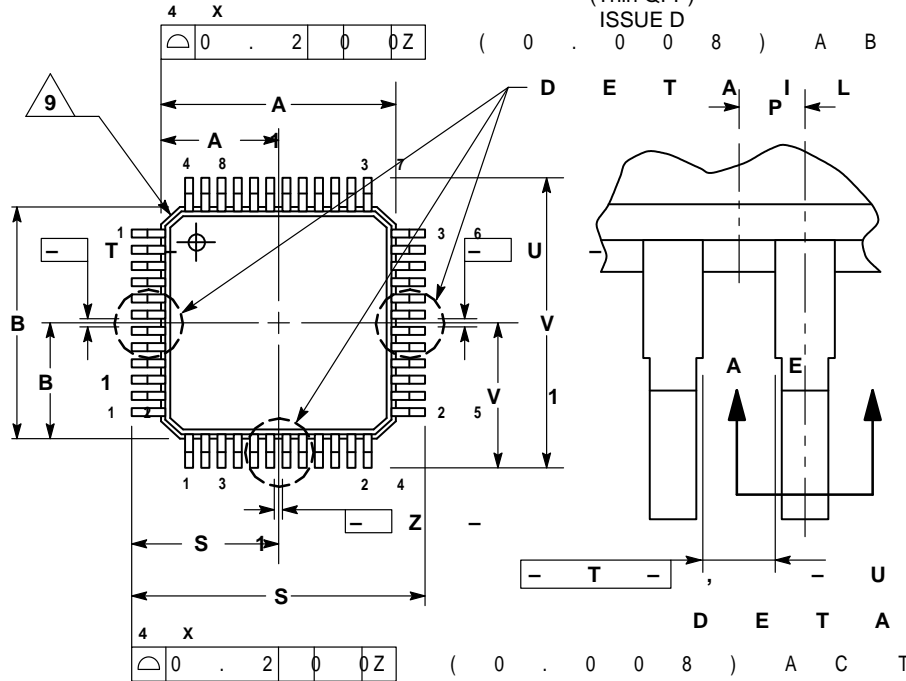


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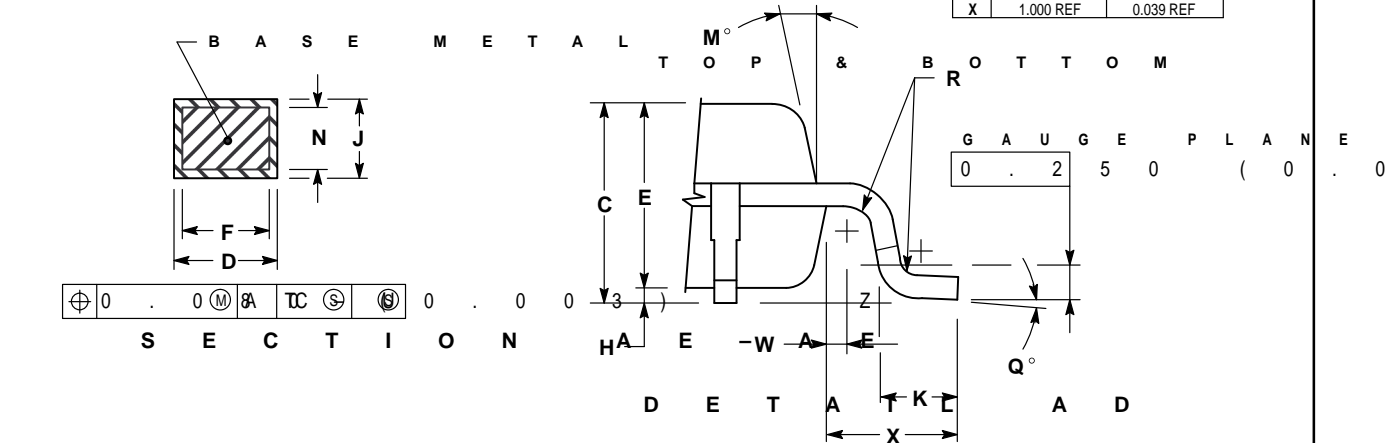
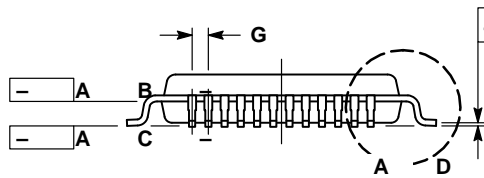
## OUTLINE DIMENSIONS

FTA SUFFIX  
PLASTIC PACKAGE  
CASE 932-02  
(Thin QFP)  
ISSUE D



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION: MILLIMETER.
  - 3 DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
  - 4 DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
  - 5 DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
  - 6 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
  - 7 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
  - 8 MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
  - 9 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	



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