Freescale Semiconductor
Data Sheet: Technical Data

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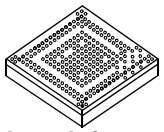
RoHS

MC13783



Package Information
Plastic Package
10 × 10 mm package

Ordering Information

Device	Device Marking or Operating Temperature Range	Package
MC13783	–30 to +85°C	MAPBGA-247

MC13783

Power Management and Audio Circuit

1 Introduction

The MC13783 is a highly integrated power management and audio component dedicated to handset and portable applications covering GSM, GPRS, EDGE, and UMTS standards. The MC13783 implements high-performance audio functions suited to high-end applications such as smartphones and UMTS handsets.

The MC13783 provides the following key benefits:

- Full power management and audio functionality in one module optimizes system size.
- High level of integration reduces the power management and audio system bill of materials.
- Versatile solution offers large possibilities of flexibility through simple programming (64 registers of 24-bit data).
- Implemented DVS saves significant battery resources in every mode (compatibility with a large number of processors).
- Dual channel voice ADC improves intelligibility.

Contents

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The detailed block diagram of the MC13783 in Figure 1 shows the wide functionality of the MC13783, including the following features:

- Battery charger interface for wall charging and USB charging
- 10 bit ADC for battery monitoring and other readout functions
- Buck switchers for direct supply of the processor cores
- Boost switcher for backlight and USB on the go supply
- Regulators with internal and external pass devices
- Transmit amplifiers for two handset microphones and a headset microphone
- Receive amplifiers for earpiece, loudspeaker, headset and line out
- 13 bit Voice CODEC with dual ADC channel and both narrow and wide band sampling
- 13 bit Stereo recording from an analog input source such as FM radio
- 16 bit Stereo DAC supporting multiple sample rates
- Dual SSI audio bus with network mode for connection to multiple devices
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry
- Dual SPI control bus with arbitration mechanism
- Multiple backlight drivers and LED control including funlight support
- USB FS/LS transceiver with OTG and CEA-936-A Carkit support
- Touchscreen interface

The main functions of the MC13783 are described in the following sections. A detailed block diagram is shown in Figure 1, on page 3.

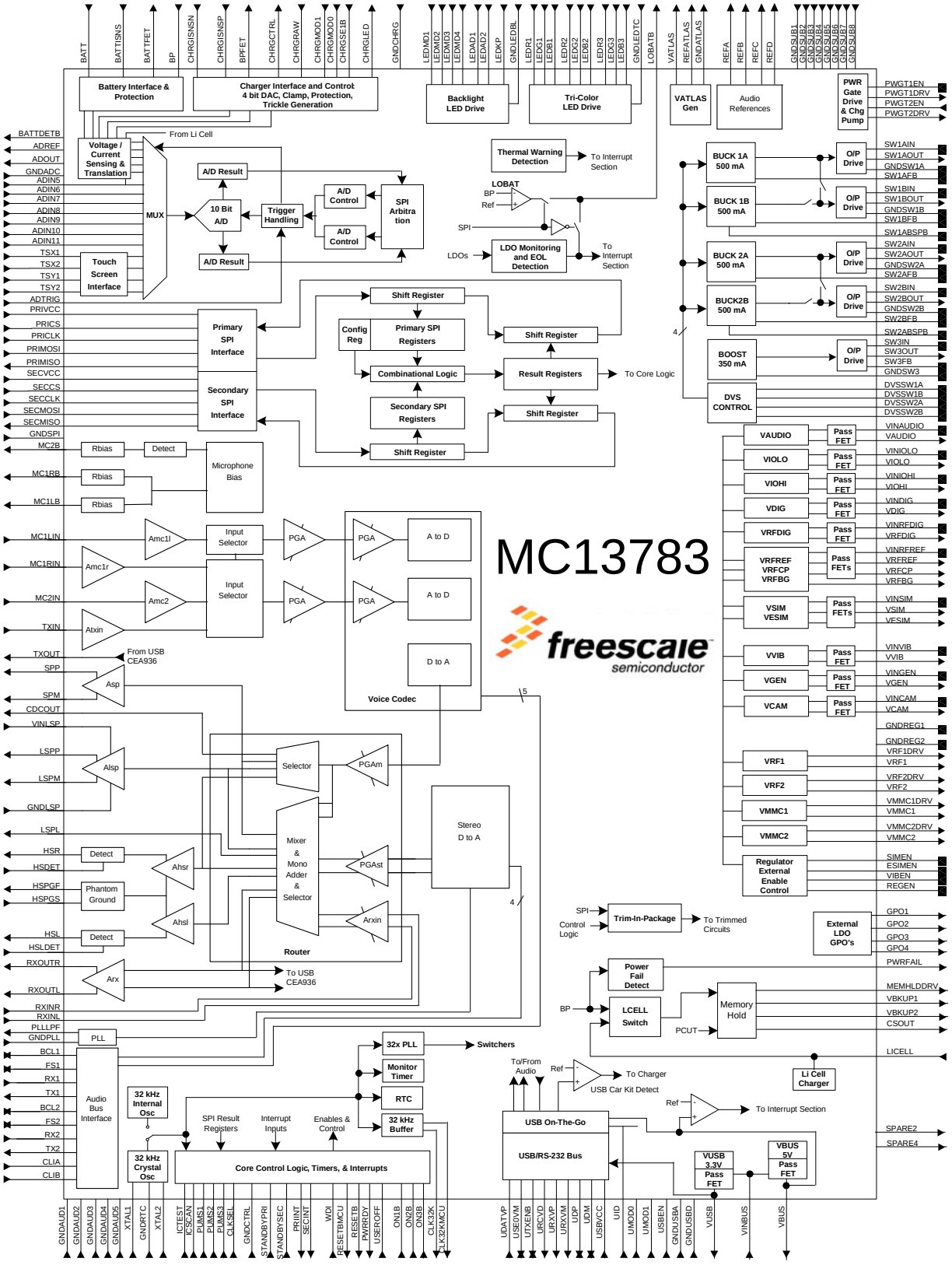

Figure 1. MC13783 Detailed Block Diagram

1.1 Audio

The audio section is composed of microphone amplifiers and speaker amplifiers, a voice CODEC, and a stereo DAC.

Three microphone amplifiers are available for amplification of two handset microphones and of the headset microphone. The feedback networks are fully integrated for a current input arrangement. A line input buffer amplifier is provided for connecting external sources. All microphones have their own stabilized supply with an integrated microphone sensitivity setting. The microphone supplies can be disabled. The headset microphone supply has a fully integrated microphone detection.

Several speaker amplifiers are provided. A bridged earpiece amplifier is available to drive an earpiece. Also, a battery supplied bridged amplifier with thermal protection is included to drive a low ohmic speaker for speakerphone and alert functionality. The performance of this amplifier allows it to be used as well for earpiece drive to support applications with a single transducer combining earpiece, speakerphone and alert functionality, thus avoiding the use of multiple transducers.

A left audio out is provided which in combination with a discrete power amplifier and the integrated speaker amplifier allows for a stereo speaker application. Two, single-ended amplifiers are included for the stereo headset drive including headset detection. The stereo headset return path is connected to a phantom ground which avoids the use of large DC decoupling capacitors. The additional stereo receive signal outputs can be used for connection to external accessories like a car kit. Via a stereo line in, external sources such as an FM radio or standalone midi ringer can be applied to the receive path.

A voice CODEC with a dual path ADC is implemented following GSM audio requirements. Both narrow band and wide band voice is supported. The dual path ADC allows for conversion of two microphone signal sources at the same time for noise cancellation or stereo applications as well as for stereo recording from sources like FM radio. A 16-bit stereo DAC is available which supports multi-clock modes. An on-board PLL ensures proper clock generation. The voice CODEC and the stereo DAC can be operated at the same time via two interchangeable buses supporting master and slave mode, network mode, as well as the different protocols like I2S.

Volume control is included in both transmit and receive paths. The latter also includes a balance control for stereo. The mono adder in the receive path allows for listening to a stereo source on a mono transducer. The receive paths for stereo and mono are separated to allow the two sources to be played back simultaneously on different outputs. The different sources can be analog mixed and two sources on the SSI configured in network mode can be mixed as well.

1.2 Switchers and Regulators

The MC13783 provides most of the telephone reference and supply voltages.

Four down converters and an up converter are included. The down, or buck, converters provide the supply to the processors and to other low voltage circuits such as IO and memory. The four down converters can be combined into two higher power converters. Dynamic voltage scaling is provided on each of the down converters. This allows under close processor control to adapt the output voltage of the converters to minimize processor current drain. The up, or boost, converter supplies the white backlight LEDs and the

regulators for the USB transceiver. The boost converter output has a backlight headroom tracking option to reduce overall power consumption.

The regulators are directly supplied from the battery or from the switchers and include supplies for IO and peripherals, audio, camera, multi media cards, SIM cards, memory and the transceivers. Enables for external discrete regulators are included as well as a vibrator motor regulator. A dedicated preamplifier audio output is available for multifunction vibrating transducers.

Drivers for power gating with external NMOS transistors are provided including a fully integrated charge pump. This will allow to power down parts of the processor to reduce leakage current.

1.3 Battery Management

The MC13783 supports different charging and supply schemes including single path and serial path charging. In single path charging, the phone is always supplied from the battery and therefore always has to be present and valid. In a serial path charging scheme, the phone can operate directly from the charger while the battery is removed or deeply discharged.

The charger interface provides linear operation via an integrated DAC and unregulated operation like used for pulsed charging. It incorporates a standalone trickle charge mode in case of a dead battery with LED indicator driver. Over voltage, short circuit and under voltage detectors are included as well as charger detection and removal. The charger includes the necessary circuitry to allow for USB charging and for reverse supply to an external accessory. The battery management is completed by a battery presence detector and an A to D converter that serves for measuring the charge current, battery and other supply voltages as well as for measuring the battery thermistor and die temperature.

1.4 Logic

The MC13783 is fully programmable via SPI bus. Additional communication is provided by direct logic interfacing. Default startup of the device is selectable by hard-wiring the power up mode select pins.

Both the call processor and the applications processor have full access to the MC13783 resources via two independent SPI busses. The primary SPI bus is able to allow the secondary SPI bus to control all or some of the registers. On top of this an arbitration mechanism is built in for the audio, the power and ADC functions. This together will avoid programming conflicts in case of a dual processor type of application.

The power cycling of the phone is driven by the MC13783. It has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures the supply of the memory and other circuits from the coin cell in case of brief power failures. A charger for the coin cell is included as well. Several pre-selectable power modes are provided such as SDRAM self refresh mode and user off mode.

The MC13783 provides the timekeeping based on an integrated low power oscillator running with a standard watch crystal. This oscillator is used for internal clocking, the control logic, and as a reference for the switcher PLL. The timekeeping includes time of day, calendar and alarm. The clock is put out to the processors for reference and deep sleep mode clocking.

1.5 Miscellaneous Functions

The drivers and comparators for a USB On-the-Go and a CEA-936-A compatible USB carkit including audio routing, as well as RS232 interfaces are provided. Special precautions are taken to allow for specific booting and accessory detection modes.

Current sources are provided to drive tricolored funlights and signaling LEDs. The funlights have preprogrammed lighting patterns. The wide programmability of the tricolored LED drivers allows for applications such as audio modulation. Three backlight drivers with auto dimming are included as well for keypad and dual display backlighting.

A dedicated interface in combination with the A to D converter allow for precise resistive touchscreen reading. Pen touch wake up is included.

2 Signal Descriptions

The below pinout description gives the pin name per functional block with its row-column coordinates, its maximum voltage rating, and a functional description.

Table 1. Pinout Listing

Pin	Location	Rating*	Function
Charger			
CHRGRAW	A18 A19 B19	EHV	1. Charger input 2. Output to battery supplied accessories
CHRGCTRL	C18	EHV	Driver output for charger path FETs M1 and M2
BPFET	B15	EHV	1. Driver output for dual path regulated BP FET M4 2. Driver output for separate USB charger path FETs M5 and M6
CHRGISNSP	B17	MV	Charge current sensing point 1
CHRGISNSN	C14	MV	Charge current sensing point 2
BP	B13	MV	1. Application supply point 2. Input supply to the MC13783 core circuitry 3. Application supply voltage sense
BATTFET	A12	MV	Driver output for battery path FET M3
BATTISNS	A14	MV	Battery current sensing point 1
BATT	D15	MV	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
CHRGMOD0	D17	LV	Selection of the mode of charging
CHRGMOD1	A16	LV	Selection of the mode of charging

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
CHRGSE1B	F15	LV	Charger forced SE1 detection input
CHRGLED	D13	EHV	Trickle LED driver output
GNDCHRG	J11	—	Ground for charger interface
LED Drivers			
LEDMD1	B8	EMV	Main display backlight LED driver output 1
LEDMD2	F9	EMV	Main display backlight LED driver output 2
LEDMD3	E9	EMV	Main display backlight LED driver output 3
LEDMD4	C9	EMV	Main display backlight LED driver output 4
LEDAD1	C8	EMV	Auxiliary display backlight LED driver output 1
LEDAD2	E8	EMV	Auxiliary display backlight LED driver output 2
LEDKP	C7	EMV	Keypad lighting LED driver output
LEDR1	B10	EMV	Tricolor red LED driver output 1
LEDG1	E11	EMV	Tricolor green LED driver output 1
LEDB1	F11	EMV	Tricolor blue LED driver output 1
LEDR2	E10	EMV	Tricolor red LED driver output 2
LEDG2	F10	EMV	Tricolor green LED driver output 2
LEDB2	G10	EMV	Tricolor blue LED driver output 2
LEDR3	F8	EMV	Tricolor red LED driver output 3
LEDG3	C10	EMV	Tricolor green LED driver output 3
LEDB3	B9	EMV	Tricolor blue LED driver output 3
GNDLEDBL	H10	—	Ground for backlight LED drivers
GNDLEDTC	J10	—	Ground for tricolor LED drivers
MC13783 Core			
VATLAS	C12	LV	Regulated supply output for the MC13783 core circuitry
REFATLAS	B11	LV	Main bandgap reference
GNDATLAS	H11	—	Ground for the MC13783 core circuitry
Switchers			
SW1AIN	K18	MV	Switcher 1A input
SW1AOUT	K17	MV	Switcher 1A output
SW1AFB	L18	LV	Switcher 1A feedback

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
DVSSW1A	J15	LV	Dynamic voltage scaling logic input for switcher 1A
GNDSW1A	L17	—	Ground for switcher 1A
SW1BIN	N18	MV	Switcher 1B input
SW1BOUT	N17	MV	Switcher 1B output
SW1BFB	M18	LV	Switcher 1B feedback
DVSSW1B	K15	LV	Dynamic voltage scaling logic input for switcher 1B
GNDSW1B	M17	—	Ground for switcher 1B
SW2AIN	P18	MV	Switcher 2A input
SW1ABSPB	P11	LV	SW1 mode configuration
SW2AOUT	R18	MV	Switcher 2A output
SW2AFB	P15	LV	Switcher 2A feedback
DVSSW2A	H15	LV	Dynamic voltage scaling logic input for switcher 2A
GNDSW2A	P17	—	Ground for switcher 2A
SW2BIN	U18	MV	Switcher 2B input
SW2BOUT	T18	MV	Switcher 2B output
SW2BFB	R17	LV	Switcher 2B feedback
DVSSW2B	J14	LV	Dynamic voltage scaling logic input for switcher 2B
GNDSW2B	T17	—	Ground for switcher 2B
SW2ABSPB	R12	LV	SW2 mode configuration
SW3IN	J17	HV	Switcher 3 input
SW3OUT	H18	HV	Switcher 3 output
SW3FB	H17	HV	Switcher 3 feedback
GNDSW3	J18	—	Ground for switcher 3
Power Gating			
PWGT1EN	L14	LV	Power gate driver 1 enable
PWGT1DRV	M15	EMV	Power gate driver 1 output
PWGT2EN	L15	LV	Power gate driver 2 enable
PWGT2DRV	K14	EMV	Power gate driver 2 output
Regulators			
VINAUDIO	U12	MV	Input regulator audio

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
VAUDIO	U10	LV	Output regulator audio
VINIOLO	U13	MV	Input regulator low voltage IO
VIOLO	V13	LV	Output regulator low voltage IO
VINIOHI	B7	MV	Input regulator high voltage IO
VIOHI	B6	LV	Output regulator high voltage IO
VINDIG	R11	MV	Input regulator general digital
VDIG	U11	LV	Output regulator general digital
VINRFDIG	K5	MV	Input regulator transceiver digital
VRFDIG	K2	LV	Output regulator transceiver digital
VINRFREF	K7	MV	Input regulator transceiver reference
VRFREF	G3	LV	Output regulator transceiver reference
VRFCP	G2	LV	Output regulator transceiver charge pump
VRFBG	C11	LV	Bandgap reference output for transceiver
VINSIM	F2	MV	Input regulator SIM card and eSIM card
VSIM	E3	LV	Output regulator SIM card
VESIM	F3	LV	Output regulator eSIM card
VINVIB	G5	MV	Input regulator vibrator motor
VVIB	E2	LV	Output regulator vibrator motor
VINGEN	G17	MV	Input regulator graphics accelerator
VGEN	G18	LV	Output regulator graphics accelerator
VINCAM	V12	MV	Input regulator camera
VCAM	V11	LV	Output regulator camera
VRF2DRV	J6	MV	Drive output regulator transceiver
VRF2	J5	LV	Output regulator transceiver
VRF1DRV	K8	MV	Drive output regulator transceiver
VRF1	J3	LV	Output regulator transceiver
VMMC1DRV	L7	MV	Drive output regulator MMC1 module
VMMC1	K6	LV	Output regulator MMC1 module
VMMC2DRV	J2	MV	Drive output regulator MMC2 module
VMMC2	K3	LV	Output regulator MMC2 module

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
SIMEN	D19	LV	VSIM enable input
ESIMEN	F16	LV	VESIM enable input
VIBEN	E19	LV	VVIB enable input
REGEN	E18	LV	Regulator enable input
GPO1	G8	LV	General purpose output 1 to be used for enabling a discrete regulator
GPO2	F6	LV	General purpose output 2 to be used for enabling a discrete regulator
GPO3	E5	LV	General purpose output 3 to be used for enabling a discrete regulator
GPO4	G9	LV	General purpose output 4 to be used for enabling a discrete regulator
GNDREG1	N12	—	Ground for regulators 1
GNDREG2	K10	—	Ground for regulators 2
USB/RS232			
UDP	C2	EMV	1. USB transceiver cable interface, D+ 2. RS232 transceiver cable interface, transmit output or receive input signal
UDM	D2	EMV	1. USB transceiver cable interface, D- 2. RS232 transceiver cable interface, receive input or transmit output signal
UID	F7	EMV	USB on the go transceiver cable ID resistor connection
UDATVP	C5	LV	1. USB processor interface transmit data input (logic level version of D+/D-) or transmit positive data input (logic level version of D+) 2. Optional USB processor interface receive data output (logic level version of D+/D-) 3. RS232 processor interface
USE0VM	C6	LV	1. USB processor interface transmit single ended zero signal input or transmit minus data input (logic level version of D-) 2. Optional USB processor interface received single ended zero output 3. Optional RS232 processor interface
UTXENB	C4	LV	1. USB processor interface transmit enable bar
URCVD	B5	LV	Optional USB receiver processor interface differential data output (logic level version of D+/D-)
URXVP	B3	LV	Optional USB receiver processor interface data output (logic level version of D+)
URXVM	B2	LV	1. Optional USB receiver processor interface data output (logic level version of D-) 2. Optional RS232 processor interface
UMOD0	H7	LV	USB transceiver operation mode selection at power up 0
UMOD1	G6	LV	USB transceiver operation mode selection at power up 1
USBEN	C3	LV	Bootmode enable for USB/RS232 interface
VINBUS	B4	EMV	Input for VBUS and VUSB regulators for USB on the go mode

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
VBUS	D3	EHV EMV	When in common input configuration, shorted to CHRGRAW 1. USB transceiver cable interface VBUS 2. Output VBUS regulator in USB on the go mode When in separate input configuration, not shorted to CHRGRAW 1. USB transceiver cable interface VBUS 2. Output VBUS regulator in USB on the go mode
VUSB	F5	MV	Output VUSB regulator as used by the USB transceiver
USBVCC	E7	LV	Supply for processor interface
GNDUSBA	A1 A2 B1	—	Ground for USB transceiver and USB cable
GNDUSBD	K9	—	Ground for USB processor interface
Control Logic			
ON1B	E16	LV	Power on/off button connection 1
ON2B	E15	LV	Power on/off button connection 2
ON3B	G14	LV	Power on/off button connection 3
WDI	F17	LV	Watchdog input
RESETB	G15	LV	Reset output
RESETBMCU	F18	LV	Reset for the processor
STANDBYPRI	H14	LV	Standby input signal from primary processor
STANDBYSEC	J13	LV	Standby input signal from secondary processor
LOBATB	N14	LV	Low battery indicator signal or end of life indicator signal
PWRRDY	U17	LV	Power ready signal after DVS and power gate transition
PWRFAIL	F13	LV	Powerfail indicator output to processor or system
USEROFF	E14	LV	User off signaling from processor
MEMHLDDRV	G12	LV	Memory hold FET drive for power cut support
CSOUT	G11	LV	Chip select output for memory
LICELL	C16	MV	1. Coincell supply input 2. Coincell charger output
VBKUP1	E12	LV	Backup output voltage for memory
VBKUP2	F12	LV	Backup output voltage for processor core
GNDCTRL	J12	—	Ground for control logic

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
Oscillator and Real Time Clock			
XTAL1	V16	LV	32.768 kHz Oscillator crystal connection 1
XTAL2	V14	LV	32.768 kHz Oscillator crystal connection 2
CLK32K	R14	LV	32 kHz Clock output
CLK32KMCU	E13	LV	32 kHz Clock output to the processor
CLKSEL	U16	LV	Enables the RC clock routing to the outputs
GNDRTC	V15	—	Ground for the RTC block
Power Up Select			
PUMS1	H6	LV	Power up mode supply setting 1
PUMS2	J7	LV	Power up mode supply setting 2
PUMS3	H5	LV	Power up mode supply setting 3
ICTEST	F14	LV	Test mode selection
ICSCAN	U14	LV	Scan mode selection
SPI Interface			
PRIVCC	N2	LV	Supply for primary SPI bus and audio bus 1
PRICLK	N5	LV	Primary SPI clock input
PRIMOSI	N8	LV	Primary SPI write input
PRIMISO	P7	LV	Primary SPI read output
PRICS	N6	LV	Primary SPI select input
PRIINT	P5	LV	Interrupt to processor controlling the primary SPI bus
SECVCC	N3	LV	Supply for secondary SPI bus and audio bus 2
SECCLK	P6	LV	Secondary SPI clock input
SECMOSI	R6	LV	Secondary SPI write input
SECMISO	R5	LV	Secondary SPI read output
SECCS	P8	LV	Secondary SPI select input
SECINT	R7	LV	Interrupt to processor controlling the secondary SPI bus
GNDSPI	L9	LV	Ground for SPI interface
A to D Converter			
BATTDETB	K13	LV	Battery thermistor presence detect output
ADIN5	M14	LV	ADC generic input channel 5, group 1

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
ADIN6	U15	LV	ADC generic input channel 6, group 1
ADIN7	R15	LV	ADC generic input channel 7, group 1
ADIN8	P14	LV	ADC generic input channel 8, group 2
ADIN9	V17	LV	ADC generic input channel 9, group 2
ADIN10	V18	LV	ADC generic input channel 10, group 2
ADIN11	V19 W18 W19	LV	ADC generic input channel 11, group 2
TSX1	P13	LV	ADC generic input channel 12 or touchscreen input X1, group 2
TSX2	L13	LV	ADC generic input channel 13 or touchscreen input X2, group 2
TSY1	P12	LV	ADC generic input channel 14 or touchscreen input Y1, group 2
TSY2	M13	LV	ADC generic input channel 15 or touchscreen input Y2, group 2
ADREF	R13	LV	Reference for ADC and touchscreen interface
ADTRIG	N15	LV	ADC trigger input
ADOUT	E6	LV	ADC trigger output
GNDADC	L12	—	Ground for A to D circuitry
Audio Bus			
BCL1	M7	LV	Bit clock for audio bus 1. Input in slave mode, output in master mode
FS1	M9	LV	Frame synchronization clock for audio bus 1. Input in slave mode, output in master mode
RX1	L5	LV	Receive data input for audio bus 1
TX1	M6	LV	Transmit data output for audio bus 1
BCL2	M8	LV	Bit clock for audio bus 2. Input in slave mode, output in master mode
FS2	M2	LV	Frame synchronization clock for audio bus 2. Input in slave mode, output in master mode
RX2	M3	LV	Receive data input for audio bus 2
TX2	M5	LV	Transmit data output for audio bus 2
CLIA	L6	LV	Clock input for audio bus 1 or 2
CLIB	L3	LV	Clock input for audio bus 1 or 2
Audio Transmit			
MC1RB	R2	LV	Handset primary or right microphone supply output with integrated bias resistor
MC1LB	P3	LV	Handset secondary or left microphone supply output with integrated bias resistor

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
MC2B	P2	LV	Headset microphone supply output with integrated bias resistor and detect
MC1RIN	V2	LV	Handset primary or right microphone amplifier input
MC1LIN	U2	LV	Handset secondary or left microphone amplifier input
MC2IN	U3	LV	Headset microphone amplifier input
TXIN	U4	LV	General purpose line level transmit input
TXOUT	V3	LV	Buffered output of CEA-936-A microphone signal
Audio Receive			
SPP	V9	LV	Handset earpiece speaker amplifier output positive terminal
SPM	V10	LV	Handset earpiece speaker amplifier output minus terminal
VINLSP	V6	MV	Handset loudspeaker and alert amplifier supply input
LSPP	V5	MV	Handset loudspeaker and alert amplifier positive terminal
LSPM	V4	MV	Handset loudspeaker and alert amplifier minus terminal
GNDLSP	V1 W1 W2	—	Ground for loudspeaker amplifier
LSPL	U5	LV	Low power output for discrete loudspeaker amplifier, associated to left channel audio
CDCOUT	U6	LV	Low power output for discrete amplifier, associated to voice CODEC channel
HSL	V8	LV	Headset left channel amplifier output
HSR	U9	LV	Headset right channel amplifier output
HSPGF	V7	LV	Headset phantom ground power line (force)
HSPGS	P10	LV	Headset phantom ground feedback line (sense)
HSDET	R10	LV	Headset sleeve detection input
HSLDET	R8	LV	Headset left detection input
RXOUTR	U7	LV	Low power receive output for accessories right channel
RXOUTL	P9	LV	Low power receive output for accessories left channel
RXINR	R9	LV	General purpose receive input right channel
RXINL	U8	LV	General purpose receive input left channel
Audio Other			
REFA	R3	LV	Reference for audio amplifiers
REFB	T3	LV	Reference for low noise audio bandgap
REFC	T2	LV	Reference for voice CODEC

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Table 1. Pinout Listing (continued)

Pin	Location	Rating*	Function
REFD	L2	LV	Reference for stereo DAC
PLLLPF	H2	LV	Connection for the stereo DAC PLL low pass filter.
GNDPLL	H3	—	Dedicated ground for the stereo DAC PLL block.
GNDAUD1	L10	—	Ground for audio circuitry 1 (analog)
GNDAUD2	M10	—	Ground for audio circuitry 2 (analog)
GNDAUD3	M11	—	Ground for audio circuitry 3 (analog)
GNDAUD4	M12	—	Ground for audio circuitry 4 (digital)
GNDAUD5	H9	—	Ground for audio circuitry 5 (digital)
Thermal Grounds			
GNDSUB1	N11	—	Non critical signal ground and thermal heatsink
GNDSUB2	K12	—	Non critical signal ground and thermal heatsink
GNDSUB3	K11	—	Non critical signal ground and thermal heatsink
GNDSUB4	H12	—	Non critical signal ground and thermal heatsink
GNDSUB5	J9	—	Non critical signal ground and thermal heatsink
GNDSUB6	J8	—	Non critical signal ground and thermal heatsink
GNDSUB7	L8	—	Non critical signal ground and thermal heatsink
GNDSUB8	L11	—	Non critical signal ground and thermal heatsink
Future Use			
SPARE2	H8	TBD	Spare ball for future use
SPARE4	H13	TBD	Spare ball for future use

* The maximum voltage rating is given per category of pins:
- EHV for Extended High Voltage (20 V)
- HV for High Voltage (7.5 V)
- EMV for Extended Medium Voltage (5.5 V)
- MV for Medium Voltage (4.65 V)
- LV for Low Voltage (3.1 V)

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 2 gives the maximum allowed voltages, current and temperature ratings which can be applied to the IC. Exceeding these ratings could damage the circuit.

Table 2. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Charger Input Voltage	-0.3	—	+20	V
USB Input Voltage if Common to Charger	-0.3	—	+20	V
USB Input Voltage if Separate from Charger	-0.3	—	+5.50	V
Battery Voltage	-0.3	—	+4.65	V
Coincell Voltage	-0.3	—	+4.65	V
Ambient Operating Temperature Range	-30	—	+85	°C
Operating Junction Temperature Range	-30	—	+125	°C
Storage Temperature Range	-65	—	+150	°C
ESD Protection Human Body Model	2.0	—	—	kV

3.2 Current Consumption

The current consumption of the individual blocks is described in detail throughout this specification. For convenience, below a summary table is included with the main characteristics. Note that the external loads are not taken into account.

Table 3. Summary of Current Consumption

Mode	Typ	Max	Unit
RTC	5	6	µA
OFF	30	45	µA
Power Cut	35	52	µA
User OFF	60	91	µA
ON Standby	135	220	µA
ON Default	620	1000	µA
ON Audio Call	7.3	9.9	mA
ON Stereo Playback	9.5	12.1	mA

4 Functional Description

4.1 Logic

The logic portions of the MC13783 includes the following:

- Section 4.1.1, "Programmability," on page 17 includes a description of the dual SPI interface.
- Section 4.1.2, "Clock Generation and Real Time Clock," on page 21 includes a description of the 32.768 kHz real time clock generation.
- Section 4.1.3, "Power Control System," on page 22 describes the power control logic, including interface and operated modes.

4.1.1 Programmability

4.1.1.1 SPI Interface

The MC13783 IC contains two SPI interface ports which allow parallel access by both the call processor and the applications processor to the MC13783 register set. Via these registers the MC13783 resources can be controlled. The registers also provide status information about how the MC13783 IC is operating as well as information on external signals. The SPI interface is comprised of the signals listed below.

Table 4. SPI Interface Pin Description

	Description
SPI Bus	
PRICLK	Primary processor clock input line, data shifting occurs at the rising edge.
PRIMOSI	Primary processor serial data input line.
PRIMISO	Primary processor serial data output line.
PRICS	Primary processor clock enable line, active high.
SECCLK	Secondary processor clock input line, data shifting occurs at the rising edge.
SECMOSI	Secondary processor serial data input line.
SECMISO	Secondary processor serial data output line.
SECCS	Secondary processor clock enable line, active high.
Interrupt	
PRIINT	Primary processor interrupt.
SECINT	Secondary processor interrupt.
Supply	
PRIVCC	Primary processor SPI bus supply.
SECVCC	Secondary processor SPI bus supply

Both SPI ports are configured to utilize 32-bit serial data words, using 1 read/write bit, 6 address bits, 1 null bit, and 24 data bits. The SPI ports' 64 registers correspond to the 6 address bits.

4.1.1.2 Register Set

The register set is given in Table 5.

Table 5. Register Set

Register		Register		Register		Register	
0	Interrupt Status 0	16	Regen Assignment	32	Regulator Mode 0	48	Charger
1	Interrupt Mask 0	17	Control Spare	33	Regulator Mode 1	49	USB 0
2	Interrupt Sense 0	18	Memory A	34	Power Miscellaneous	50	Charger USB 1
3	Interrupt Status 1	19	Memory B	35	Power Spare	51	LED Control 0
4	Interrupt Mask 1	20	RTC Time	36	Audio Rx 0	52	LED Control 1
5	Interrupt Sense 1	21	RTC Alarm	37	Audio Rx 1	53	LED Control 2
6	Power Up Mode Sense	22	RTC Day	38	Audio Tx	54	LED Control 3
7	Identification	23	RTC Day Alarm	39	SSI Network	55	LED Control 4
8	Semaphore	24	Switchers 0	40	Audio Codec	56	LED Control 5
9	Arbitration Peripheral Audio	25	Switchers 1	41	Audio Stereo DAC	57	Spare
10	Arbitration Switchers	26	Switchers 2	42	Audio Spare	58	Trim 0
11	Arbitration Regulators 0	27	Switchers 3	43	ADC 0	59	Trim 1
12	Arbitration Regulators 1	28	Switchers 4	44	ADC 1	60	Test 0
13	Power Control 0	29	Switchers 5	45	ADC 2	61	Test 1
14	Power Control 1	30	Regulator Setting 0	46	ADC 3	62	Test 2
15	Power Control 2	31	Regulator Setting 1	47	ADC 4	63	Test 3

4.1.1.3 Interface Requirements

4.1.1.3.1 SPI Interface Description

The operation of both SPI interfaces is equivalent. Therefore, all SPI bus names without prefix PRI or SEC correspond to both the PRISPI and SECSPI interfaces.

The control bits are organized into 64 fields. Each of these 64 fields contains 32 bits. A maximum of 24 data bits is used per field. In addition, there is one “dead” bit between the data and address fields. The remaining bits include 6 address bits to address the 64 data fields and one write enable bit to select whether the SPI transaction is a read or a write.

For each SPI transfer, first a one is written to the read/write bit if this SPI transfer is to be a write. A zero is written to the read/write bit if this is to be a read command only. If a zero is written, then any data sent after the address bits are ignored and the internal contents of the field addressed do not change when the 32nd CLK is sent. Next the 6-bit address is written, MSB first. Finally, data bits are written, MSB first. Once all the data bits are written then the data is transferred into the actual registers on the falling edge of the 32nd CLK.

The default CS polarity is active high. The CS line must remain active during the entire SPI transfer. In case the CS line goes inactive during a SPI transfer all data is ignored. To start a new SPI transfer, the CS line must go inactive and then go active again. The MISO line will be tri-stated while CS is low.

Note that not all bits are truly writable. Refer to the individual subcircuit descriptions to determine the read/write capability of each bit. All unused SPI bits in each register must be written to a zero. SPI readbacks of the address field and unused bits are returned as zero. To read a field of data, the MISO pin will output the data field pointed to by the 6 address bits loaded at the beginning of the SPI sequence.

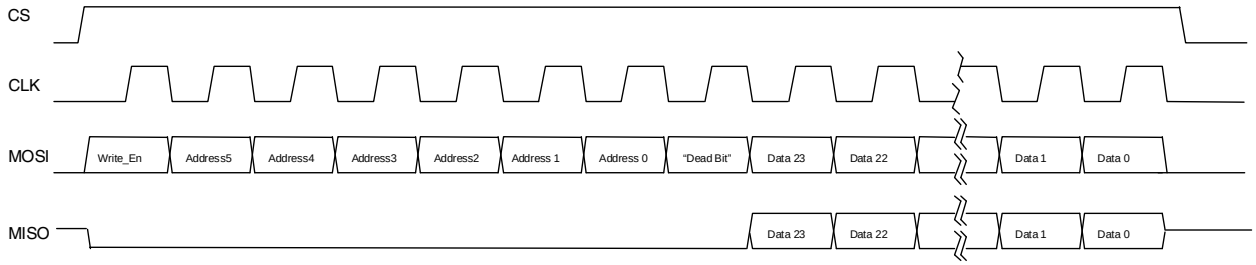

Figure 2. SPI Transfer Protocol Single Read/Write Access

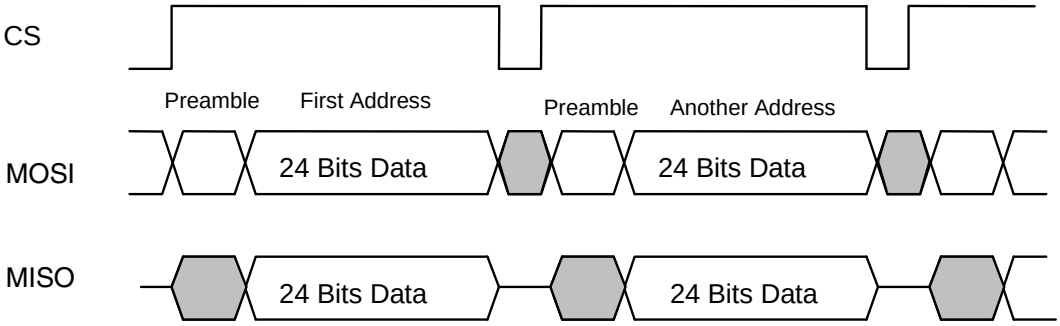

Figure 3. SPI Transfer Protocol Multiple Read/Write Access

4.1.1.3.2 SPI Requirements

The requirements for both SPI interfaces are equivalent. Therefore, all SPI bus names without prefix PRI or SEC correspond to both SPI interfaces. The below diagram and table summarize the SPI electrical and timing requirements. The SPI input and output levels are set independently via the PRIVCC and SECVCC pins by connecting those to the proper supply.

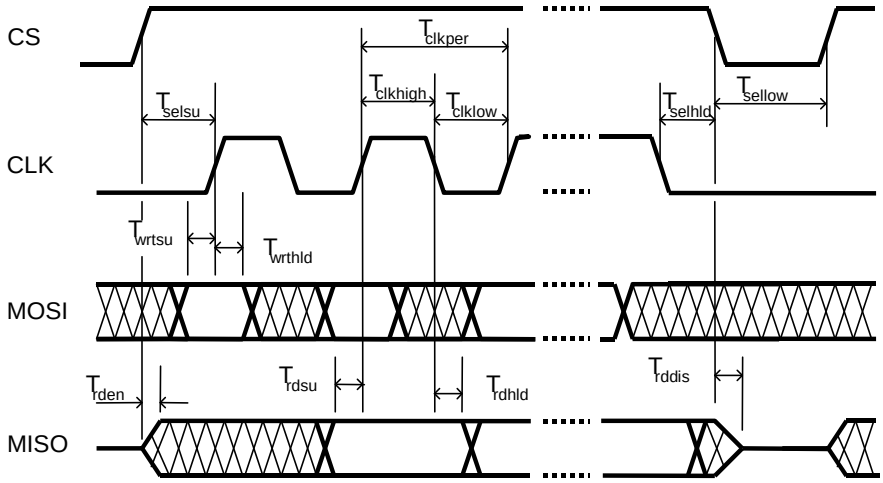

Figure 4. SPI Interface Timing Diagram

Table 6. SPI Interface Timing Specifications

Parameter	Description	T min (ns)
T_{selsu}	Time CS has to be high before the first rising edge of CLK	20
T_{selhld}	Time CS has to remain high after the last falling edge of CLK	20
T_{sellow}	Time CS has to remain low between two transfers	20
T_{clkper}	Clock period of CLK[1]	50
$T_{clkhigh}$	Part of the clock period where CLK has to remain high	20
T_{clklow}	Part of the clock period where CLK has to remain low	20
T_{wrtsu}	Time MOSI has to be stable before the next rising edge of CLK	5
T_{wrthld}	Time MOSI has to remain stable after the rising edge of CLK	5
T_{rdsu}	Time MISO will be stable before the next rising edge of CLK	5
T_{rdhld}	Time MISO will remain stable after the falling edge of CLK	5
T_{rden}	Time MISO needs to become active after the rising edge of CS	5
T_{rddis}	Time MISO needs to become inactive after the falling edge of CS	5

[1] Equivalent to a maximum clock frequency of 20 MHz.

Table 7. SPI Interface Logic IO Specifications

Parameter	Condition	Min	Max	Units
Input High CS, MOSI, CLK	—	0.7*VCC	VCC+0.5	V
Input Low CS, MOSI, CLK	—	0	0.3*VCC	V
Output Low MISO, INT	Output sink 100 μA	0	0.2	V
Output High MISO, INT	Output source 100 μA	VCC-0.2	VCC	V
Note: VCC refers to PRIVCC and SECVCC respectively.				

4.1.2 Clock Generation and Real Time Clock

4.1.2.1 Clock Generation

The MC13783 generates a 32.768 kHz clock as well as several 32.768 kHz derivative clocks that are used internally for control. In addition, a 32.768 kHz square wave is output to external pins.

4.1.2.1.1 Clocking Scheme

The MC13783 contains an internal RC oscillator powered from VATLAS that delivers a 32 kHz nominal frequency (±20%) at its output when an external 32.768 kHz crystal is not present. The RC oscillator will then be used to run the debounce logic, the PLL for the switchers, the real time clock (RTC) and internal control logic, and can also be output on the CLK32K pin.

4.1.2.2 Real Time Clock

This section provides an overview of the Real Time Clock (RTC).

4.1.2.2.1 Time and Day Counters

The real time clock runs from the 32 kHz clock. This clock is divided down to a 1 Hz time tick which drives a 17 bit time of day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399 and will then roll over to 0. When the roll over occurs, it increments the 15-bit DAY counter. The DAY counter can count up to 32767 days. The 1Hz time tick can be used to generate an 1HZI interrupt. The 1HZI can be masked with corresponding 1HZM mask bit.

If the TOD and DAY registers are read at a point in time in which DAY is incremented, then care must be taken that, if DAY is read first, DAY has not changed before reading TOD.

In order to guarantee stable TOD and DAY data, all SPI reads and writes to TOD and DAY data should happen immediately after the 1HZI interrupt occurs. Alternatively, TOD or DAY readbacks could be double-read and then compared to verify that they haven't changed. This requirement results from the fact that the 32.768 kHz clock is completely independent of the SPI clock and the two cannot be synchronized.

4.1.2.2.2 Time of Day Alarm

A Time Of Day (TOD) alarm function can be used to turn on the phone and alert the processor. If the phone is already on, the processor will be interrupted. The TODA and DAYA registers are used to set the alarm time. When the TOD counter is equal to the value in TODA and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

MC13783 makes it convenient to schedule multiple daily events, where a single list could be used, or to skip any number of days.

4.1.3 Power Control System

The power control system on MC13783 interfaces with the processors via different IO signals and the SPI bus. It also uses on-chip signals and detector outputs. It supports a system with different operating modes as described below.

Table 8. MC13783 Operating Modes

Mode	Description
Off	Only the MC13783 core circuitry at VATLAS and the RTC module are powered. To exit the Off mode requires a turn on event.
Cold Start	The switchers and regulators are powered up sequentially to limit the inrush current. At the end of the start-up phase, the RESETB and RESETBMCU will be made high and the circuit transitions to On.
On	The circuit is fully powered and under SPI control. To stay in this mode, the WDI pin has to be high and remain high. If not, the part will transition to Off mode.
Memory Hold	All switchers and regulators are powered off except for VBKUP1 and VBKUP2. The RESETB and RESETBMCU are low. The MC13783 enters Cold Start mode when a turn on event occurs.
User Off	All switchers and regulators are powered off except for VBKUP1 and VBKUP2. RESETB is low and RESETBMCU is kept high. The 32 kHz output signal CLK32KMCU can be maintained in this mode as well. The MC13783 enters Warm Start mode when a turn on event occurs.
Warm Start	The switchers and regulators are powered up sequentially to limit the inrush current. The reset signals RESETB is kept low and RESETBMCU is kept high and CLK32KMCU can be kept active. At the end of the warm start up phase, the RESETB will be made high and the circuit transitions to On.
Power Cuts	Defined as a momentary loss of power. This can be caused by battery contact bounce or a user-initiated battery swap. The memory and the processor core are automatically backed up in that case by the coin cell depending on the power cut support mode selected. The maximum duration of a power cut as well as the maximum number of power cuts to be supported are programmable. When exiting the power cut mode due to reapplication of power the system will start up again on the main battery and revert back to the battery supplied modes.
Turn On Events	If the MC13783 is in Off, User Off or Memory Hold mode, the circuit can be powered on via a turn-on event. The turn-on events are listed below. To indicate to the processor which turn-on event occurred, an interrupt bit is associated with each of the turn-on events. ON1B, ON2B or ON3B pulled low, a power on/off button is connected here. • CHRGRAW pulled high which is equivalent to plugging in a charger. • BP crossing the minimum operating threshold which corresponds to attaching a charged battery to the phone. • VBUS pulled high which is equivalent to plugging in a supplied USB cable. • Time of day alarm which allows powering up a phone at a preset time.

The default power up state and sequence of the MC13783 is controlled by the power up mode select pins PUMS1, PUMS2 and PUMS3. In total three different sequences and five different default voltage setting combinations are provided. At power up all regulators and switchers are sequentially enabled at equidistant steps of 2ms to limit the inrush current.

4.2 Switchers and Regulators

4.2.1 Supply Flow

The switch mode power supplies and the linear regulators are dimensioned to support a supply flow based upon Figure 5.

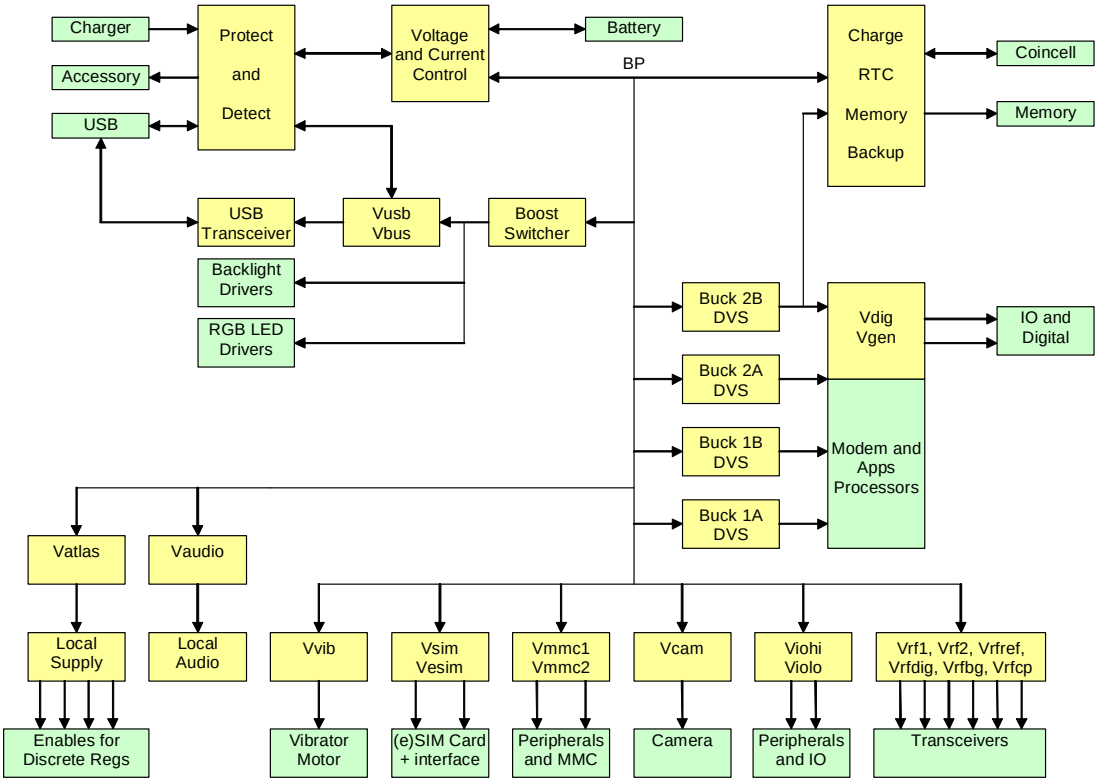

Figure 5. Supply Distribution

The minimum operating voltage for the supply tree, while maintaining the performance as specified, is 3.0 V. For lower voltages the performance may be degraded.

Table 9 summarizes supply output voltages.

Table 9. Regulator Output Voltages

Supply	Output (V)	Load (mA)	
SW1A	0.900 - 1.675 in 25 mV steps, 1.700 - 2.200 in 100 mV steps	500	1A
SW1B		500	
SW2A		500	1A
SW2B		500	
SW3	5.0 / 5.5	350/300	
VAUDIO	2.775	200	
VIOHI	2.775	200	

Table 9. Regulator Output Voltages (continued)

Supply	Output (V)	Load (mA)
VIOLO	1.2/1.3/1.5/.18	150 (Vout < 1.5V)/200 (Vout ≥ 1.5V)
VDIG	1.2/1.3/1.5/.18	150 (Vout < 1.3V)/200 (Vout ≥ 1.3V)
VRFDIG	1.2/1.5/1.8/1.875	150 (Vout < 1.8V)/200 (Vout ≥ 1.8V)
VGEN	1.1/1.2/1.3/1.5/1.8/2.0/2.4/2.775	150 (Vout < 1.5V)/200 (Vout ≥ 1.5V)
VCAM	1.5/1.8/2.5/2.55/2.6/2.75/2.8/3.0	150
VRFBG	1.250	0.1
VRFREF	2.475/2.600/2.700/2.775	50
VRFCP	2.700/2.775	50
VSIM	1.8/2.9	60
VESIM	1.8/2.9	60
VVIB	1.3/1.8/2.0/3.0	200
VUSB	2.775/3.3	50
VBUS	5.0	50
VRF1	1.5/1.875/2.7/2.775	350
VRF2	1.5/1.875/2.7/2.775	350
VMMC1	1.6/1.8/2.0/2.6/2.7/2.8/2.9/3.0	350
VMMC2	1.6/1.8/2.0/2.6/2.7/2.8/2.9/3.0	350

Table 10 lists characteristics that apply to MC13783 regulators. Table 11 on page 25 lists characteristics that apply only to the buck switchers.

Table 10. Regulator General Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operating Input Voltage Range Vinmin to Vinmax	—	Vnom + 0.3		4.65	V
Output Voltage Vout	Vinmin < Vin < Vinmax ILmin < IL < ILmax	Vnom - 3%	Vnom	Vnom + 3%	V
Load Regulation	1mA < IL < ILmax For any Vinmin < Vin < Vinmax	—	—	0.20	mV/mA
Active Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	20	30	µA
Low Power Mode Quiescent Current	Vinmin < Vin < Vinmax IL = 0	—	5	10	µA
PSRR	IL = 75% of ILmax 20 Hz to 20 kHz Vin = Vnom + 1V	50	60	—	dB

Table 10. Regulator General Characteristics (continued)

Parameter	Condition	Min	Typ	Max	Units
Minimum Bypass Capacitor Value	Used as a condition for all other parameters.	-35%	2.2	+35%	µF
Minimum Bypass Capacitor Value for: VRFREF, VRFCP, VIOHI, VSIM, VESIM	Used as a condition for all other parameters.	-35%	1	—	µF
Bypass Capacitor Value for VAUDIO	Used as a condition for all other parameters.	-35%	1	+35%	µF
Bypass Capacitor Value for VRFBG	Used as a condition for all other parameters.	—	100	—	nF
Bypass Capacitor ESR	10 kHz - 1 MHz	0	—	0.1	Ω

Table 11. Buck Switcher Characteristics

Parameter	Condition	Min	Typ	Max	Units
Output Voltage	2.8 V < BP < 4.65 V 0 < IL < 500 mA	0.900 V to 1.675 V in 25 m V steps 1.700 V to 2.200 V in 100 V steps			V
Output Accuracy	PWM Mode, including ripple and load regulation	-50	—	+50	mV
Transient Load Response	IL from 5 mA to 400 mA in 1µs IL from 400 mA to 5 mA in 1µs	—	—	+/- 25	mV
Effective Quiescent Current Consumption	PWM MODE	—	50	—	µA
	PFM MODE	—	15	—	µA
External Components	Inductor	-20%	10	+20%	µH
	Inductor Resistance	—	—	0.16	Ω
	Bypass Capacitor	-35%	22	+35%	µF
	Bypass Capacitor ESR	0.005	—	0.1	Ω

The buck switchers support dynamic voltage scaling (DVS). The buck switchers are designed to directly supply the processor cores. To reduce overall power consumption, core voltages of processors may be varied depending on the mode the processor is in. The DVS scheme of the buck switchers allows to transition between the different set points in a controlled and smooth manner.

For reduced current drain in low power modes, parts of a processor may be power gated, that is to say, the supply to that part of the processor is disabled. To simplify the supply tree and to reduce the number of external components while maintaining flexibility, power gate switch drivers are included.

4.3 Audio

4.3.1 Dual Digital Audio Bus

4.3.1.1 Interface

The MC13783 is equipped with two independent digital audio busses. Both busses consist of a bit clock, word clock, receive data and transmit data signal lines. Both busses can be redirected to either the voice CODEC or the stereo DAC and can be operated simultaneously. In addition to the afore mentioned signal lines, two system clock inputs are provided which can be selected to drive the voice CODEC or the stereo DAC. In the latter case, a PLL is used to generate the proper internal frequencies. During simultaneous use of the both busses, two different system clocks can be selected by the voice CODEC and the stereo DAC.

4.3.1.2 Voice CODEC protocol

The serial interface protocol for the voice CODEC can be used in master and in slave mode. In both modes, it can operate with a short or a long frame sync and data is transmitted and received in a two's compliment format.

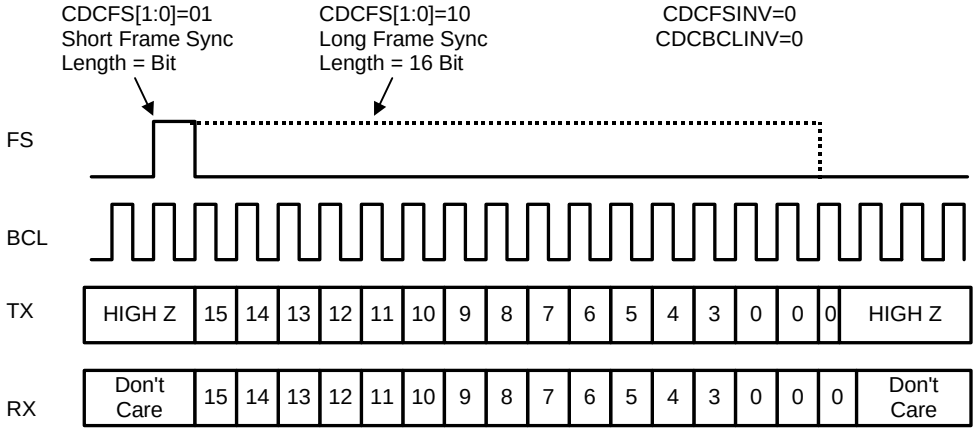

Figure 6. Voice Codec Timing Diagram Example 1

When the voice CODEC is in slave mode, the FS input must remain synchronous to the CLI frequency. In master mode all clocks are internally generated based on the CLI signal.

Additional programmability of the interface for both master and slave mode include bus protocol selection and FS and BCL inversion. There is also the possibility to activate the clocking circuitry independent from the voice CODEC.

4.3.1.3 Stereo DAC protocol

The serial interface protocol for the stereo DAC supports the industry standard MSB justified mode and an I2S mode. In industry standard mode, FS will be held high for one 16-bit data word and low for the next 16 bits. I2S mode is similar to industry standard mode except that the serial data is delayed one BCL period. Data is received in a two's compliment format. A network mode is also available where the stereo

DAC will operate in its assigned time slot. A total of maximum 4 time slot pairs are supported depending on the settings of the clock speed. In this case, the sync signal is no longer a word select but a short frame sync. In all modes, the polarity of both FS and BCL is programmable by SPI. There is also the possibility to activate the clocking circuitry independent from the stereo DAC.

4.3.1.4 Audio Port Mixing

In network mode, the receive data from two right channel time slots and of two left channel time slots can be added. One left/right time slot pair is considered to represent the main audio flow whereas the other time slot pair represents the secondary flow. The secondary flow can be attenuated with respect to the main flow by 0 dB, 6 dB and 12 dB which should be sufficient to avoid clipping of the composite signal. In addition, the composite signal can be attenuated with 0 dB or 6 dB.

4.3.2 Voice CODEC

4.3.2.1 A/D Converters

The A/D portion of the voice CODEC consists of two A/D converters which convert two incoming analog audio signals into 13-bit linear PCM words at a rate of 8 kHz or 16 kHz. Following the A/D conversion, the audio signal is digitally band pass filtered. The converted voice is available on the audio bus. If both A/D channels are active, the audio bus is operated in a network mode.

Table 12. Telephone CODEC A/D Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Peak Input (+3 dBm0)	single ended	REFC-0.68		REFC+0.68	V
CODEC PSRR	with respect to BP, 0 to 20 kHz	80	90	—	dB_P
Total Distortion (noise and harmonic)	at 1.02 kHz (linear) 0 dBm0 8.0 kHz measurement BW out	60	70	—	dB_P
Idle Channel Noise	0 db PGA gain incl. microphone amp	—	—	-72	$dBm0_P$
Inband Spurious	0 dBm0 at 1.02 kHz input, 300 Hz to 3.0 kHz (8 kHz sample rate)	—	—	-48	dB

4.3.2.2 D/A Converter

The D/A portion of the voice CODEC converts 13-bit linear PCM words entering at a rate of 8 kHz and 16 kHz into analog audio signals. Prior to this D/A conversion, the audio signal is digitally band-pass filtered.

Table 13. Telephone CODEC D/A Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Peak Output (+3 dBm0)	single ended output	REFC - 1		REFC + 1	V
CODEC PSRR	with respect to B+, 20 Hz to 20 kHz,	80	90	—	dB
Total Distortion (noise and harmonic)	at 1.02 kHz, 0 dBm0, 20 kHz measurement BW out	65	75	—	dB
Idle Channel Noise	at CODEC output, BW out = 20 kHz A weighted	—	-78	-74	dBm0
Inband Spurious	0 dBm0 at 1.02 kHz to 3.4 kHz input. 300 Hz to 20.0 kHz	—	—	-50	dB

4.3.2.3 Clock Modes

In master mode the CLI is divided internally to generate the BCL and FS signals. In slave mode these clocks have to be supplied and in that case there is no imposed relationship between BCL and the other clocks as long as it is high enough to support the number of time slots requested. The supported clock rates are 13.0 MHz, 15.36 MHz, 16.8 MHz, 26.0 MHz and 33.6 MHz.

4.3.3 Stereo DAC

4.3.3.1 D/A Converter

The stereo DAC is based on a 16-bit linear left and right channel D/A converter with integrated filtering.

Table 14. Stereo DAC Main Performance Specifications

Parameter	Condition	Min	Typ	Max	Units
Absolute Gain	Input at 0 dBFS, from 20 Hz to 20 kHz	-0.5	—	+0.5	dB
L/R Gain Mismatch	Input at -3 dBFS, 1.02 kHz	—	0.2	0.3	dB
Dynamic Range	(SNDR at -60 dBFS and 1.02 kHz) + 60 dB, 20 kHz BW out, A weighted	92	96	—	dB
Output PSRR	with respect to battery, input at 0 dBFS, from 20 Hz to 20 kHz A weighted	90	—	—	dB
Spurious	input at -3 dBFS, from 20 Hz to 20 kHz, 20 kHz BW out Includes idle tones	—	—	-75	dB

4.3.3.2 Clock Modes

The stereo DAC incorporates a PLL to generate the proper clocks in master and in slave modes. The PLL requires an external C//RC loop filter.

In Master Mode, the PLL of the Stereo DAC generates FS and BCL signal based on the reference frequency applied through one of the CLI inputs. The CLI frequencies supported are 3.6864 MHz, 12 MHz, 13 MHz, 15.36 MHz, 16.8 MHz, 26 MHz and 33.6 MHz. The PLL will also generate its own master clock MCL used by the stereo DAC itself.

In Slave Mode, FS and BCL are applied to the MC13783 and the MCL is internally generated by the PLL based on either FS or BCL.

A special mode is foreseen where the PLL is bypassed and CLI can be used as the MCL signal. In this mode, MCLK must be provided with the exact ratio to FS, depending on the sample rate selected.

In the network mode, it's possible to select up to 8 time slots (4 time slot pairs).

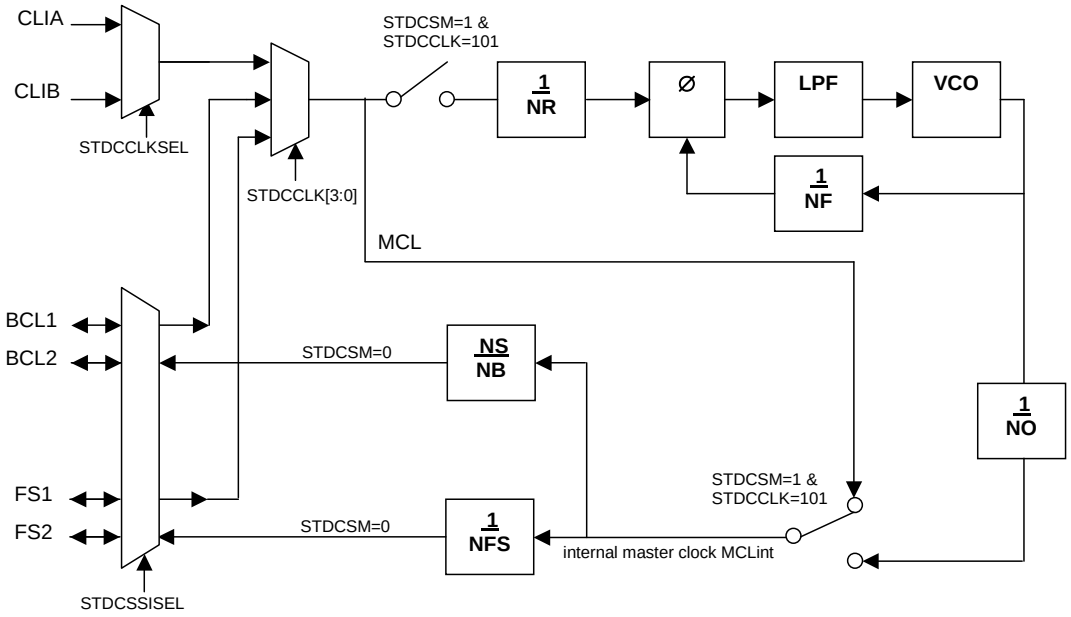

Figure 7. Stereo DAC PLL Block Diagram

Table 15. Stereo DAC Sample Rate Selection SPI Bits

SR3	SR2	SR1	SR0	FS	N_{FS}	MCL	N_B	BCL
0	0	0	0	8000	512	4096k	16	256k
0	0	0	1	11025	512	5644.8k	16	352.8k
0	0	1	0	12000	512	6144k	16	384k
0	0	1	1	16000	256	4096k	8	512k
0	1	0	0	22050	256	5644.8k	8	705.6k
0	1	0	1	24000	256	6144k	8	768k
0	1	1	0	32000	128	4096k	4	1024k
0	1	1	1	44100	128	5644.8k	4	1411.2k

Table 15. Stereo DAC Sample Rate Selection SPI Bits (continued)

SR3	SR2	SR1	SR0	FS	N_{FS}	MCL	N_B	BCL
1	0	0	0	48000	128	6144k	4	1536k
1	0	0	1	64000	64	4096k	2	2048k
1	0	1	0	96000	64	6144k	2	3072k
1011 to 1111 are reserved combinations								

4.3.4 Audio Input Section

4.3.4.1 Microphone Bias

Two microphone bias circuits are provided. One circuit supplies up to two handset microphones via the two outputs MC1RB and MC1LB. The second circuit supplies the headset microphone via MC2B. The microphone bias resistors of 2.2 kOhm are included. The bias circuits can be enabled and disabled.

The bias MC2B includes a microphone detect circuit which monitors the current flow through the output both when the bias is disabled or enabled. This will generate an interrupt to the processor. In this way the attach and removal of a headset microphone is detected. Also it allows to include a send/end series switch with the microphone for signaling purposes. When the output of the MC2B gets out of regulation, an interrupt is generated. This allows for connecting a switch in parallel to the microphone.

Table 16. MC1RB, MC1LB and MC2B Parametric Specifications

Parameter	Condition	Min	Typ	Max	Units
Microphone Bias Internal Voltage	MC1RB, MC1LB IL = 0 MC2B	2.23 2.00	2.38 2.10	2.53 2.20	V
Output Current	Source only	0	—	500	µA
PSRR	with respect to BP 20 Hz - 10 kHz	90	—	—	dB
Output Noise	Includes REFA noise CCITT psophometricly weighted	—	1.5	3.0	µVrms

4.3.4.2 Microphone Amplifiers

Figure 8 on page 31 shows a block diagram of the microphone amplifier section. A selection can be made between one of the three amplified inputs: the handset microphone connected to MC1RIN, the headset microphone connected to MC2IN, and the line input TXIN. The selected channel can be fed into the receive channel for test purposes. In addition a second amplified input channel can be selected for the second handset microphone connected to MC1LIN. The gain towards to voice CODEC can be programmed in 1 dB steps from –8 dB to +23 dB.

In addition to the microphone amplifier paths, there is also the possibility to route the stereo line in signal from RXINR and RXINL to the voice CODEC dual ADC section. This allows for 13-bit, 16 kHz sampled stereo recording of an analog source such as FM radio.

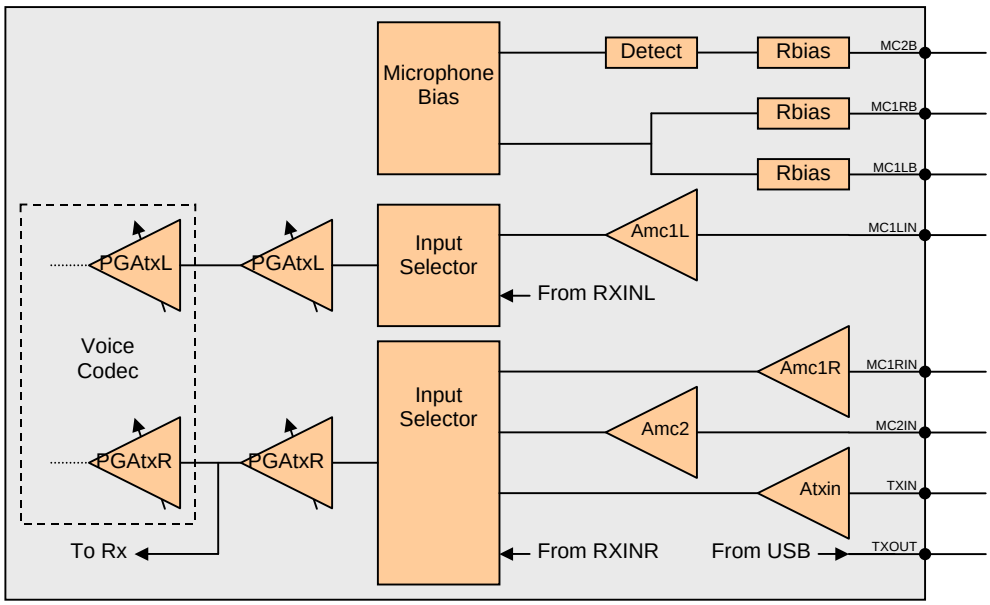

Figure 8. Audio Input Section Diagram

Table 17. Amplifiers Amc1L, Amc1R, Amc2, Atxin Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Gain (V to V)	at 1.0 kHz	Vin = 100 mVpp	11.8	12	12.2	dB
Input Impedance (V to V)	Amc1L, Amc1R, Amc2	—	8.5	10	11.7	kΩ
	Atxin	—	—	40	—	kΩ
Gain (Atxin)	TXIN to Voice Codec	—	-0.2	0	0.2	dB
PSRR	with respect to BP 20 Hz – 10 kHz inputs AC grounded	—	—	90	—	dB
Input Noise	input to REFA	CCITT psophometricly weighted	—	—	1	μV_{RMS}

4.3.5 Audio Output Section

4.3.5.1 Audio Signal Routing

Figure 9 on page 32 shows a block diagram of the audio output section is given indicating the routing possibilities.

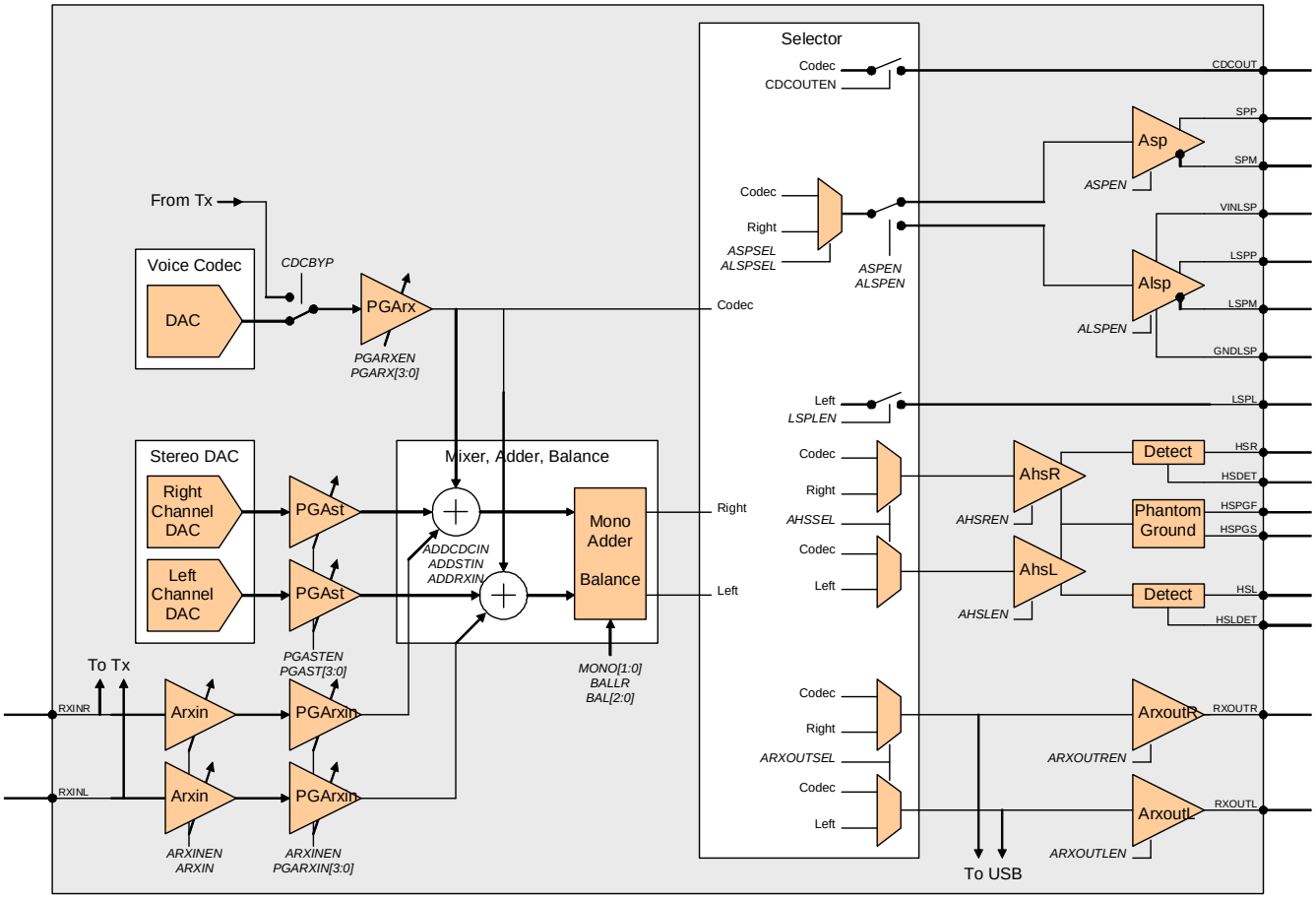

Figure 9. Audio Output Section Diagram

Four signal sources can be used in the receive path. The voice CODEC receive signal, the voice CODEC transmit signal (for test purposes), the stereo DAC and an external stereo source like an FM radio. The latter can also be routed to the voice CODEC ADC section for recording purposes. Each of the input source signals is amplified via an independently programmable gain amplifier. The amplified signals are fed into a mixer where the different signals can be mixed. The mixed signal goes through a mono adder and balance circuit which can create a mono signal out of the stereo input signals, and allows for balance control. Via the selector, the composite signal is then directed to one or more of the outputs. These are the regular phone earpiece (Asp), the loudspeaker for hands free or ringing (Alsp), the stereo headset (Ahsr, Ahsl) and the stereo line out. The voice CODEC output signal can also follow an independent route to all of the amplifiers via the additional selector inputs. In addition to the amplifiers, low power outputs are available at LSPL and CDCOUT.

4.3.5.2 Programmable Gain Amplifiers

The gain of the audio in both left and right channels is independently controlled in the programmable gain amplifiers to allow for balance control. The input level from the external stereo source can be pre-amplified by Arxin of 18 dB and the programmable gain amplifier PGArxin to get it at the same level as the other sources before going into the audio input mixer block. The amplifiers are programmable in 3 dB steps from –33 dB to +6 dB.

4.3.5.3 Balance, Mixer, Mono Adder and Selector Block

The mixer is a summing amplifier where the different input signals can be summed. The relative level between the input signals is to be controlled via the PGArx, PGAst, and PGArxin amplifiers respectively.

The mono adder in the stereo channel can be used in four different modes: stereo (right and left channel independent), stereo opposite (left channel in opposite phase), mono (right and left channel added), mono opposite (as mono but with outputs in opposite phase).

The balance control allows for attenuating either the right or the left channel with respect to the other channel. The balance control setting is applied independent of which input channel is selected.

The selector opens the audio path to the audio amplifiers and can be seen as an analog switch.

4.3.5.4 Earpiece Speaker Amplifier Asp

The Asp amplifier drives the earpiece of the phone in a bridge tied load configuration. The feedback network of the Asp amplifier is fully integrated.

Table 18. Amplifier Asp Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Differential Output Swing	—	—	4.0	—	—	V_{PP}
Gain	Single Ended, 1.0 kHz	Vin = 100 mVpp	3.8	4.0	4.2	dB
THD (2^{nd} and 3^{rd})	1.0 kHz	V_{OUT} = 2 Vp	—	—	0.1	%
	1.0 kHz	V_{OUT} = 100 mVp	—	—	0.1	%
	1.0 kHz	V_{OUT} = 10 mVp	—	—	0.1	%
PSRR	with respect to BP 20 Hz – 20 kHz inputs AC grounded A Weighted	—	90	—	—	dB
Input Noise	A weighted Including PGA Noise	—	—	—	20	μV_{RMS}
Load Impedance	—	—	—	16	—	Ω

4.3.5.5 Loudspeaker Amplifier Alsp

The concept of the Alsp amplifier is especially developed to be able to drive one loudspeaker during handset, speakerphone and alert modes. It adopts a fully differential topology in order to be able to reach high PSRR performance while Alsp is powered directly by the telephone battery. The feedback network of the Alsp amplifier is fully integrated.

Under worst case conditions the dissipation of Alsp is considerable. To protect the amplifier against overheating, a thermal protection is included which shuts down the amplifier when the maximum allowable junction temperature within Alsp is reached.

Table 19. Amplifier Alsp Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Differential Output Swing	BP = 3.05 V	—	5.0	—	—	V_{PP}
	BP = 3.4 V in 8Ω	—	5.6	—	—	V_{PP}
Supply Voltage	—	—	3.05	—	4.65	V
Gain	1.0 kHz	Vin = 100 mVpp	5.8	6	6.2	dB
THD (2^{nd} and 3^{rd})	1.0 kHz, BP = 3.4 V	V_{OUT} = 5 Vpp	—	3	5	%
	1.0 kHz, BP = 4 V	V_{OUT} = 5 Vpp	—	1	3	%
	1.0 kHz	V_{OUT} = 1 Vpp	—	—	0.1	%
	1.0 kHz	Vout = 10 mVrms	—	—	0.1	%
PSRR	with respect to BP 20 Hz – 20 kHz inputs AC grounded A Weighted	—	90	—	—	dB
Input Noise	A weighted	—	—	—	20	μV_{RMS}
Load Impedance	Resistance	—	6.4	8	38	Ω

4.3.5.6 Headset Amplifiers Ahsr/Ahsl

The Ahsr and Ahsl amplifiers are dedicated for amplification to a stereo headset, the Ahsr for the right channel and Ahsl for the left channel. The feedback networks are fully integrated.

The return path of the headset is provided by the phantom ground which is at the same DC voltage as the bias of the headset amplifiers. This avoids the use of large sized capacitors in series with the headset speakers. All outputs withstand shorting to ground or to phantom ground.

Table 20. Amplifiers Ahsr and Ahsl Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Singled-Ended Output Swing	32 Ohm load 16 Ohm load		2 1.6	2.2 1.8	—	V_{PP}
Gain	1.0 kHz	Vin = 100 mVpp	-0.2	0	0.2	dB

Table 20. Amplifiers Ahsr and Ahsl Performance Specifications (continued)

Parameter	Condition		Min	Typ	Max	Units
THD (2^{nd} and 3^{rd})	1.0 kHz	V_{OUT} = 1 V_{PP}	—	0.03	0.1	%
		V_{OUT} = 10 mV_{RMS}	—	0.03	0.1	%
PSRR	with respect to BP 20 Hz - 20 kHz inputs AC grounded A Weighted		90	—	—	dB
Input Noise	A weighted		—	—	20	μV_{RMS}
Load Impedance	Resistance		12.8	16	38	Ω

The MC13783 provides a headset detection scheme based on the sleeve detection, left channel impedance detection and microphone bias detection which is valid for headsets with or without phantom ground connection. It is compatible with mono headsets where the left channel is connected to ground.

4.3.5.7 Line Output Amplifier Arxout

The Arxout amplifier combination is a low power stereo amplifier. It can provide the stereo signal to for instance an accessory connector. The same output of the selector block is used for the internal connection to the USB transceiver for CEA-936-A Carkit support.

Table 21. Arx Performance Specifications

Parameter	Condition		Min	Typ	Max	Units
Gain	1.0 kHz	Vin = 100 mVpp	-0.2	0	+0.2	dB
Single Ended Output Swing	Includes reverse bias protection purpose	—	1.8	2	—	Vpp
PSRR	with respect to BP 20 Hz – 20 kHz inputs AC grounded A Weighted	—	90	—	—	dB
THD (2^{nd} and 3^{rd})	gain = 0 dB	V_{OUT} = 1 V_{PP}	—	—	0.1	%
		V_{OUT} = 100 mV_{RMS}	—	—	0.1	%
		V_{OUT} = 10 mV_{RMS} (3)	—	—	0.1	%
External Load Impedance	—	—	1	—	—	kΩ
Output Noise	gain = 0 dB A weighted 20 Hz - 20 kHz Per output (2)	—	—	15	20	μV_{RMS}

4.3.6 Audio Control

4.3.6.1 Supply

The audio section is supplied from a dedicated regulator VAUDIO, except for the loudspeaker amplifier Alsp which is directly supplied from the battery. A low power standby mode controlled by the standby pins is provided for VAUDIO in which the bias current is reduced. The output drive capability and performance are limited in this mode. The nominal output voltage for VAUDIO is 2.775 V. A 1uF (± 35%) bypass capacitor is needed at the output of the VAUDIO regulator.

4.3.6.2 Bias and Anti-Pop

The audio blocks have a bias which can be enabled separately from the rest of the MC13783. When enabled, the audio bias voltages can be ramped fast or slow to make any pop sub audio and therefore not audible.

4.3.6.3 Arbitration Logic

The audio functions can be operated by both the primary and secondary SPI.

4.4 Battery Management

4.4.1 Battery Interface and Control

The battery interface is optimized for single charger input coming from a standard wall charger or from a USB bus. The charger has been designed to support three different configurations where the charger and USB bus share the same input pin (CHRGRAW): these are dual path charging, serial path charging, and single path charging. In addition, provisions have been taken for a separate input configuration where the charger and USB supply are on separate inputs. In all cases except for single path charging, the battery interface allows for so called dead battery operation. An example of serial path charging is shown in Section 4.4.1.1, “Serial Path Configuration Example,” on page 37.

This section includes the following subsections:

The mode of operation for the charger interface is selected via the CHRGMOD1 and CHRGMOD0 pins as given in Table 22.

Table 22. Charger Mode Selection

CHRGMOD1	CHRGMOD0	Charger Mode
Hi Z	GND	Dual Path
Hi Z	Hi Z	Single Path
Hi Z	VATLAS	Serial Path

Table 22. Charger Mode Selection (continued)

CHRGMOD1	CHRGMOD0	Charger Mode
VATLAS	GND	Separate Input Dual Path
VATLAS	Hi Z	Separate Input Single Path
VATLAS	VATLAS	Separate Input Serial Path
GND	GND	Reserved
GND	Hi Z	Reserved
GND	VATLAS	Reserved

4.4.1.1 Serial Path Configuration Example

In serial path configuration, the current path used for charging the battery is the same as the supply path from charger to radio B+. Refer to the block diagram example in Figure 10 on page 37.

Transistors M1 and M2 control the charge current and provide a voltage clamping function in case of no battery or in case of a dead battery to allow the application to operate. In both cases transistor M3 is non-conducting and the battery is charged with a trickle charge current internal to the MC13783. The transistor M3 is conducting in case the battery has to be connected to the application like for normal operation or for standalone trickle charging. Transistor M2 is non-conducting in case the charger voltage is too high. A current can be supplied from the battery to an accessory by having all transistors M1, M2 and M3 conducting.

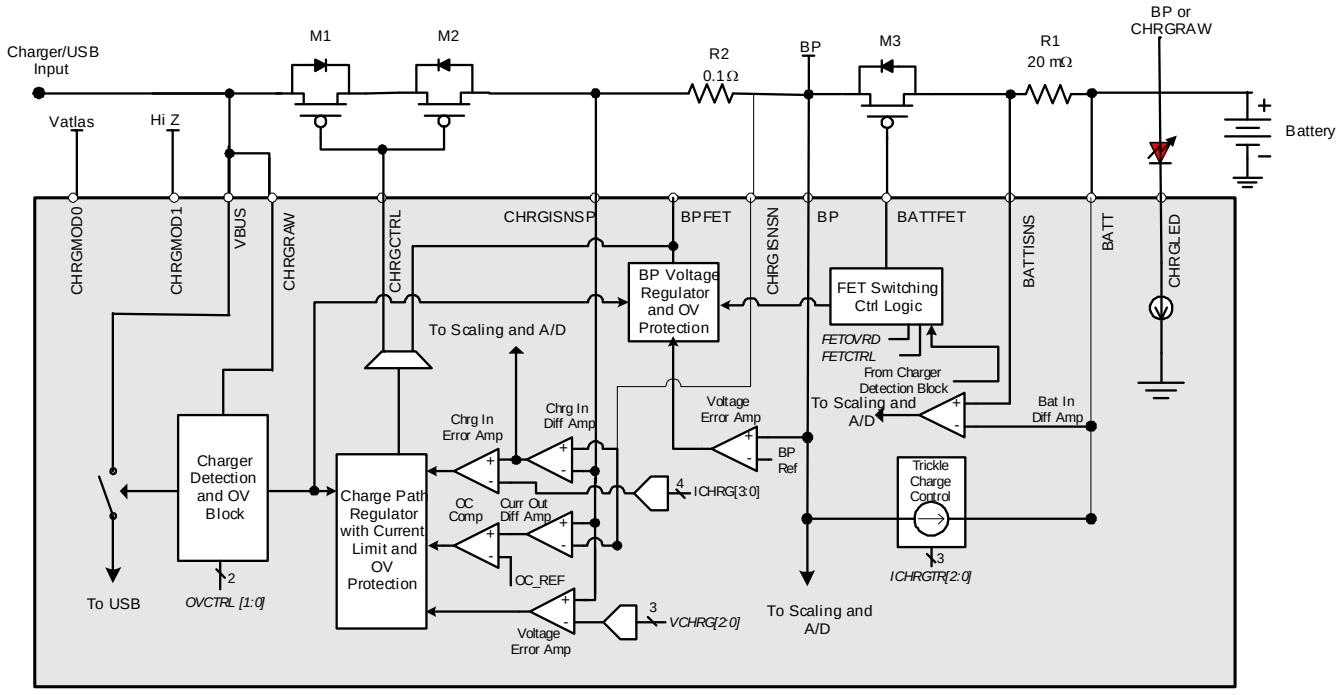

Figure 10. Serial Path Interface Block Diagram

Table 23. Voltage and Current Settings

Parameter	Set Points
Regulated charge voltage at BP	Programmable voltage setting of 3.80/4.05/4.15/4.20/4.25/4.30/4.375/4.50V.
Regulated charge current through M1M2	Programmable current from 0 to 1600 mA in 14 steps, and fully on mode.
Internal trickle charge current	Programmable current from 0 to 84mA in steps of 12mA.

4.4.1.2 Charger Operation

4.4.1.2.1 CEA-936-A

The CEA-936-A carkit specification allows a USB connection to be used not only as an USB interface but also as a generic supply plus analog audio interface. The purpose is to standardize the carkit interface over a USB connection. The USB VBUS line in this case is used to provide a supply within the USB voltage limits and with at least 500 mA of current drive capability. However, this also opens the possibility to create a range of USB compatible wall chargers, referred to as CEA-936-A charger in the remainder of this chapter. The CEA-936-A standard also allows providing a supply from the phone to the accessory over the VBUS line, just like in the USB on the go case.

4.4.1.2.2 Standalone Trickle Charging

The MC13783 has a standalone trickle charge mode of operation in order to ensure that a completely discharged battery can be charged without the Microprocessor's control. Upon plugging a valid charger to the phone, the trickle cycle is started. For battery voltages below 2.7 V, the trickle charge current level is set at 70 mA. When the battery voltage increases above the threshold, the trickle charge level is increased to 266 mA. When the battery voltage rises above the threshold sufficient for phone operation, a power up sequence is automatically initiated. Even after the phone has powered up, the Standalone trickle charge will remain on until software enables charging. If the battery voltage was already greater than the voltage needed for phone operation when a charger is attached, the phone will power up immediately without starting a trickle charge cycle. The trickle charge is terminated upon charge completion, time out, or by software control.

For the single path charging configuration, standalone trickle charging is only available for the SE1 = LOW condition. The charge level remains constant at the lower 70 mA threshold through all battery voltage ranges—that is, there is no increased charge current at the 2.7 V threshold.

Standalone Trickle charging is not available for the SE1 = HIGH / Single Path charging case.

4.4.1.3 Coin Cell

The coin cell charger circuit will function as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The output voltage is selectable. The coin cell charger voltage is programmable in the ON state. In the User Off modes, or in the Off state, the coincell charger will continue to charge to the predefined voltage setting but at a lower maximum current. In practice, this means that if in Off state the coin cell is fully charged, the coin cell charger will only

provide the leakage current of the coin cell. The RTC will run from VATLAS in this case. A capacitor should be placed from LICELL to ground if no coin cell is used.

4.4.2 ADC Subsystem

4.4.2.1 Converter Core

The ADC core is a 10 bit successive approximation converter.

4.4.2.2 Input Selector

The ADC has two groups of 8 input channels. ADSEL selects between two groups of input signals. If set to zero then group 0 is read and stored, if set to 1 then group 1 is read and stored. This is done to shorten the total read time and to reduce the required storage of converted values. The table below gives an overview of the attribution of the A to D channels.

Table 24. ADC Inputs

	Channel	Signal read	Expected Input Range	Scaling	Scaled Version
Group 0 – ADSEL=0	0	Battery Voltage (BATT)	2.50 – 4.65 V	- 2.40 V	0.10 – 2.25 V
	1	Battery Current (BATT – BATTISNS)	-50 - +50 mV	x20	-1.00 - +1.00 V
	2	Application Supply (BP)	2.50 – 4.65 V	- 2.40 V	0.10 – 2.25 V
	3	Charger Voltage (CHRGRAW)	0 – 10 V / 0 – 20 V	/5 /10	0 – 2.00 V 0 – 2.00 V
	4	Charger Current (CHRGISNSP-CHRGISNSN)	-250mV – +250 mV	X4	-1.00 – 1.00 V
	5	General Purpose ADIN5 / Battery Pack Thermistor	0 – 2.30 V	No	0 – 2.30 V
	6	General Purpose ADIN6 / Backup Voltage (LICELL)	0 – 2.30 V / 1.50 – 3.50 V	No / - 1.20 V	0 – 2.30 V 0.30 – 2.30 V
	7	General Purpose ADIN7 / UID / Die Temperature	0 – 2.30 V / 0 – 2.55 V / TBD	No / x0.9 / No	0 – 2.30 V
Group 1 – ADSEL=1	8	General Purpose ADIN8	0 - 2.30 V	No	0 – 2.30 V
	9	General Purpose ADIN9	0 - 2.30 V	No	0 – 2.30 V
	10	General Purpose ADIN10	0 - 2.30 V	No	0 – 2.30 V
	11	General Purpose ADIN11	0 - 2.30 V	No	0 – 2.30 V
	12	General Purpose TSX1 / Touchscreen X-plate 1	0 - 2.30 V	No	0 – 2.30 V
	13	General Purpose TSX2 / Touchscreen X-plate 2	0 - 2.30 V	No	0 – 2.30 V
	14	General Purpose TSY1 / Touchscreen Y-plate 1	0 - 2.30 V	No	0 – 2.30 V
	15	General Purpose TSY2 / Touchscreen Y-plate 2	0 - 2.30 V	No	0 – 2.30 V

4.4.2.3 Control

The ADC parameters are programmed by the processors via SPI. Locally on MC13783, the different ADC requests are arbitrated and executed. When a conversion is finished, an interrupt is generated to the processor which started the conversion.

4.4.2.3.1 Starting Conversions

The ADC will have the ability to start a series of conversions based on a rising edge of the ADTRIG signal or directly initiated by SPI.

Once conversion is initiated all 8 channels will be sequentially converted and stored in registers or eight conversions on one channel will be performed and stored. The conversion result can digitally be compared with respect to a preset value for threshold detection.

The conversion will begin after a delay set between 0 and 8 ms. The delay between conversions can be made equal to this delay.

To avoid that the ADTRIG input involuntarily triggers a conversion, a bit can be set which will make the ADC ignores any transition on the ADTRIG pin.

4.4.2.3.2 Reading Conversions

Once a series of eight A/D conversions is complete, they are stored in one set of eight internal registers and the values can be read out by software.

4.4.2.4 Pulse Generator

A SPI controllable pulse generator is available at ADOUT synchronized with the ADC conversion. This pulse can be used to enable or drive external circuits only during the period of 4 or 8 ADC conversions.

4.4.2.5 Dedicated Channels Reading

4.4.2.5.1 Battery Current

Traditional battery capacity estimation is based on battery terminal voltage reading combined with estimated phone current drain based on emitted PA power. For improved battery capacity estimation, especially in non transmit mode like gaming, this method is too approximate. To improve the estimation, the current out of the battery must be quantified more accurately. For this, on the MC13783, the current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS.

4.4.2.5.2 Charge Current

The charge current is read by monitoring the voltage drop over the charge current sense resistor.

4.4.2.5.3 Battery Thermistor

If a battery is equipped with a battery thermistor, its value can be read out via the ADC input ADIN5. The biasing and sensing circuit is entirely integrated and is only powered during the A to D conversions.

4.4.2.5.4 Die Temperature and UID

The die temperature can be read out on the ADIN7 channel. Alternatively, the UID voltage can be read out on the ADIN7 channel.

4.4.2.6 Touch Screen Interface

The touchscreen interface provides all circuitry required for the readout of a 4-wire resistive touchscreen. The touchscreen X plate is connected to TSX1 and TSX2 while the Y plate is connected to TSY1 and TSY2. A local supply ADREF will serve as a reference. Several readout possibilities are offered.

In *interrupt mode*, a voltage is applied via a high impedance source to only one of the plates, the other is connected to ground. When the two plates make contact both will be at a low potential. This will generate a pen interrupt to the processor. This detection does not make use of the ADC core.

A finger will connect both plates over a wider area then a stylus. To distinguish both sources, in the *contact resistance mode* the resistance between the plates is measured by applying a voltage difference between the X and the Y plate. The current through the plates is measured.

Since the plate resistance varies from screen to screen, measuring its value will improve the pressure measurement. Also, it can help in determining if more than 1 spot is touched on the screen. In the *plate measurement mode*, a potential is applied across one of the plates while the other plate is left floating. The current through the plate is measured.

The contact resistance mode and plate measurement mode are together referred to as *resistive mode*.

To determine the XY coordinate pair, in *position mode* a voltage difference over the X plate is read out via the Y plate for the X-coordinate and vice versa for the Y- coordinate readout. In the MC13783, during the *position mode* the contact resistance is read as well in addition to the XY coordinate pair.

To perform touchscreen readings, the processor will have to set one of the touchscreen interface readout modes, program the delay between the conversions, trigger the ADC via one of the trigger sources, wait for an interrupt indicating the conversion is done, and then read out the data. In order to reduce the interrupt rate and to allow for easier noise rejection, the touchscreen readings are repeated in the readout sequence. In this way, in total eight results are available per readout.

Table 25. Touchscreen Reading Sequence

ADC Trigger	Signals sampled in Resistive Mode	Signals sampled in Position Mode	Readout Address
0	X plate resistance	X position	000
1	X plate resistance	X position	001
2	X plate resistance	X position	010
3	Y plate resistance	Y position	011
4	Y plate resistance	Y position	100
5	Y plate resistance	Y position	101
6	Contact resistance	Contact resistance	110
7	Contact resistance	Contact resistance	111

4.4.2.7 ADC Arbitration

The ADC converter and its control is based on a single ADC converter core. Since the data path is 24 bits wide, results for 2 conversion results (10 bits each) can be read back in each SPI read sequence. For support of queued conversion requests, the SPI has the ability to write to the two sets of ADC control, namely “its own” ADC and “the other” ADC or ADC BIS.

The write access to the control of ADC BIS is handled via the ADCBISn bits located at bit position 23 of the ADC control registers. By setting this bit to a 1, the control bits which follow are directed to the ADC BIS. ADCBISn will always read back 0 and there is no read access to the ADCBIS control bits. The read results from the ADC conversions are available in two separate registers ADC result registers ADC0 and ADC1.

4.5 Miscellaneous Functions

Miscellaneous functions are described in the following sections:

- Section 4.5.1, “Connectivity on page 42
- Section 4.5.2, “Lighting System on page 45

4.5.1 Connectivity

This section summarizes the following interface information:

- Section 4.5.1.1, “USB Interface on page 42
- Section 4.5.1.2, “RS-232 Interface on page 45
- Section 4.5.1.3, “CEA-936-A Accessory Support on page 45
- Section 4.5.1.4, “Booting Support on page 45

4.5.1.1 USB Interface

4.5.1.1.1 Supplies

The USB interface is supplied by the VUSB (3.3 V) and the VBUS (5.0 V) regulators. The VBUS regulator takes the boost supply and regulates it down to the required USBOTG level which is provided to VBUS in the case of a USBOTG connection. The transceiver itself is supplied from VUSB. The VUSB regulator by default is supplied by BP and by SPI programming can be boost or VBUS supplied as well.

4.5.1.1.2 Detect

Comparators are used to detect a valid VBUS, and to support the USB OTG session request protocol.

4.5.1.1.3 Transceiver

The USB transceiver data flow is depicted in below diagram. The processor interface IO level is set to USBVCC.

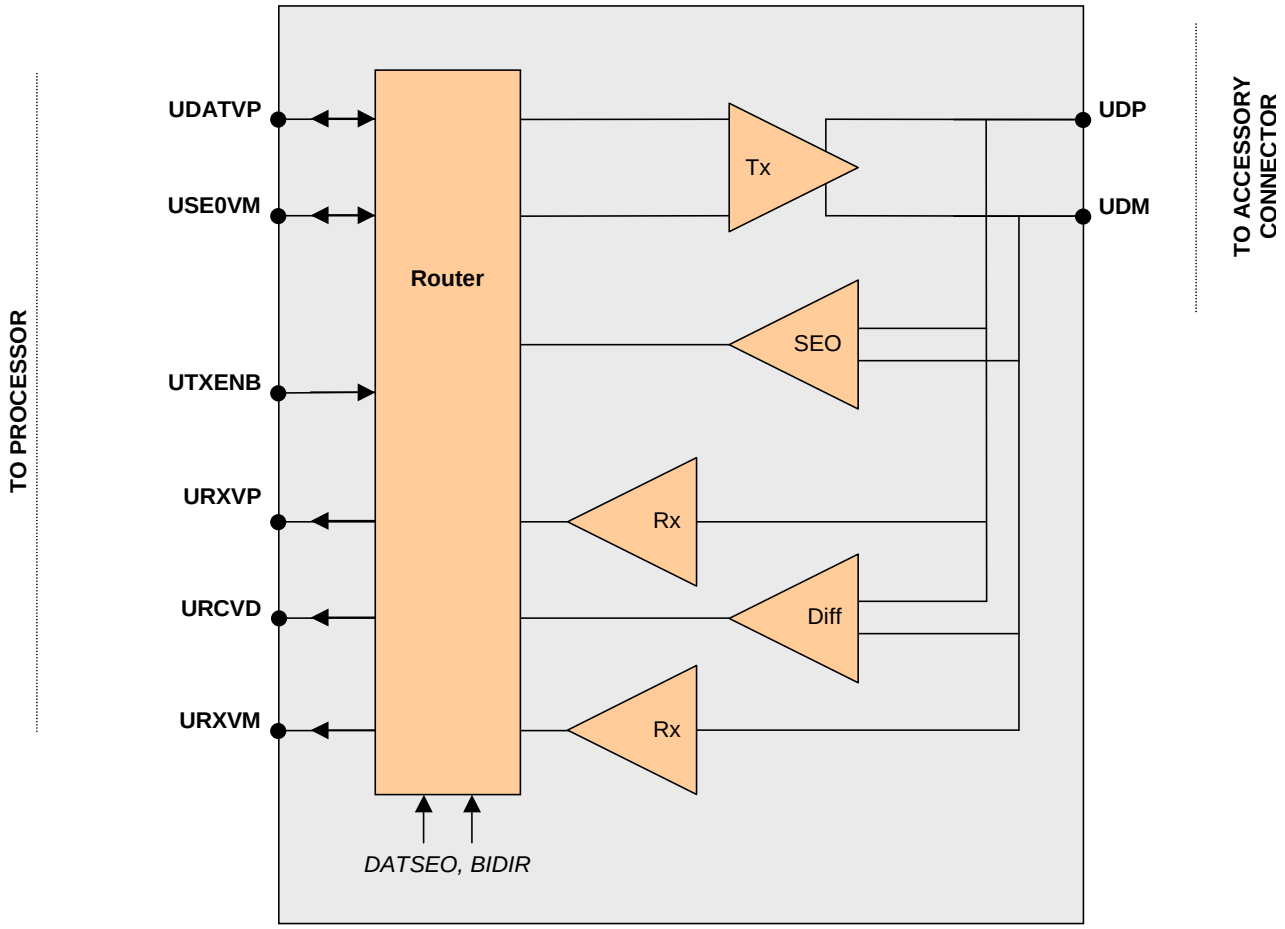

Figure 11. USB/RS232 Transceiver Data Flow

Upon a USB legacy host detection, an interrupt is generated but neither the transceiver nor the VUSB regulator are automatically enabled. This must be done by software before data transmission. The transceiver can also be enabled during boot mode.

Via SPI bits DATSE0 and BIDIR, one of the four USB operating modes can be selected. However, when starting up in a boot mode, there is no up front SPI programming possible. The default operating mode is then determined by the setting of the UMOD pin as indicated in Table 26.

Table 26. USB Mode Selection

USB Mode		Mode Selection		Mode Description		Corresponding UMOD0/UMOD1 Setting
		DATSE0	BIDIR	UTXENB = Low	UTXENB = High	
Differential	unidirectional (6-wire)	0	0	UDATVP → UDP USE0VM → UDM	UDP → URXVP UDM → URXVM UDP/UDM → URCVD	Don't Care / To VATLAS
	bidirectional (4-wire)		1	UDATVP → UDP USE0VM → UDM	UDP → UDATVP UDM → USE0VM UDP/UDM → URCVD	To VATLAS / To Ground
Single Ended	unidirectional (6-wire)	1	0	UDATVP→ UDP/UDM USE0VM → FSE0[1]	UDP → URXVP UDM → URXVM UDP/UDM → URCVD	To Ground / To Ground
	bidirectional (3-wire)		1	UDATVP → UDP/UDM USE0VM → FSE0	UDP/UDM → UDATVP (active) UDP → UDATVP (suspend) RSE0 → USE0VM	Open / To Ground

1 FSE0 stands for forced SE0, RSE0 stands for received SE0.

4.5.1.1.4 Full Speed/ Low Speed Configuration

The USB transceiver supports the low speed mode of 1.5 Mbits/second and the full speed mode of 12 Mbits/second. To indicate the speed to the host an internal 1.5 kOhm pull up to VUSB is used. Via SPI this resistor can be connected to UDP to indicate full speed, or to UDM to indicate low speed.

4.5.1.1.5 USB Suspend

USB suspend mode is enabled through SPI. When set, the USB transceiver enters a low power mode which reduces the transceiver current drain to below 500 µA. In USB suspend mode, the VUSB regulator remains enabled and the VBUS detect comparators remain enabled, while the single ended receivers are switched from a comparator to a Schmitt-trigger buffer.

4.5.1.1.6 USB On-The-Go

USBOTG support circuitry is added in order to allow a phone to act as a dual-role USBOTG device. In accordance with USBOTG requirements, the pull down resistors on UDP and UDM can be switched in or out individually via SPI. Furthermore, the pulls down resistors are integrated on-chip.

The USBOTG specification requires that during the session request protocol, the D+ (full speed) line is pulled up for a duration of 5 to 10 msec. In order to reduce the SPI traffic, the MC13783 has an integrated timer used for this task.

To support VBUS pulsing, there is a programmable current limit and timer on the VBUS regulator. During VBUS pulsing, the lower current limit allows for easier detection of a legacy host device on the far end of the USB cable.

It is possible to have the transceiver automatically connect the data pull-up to VUSB any time a SE0 is detected. This enables the phone to meet the USBOTG timing requirements without unduly taxing the software.

An ID detector is used to determine if a mini-A or mini-B style plug has been inserted into a mini-AB style receptacle on the phone. The ID voltage can be read out via the ADC channel ADIN7.

4.5.1.2 RS-232 Interface

In RS232 mode, USBVCC is used for the supply of the interface with the microprocessor. VUSB is used as the supply for the RS232 transceiver and the drivers at the cable side. In this mode, the USB transceiver is tri-stated and the USB module IC pins are re-used to pass the RS232 signals from the radio connector to the digital sections of the radio.

Flexibility is provided for RS232 Rx and Tx signal swapping at the cable side interface pins UDP and UDM, and the possibility to enable the RS232 receiver while tri-stating the transmitter.

4.5.1.3 CEA-936-A Accessory Support

Support for CEA-936-A is provided, including provision for audio muxing to UDP and UDM and ID interrupt generation. All audio path switches are residing in the USB block and are powered from the VUSB regulator. Please refer to CEA-936-A specification for details.

4.5.1.4 Booting Support

The MC13783 supports booting on USB. The boot mode is entered by the USBEN pin being forced high by the booting equipment which enables the transceiver.

4.5.2 Lighting System

The lighting system of MC13783 is comprised of independent controlled circuitry for backlight drivers and tri-color LED drivers. This integration provides flexible backlighting and fun lighting for products featuring multi-zone and multi-color lighting implementations. Figure 12 illustrates the lighting system utilization for a typical application.

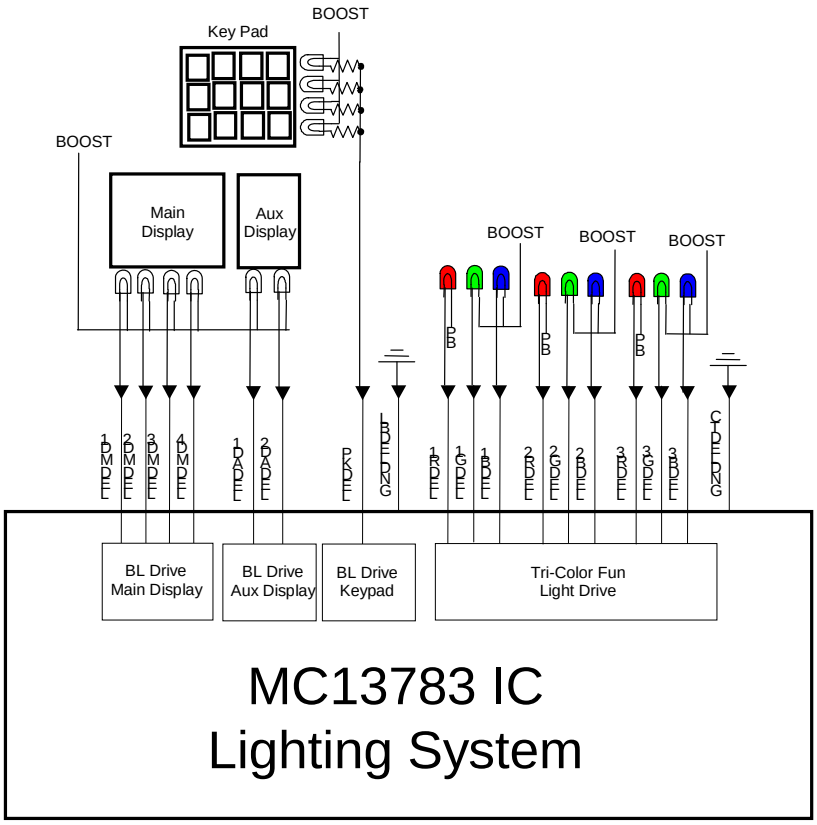

Figure 12. MC13783 Lighting System

4.5.2.1 Backlight Drivers

The backlight drivers are generally intended for White LED (WLED) backlighting of color LCD displays or white/blue LED backlighting for key pads. The drivers consists of independently programmable current sinking channels. SPI registers control programmable features such as DC current level, auto ramping / dimming and PWM settings.

Three zones are provided for typical applications which may include backlighting a main display, auxiliary display, and key pad. However, the drivers can be utilized for other lighting schemes such as an integrated WLED flashlight or even non-LED system applications requiring programmable current sinks.

The integrated boost switcher provided on the MC13783 is used to supply the backlights. It automatically adapts its output voltage to allow for power optimized biasing of white and/or blue LEDs. Alternatively, any other available source with sufficient current drive and output voltage for necessary diode headroom may be used (5.5 V should not be exceeded).

4.5.2.2 Tri-Color LED Drivers

The tri-color circuitry provides expanded capability for independent lighting control and distribution that supplements the backlight drivers circuitry. The tri-color drivers have the same basic programmability as the backlight drivers, with similar bit control for current level, duty cycle control, and ramping. A boosted

supply such as the on-chip boost switcher should be used to ensure adequate headroom if necessary, such as for driving blue LEDs.

The channel naming assignments are R, G, and B representative of applications which use red, green, and blue colored LEDs on each of the respective zones. One set of RGB drivers constitute a tri-color bank, and the MC13783 features three tri-color banks.

Each tri-color LED driver is programmable for independent control of timing and current levels. Programmable fun light patterns are also provided to allow initiation of predefined lighting routines with convenient SPI efficiency, reducing the communication burden of running complex lighting sequences.

5 Package Information

The package style is a low profile BGA, pitch 0.5 mm, body 10 × 10mm, semi populated 19 × 19 matrix, ball count 247 including 4 sets of triple corner balls and 4 spare balls.

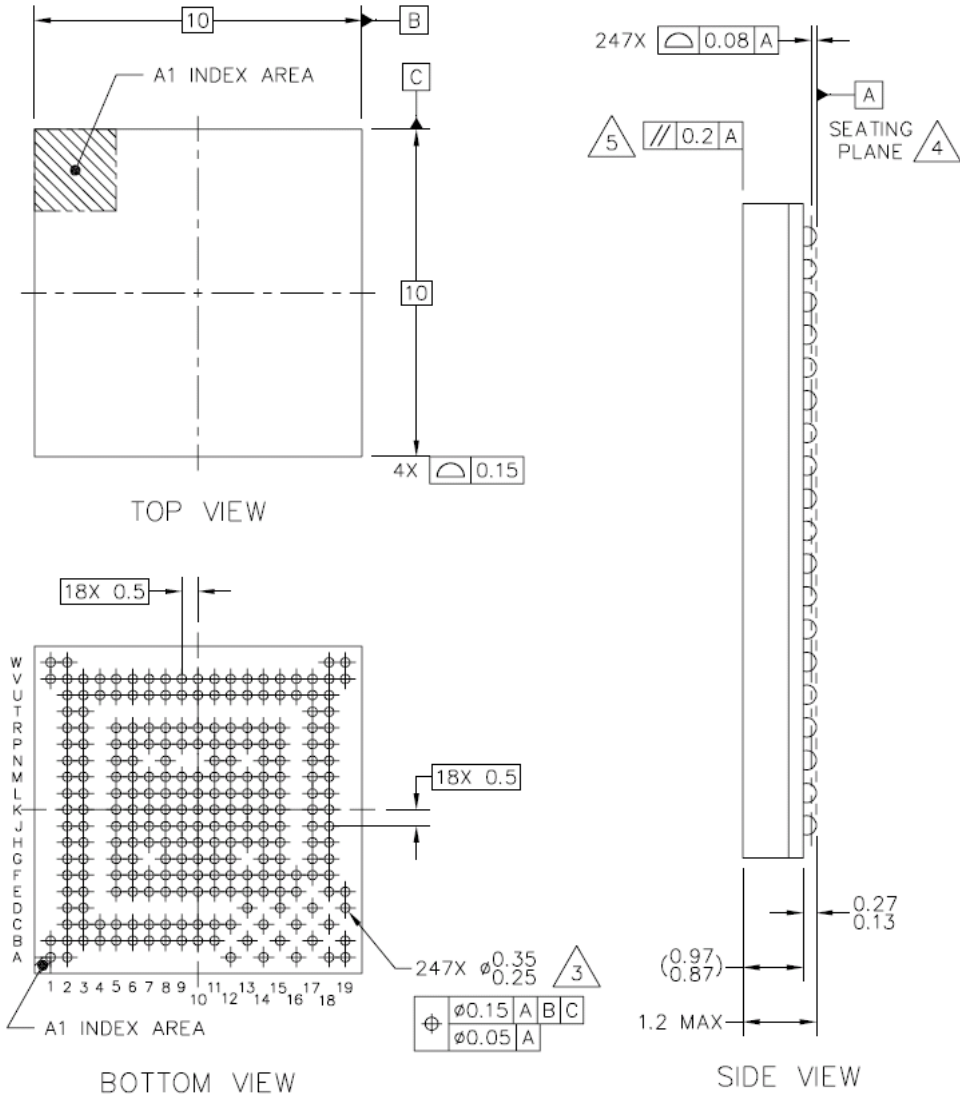

Figure 13. Package Drawing

6 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com on the Documentation page.

Table 27 summarizes revisions to this document since the previous release (Rev. 3.4).

Table 27. Revision History

Location	Revision
Table 1	Change SW3IN to HV in Table 1.
Table 3	Updated consumption numbers in Table 3.
Table 9	Changed VRFBG max load to 0.1mA in Table 9
Table 9	Updated loads on LDOs vs. Output voltage in table 9
Table 10	Note added in table 10 to add 3 more rows for various capacitor values.
Table 4.4.1.2.2	Updated trickle levels in section 4.4.1.2.2
Table 4.4.1.2.2	Comment added to section 4.4.1.2.2: For the single path charging configuration, Standalone trickle charging is only available for the SE1 = LOW condition. The charge level remains constant at the lower 70mA threshold through all battery voltage ranges. That is, there is no increased charge current at the 2.7V threshold. Standalone Trickle charging is not available for the SE1 = HIGH / Single Path charging case.

NOTES

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