Hex Buffer

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage, V_{DD}.

The input–signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS–to–TTL/DTL converter (V_{DD} = 5.0 V, V_{OL} \leq 0.4 V, I_{OL} \geq 3.2 mA).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

Features

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- V_{IN} can exceed V_{DD}
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in}	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
V _{out}	Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
l _{in}	Input Current (DC or Transient) per Pin	±10	mA
l _{out}	Output Current (DC or Transient) per Pin	±45	mA
PD	Power Dissipation, per Package (Note 1) (Plastic) (SOIC)	825 740	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
ΤL	Lead Temperature (8–Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: See Figure 3.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the V_{SS} pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high–impedance circuit. For proper operation, the ranges $V_{SS} \le V_{in} \le 18$ V and $V_{SS} \le V_{out} \le V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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SOIC-16 D SUFFIX CASE 751B

TSSOP-16 DT SUFFIX CASE 948F

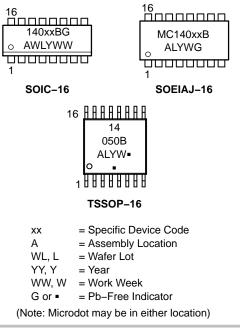
PIN ASSIGNMENT

F SUFFIX

CASE 966

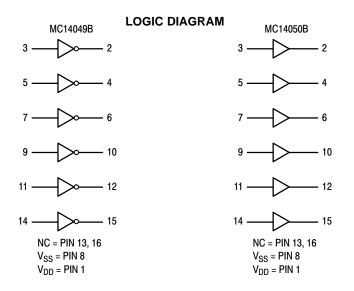
	1•	16] NC
	2	15] OUT _F
IN _A [3	14] IN _F
	4	13] NC
IN _B [5	12] OUT _E
OUT _C [6	11] IN _E
IN _C [7	10] OUT _D
v _{ss} [8	9] IN _D

MARKING DIAGRAMS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.



ORDERING INFORMATION

Device	Package	Shipping [†]		
MC14049BDG	SOIC-16 (Pb-Free)	48 Units / Rail		
MC14049BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel		
NLV14049BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel		
MC14049BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel		
	1			
MC14050BDG	SOIC-16	48 Units / Rail		
	(Pb-Free)			
NLV14050BDG*	SOIC-16	48 Units / Rail		
	(Pb-Free)			
MC14050BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel		
NLV14050BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel		
MC14050BDTG	TSSOP-16 (Pb-Free)	96 Units / Rail		
NLV14050BDTG*	TSSOP-16 (Pb-Free)	96 Units / Rail		
MC14050BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel		
MC14050BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. *NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

				-55	5°C		+25°C		+12	5°C	
Characteristic		Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD}	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V _{in} = 0	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- -	4.95 9.95 14.95	- - -	Vdc
Input Voltage $(V_O = 4.5 \text{ Vdc})$ $(V_O = 9.0 \text{ Vdc})$ $(V_O = 13.5 \text{ Vdc})$	"0" Level	V _{IL}	5.0 10 15	_ _ _	1.5 3.0 4.0	_ _ _	2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	Vdc
$(V_{O} = 0.5 \text{ Vdc})$ $(V_{O} = 1.0 \text{ Vdc})$ $(V_{O} = 1.5 \text{ Vdc})$	"1" Level	V _{IH}	5.0 10 15	3.5 7.0 11		3.5 7.0 11	2.75 5.50 8.25		3.5 7.0 11		Vdc
$\begin{array}{l} \text{Output Drive Current} \\ (\text{V}_{\text{OH}} = 2.5 \ \text{Vdc}) \\ (\text{V}_{\text{OH}} = 9.5 \ \text{Vdc}) \\ (\text{V}_{\text{OH}} = 13.5 \ \text{Vdc}) \end{array}$	Source	I _{ОН}	5.0 10 15	-1.6 -1.6 -4.7	_ _ _	-1.25 -1.30 -3.75	-2.5 -2.6 -10		-1.0 -1.0 -3.0	_ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	3.75 10 30	- - -	3.2 8.0 24	6.0 16 40		2.6 6.6 19	- - -	mAdc
Input Current		l _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V _{in} =	: 0)	C _{in}	-	-	_	-	10	20	-	-	pF
Quiescent Current (Per I	Package)	I _{DD}	5.0 10 15	_ _ _	1.0 2.0 4.0	_ _ _	0.002 0.004 0.006	1.0 2.0 4.0	_ _ _	30 60 120	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, per package) (C _L = 50 pF on all outputs, all buffers switching		Ι _Τ	5.0 10 15			$I_{T} = (3)$	1.8 μΑ/kHz) f 3.5 μΑ/kHz) f 5.3 μΑ/kHz) f	+ I _{DD}			μAdc

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

The formulas given are for the typical characteristics only at +25°C
 To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$

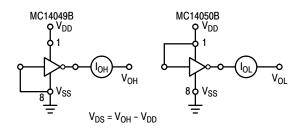
Where: I_T is in μ A (per Package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency and k = 0.002.

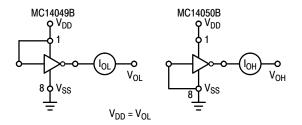
AC SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = + 25^{\circ}C$)

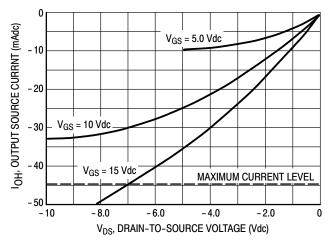
Characteristic	Symbol	V _{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (0.7 \text{ ns/pF}) C_1 + 65 \text{ ns}$	t _{TLH}	5.0		100	160	ns
$t_{TLH} = (0.25 \text{ ns/pF}) \text{ C}_{L} + 37.5 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) \text{ C}_{L} + 37.5 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) \text{ C}_{L} + 30 \text{ ns}$		10 15	-	50 40	80 60	
Output Fall Time	t _{THL}	13	_	40	00	ns
t _{THL} = (0.2 ns/pF) C _L + 30 ns t _{THL} = (0.06 ns/pF) C _L + 17 ns t _{THL} = (0.04 ns/pF) C _L + 13 ns		5.0 10 15	- - -	40 20 15	60 40 30	
Propagation Delay Time $t_{PLH} = (0.33 \text{ ns/pF}) \text{ C}_{L} + 63.5 \text{ ns}$ $t_{PLH} = (0.19 \text{ ns/pF}) \text{ C}_{L} + 30.5 \text{ ns}$ $t_{PLH} = (0.06 \text{ ns/pF}) \text{ C}_{L} + 27 \text{ ns}$	t _{PLH}	5.0 10 15	- - -	80 40 30	140 80 60	ns
Propagation Delay Time $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$	t _{PHL}	5.0 10	-	40 20	80 40	ns
t _{PHL} = (0.05 ns/pF) C _L + 12.5 ns		15	-	15	30	

5. The formulas given are for the typical characteristics only at 25°C.

6. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.









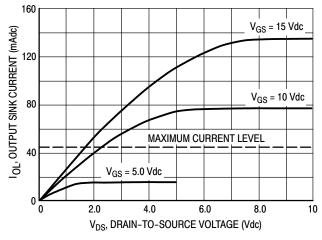


Figure 2. Typical Output Sink Characteristics

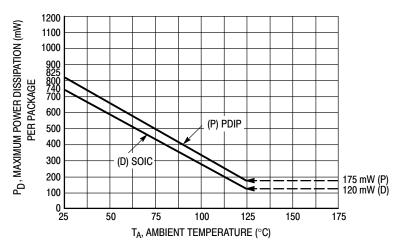


Figure 3. Ambient Temperature Power Derating

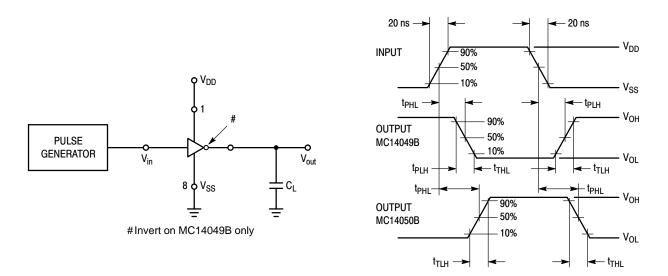
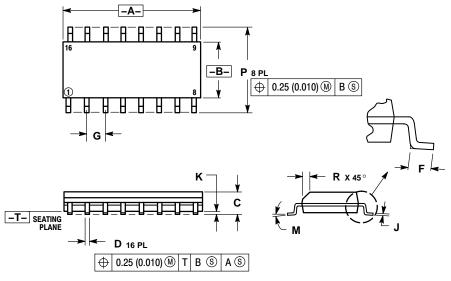


Figure 4. Switching Time Test Circuit and Waveforms

PACKAGE DIMENSIONS

SOIC-16 **D SUFFIX** CASE 751B-05 ISSUE K

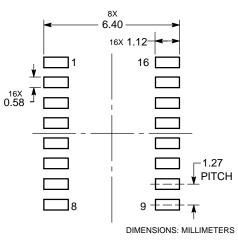


NOTES:

- 1.
- 2. 3.
- 4.
- TES: DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. 5.

	MILLIN	IETERS	INC	HES		
DIM	MIN MAX		MIN	MAX		
Α	9.80	10.00	0.386	0.393		
В	3.80	4.00	0.150	0.157		
C	1.35	1.75	0.054	0.068		
D	0.35	0.49	0.014	0.019		
F	0.40	1.25	0.016 0.04			
G	1.27	BSC	0.050	BSC		
J	0.19	0.25	0.008	0.009		
Κ	0.10	0.25	0.004	0.009		
М	0 °	7°	0 °	7°		
Ρ	5.80	6.20	0.229	0.244		
R	0.25	0.50	0.010	0.019		

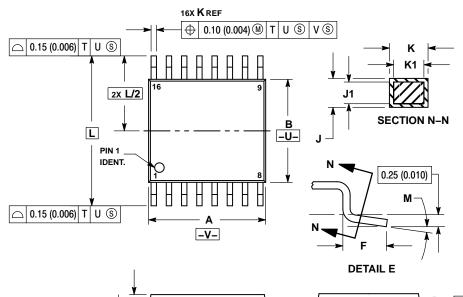
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS





G

С

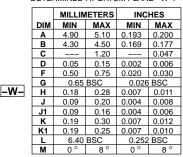
D

○ 0.10 (0.004)

-T- SEATING PLANE

NOTES: 1. DIMENSIONING AND TOLERANCING PER

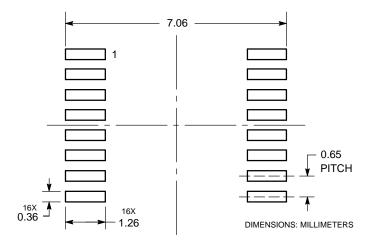
- ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EYCEED 0.25 (0.410) PEP SIDE 3.
- NOT EXCEED 0.25 (0.010) PER SIDE. 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL
- CONDITION. 6. TERMINAL NUMBERS ARE SHOWN FOR
- TERMINEL NOMBERS ARE SHOWN REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.



SOLDERING FOOTPRINT*

н

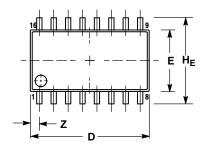
DETAIL E

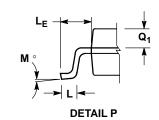


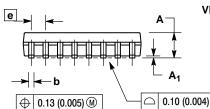
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

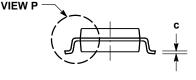
PACKAGE DIMENSIONS

SOEIAJ-16 **F SUFFIX CASE 966 ISSUE A**









NOTES:

DIMENSIONING AND TOLERANCING PER ANSI

1. DIMENSIONING DIVE ... Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15

(0.006) PER SIDE. . TERMINAL NUMBERS ARE SHOWN FOR

REFERENCE ONLY. 5. THE LEAD WIDTH DIMENSION (b) DOES NOT 5 INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A ₁	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
C	0.10	0.20	0.007	0.011	
D	9.90	10.50	0.390	0.413	
E	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050) BSC	
HE	7.40	8.20	0.291	0.323	
L	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
Μ	0 °	10 °	0 °	10 °	
Q ₁	0.70	0.90	0.028	0.035	
Z		0.78		0.031	

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