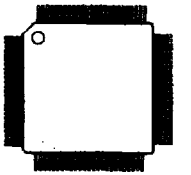
MC141518

LCD Segment Driver
CMOS

The MC141518 is a high voltage passive LCD Segment driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 80 segment driving outputs for 64 MUX or lower LCD panel. The MC141518 is a companion chip of MC141516 (Backplane driver). It can be directly connected to the display controller inside the Motorola microcomputer MC68HC05L11.

- Operating Supply Voltage Range-
  Logic (V_{DD}): 2.7V to 5.5V
  Segment Drivers (V_{LCD}): 6.0V to 13V
- Operating Temperature Range: -20 to 70°C
- 80 LCD segment driving signals
- Driving Duty Cycle (MUX): 1/32 to 1/64
- Casadable for more LCD segment driving outputs
- Serial interface for both display data and control instruction transfers
- 100-pin TQFP (Thin Quad Flat Package)



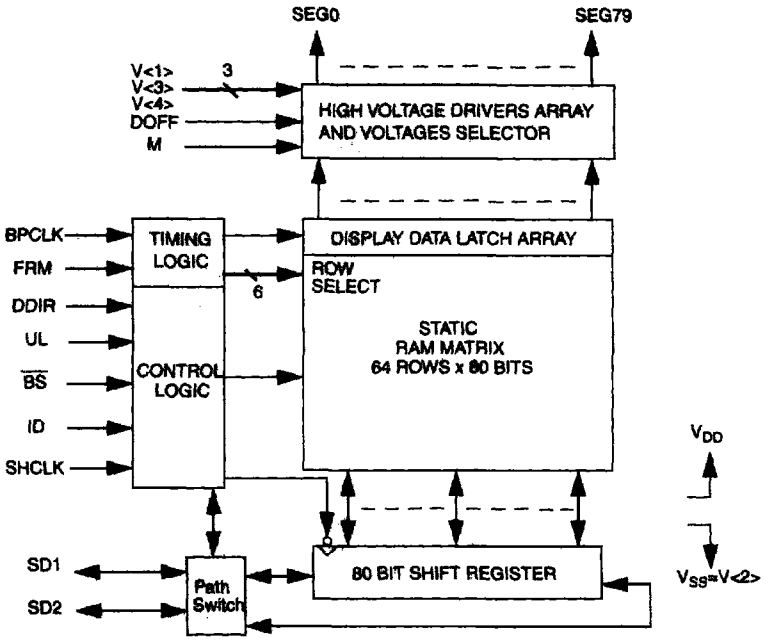
MC141518FJ
TQFP

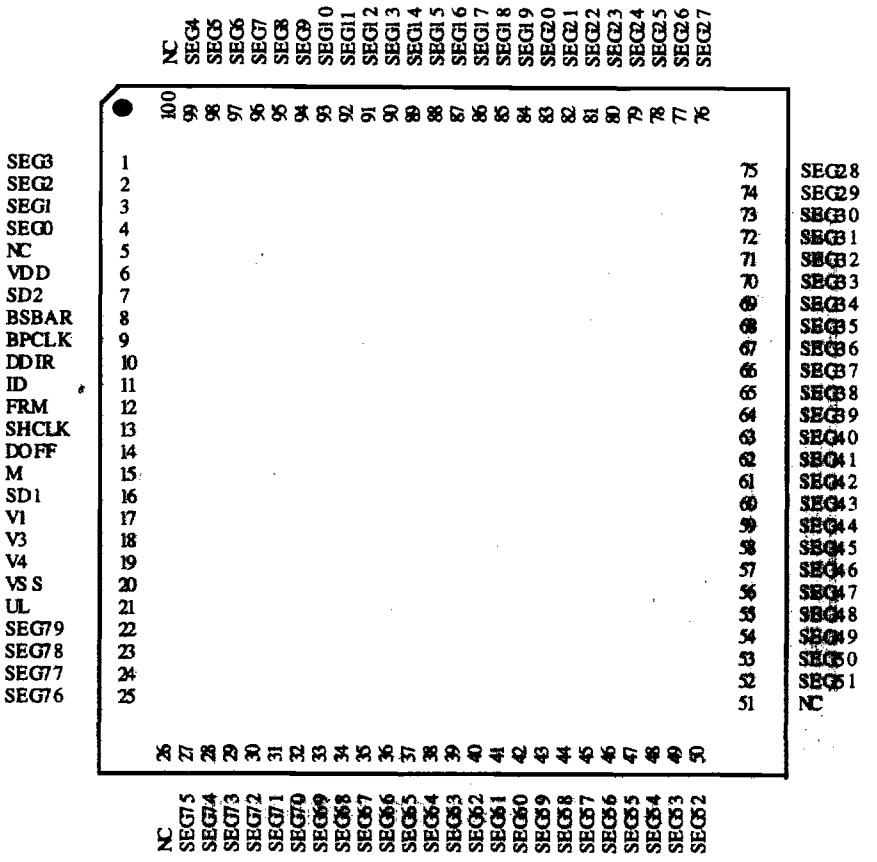
MCC141518
DIE

ORDERING INFORMATION

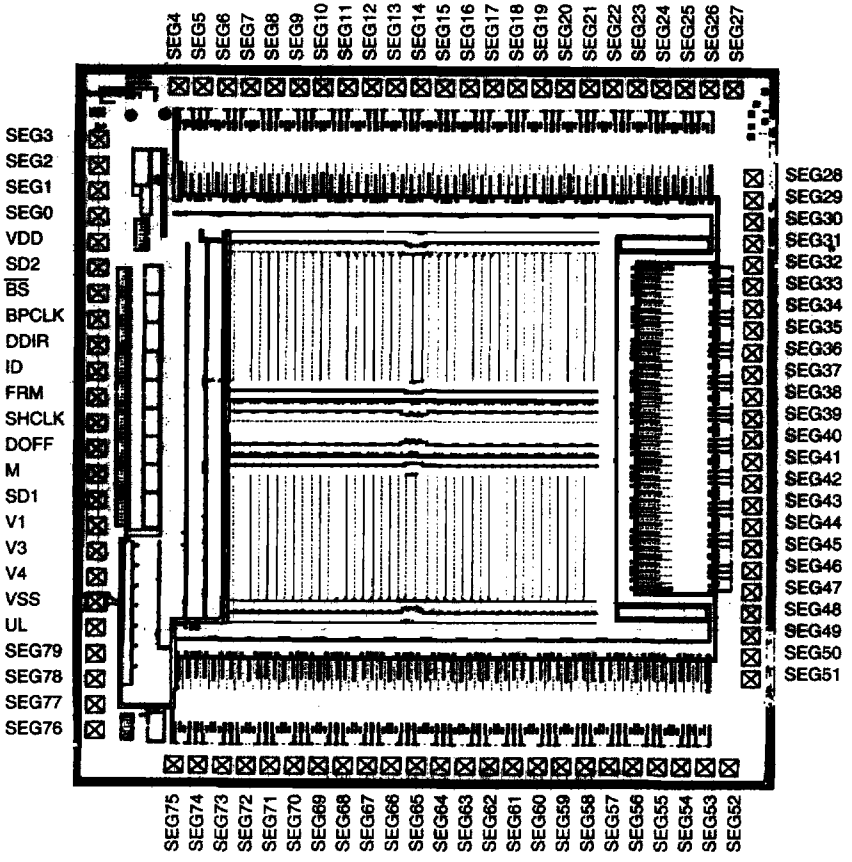
MC141518FJ	TQFP
MCC141518	DIE

BLOCK DIAGRAM





MC141518FJ Pin Assignment



MCC141518 PAD ASSIGNMENT

MAXIMUM RATINGS* (Voltages Reference to V_{SS}, T_A=25 °C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7	V
V<1>		V_{SS} -0.3 to V_{SS} +15	V
V_{in}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to +70	°C
T_{stg}	Storage Temperature Range	-65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description Section.

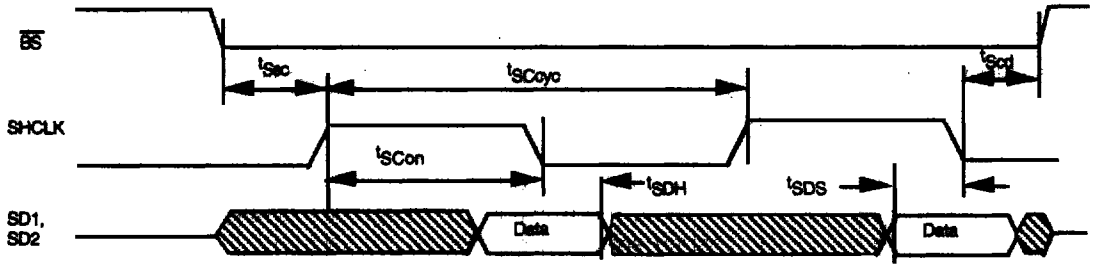
The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range Vss < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either Vss or VDD). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=25°C, V_{DD}=5.0V, V<1>=13V)

Symbol	Parameter		Min	Max	Unit
V_{IH}	Input High Voltage	BPCLK, FRM, M, ID, DDIR	0.7xV_{DD}	V_{DD}	V
		$\overline{BS}$, SD1, SD2, SHCLK, DOFF			
V_{IL}	Input Low Voltage	BPCLK, FRM, M, ID, DDIR	V_{SS}	0.3xV_{DD}	V
		$\overline{BS}$, SD1, SD2, SHCLK, DOFF			
V_R	Data Retention		2.0	-	V
I_{in}	Input Current	BPCLK, FRM, M, ID, DDIR	-	±1	uA
		$\overline{BS}$,SD1, SD2, SHCLK, DOFF			
C_{in}	Capacitance	BPCLK, FRM, M, ID, DDIR,	-	8	pF
		$\overline{BS}$,SD1, SD2, SHCLK, DOFF			
V_{OH}	Output High Voltage	SD1, SD2	0.8xV_{DD}	V_{DD}	V
V_{OL}	Output Low Voltage	SD1, SD2	V_{SS}	0.2xV_{DD}	V
	Operating Voltages				
V_{DD}	Supply Voltage (referenced to V_{SS})		2.7	5.5	V
V<1>	LCD Voltage (referenced to V_{SS})		0.0	+13	V
	Operating supply current V_{DD} (V_{DD}=5V, V<1>=13V, M=2MHz)				
I_{ACC}	Dynamic Mode (Display on, R/W access, BPCLK=4KHz, SHCLK=5MHz)		-	200	uA
I_{DP}	(Display on, R/W disable, BPCLK=4KHz)		-	20	uA
I_{SB}	Standby Mode(Display off, R/W disable)		-	5	uA
	Operating supply current V<1> (V<1>=13V)				
I_{LDP}	Display Mode		-	30	uA
I_{LSB}	Standby Mode		-	2	uA

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V +/-5%, V_{SS}=0, T_A=25°C, V<1>=13V)

Symbol	Parameter	Min	Max	Unit
t_{SCcyc}	Shift Clock Cycle Time	200	-	ns
t_{SCon}	Shift Clock On Time	100	-	ns
t_{SDS}	Serial Data Setup Time	50	-	ns
t_{SDH}	Serial Data Hold Time	10	-	ns
t_{Ssc}	Select to clock on	100	-	ns
t_{Scs}	Clock on to device disable	10	-	ns



MC141518 Timing Diagram (with $\overline{BS}$ = 0)

PIN DESCRIPTIONS

V_{DD} and V_{SS}

Power is supplied to the driver using these two pins. V_{DD} is power and V_{SS} is ground.

V<1>,V<3>,V<4>

These are the inputs of voltage levels for the LCD driving signals (Fig. 2).

DOFF

This is an input pin to turn off the LCD. If it is set, all the high voltage drivers are switched off.

FRM

This is an input pin for frame timing synchronisation. This pin is connected either to FRM of the microcomputer MC68HC05L11 or to FRM of the Backplane driver MC141516.

BPCLK

This is an input pin for a periodic signal from the microcomputer to segment driver for timing synchronisation. This pin is connected either to BPCLK of the microcomputer MC68HC05L11 or to BPCLK of the Backplane driver MC141516.

SEG0-SEG79

These 80 output lines provide the segment driving signals to the LCD panel. They are all high impedance while the display is turned off (i.e. DOFF is selected).

$\overline{BS}$

This is the Bank Select pin. It is an active low input for chip enable.

UL

This pin is used to set the segment driver to support the Upper or Lower panel for a split LCD panel system. Since any segment driver to the upper panel will be 180 degree rotated with respect to the lower panel's segment drivers, to maintain easier routing and consistent in data format, the serial data direction has to be reversed. Therefore whenever UL is tied high, the serial data direction inside the segment drivers will be reversed with respect to the serial data direction as UL is ground. Details about the serial data direction can be found in the SD1, SD2 description.

SD1, SD2

These pins are two bidirectional serial data lines connected to either one of the two serial ports of the microcomputer MC68HC05L11 (UD1, UD2 LD1 and LD2) depending on the UL pin. If the segment driver is set to serve the upper panel with its UL tied high, serial data direction between SD1 and SD2 is reversed. In such case, SD1 is connected either to UD1 or to LD1 of MC68HC05L11. SD2 is then connected to UD2 or LD2 of MC68HC05L11. However, if the UL pin is ground, SD1 and SD2 are then connected to UD2 and UD1, or LD2 and LD1 of MC68HC05L11 respectively. SD1 and SD2 allow the display data or instruction from the microcomputer entering the segment driver in both directions. During $\overline{BS}$ high, these two pins are high impedance. In case of an instruction from the microcomputer with ID pin set. SD1 and SD2 are disconnected from the 80-bit shift register and form a transparent loop. Instruction bits entering the segment through a serial port (say SD1) are exported to its cascading device immediately through another serial port (i.e. SD2). In such a way, this instruction from the microcomputer can be broadcasted to a bank of cascading segments. See Typical Application Section for typical system connections.

ID

This is the Instruction/Data pin. If this pin is set, an instruction byte is shifting in from the bidirectional data lines as soon as $\overline{BS}$ goes low. Otherwise, data in the bidirectional lines is the display data. (See SD1 and SD2 definitions). Instructions are described in Table 2. Though each instruction has eight bits, the segment needs 12 SHCLK cycles to complete it. Eight cycles to fill in the internal instruction register and the last four cycles are use for instructions processing. Once the instruction is completed, additional SHCLK is ignored until $\overline{BS}$ signal toggles from high to low again. See Figure 1 for details. Notice that internal sampling for the instruction register should be as the order of MSB to LSB if DDIR is 0 and LSB to MSB if DDIR is 1, doesn't matter what UL is.

SHCLK

This is the shift clock from the microcomputer MC68HC05L11 to the segment for clocking the serial data on SD1 and SD2.

DDIR

It is an input pin specifying the direction of the serial data. DDIR definition is also affected by UL pin as specified in Table 2. If UL pin is found low and DDIR is set, the serial data enters the segment driver through SD1 and leaves the segment driver through SD2. If both UL and DDIR are zeros, SD1 and SD2 are redefined as output and input respectively. If UL pin is high and DDIR is set, the serial data then enters the segment driver through SD2 and leaves the segment driver through SD1. If UL is high but DDIR is clear, SD2 and SD1 are output and input respectively.

UL	DDIR	Internal Serial Data Direction
0	0	←SD2——bidirectional shifter register——SD1→
0	1	←SD2——bidirectional shifter register——SD1←
1	0	←SD2——bidirectional shifter register——SD1←
1	1	→SD2——bidirectional shifter register——SD1→

Table 1. Summary of Data Direction Flow Responding To DDIR and UL Bit.

OPERATION OF LCD DRIVER

INTRODUCTION

The LCD segment driver is capable of 1:6 bias (for 32 mux) to 1:9 bias (for 64 mux), depending on the voltage divider ratio of Fig.2. The ratio of bias (a) is defined as

$$1:\frac{4xR1+R2}{R1}=1:a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a=\sqrt{mux}+1$$

To set up a multiplex ratio, please refer to either Section 10.6.2., the Technical data of MC68HC05L11 or the Advanced Information of the Backplane MC141516.

CONTROL LOGIC produces the control signals necessary for display RAM read/write and serial data latching. This Control Logic can be controlled by the MCU through the serial interface with ID set. MCU writing a byte of instruction (ID7 to ID0) to the Segment Control Register through the serial interface will cause Segment driver(s) to carry functions as shown as Table 2.

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	ROW ADDRESS (WRITE IN)					
0	1	ROW ADDRESS (READ FROM)					
1	0	SCROLL UP ADVANCE					
1	1	X	X	X	CLR SH	X	RESET

TABLE 2. A Summary of the Control Functions of Segment Driver

ROW ADDRESS(WRITE IN) instruction causes the segment driver(s) to load the content of the 80 BITS SHIFT REGISTER into a row of RAM which address is specified by ID5 to ID0.

ROW ADDRESS(READ FROM) instruction causes the segment driver(s) to copy a row of RAM which address is specified by ID5 to ID0 into the 80 BIT SHIFT REGISTER.

SCROLL UP ADVANCE instruction causes the segment driver(s) to do vertically scroll up or down. The content of ID5 to ID0 represents the vertical offset of the new screen to the current screen. This vertical offset is added up with an old offset which is stored in a register called the VERTICAL SCROLL VECTOR REGISTER. The sum of these is the new offset and will be stored in the VERTICAL SCROLL VECTOR REGISTER. The VERTICAL SCROLL VECTOR REGISTER is default zero during power-on.

RESET BIT0 Writing an "1" to this bit will clear the VERTICAL SCROLL VECTOR REGISTER.

CLRSH BIT2 Writing an "1" to this bit will clear the content of the 80 BIT SHIFT REGISTER.

An instruction (ID7 to ID0) is transferred to the segment driver through the serial interface as Figure 1 demonstrated. Figure 1-a shows a case that the DDIR bit is clear. The most significant bit ID7 of the instruction will come in as the first bit. After 8 SHCLK cycles, a byte of instruction data is kept in an instruction register. However, the instruction needs another 4 cycles to complete, as long as $\overline{BS}$ holds low, segment driver will wait for these 4 cycles to complete the instruction. After the instruction, the segment driver will ignore any coming SHCLK cycle until the signal $\overline{BS}$ toggles from high to low again. Figure 1-b shows in case of DDIR bit set. The UL bit will not affect the order of instruction shifting. For most case, user does not need to worry about the order of shifting if the segment is connected to the display controller in the microcomputer MC68HC05L11.

TIMING LOGIC, according to BPCLK and FRM, fills the DISPLAY DATA LATCH ARRAY with rows of RAM matrix's content periodically starting from the row address specified in the VERTICAL SCROLL VECTOR REGISTER.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels among <V1>, <V3>, <V4> and <V2>. (See Fig. 2).

DISPLAY DATA LATCH ARRAY is used to buffer up a row of display data from RAM.

STATIC RAM MATRIX consists of 64 rows x 80 bits of SRAM cell. The content of these RAM cells can be read from/written to the 80 BIT SHIFT REGISTER.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as seg(x) in Fig. 3.

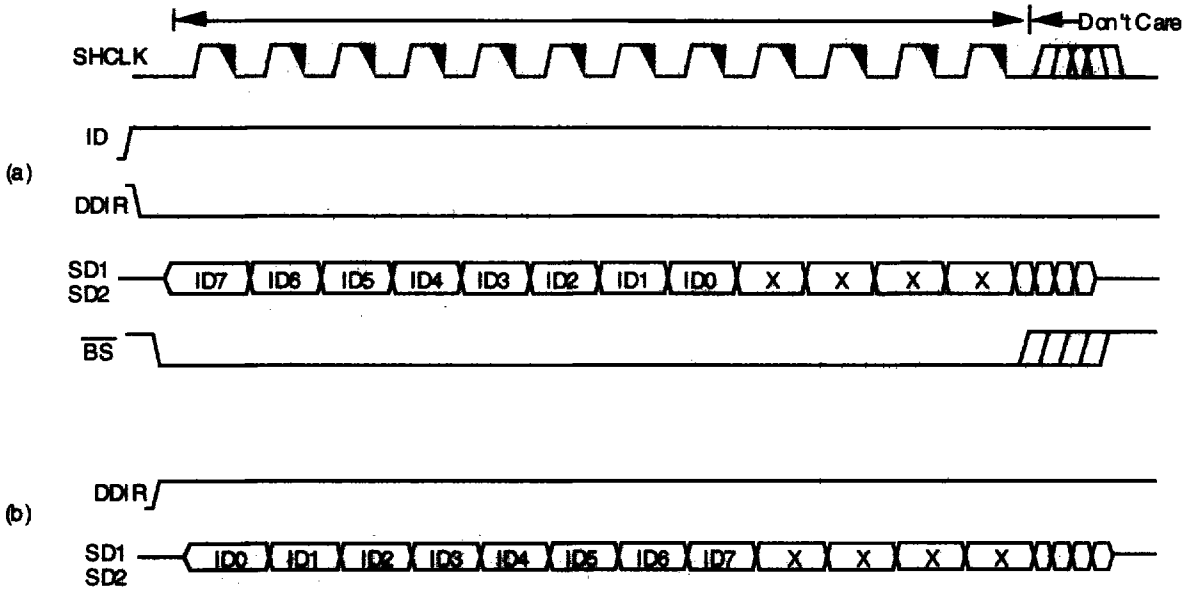


Figure 1. The order of instruction byte shifted

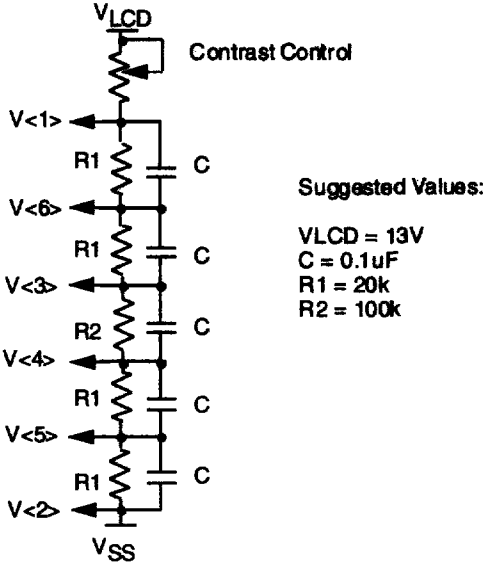


Figure 2. External Voltage Divider

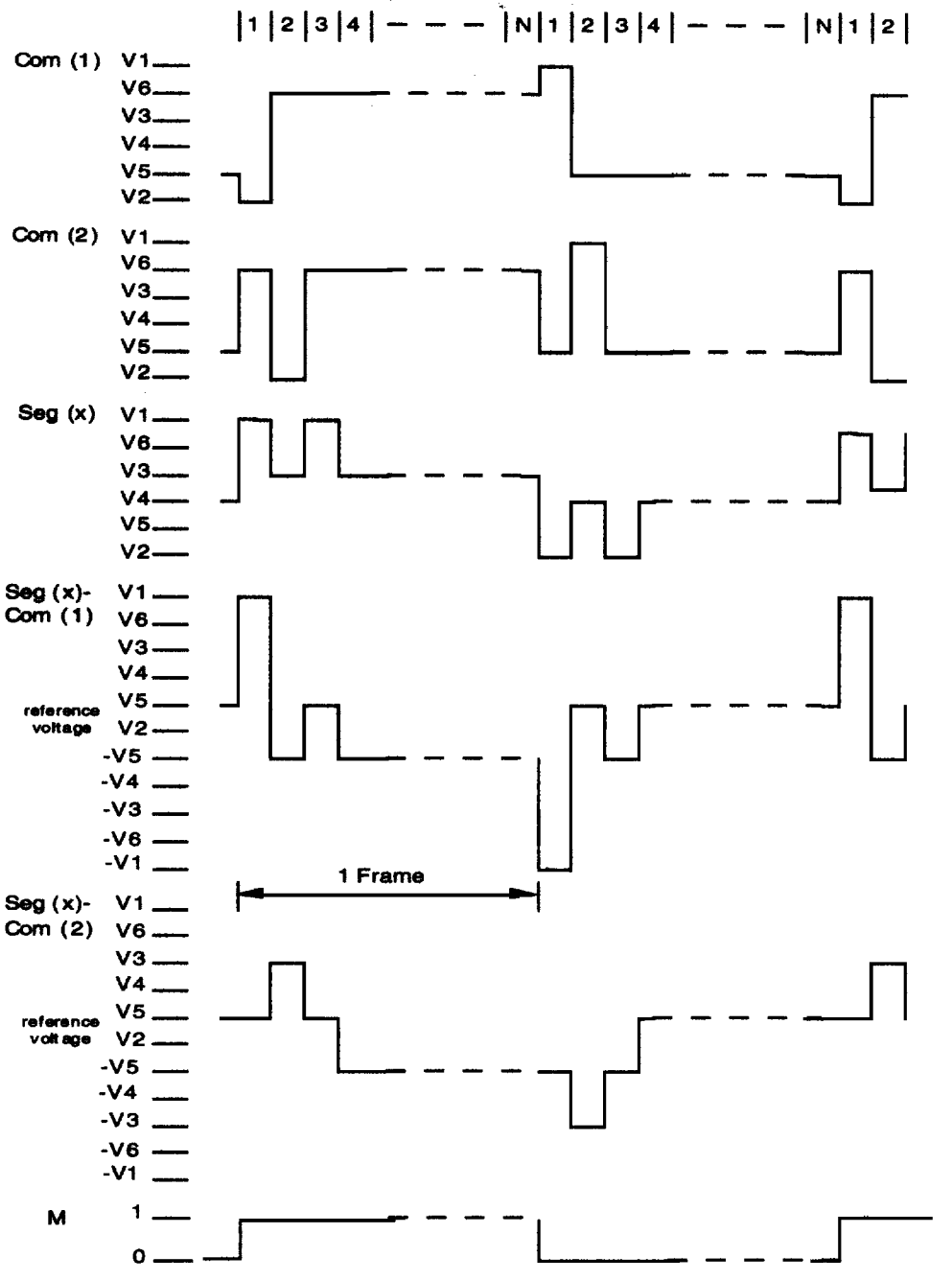
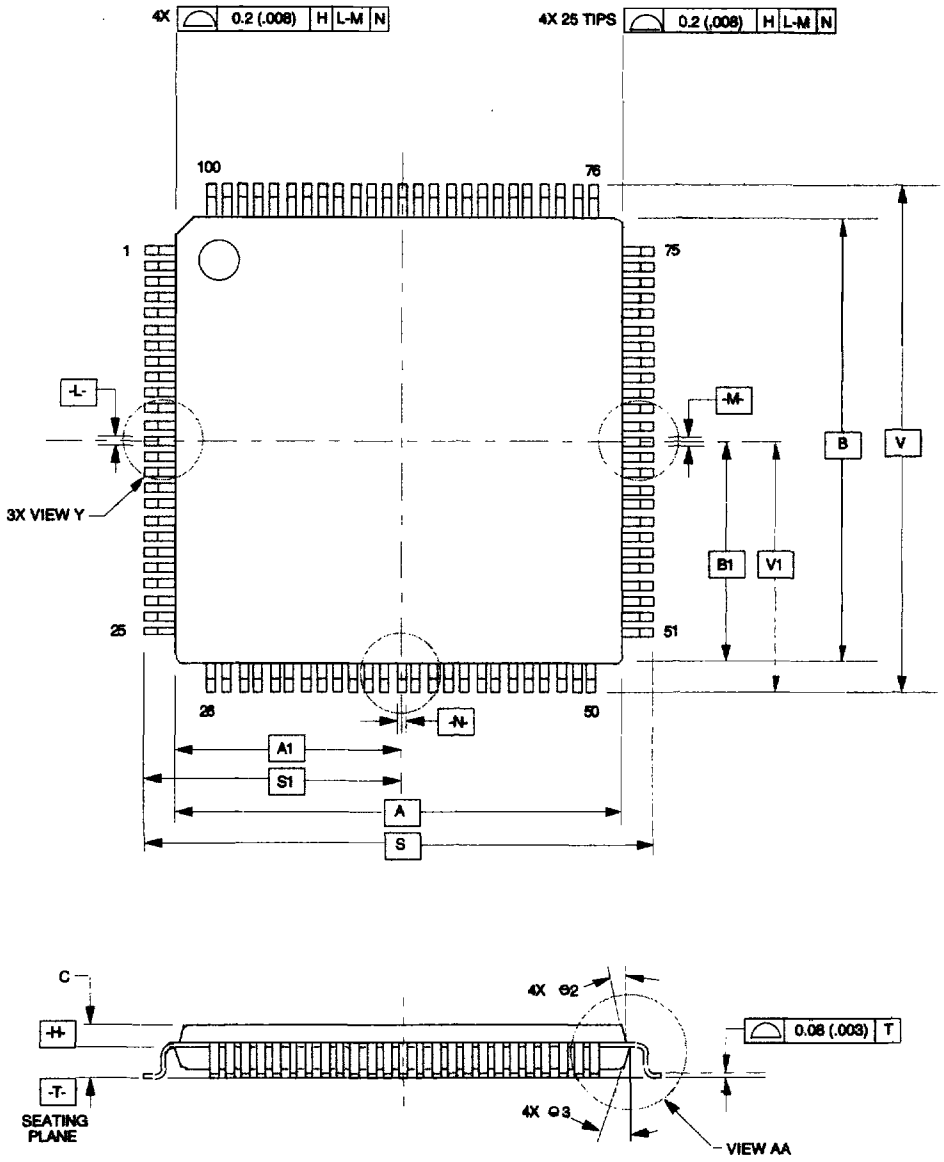


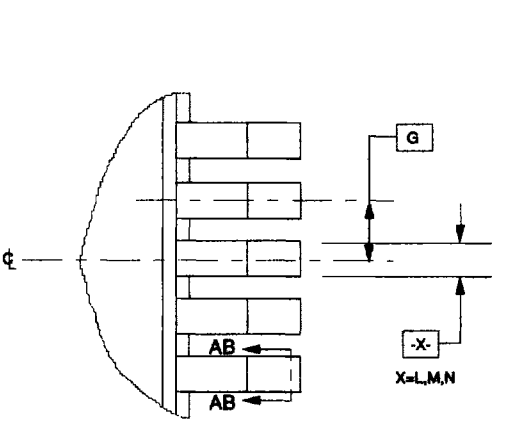
Figure 3. Driving waveforms of 1:N multiplex

PACKAGE DIMENSIONS

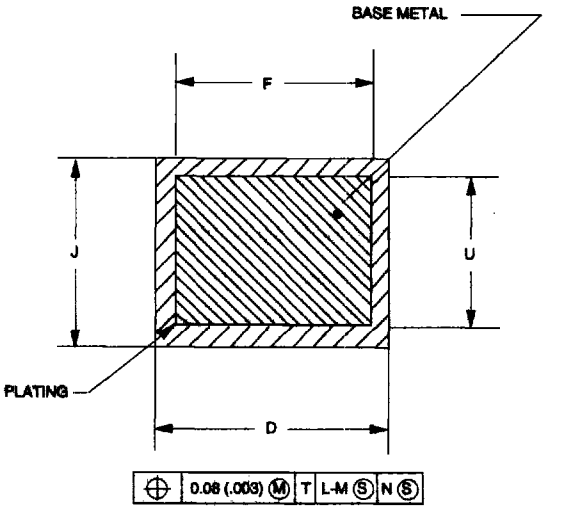
MC141518FJ
TQFP PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



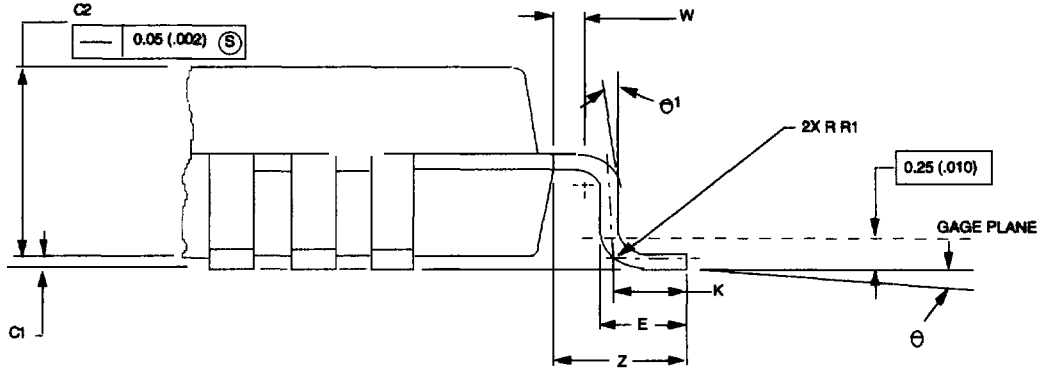
MC141518FJ
TQFP PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



VIEW Y



SECTION AB-AB
ROTATED 90° CLOCKWISE



VIEW AA

MC141518FJ TQFP PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	14.00	BSC	.551	BSC	K	0.50	REF	.020	REF
A1	7.00	BSC	.276	BSC	R1	0.08	0.20	.003	.008
B	14.00	BSC	.551	BSC	S	16.00	BSC	.630	BSC
B1	7.00	BSC	.276	BSC	S1	8.00	BSC	.315	BSC
C	---	1.70	---	.066	U	0.09	0.16	.004	.006
C1	0.05	0.20	.002	.008	V	16.00	BSC	.630	BSC
C2	1.30	1.50	.051	.059	V1	8.00	BSC	.315	BSC
D	0.10	0.30	.004	.012	W	0.20	REF	.008	REF
E	0.45	0.75	.016	.030	Z	1.00	REF	.039	REF
F	0.15	0.23	.006	.009	θ	0°	7°	0°	7°
G	0.50	BSC	.020	BSC	θ1	0°	---	0°	---
J	0.07	0.20	.003	.008	θ2	12°	REF	12°	REF
					θ3	12°	REF	12°	REF

NOTES:

1. Dimensions and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane [-H-] is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums [-L-], [-M-] and [-N-] to be determined at datum plane [-H-].
5. Dimensions S and V to be determined at seating plane [-T-].
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.25(.010) per side. Dimensions A and B do include mold mismatch and are determined at datum plane [-H-].
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the lead width to exceed 0.46 (.018). Minimum space between protrusion and adjacent lead or protrusion 0.07 (.003).

MCC141518 PAD COORDINATES: (UNIT: μM)

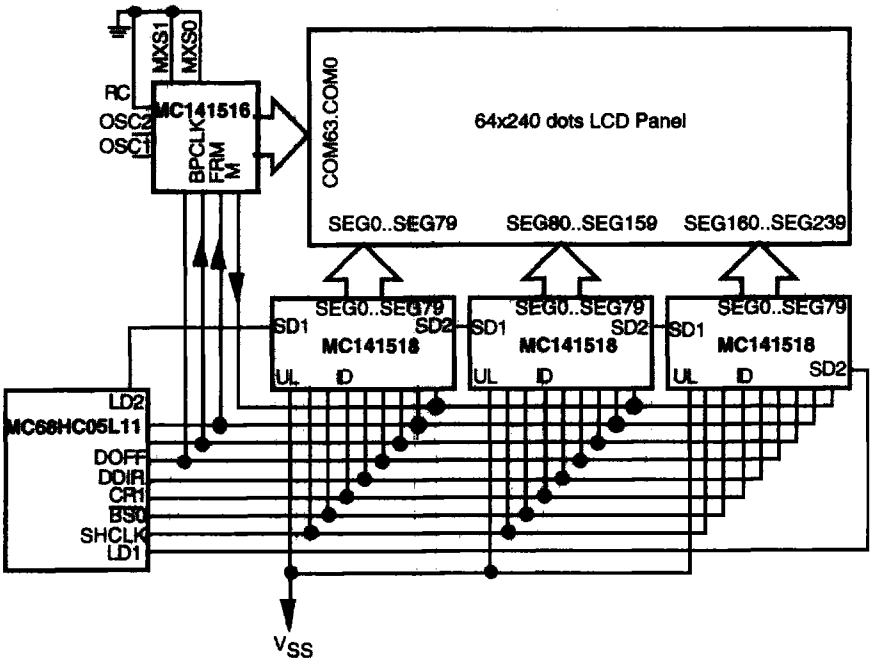
PIN NAME	X	Y	PIN NAME	X	Y
SEG3	-1835.9	-1898.5	SEG75	2180.1	-1442.5
SEG2	-1670.9	-1898.5	SEG74	2180.1	-1302.5
SEG1	-1505.9	-1898.5	SEG73	2180.1	-1162.5
SEG0	-1340.9	-1898.5	SEG72	2180.1	-1022.5
V_{DD}	-1175.9	-1898.5	SEG71	2180.1	-882.5
SD2	-1010.9	-1898.5	SEG70	2180.1	-742.5
$\overline{BS}$	-845.9	-1898.5	SEG69	2180.1	-602.5
BPCLK	-680.9	-1898.5	SEG68	2180.1	-462.5
DDIR	-515.9	-1898.5	SEG67	2180.1	-322.5
ID	-350.9	-1898.5	SEG66	2180.1	-182.5
FRM	-185.9	-1898.5	SEG65	2180.1	-42.5
SHCLK	-20.9	-1898.5	SEG64	2180.1	97.5
DOFF	144.1	-1898.5	SEG63	2180.1	237.5
M	309.1	-1898.5	SEG62	2180.1	377.5
SD1	474.1	-1898.5	SEG61	2180.1	517.5
V1	639.1	-1898.5	SEG60	2180.1	657.5
V3	804.1	-1898.5	SEG59	2180.1	797.5
V4	969.1	-1898.5	SEG58	2180.1	937.5
V_{SS}	1134.1	-1898.5	SEG57	2180.1	1077.5
UL	1299.1	-1898.5	SEG56	2180.1	1217.5
SEG79	1464.1	-1898.5	SEG55	2180.1	1357.5
SEG78	1629.1	-1898.5	SEG54	2180.1	1497.5
SEG77	1794.1	-1898.5	SEG53	2180.1	1637.5
SEG76	1959.1	-1898.5	SEG52	2180.1	1777.5

PIN NAME	X	Y	PIN NAME	X	Y
SEG4	-2179.9	-1442.5	SEG28	-1809.9	1898.5
SEG5	-2179.9	-1302.5	SEG29	-1469.9	1898.5
SEG6	-2179.9	-1162.5	SEG30	-1329.9	1898.5
SEG7	-2179.9	-1022.5	SEG31	-1189.9	1898.5
SEG8	-2179.9	-882.5	SEG32	-1049.9	1898.5
SEG9	-2179.9	-742.5	SEG33	-909.9	1898.5
SEG10	-2179.9	-602.5	SEG34	-769.9	1898.5
SEG11	-2179.9	-462.5	SEG35	-629.9	1898.5
SEG12	-2179.9	-322.5	SEG36	-489.9	1898.5
SEG13	-2179.9	-182.5	SEG37	-349.9	1898.5
SEG14	-2179.9	-42.5	SEG38	-209.9	1898.5
SEG15	-2179.9	97.5	SEG39	-69.9	1898.5
SEG16	-2179.9	237.5	SEG40	70.1	1898.5
SEG17	-2179.9	377.5	SEG41	210.1	1898.5
SEG18	-2179.9	517.5	SEG42	350.1	1898.5
SEG19	-2179.9	657.5	SEG43	490.1	1898.5
SEG20	-2179.9	797.5	SEG44	630.1	1898.5
SEG21	-2179.9	937.5	SEG45	770.1	1898.5
SEG22	-2179.9	1077.5	SEG46	910.1	1898.5
SEG23	-2179.9	1217.5	SEG47	1050.1	1898.5
SEG24	-2179.9	1357.5	SEG48	1190.1	1898.5
SEG25	-2179.9	1497.5	SEG49	1330.1	1898.5
SEG26	-2179.9	1637.5	SEG50	1470.1	1898.5
SEG27	-2179.9	1777.5	SEG51	1610.1	1898.5

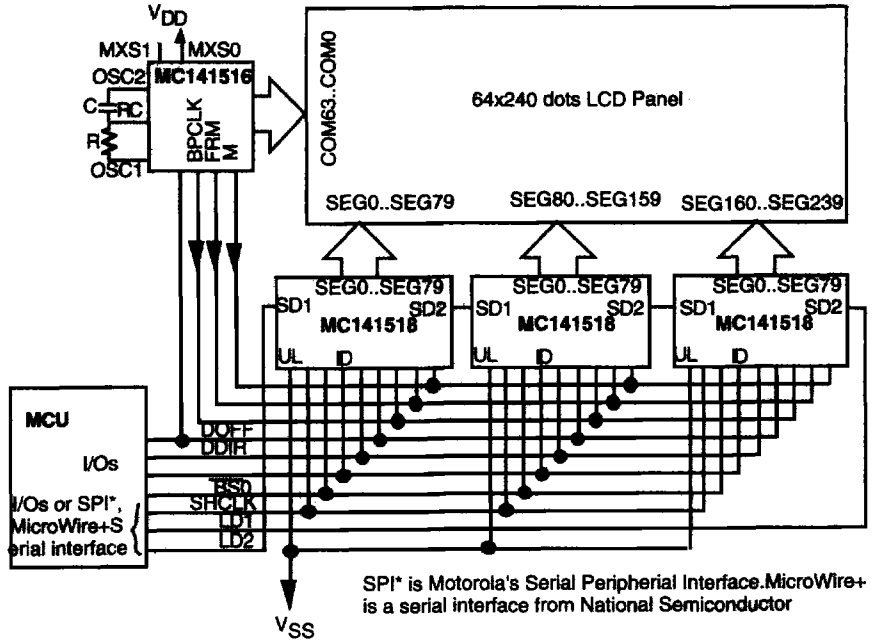
Die size: 193.5 x 167.0 mil^2
Note: 1 mil ~ 25.4μm

TYPICAL APPLICATIONS

64x240 SINGLE PANEL LCD SYSTEM WITH MC68HC05L11



64x240 SINGLE PANEL LCD SYSTEM WITH OTHER MCU



SPI* is Motorola's Serial Peripherial Interface.MicroWire+ is a serial interface from National Semiconductor

64x240x2 SPLIT PANEL LCD SYSTEM