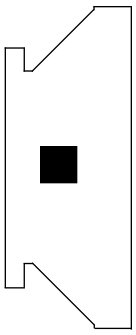
MC141519

LCD Segment Driver
CMOS

The MC141519 is an LCD segment driver chip which consists of 160x80 static RAM for display storage and provides 160 high voltage LCD driving signals.

It is a companion chip of MC141512T Backplane driver for medium LCD panels. All these chips are controlled by the MC68HC05L11 microcomputer.

- Operating Supply Voltage Range-
  Control Logic, RAM and Latch (V_{DD} Pin): 2.7 to 5.5V
  Segment drivers (V_{LCD} Pin): 8.0 to 20V
- Operating Temperature Range: -20 to 80˚C
- Direct serial data interface with the MC68HC05L11
- 160 x 80 Static RAM (Display RAM)
- 160 LCD Segment Driving Signals
- Selectable 1:16 to 1:80 Multiplex Ratios
- Expansion to higher driver count by cascade
- Available in TAB Form:
  TAB (Tape Automated Bonding), 186 contacts

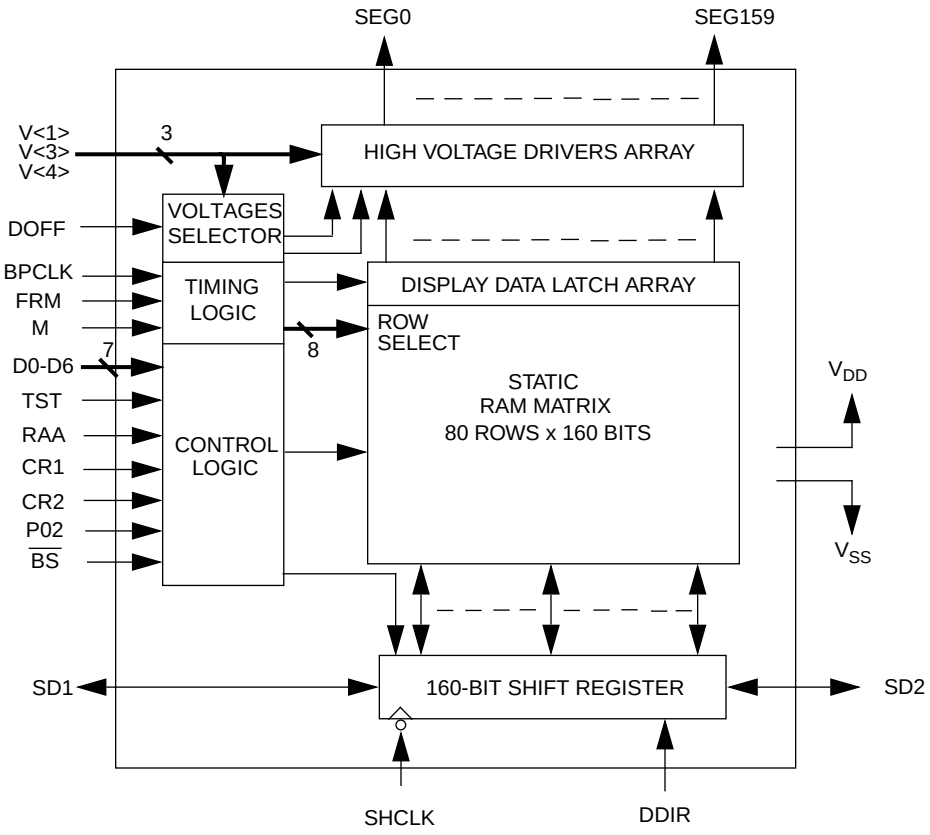


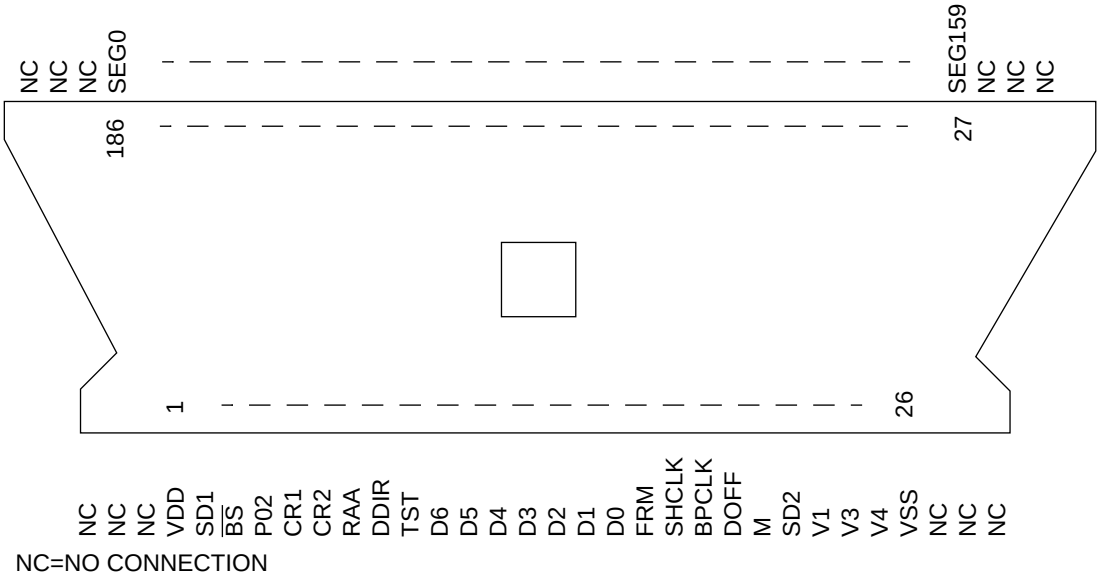
MC141519T
TAB

ORDERING INFORMATION

MC141519T	TAB

BLOCK DIAGRAM





TAB Package Pin Assignment (copper view)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A = 25˚C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
V<1>		V_{SS}-0.3 to V_{SS}+22.0	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to 80	˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

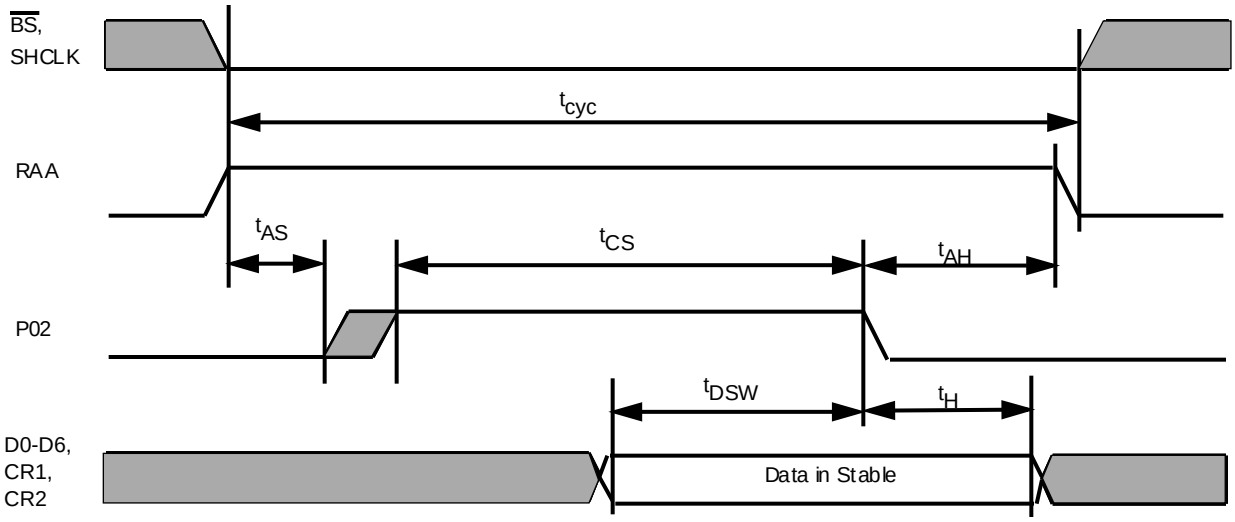
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25˚C, V_{DD} = 5.0V)

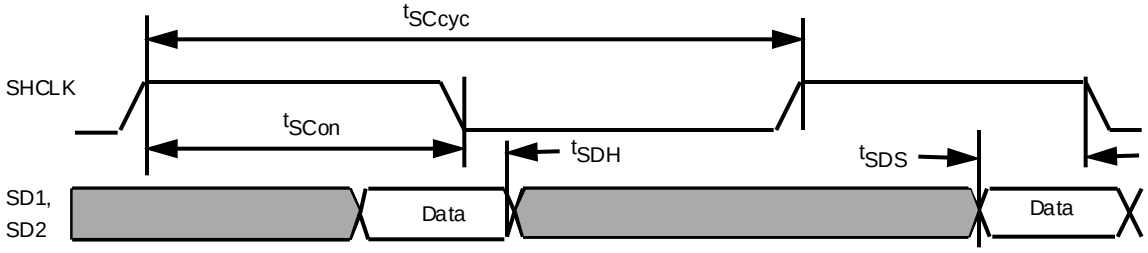
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input High Voltage BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	0.7xV_{DD}	-	V_{DD}	V
V_{IL}	Input Low Voltage BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	V_{SS}	-	0.3xV_{DD}	V
V_R	Data Retention	2.0	-	-	V
I_{in}	Input Current BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	-	-	1	uA
C_{in}	Capacitance BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	-	-	8	pF
V_{OH}	Output High Voltage SD1,SD2	0.8xV_{DD}	-	V_{DD}	V
V_{OL}	Output Low Voltage SD1,SD2	V_{SS}	-	0.2xV_{DD}	V
	Operating Voltages				
V_{DD}	Supply Voltage (referenced to V_{SS})	2.7	-	5.5	V
V<1>	LCD Voltage (referenced to V_{SS})	8.0	-	20.0	V
	Operating supply current (V_{DD})(V_{DD}=5V, referenced to V_{SS})				
I_{ACC}	Access Mode	-	150	200	uA
I_{DP}	Display Mode	-	30	100	uA
I_{SB}	Standby Mode	-	1	10	uA
	Operating supply current (V<1>)(V<1>=20V, referenced to V_{SS})				
I_{LDP}	Display Mode	-	12	20	uA
I_{LSB}	Standby Mode	-	1	10	uA

AC ELECTRICAL CHARACTERISTICS(V_{DD}=2.7V-5.5V, V_{SS}=0, T_A=25˚C)

Symbol	Parameter	Min	Max	Unit
t_{cyc}	Access Cycle Time	235	-	ns
t_{AS}	Access Set up Time	100	-	ns
t_{AH}	RAA Hold Time	0	-	ns
t_{CS}	Chip Select Pulse Width	135	-	ns
t_{DSW}	Data SetUp Time	100	-	ns
t_H	Input Hold Time	10	-	ns
t_{SCcyc}	Shift Clock Cycle Time	200	-	ns
t_{SCon}	Shift Clock On Time	100	-	ns
t_{SDS}	Serial Data Setup Time	50	-	ns
t_{SDH}	Serial Data Hold Time	10	-	ns



Parallel Access Timing



Serial Access Timing (with $\overline{BS}$ = 0)

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

Power is supplied to the driver using these two pins. V_{DD} is power and V_{SS} is ground.

V<1>, V<3>, V<4>

These are the levels of voltage generated from an external voltages divider (Fig. 2). These voltage provide different voltage levels for shaping up the display output waveforms Seg0 - Seg159.

DOFF

This is an output from MC68HC05L11 to signal the backplane driver to turn off LCD. If this pin is clear, the segment driver supplies LCD with driving signal. If this pin is set, the segment driver outputs is high-impedance and LCD display is disabled.

FRM

A periodic active high input to the segment driver for frame timing synchronization. This pin is connected to the signal FRM of MC68HC05L11. The frequency depends on the bias ratio and BPCLK signal.

BPCLK

A periodic clock output from MC68HC05L11 to the segment driver for timing synchronization. The signal controls the refresh timing of LCD display.

M

A periodic output from backplane driver. This pin is used for synchronization among display drivers.

D0 - D6

A seven-bit input-only data bus which is connected to the D0 - D6 of MC68HC05L11. These pins are used for address input and control input. Refer to Fig.1 for definition.

TST

The test pin should be pulled-low or connected to D7 of MC68HC05L11 during normal operation.

P02

A bus clock input that is used for data bus timing synchronization. This pin is connected to P02 of MC68HC05L11.

$\overline{BS}$

This is an active low input for chip select.

RAA

It is a strobe signal from MC68HC05L11 indicating that a valid segment control data is on D0 - D6 for a period of P02.

CR1, CR2

These two control signals from MC68HC05L11 to Segment driver describing the nature of the content in D0 - D6. The effect of CRs are shown on Fig 1.

SD1, SD2

These two pins are two bi-directional data lines connecting to the UD2 or LD2 and UD1 or LD1 respectively. These allow the display data from MC68HC05L11 entering the segment driver in both directions.

SHCLK

This is the shift clock from MC68HC05L11 to segment driver for clocking the serial data on SD1 and SD2. See Timing Diagram for illustration.

DDIR

It is an input pin carrying the signal from MC68HC05L11 to segment driver to control the direction of the serial data. In lower panel mode, if DDIR is set, the serial data enters the segment driver through SD1 and leaves the segment driver through SD2. If DDIR is clear, SD1 and SD2 are redefined as an output and input respectively.

SEG0 - SEG159

These 160 output lines provide the segment driving signal to the LCD panel. They are all in high-impedance state while the display is turned off (i.e. DOFF is set).

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

INTRODUCTION

The LCD segment driver can support multiplex ratio of a LCD system up to 80 and cascading of more than one driver for expansion is possible. It can be set from 1:5 bias (for 16 mux) to 1:10 bias (for 80 mux), by the voltage divider ratio of Fig.2. The ratio of bias or the contrast ratio (a) is defined as

$$1:\frac{4xR1+R2}{R1}=1:a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a=\sqrt{mux}+1$$

To set up a multiplex ratio, please refer to MC68HC05L11D/H Technical Data Section 10.

CONTROL LOGIC produces the control signals necessary for display RAM read / write and serial data latching. This Control Logic is directly supervised by the MCU through the Data Bus, i.e. D0 - D6, CR1 and CR2. MCU writing a byte of instruction to the Segment Control Register will cause Segment Driver(s) to fetch this instruction from the Data Bus and the command executed at the next P02 cycle. Fig.1 shows the functions of which the Control Logic will carry out in respond to MCU access through the Segment Control Register.

ROW ADDRESS(WRITE IN) instruction causes Segment driver(s) to load the content of the SHIFT REGISTER into a row of RAM which address is specified by D6 to D0.

ROW ADDRESS(READ FROM) instruction causes Segment driver(s) to copy a row of RAM which address is specified by D6 to D0 into the 160 BIT SHIFT REGISTER.

SCROLL UP ADVANCE instruction causes Segment driver(s) to do a vertical scroll up or down.

The content of D6 to D0 only represents the vertical offset of the new screen to the current screen. This vertical offset presenting in the Data Bus then is added up with an old offset which is stored in a register called the VERTICAL SCROLL VECTOR REGISTER to generate a new offset. This new offset will then be stored in the VERTICAL SCROLL VECTOR REGISTER. Periodically the content of this register will be fetched and loaded into a presettable counter in the TIMING LOGIC to generate the row addresses for screen refreshing.

RESET BIT0 Writing a “1” to this bit will set the VERTICAL SCROLL VECTOR REGISTER to zero.

UL BIT1 If this bit is set, the segment driver serves the upper panel in case of splitted panel. This will cause a swap in signals flow between SD1 and SD2.

CLRSH BIT2 Writing an “1” to this bit will clear the content of the 160-BIT SHIFT REGISTER.

TIMING LOGIC, according to M, BPCLK and FRM, fills the DISPLAY DATA LATCH ARRAY with rows of RAM matrix’s content periodically starting from the row address specified by the VERTICAL SCROLL VECTOR REGISTER.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from the external voltage divider. (See Fig. 2).

DISPLAY DATA LATCH ARRAY is used to buffer up a row of display data from RAM.

STATIC RAM MATRIX consists of 160x80 bits of SRAM cell. The content of these RAM cells can be altered by read/write from/to the shift register with the Segment Control Interface (refer to MC68HC05L11D/H Technical Data Section 10).

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Seg(x) in Fig 3.

SHIFT REGISTER is a 160-bit bi-directional register which acts as an input either from SD1 or SD2. The direction of data flow depends on the content of DDIR. And, it can be swapped by setting the UL bit to high. Data enter this shift register in serial. Shift register latches data at the falling edge of the signal SHCLK. See Timing Diagram for illustration.

CR2	CR1	D6	D5	D4	D3	D2	D1	D0
0	0	ROW ADDRESS (WRITE IN)						
0	1	ROW ADDRESS (READ FROM)						
1	0	SCROLL UP ADVANCE						
1	1	X	X	X	X	CLR SH	UL	RESET

FIGURE 1 - A Summary of the Control Functions of Segment Driver

DDIR	UL	SD1	SD2
1	0	input	output
0	0	output	input
1	1	output	input
0	1	input	output

FIGURE 1A - Relationship between DDIR, UL, SD1 and SD2

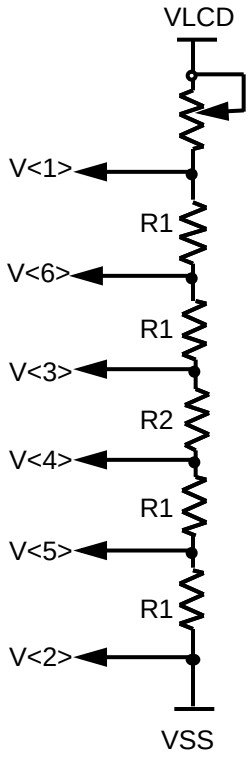


FIGURE 2 - External Voltage Divider

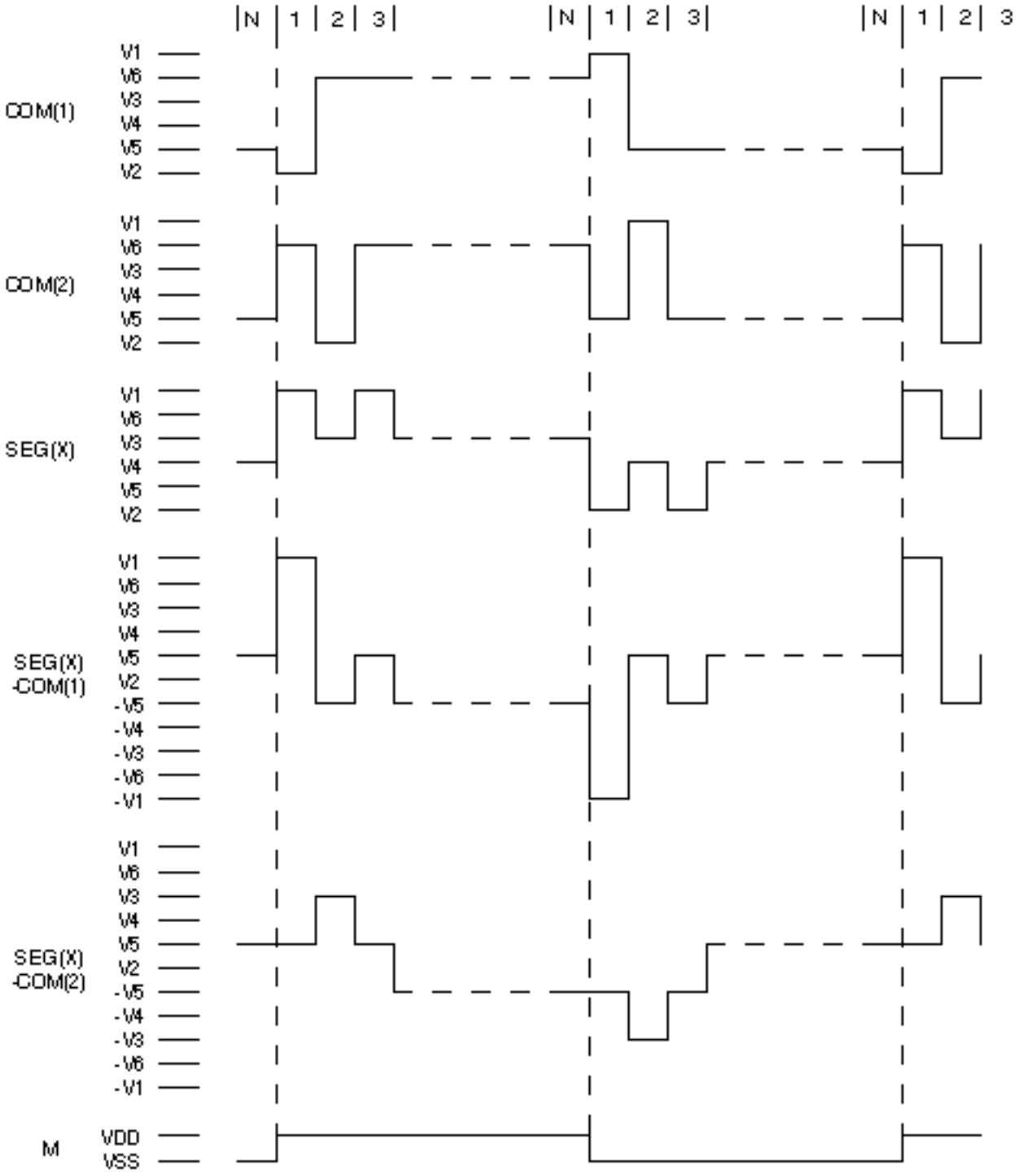
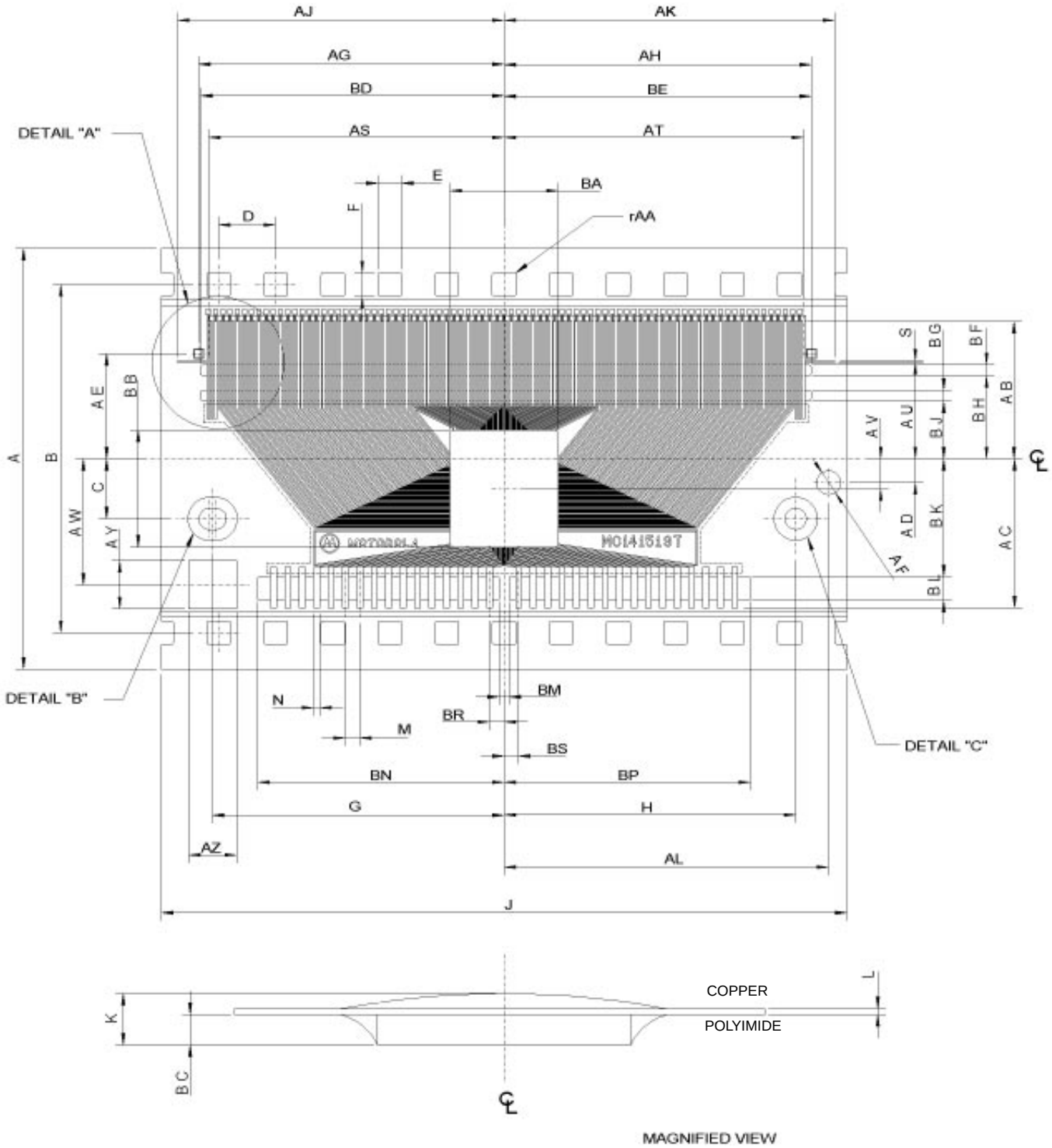


FIGURE 3 - Driving Waveforms of 1:N multiplex

(M is used for timing synchronization)

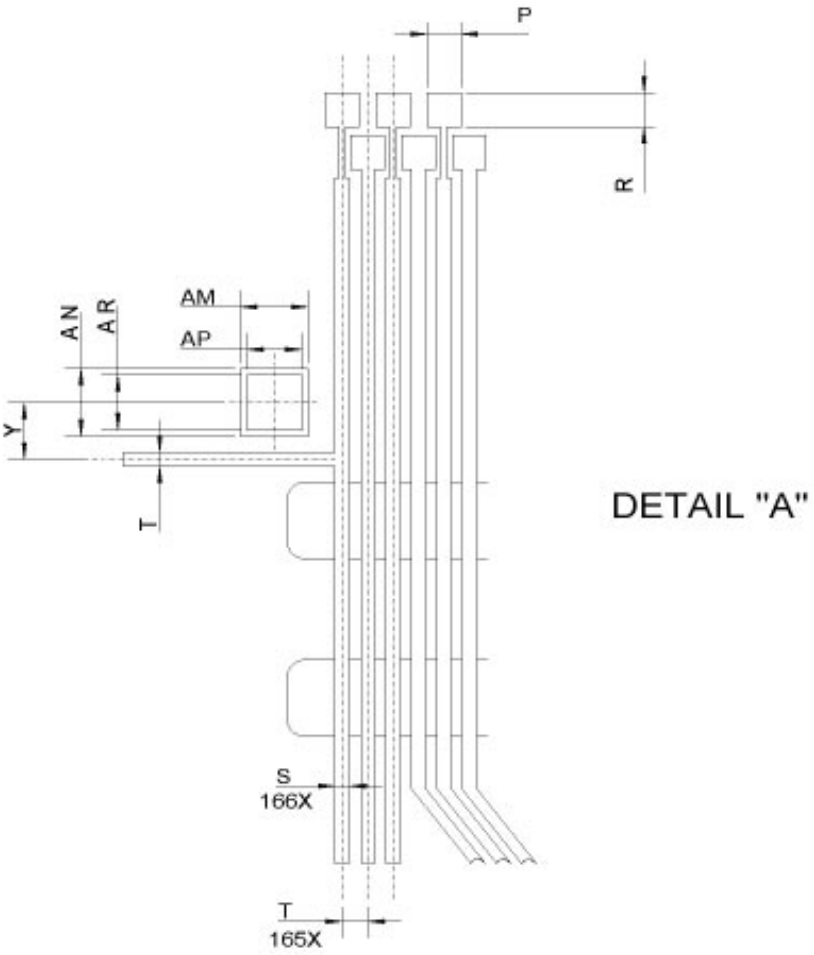
PACKAGE DIMENSIONS

MC141519T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)

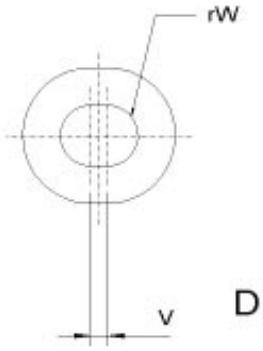


Reference: 98ASL00157A	Issue “0” released on 08/12/94

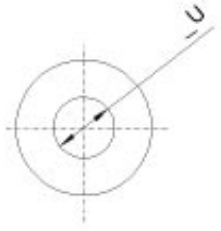
MC141519T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



DETAIL "A"



DETAIL "B"



DETAIL "C"

Reference: 98ASL00157A	Issue “0” released on 08/12/94

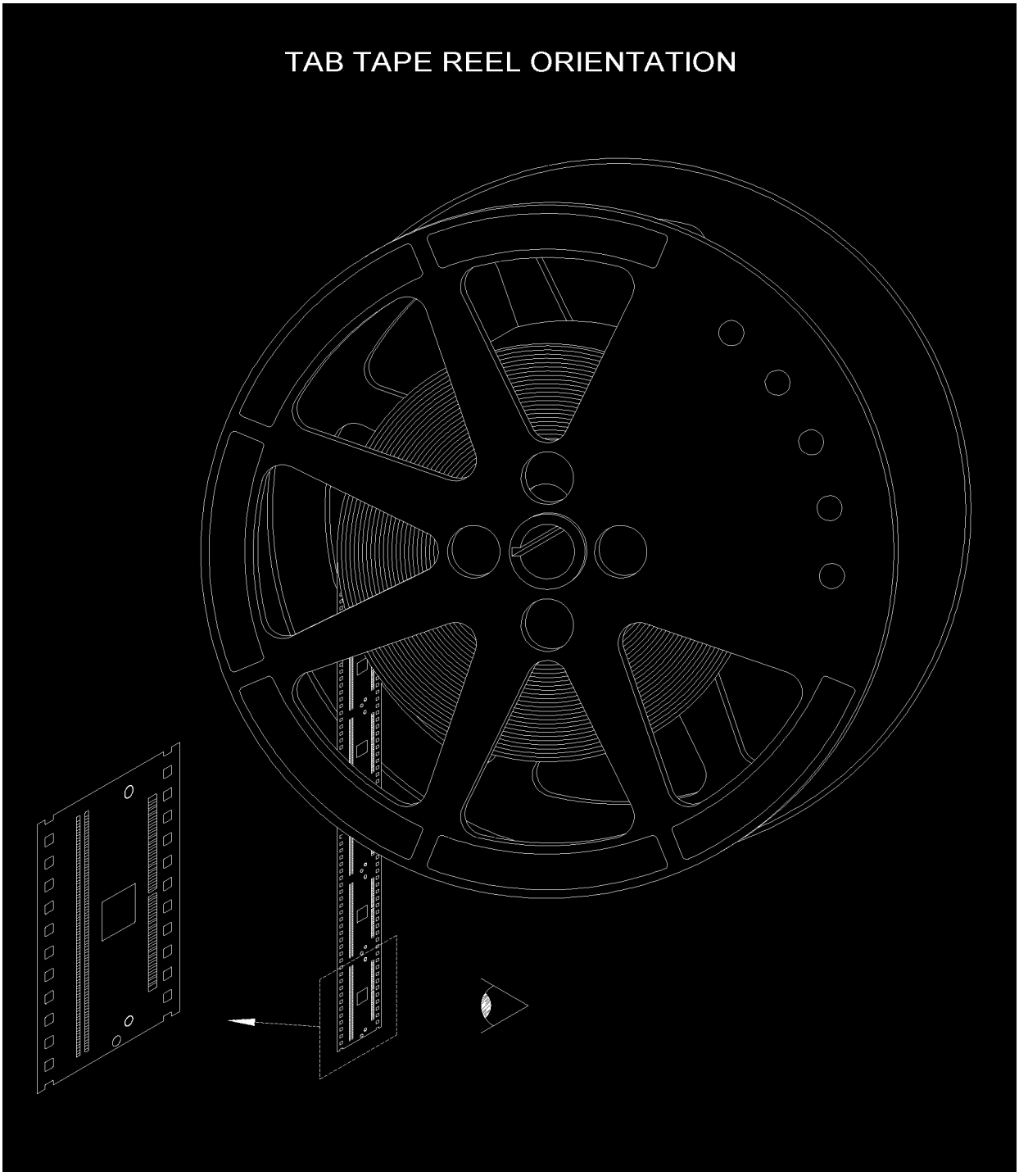
MC141519T TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	**Min**	**Max**	**Min**	**Max**	**Dim**	**Min**	**Max**	**Min**	**Max**
A	34.775	35.175	1.3691	1.3848	AK	27.430	27.530	1.0799	1.0839
B	28.927	29.027	1.1389	1.1428	AL	26.500	27.500	1.0433	1.0827
C	4.950	5.050	0.1949	0.1988	AM	0.750	0.850	0.0295	0.0335
D	4.720	4.780	0.1858	0.1882	AN	0.750	0.850	0.0295	0.0335
E	1.951	2.011	0.0768	0.0792	AP	0.600	0.700	0.0236	0.0276
F	1.951	2.011	0.0768	0.0792	AR	0.600	0.700	0.0236	0.0276
G	24.200	24.300	0.9528	0.9567	AS	24.551	24.649	0.9666	0.9704
H	24.200	24.300	0.9528	0.9567	AT	24.850	24.950	0.9784	0.9823
J	56.500	57.500	2.2244	2.2638	AU	7.937	8.037	0.3125	0.3164
K	0.686	0.838	0.0270	0.0330	AV	2.450	2.550	0.0965	0.1004
L	0.0675	0.0825	0.0027	0.0033	AW	10.000	11.000	0.3937	0.4331
M	1.190	1.210	0.0469	0.0476	AY	3.500	4.500	0.1378	0.1772
N	0.480	0.520	0.0189	0.0205	AZ	3.500	4.500	0.1378	0.1772
P	0.350	0.450	0.0138	0.0177	BA	-	8.996	-	0.3542
R	0.350	0.450	0.0138	0.0177	BB	-	9.750	-	0.3839
S	0.150	0.190	0.0059	0.0075	BC	0.5794	0.6294	0.0228	0.0248
T	0.290	0.310	0.0114	0.0122	BD	25.200	25.300	0.9921	0.9961
U	1.750	1.850	0.0689	0.0728	BE	25.500	25.600	1.0039	1.0079
V	0.450	0.550	0.0177	0.0217	BF	0.850	0.950	0.0335	0.0374
W	0.850	0.950	0.0335	0.0374	BG	0.850	0.950	0.0335	0.0374
Y	0.622	0.722	0.0245	0.0284	BH	6.850	6.950	0.2697	0.2736
AA	-	0.20	-	0.0079	BJ	4.750	4.850	0.1870	0.1909
AB	10.900	11.900	0.4291	0.4685	BK	9.750	9.850	0.3839	0.3878
AC	12.150	12.650	0.4783	0.4980	BL	1.950	2.050	0.0768	0.0807
AD	1.500	2.500	0.0591	0.0984	BM	0.750	0.850	0.0295	0.0335
AE	8.690	8.790	0.3421	0.3461	BN	20.450	20.550	0.8051	0.8091
AF	1.950	2.050	0.0768	0.0807	BP	20.450	20.550	0.8051	0.8091
AG	25.350	25.450	0.9980	1.0020	BR	1.150	1.250	0.0453	0.0492
AH	25.510	25.610	1.0043	1.0083	BS	1.150	1.250	0.0453	0.0492
AJ	27.130	27.230	1.0681	1.0720					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper thickness: 1oz.
4. Tin plating thickness: 0.4um.
5. 12 sprocket hole device.

Reference: 98ASL00157A Issue “0” released on 08/12/94

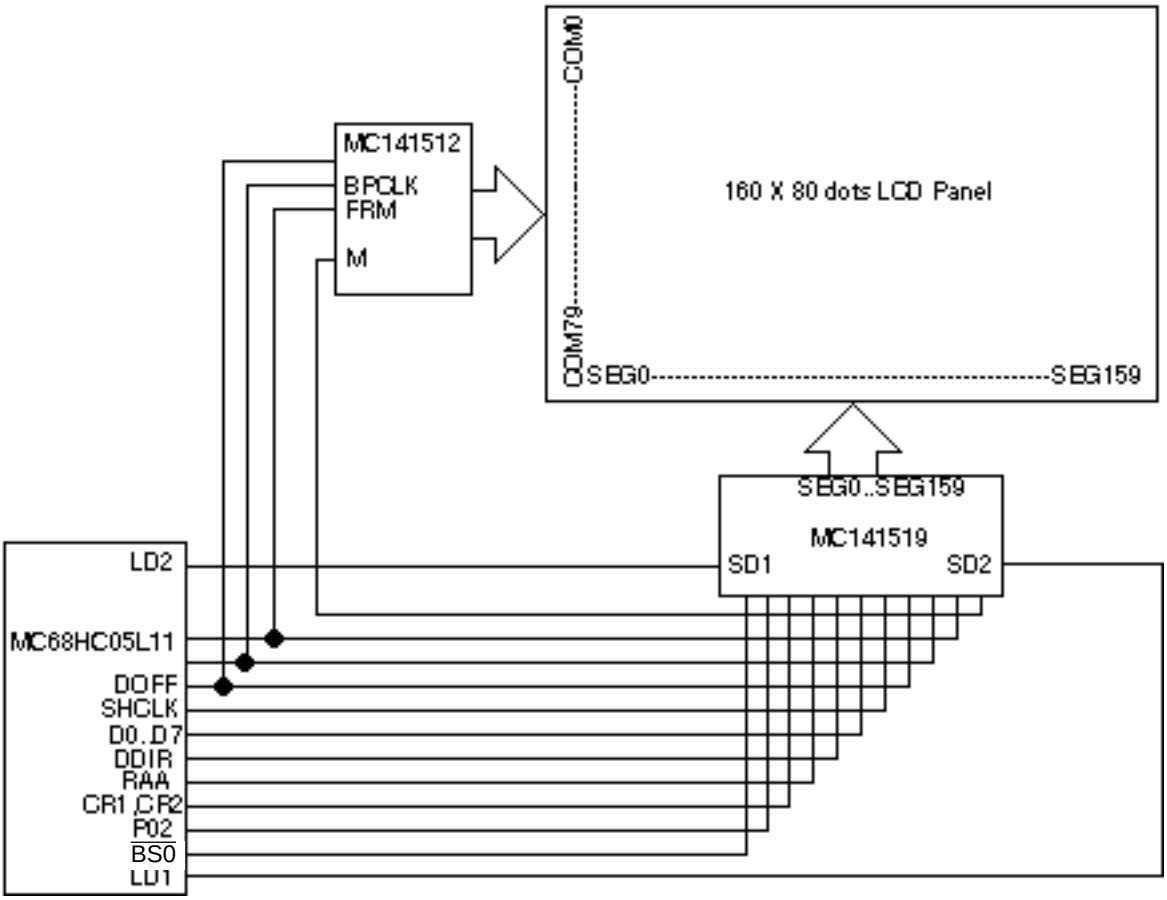
TAB TAPE REEL ORIENTATION



Reference: 98ASL00157A	Issue “0” released on 08/12/94

TYPICAL APPLICATIONS

160 x 80 SINGLE PANEL LCD SYSTEM WITH MC68HC05L11



320 x 160 SPLIT PANEL LCD SYSTEM WITH MC68HC05L11