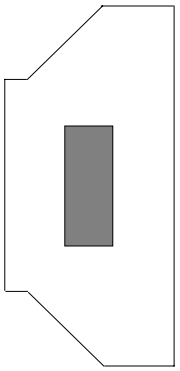
MC141535

LCD Segment / Common Driver with Controller
CMOS



ORDERING INFORMATION

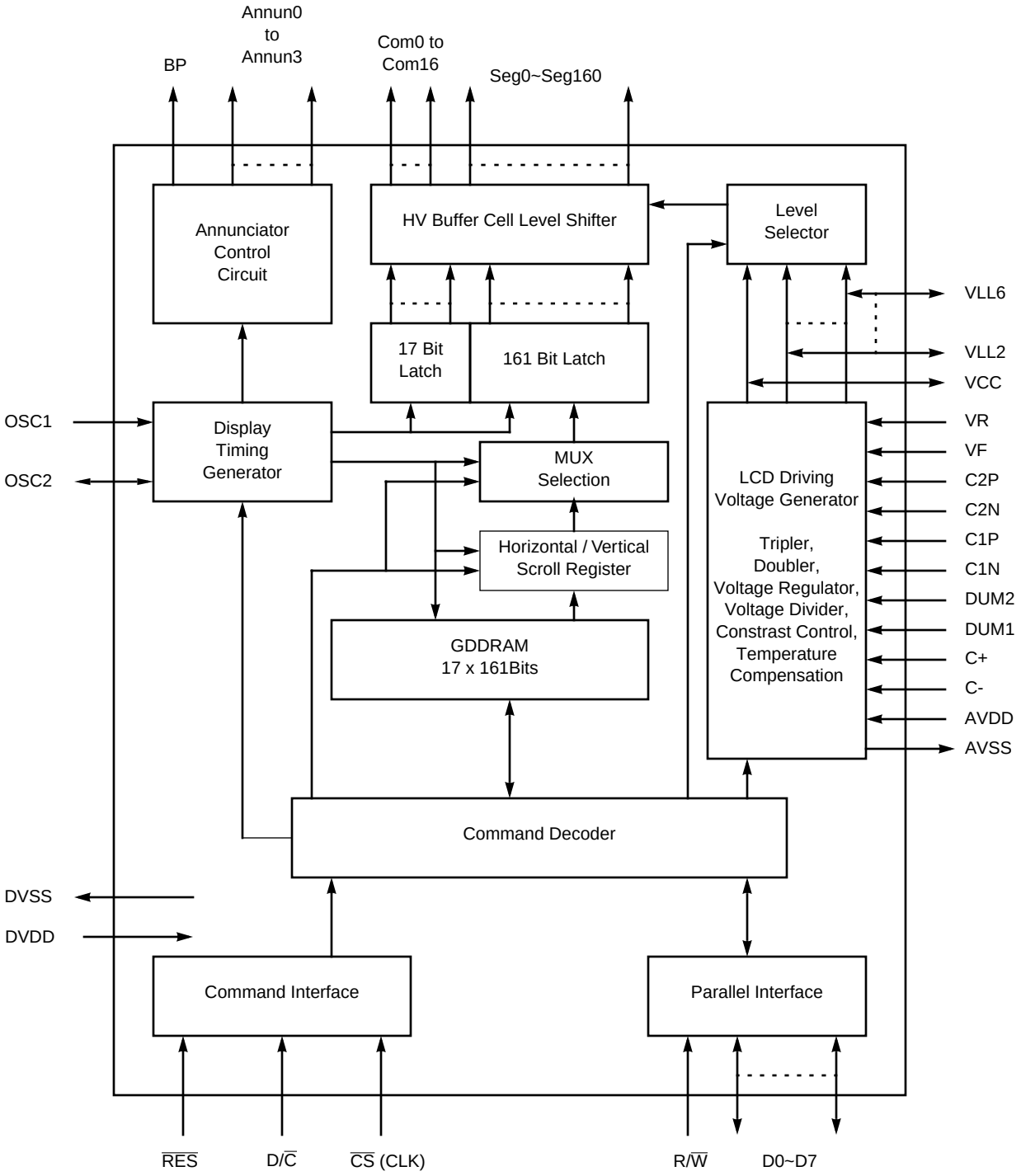
MC141535T	TAB
MCC141535Z	Gold Bump Die

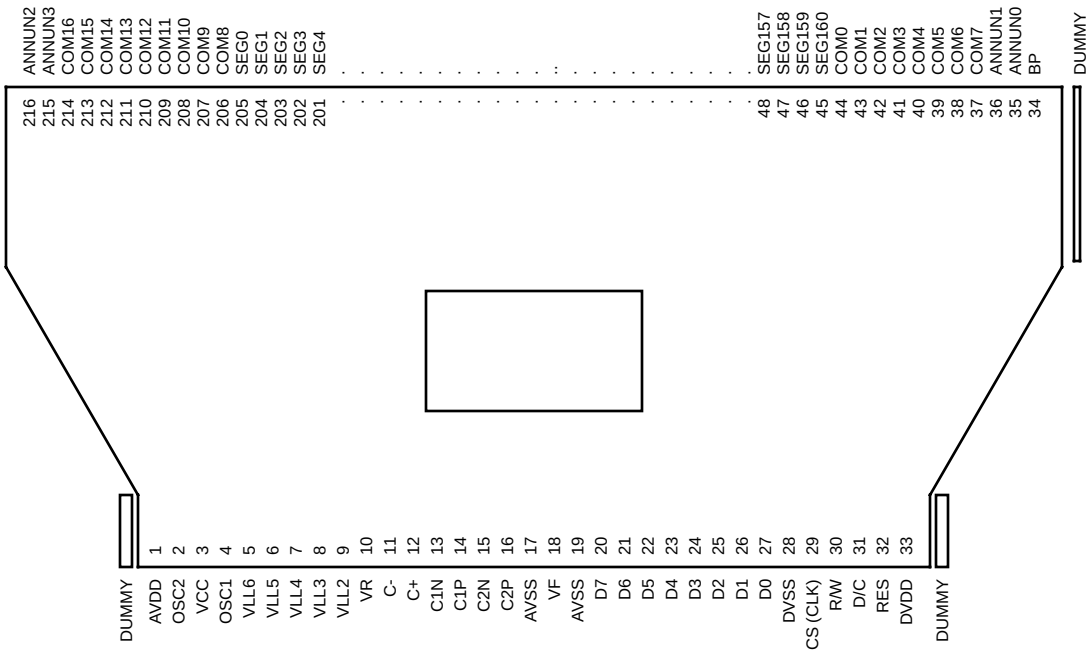
MC141535 is a CMOS LCD Driver which consists of 4 annunciator outputs and 178 high voltage LCD driving signals (17 rows and 161 segments). It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD bias voltage generator circuit so that limited external components are required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 Bit Parallel Interface
- Graphic Mode Operation
- On Chip Graphic Display Data RAM
- Four Static Annunciator (Icon) Drivers
- Low Power Icon Mode Driven by Com16 in Special Driving Scheme
- 161 Segment Drivers, 17 Row Drivers
- 1:5 Bias Ratio
- 1/17 Multiplex Ratio
- Master Clear RAM (Main Dot Matrix Display / Icons Display)
- Vertical and Horizontal Scrolling for Main Display
- Re-mapping of Row and Column Drivers
- Selectable LCD Driving Voltage Temperature Compensation
- 16 Level Internal Contrast Control
- External Contrast Control
- Standard TAB, Gold Bump Die

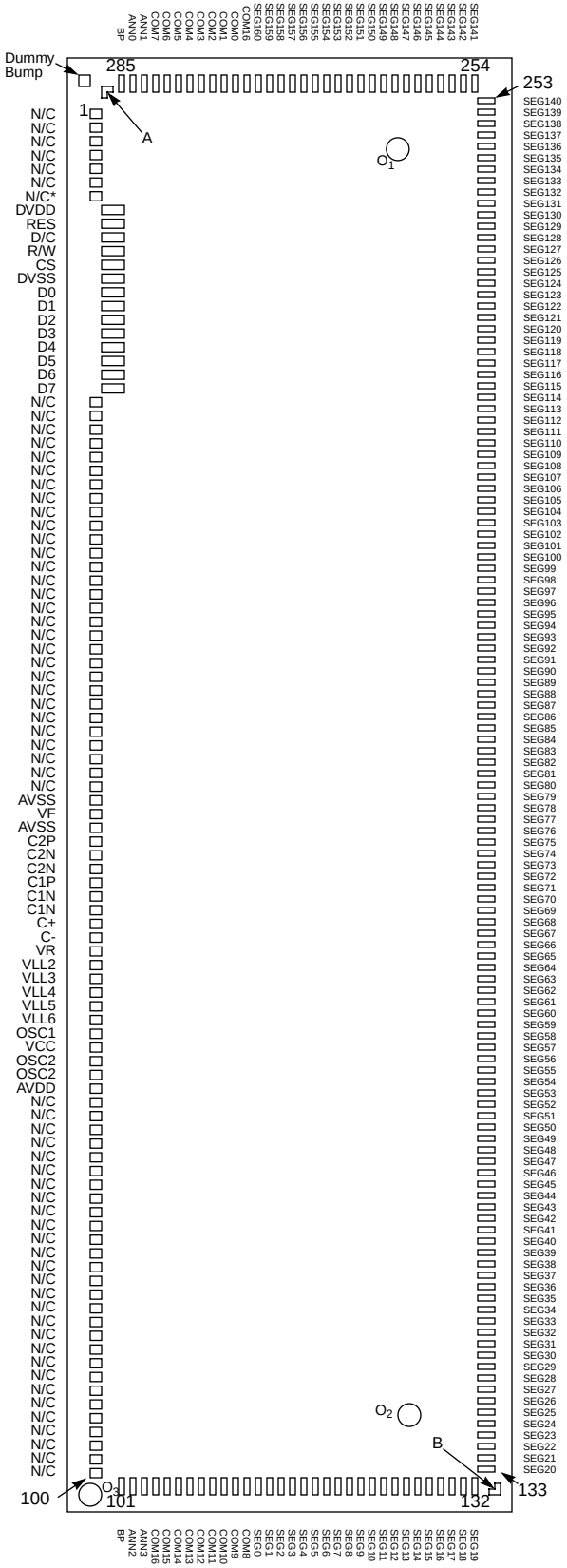
REV 5
2/98

Block Diagram





MC141535T PIN ASSIGNMENT
(COPPER VIEW)

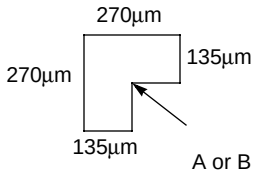


MC141535 Die Pad Assignment

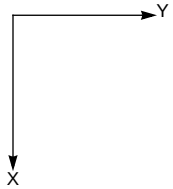
Alignment Mark Co-ordination

	X (µm)	Y(µm)
A	5156.	1267.3
B	5184	1359
O_1	-4483.3	556.1
O_2	4388.2	556.1
O_3	5165.8	-1349.4
D	-5267.9	-1311.8
d	444	

O_1, O_2 and O_3 are the centers of the circular alignment marks which diameter are d. D is the center of the square dummy bump with edges equal to 270µm



The “L” shape alignment mark



MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
	Operating Temperature		
T_{A1}	For Using Internal Oscillator	-25 to +85	˚C
T_{A2}	For Using External Oscillator	-30 to +85	˚C
T_{stg}	Storage Teperature Range	-65 to +150	˚C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
V_{SS} = AV_{SS} = DV_{SS} (DV_{SS} = V_{SS} of Digital circuit, AV_{SS} = V_{SS} of Analogue Circuit)
V_{DD} = AV_{DD} = DV_{DD} (DV_{DD} = V_{DD} of Digital circuit, AV_{DD} = V_{DD} of Analogue Circuit)

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Supply voltage (Absolute value Referenced to V_{SS})					
DV_{DD}	Operating Range of Logic Circuit Supply DV_{DD}		2.4	3.0	3.5	V
AV_{DD}	Operating Range of Voltage Generator Circuit Supply AV_{DD}		2.4	-	3.5	V
	Supply Current (Measure with V_{DD} fixed at 3.0V)					
I_{AC}	Access Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Accessing, T_{cyc}=1MHz, Osc. Freq. =38.4kHz, 1/17 Duty Cycle,1/7 Bias.	0	200	300	µA
I_{DP1}	Display Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Normal Display Mode, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz.	0	70	100	µA
I_{DP2}	Display Mode Supply Current Drain from Pin AVDD and DVDD	Internal DC/DC Converter On, Display On, Normal Display Mode, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz. Horizontal Scrolling	0	78	110	µA
I_{ICON}	Display Mode Supply Current Drain from Pin AVDD and DVDD	Internal DC/DC Converter On, Display On, Icon Display Mode, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz.	-	15	30	µA
I_{SB1}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD	Display Off, Oscillator Disabled, R/W Halt	0	300	500	nA
I_{SB2}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, External Oscillator and Frequency = 38.4kHz.	0	2.5	5	µA
I_{SB3}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 38.4kHz.	0	5	7	µA
	VLCD Voltage					
V_{CC1}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Tripler Enable, Osc. Freq. = 38.4kHz, Regulator Enabled, Divider Enabled	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Doubler Enable, Osc. Freq. = 38.4kHz, Regulator Enabled, Divider Enabled	-	2*AV_{DD}	10.5	V
V_{LCD}	LCD Driving Voltage input at pin V_{CC}.	Internal DC/DC Converter Disabled.	AV_{DD}	-	10.5	V
	Output Voltage					
V_{OH1}	Output High Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0	-	0.1*V_{DD}	V
V_{R1}	LCD Driving Voltage Source at Pin VR	Regulator Enabled	0	-	V_{CC}-0.5	V
V_{R2}	LCD Driving Voltage Source at Pin VR	Regulator Disabled	-	0	-	V
V_{R3}	Delta of VR Voltage Drop	Regulator Enabled, I_{out}=50µA	0	-	VCC	V
ΔV_R	Variation of V_R Input (V_{DD} is fixed)	Regulator Enabled	-	±1	±2.5	%

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Input Voltage					
V_{IH1}	Input High Voltage at Pins, $\overline{RES}$, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1 and OSC2.		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage at Pins, $\overline{RES}$, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1 and OSC2.		0	-	0.2*V_{DD}	V
	LCD Display Voltage. (LCD Driving Voltage Output from Pins VLL6, VLL5, VLL4, VLL3 and VLL2.)	Voltage Drivder Enabled, Regulator Enabled.				
V_{LL6}			-	V_R	-	V
V_{LL5}			-	0.8*V_R	-	V
V_{LL4}			-	0.6*V_R	-	V
V_{LL3}			-	0.4*V_R	-	V
V_{LL2}			-	0.2*V_R	-	V
V_{LL6}		External Voltage Generator, Voltage Divider Disable, Regulator Enabled.	1/2V_{CC}	-	V_{CC}	V
V_{LL5}			1/2V_{CC}	-	V_{CC}	V
V_{LL4}			1/2V_{CC}	-	V_{CC}	V
V_{LL3}			0	-	1/2V_{CC}	V
V_{LL2}			0	-	1/2V_{CC}	V
	Output Current					
I_{OH}	Output High Current Source from Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=VDD-0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain from Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Drain Source at pins D0-D7 and OSC2		-1	-	1	µA
I_{IL}/I_{IH}	Input Current at pins $\overline{RES}$, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$ OSC1 and OSC2.		-1	-	1	µA
Ron	On Resistance Channel Resistance between LCD Driving Signal Pins (SEG and COM) and Driving Voltage Input Pins (V_{LL2} to V_{LL6}).	During Display on, 0.1V Apply between Two Terminals, V_{CC} within Operating Voltage Range.	-	-	10	kΩ
V_{SB}	Memory Retention Voltage (DV_{DD}) Standby Mode, Retained All Internal Configuration and RAM Data		2	-	3.5	V
C_{IN}	Input Capacitance OSC1, OSC2 and All Logic Pins		-	5	7.5	pF

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, DV_{DD}=2.4-3.15V, T_A=25˚C)

	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled.	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled.	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled.	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled.	-	-0.35	-	%

* The formular for the temperature coefficient is:

$$TC(\%) = \frac{VR \text{ at } 50^\circ C - VR \text{ at } 0^\circ C}{50^\circ C - 0^\circ C} \times \frac{1}{VR \text{ at } 25^\circ C} \times 100\%$$

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, AV_{DD}=DV_{DD}=2.4 to 3.15V, T_A=25˚C)

Total variation of VR ΔV_{RT} is affected by ther following factors :

Process varition of Regulator ΔV_R

External V_{DD} Variation contributed to Regulator ΔV_{VDD}

External resistor pair Ra/Rf contributed to Regulator ΔV_{res}

where $\Delta V_{RT} = \sqrt{(\Delta V_R)^2 + (\Delta V_{V_{DD}})^2 + (\Delta V_{res})^2}$

Assume external V_{DD} varition is +/-6% at 3.15V and 1% varition resistor used at application.

	TC Level	ΔV_{VDD} (%)	ΔV_R (%)	ΔV_{res} (%)	ΔV_{RT} (%)
Reference Generator	TC0	±6.0	±2.5	±1.414	±6.652
	TC1	±4.0			±4.924
	TC2	±2.5			±3.805
	TC3	±1.4			±3.195

AC ELECTRICAL CHARACTERISTICS (T_A=25˚C, Voltage referenced to V_{SS}, V_{DD}=2.4 to 3.15V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Oscillation Frequency.	Normal Display Frequency Selected				
F_{OSC1}	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	38.4	-	kHz
F_{ANN1}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP		-	18.75	-	Hz
F_{FRM1}	LCD Driving Signal Frame Freqency.	Graphic or Icon Display Mode.	-	60	-	Hz
	Oscillation Frequency.	Slow Display Frequency Selected				
F_{ANN2}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP With Low Display Frequency Enabled		-	9.375	-	Hz
F_{FRM2}	LCD driving Signal Frame Freqency. (Graphic or Icon Display Mode With Low Display Frequency Enabled.)		-	30	-	Hz
OSC	Internal Oscillation Frequency Internal OSC Oscillation Frequency with Different Value of Feedback Resistor. (Internal Oscillator Enabled. V_{DD} within Operation Range.)		See Figure 1 for the relationship			

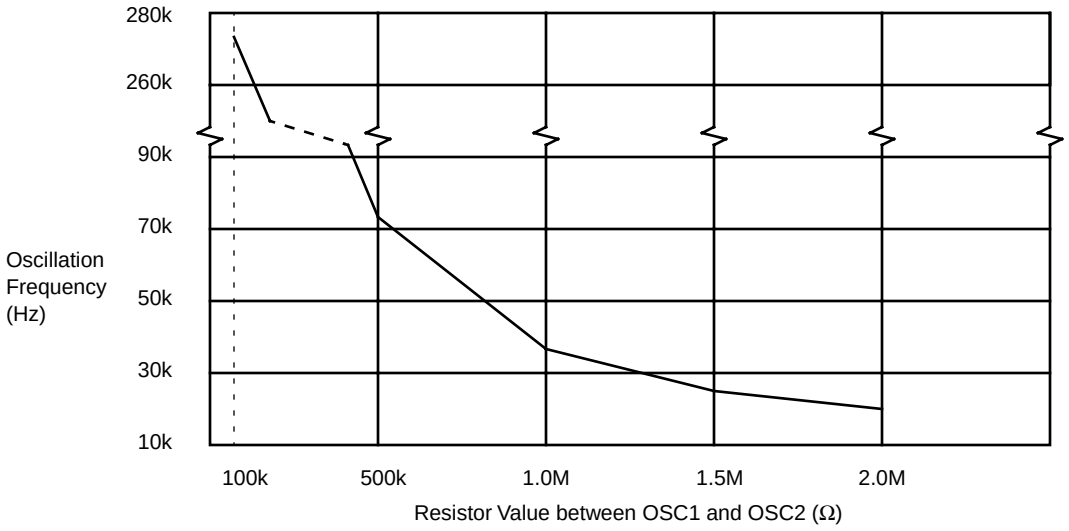


Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value

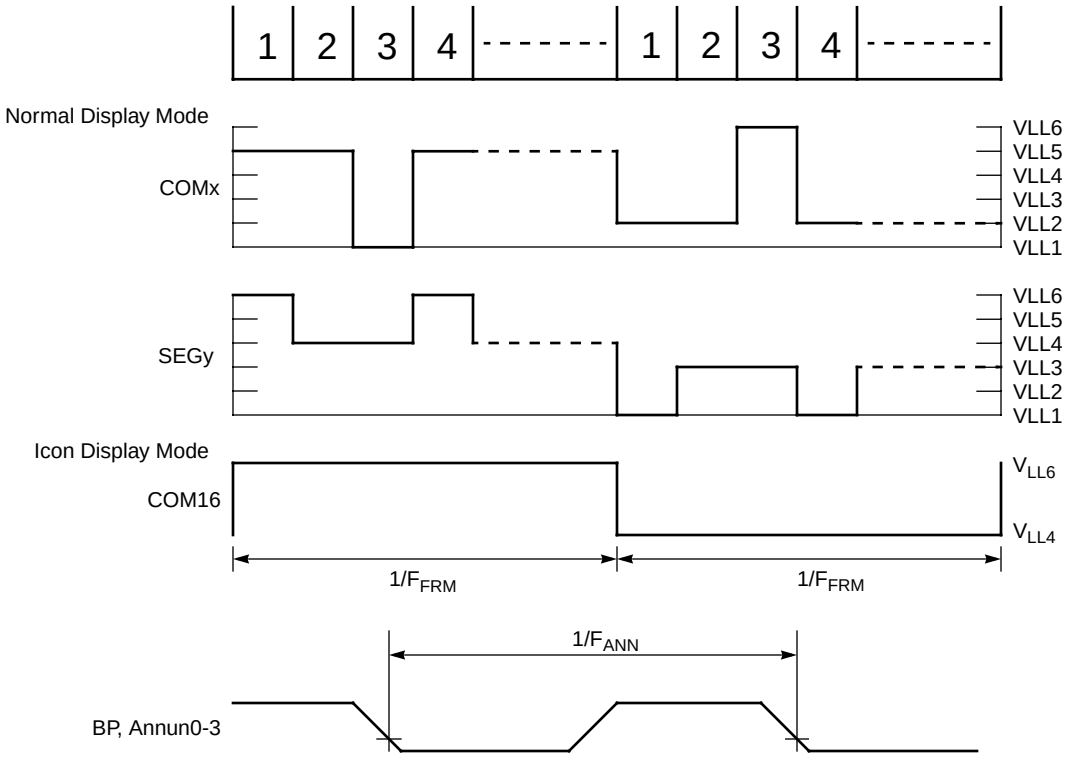
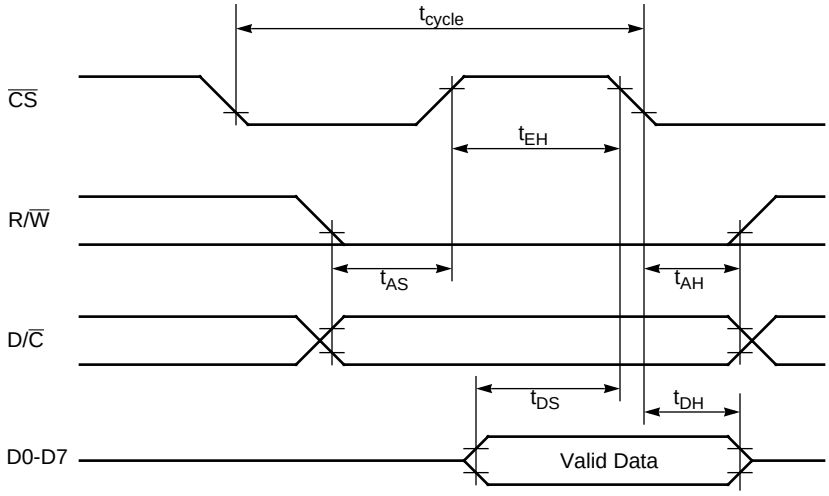


Figure 2. LCD Driving Signal Timing Diagram

TABLE 2a. Parallel Timing Characteristics (Write Cycle) (T_A=-10 to 60˚C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DS}	Data Setup Time	290	-	-	ns
t_{DH}	Data Hold Time	0	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns



Figre 3. Timing Characteristics (Write Cycle)

TABLE 2b. Parallel Timing Characteristics (Read Cycle) (T_A=-10 to 60˚C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	375	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DD}	Data Setup Time	-	-	350	ns
t_{DH}	Data Hold Time	7	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns

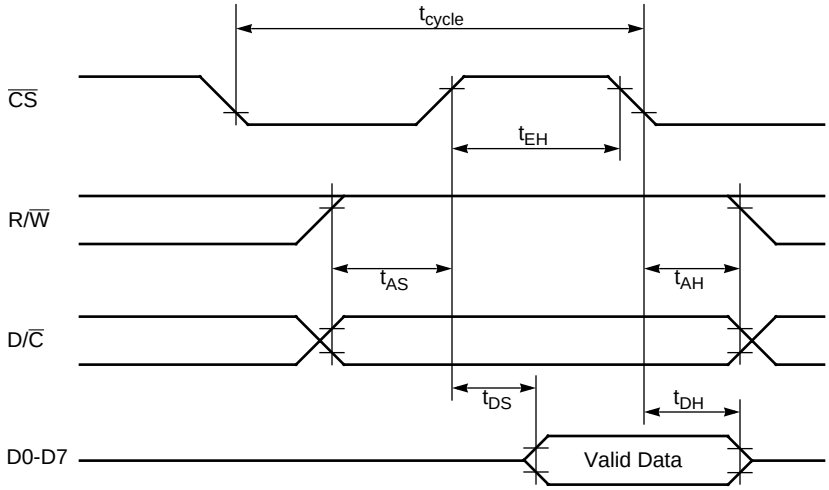


Figure 4. Timing Charecteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)

This input pin tell the LCD driver the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Chip Select / Input Clock)

This pin is normal Low clock input. Data on D0-D7 is latched at the falling edge of $\overline{CS}$.

$\overline{RES}$ (Reset)

An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 μs.

D0-D7 (Data)

This bi-directional bus is used for data / command transfering.

R/$\overline{W}$ (Read / Write)

This is an input pin. To read the display data RAM or the internal status (Busy / Idel), pull this pin High. The R/$\overline{W}$ input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)

For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value should be connected between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Osscillator Input)

For internal oscillator mode, this is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2

Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit if internal divider is enable. For Internal DC/DC Converter enabled, a capacitor to AV_{SS} is required on each pin.

C1N and C1P

If Internal DC/DC Converter is enabled, a capacitor is required to connect these two pins.

C2N and C2P

If Internal DC/DC Converter and Tripler are enabled, a capacitor is required between these two pins. Otherwise, leave these pins open.

C+ and C-

If internal drivider circuit is enabled, a capacitor is required to connect between these two pins.

VR and VF

This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 μF capacitor placed between VR and AVSS. (Refer to the Application Circuit)

COM0-COM16 (Row Drivers)

These pins provide the row driving signal to LCD panel. Com0-Com15 are used in 16 mux display. Com16 is used to drive the non-static icons. Output is low during display off.

SEG0-SEG160 (Column Drivers)

These 161 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)

This pin combines with Annun0-Annun3 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of F_{ANNn} Hz. It outputs low when oscillator is disabled.

Annun0 - Annun3 (Annunciator Frontplanes)

These pins are four independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a F_{ANNn} Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When all annunciators are disabled, all these pins output 0V.

AVDD and AVSS

AVDD is the positive supply to LCD bias voltage generator. AVSS is ground.

VCC

For using the Internal DC/DC Converter, a 0.1 μF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS

Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C high, data is written to Graphic Display Data RAM (GDDRAM). D/C low indicates that the input at D0-D7 is interpreted as a Command.

Reset is of same function as Power ON Reset (POR). Once RES received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7), R/W, and the CS. The R/W input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/W input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The CS input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (161x17 = 2737 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

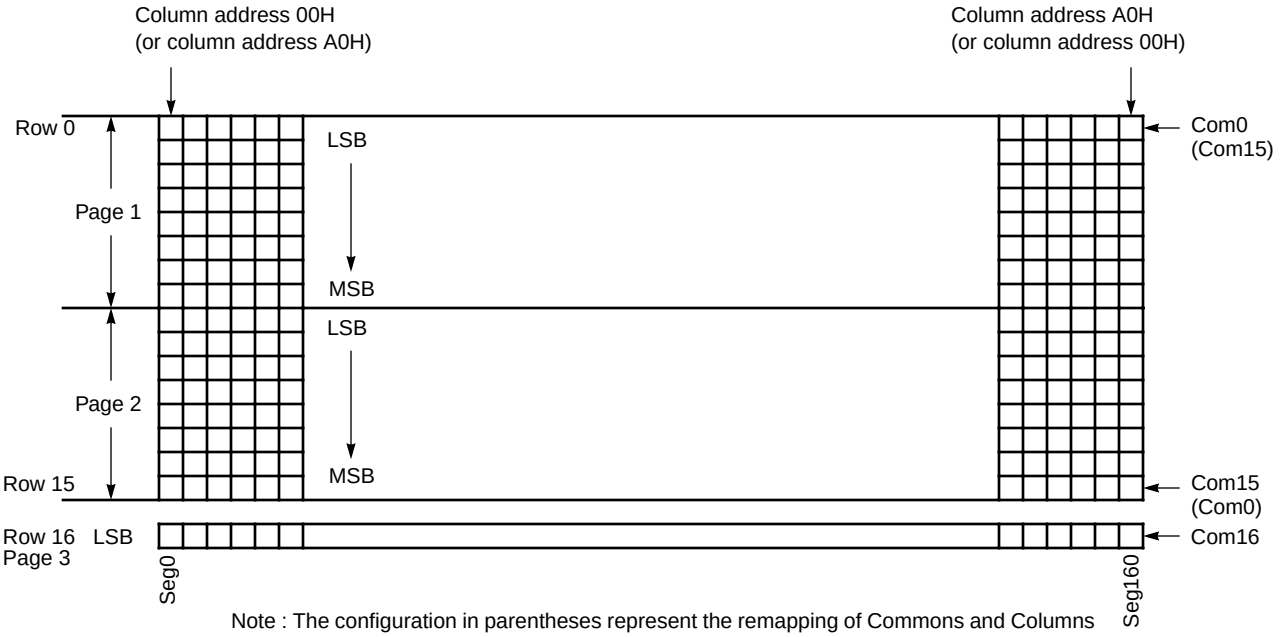


Figure 5. Graphic Display Data RAM (GDDRAM) Address Map

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 15kHz to 50kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 4 annunciators and BP are generated by this module. The 4 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit. Before turning the annunciators on, the oscillator must be on in advance. Annunciator output waveform shown in Figure 7.

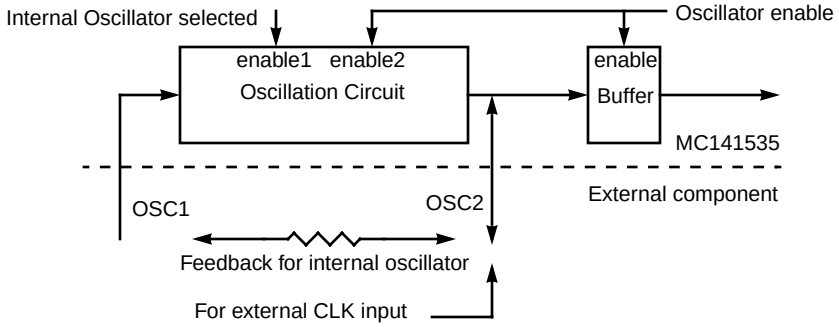


Figure 6. Oscillator Circuitry

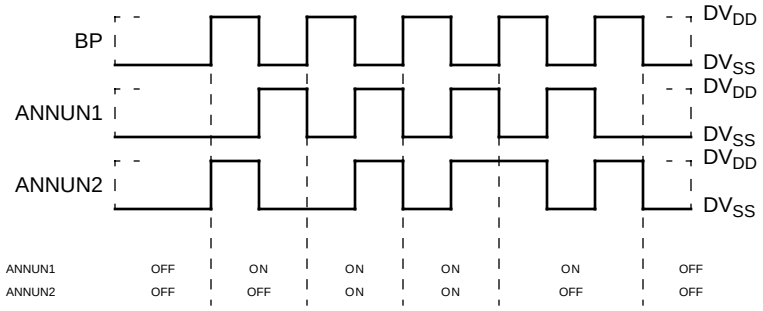


Figure 7. Annunciators and BP Display Waveform

LCD Driving Voltage Generator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Either Doubler or Tripler can be enabled.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. it can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.

All blocks can be individually turned off if external voltage generator is employed.

Voltage Regulator

1. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
2. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.

17 Bit Latch / 161 Bit Latch

A 178 bit long register which carrys the display signal information. First 32 bits are Common driving signals and other 161 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shift-er which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Horizontal Shifter

This Horizontal Shifter shift the 16 rows of GDDRAM data horizontally according to the value in the Horizontal Scroll register (which is programmable through sending two commands consecutively). Such Horizontal Shifter's output will go to the 161 Bit Latch for display.

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 8a, 8b and 8c illustrate the desired multiplex scheme.

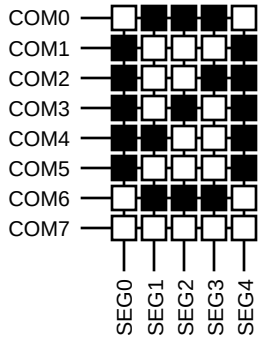


Figure 8a. LCD Display Example “0”

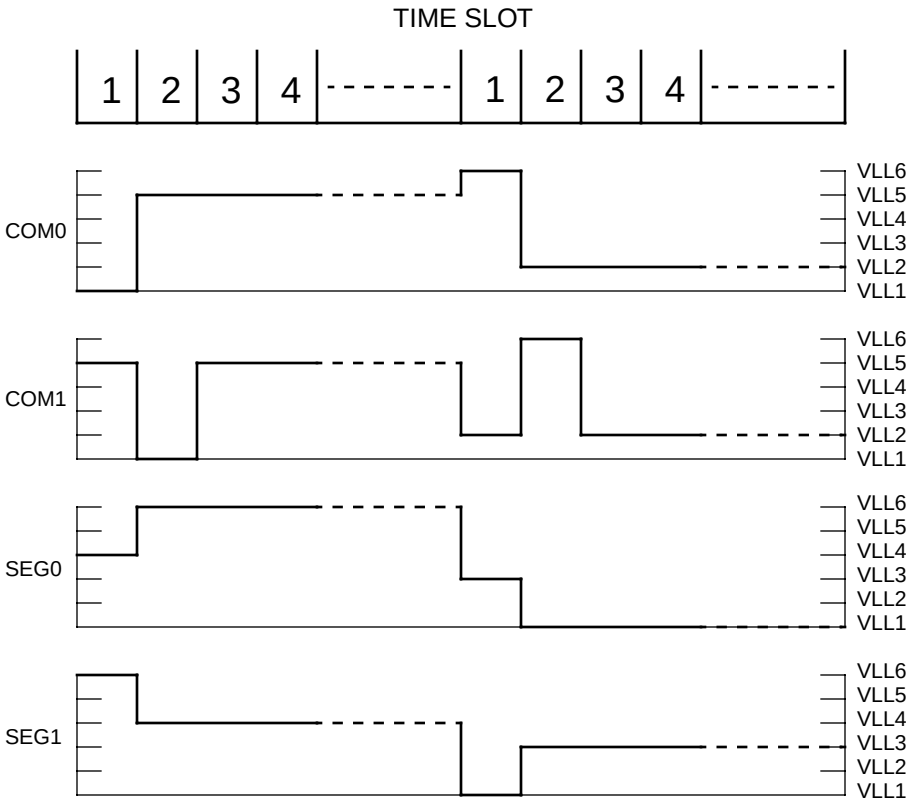


Figure 8b. LCD Driving Signal from MC141535

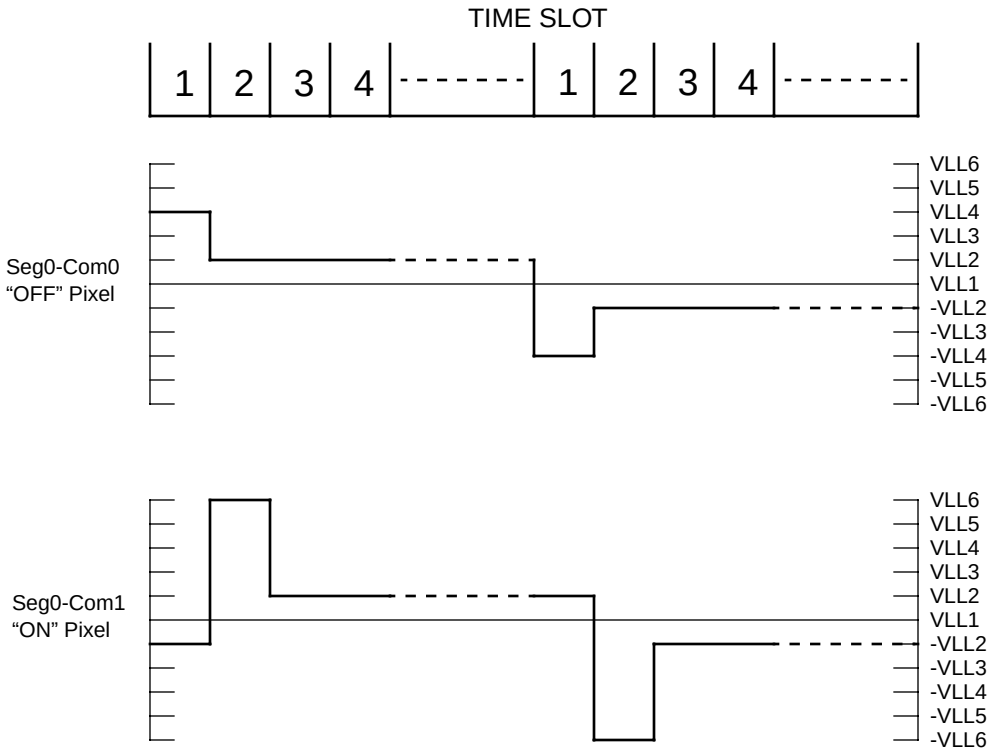


Figure 8c. Effective LCD waveform on LCD pixel

Command Description

Set Display On/Off (Display Mode / Stand-by Mode)

This Displat On command turns the LCD Common and Segment outputs on and has no effect to the annunciator output. This command starts the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note : "Oscillator On" command should be sent before "Display On" is selected)

The Display Off command turns the display off and the states of the LCD driver are as follow during display off :

1. The Common and Segment outputs are fixed at V_{LL1} (V_{SS}).
2. The bias Voltage Generator is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The status of the Annunciators and Oscillator are not affected by this command. The Oscillator is not affected by this command either.

Set Horizontal Scroll

This command is used in combination with “Set Horizontal Scroll Value” to set the LCD driver to scroll the display horizontally. The next input from D0 to D7 is the scroll value. Note that Row16 is not affected by this command.

Set Horizontal Scroll Value

When display is turned on, this command maps the selected GDDRAM column (00H-A0H) to Seg0-Seg160. With scroll value equals to 0, Col 0 of GDDRAM is mapped to Seg0 and Col 1 through Col 160 are mapped to Seg 1 through Seg160 respectively. With Scroll value equals to 1, Col 1 of GDDRAM is mapped to Seg 0, then Col 2 through Col 160 will be mapped to Seg 1 through Seg 159 respectively and Col 0 will be mapped to Seg 160. This command must issue follow command "Set Horizontal Scroll".

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-A0H (161 columns) in combination with the command “Set MSB of GDDRAM Column Address“. The column address will be increased automatically after a read or write operation. Refer “Address Incement Table” and command “Set GDDRAM Page Address” for further information.

Set MSB of GDDRAM Column Address

This command set the MSB of the GDDRAM Column address pointer. Set this MSB to 0 for accessing the 00H-7FH address; while set this MSB to 1 for accessing 80H-A0H address

Set GDDRAM Page Address

This command positions the row address to 1 of 3 possible positions in GDDRAM. Refer to figure 5.

Master Clear GDDRAM

This command is to clear the content of page 1 and 2 of the Display Data RAM. Issue this command followed by a dummy write command.

Master Clear Icons

This command is used to clear the data in page 3 of GDDRAM which storing the icon line data. Before using this command, set the page address to page 3 by the command “Set GDDRAM Page Address”. A dummy write data operation is also needed after this “Master Clear Icons” command to make the clear icon action effective.

Set Display Mode

This command switch the driver to full display mode or icon display mode. In low power icon mode, only icons (driven by COM16) and annunciators are displayed.

Set Vertical Scroll Value

This command maps the selected GDDRAM row (00H-0FH) to Com0. With scroll value equals to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 15 are mapped to Com1 through Com15 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 15 will be mapped to Com1 through Com14 respectively and Row 0 will be mapped to Com15.

Save / Restore Column Address

With bit option = 1 in this command, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With a bit option = 0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 160 of GDDRAM mapped to Seg0-Seg160 respectively;
2. Column 0 - Column 160 of GDDRAM mapped to Seg160-Seg0 respectively.

Detail information please refer to section “Display Output Description”.

Set Row Mapping

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row 15 of GDDRAM to Com0 - Com15 respectively;
2. Row 0 - Row 15 of GDDRAM to Com15 - Com0 respectively.

Output of Row 16 (Com16) will not be changed by this command. See section “Display Output Description” for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 4 stand alone annunciator drivers.

Set Oscillator Enable / Disable

This command is used to either turn on or off the oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command “Set Display On/Off” and “Set Annunciator Control Signals”. See command “Set External / Internal Oscillator” for more information

Set External / Internal Oscillator

This command is used to select either internal or external oscillator. When Internal Oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Set Internal DC/DC Converter On/Off

Use this command selects the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Turn off the Internal DC/DC Converter if external Vcc is provided.

Set Voltage Doubler / Tripler

Use this command to select Doubler or Tripler when the Internal DC/DC Converter is on.

Set Internal Regulator On/Off

Choose bit option 0 to disable the Internal Regulator. Choose bit

option 1 to enables the Internal Regulator which consists of the internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltge Divider is disabled, external bias can be used for V_{LL6} to $V_{LL2.}$ If the Interna Voltagel Divider is enabled, the internal circuit will generated the 1:5 bias driving voltage.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The constrast level starts from the lowest value after POR.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use. After power-on reset, the contrast level is the lowest.

Read Contrast Value

This command allows the user to read the current contrast level value. With R/$\overline{W}$ input high (READ), D/$\overline{C}$ input low (COMMAND) and D7 D6 D5 D4 are equal to 0 0 0 1, the value of the internal contrast value can be read on D0-D3 at the falling edge of CS.

Set Temperature Coefficient

A temperature gradient selector circuit controlled by two control bits TC1 and TC2. This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

Set Display Frequency

This commnad set the LCD panel display to normal frequency or slow frequency.

COMMAND TABLE

Bit Pattern	Command	Comment
$000000X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using X_1X_0 as address bits. X_1X_0=00 : page 1 (POR) X_1X_0=01 : page 2 X_1X_0=10 : page 3
$0001X_3X_2X_1X_0$	Set / Read Contrast Level	With R/$\overline{W}$ pin input low, set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR. With R/$\overline{W}$ pin input high, and at the rising edge of $\overline{CS}$, the value of the internal contrast register will be latched out at D3 D2 D1 D0 pins, i.e. $X_3X_2X_1X_0$, at the rising edge of $\overline{CS}$.
$0010000X_0$	Set Voltage Doubler / Tripler	X_0=0: Tripler enable (POR) X_0=1: Doubler enable
$0010001X_0$	Set Column Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg119
$0010010X_0$	Set Row Mapping	X_0=0 : Row0 to Com0 X_0=1: Row0 to Com15
$0010011X_0$	Set MSB of GDDRAM Column Address	X_0=0 : MSB = 0 (POR) X_0=1 : MSB = 1
$0010100X_0$	Set Display On/Off	X_0=0: display off (POR) X_0=1: display on
$0010101X_0$	Set Internal DC/DC Converter On/Off	X_0=0: Internal DC/DC Converter off(POR) X_0=1: Internal DC/DC Converter on
$0010110X_0$	Set Internal Regulator Enable	X_0=0: Internal Regulator off (POR) X_0=1: Internal Regulator on When application uses a supply with built-in temperature compensation, the regulator should be disabled .
$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: Internal Voltage Divider off(POR) X_0=1: Internal Voltage Divider on When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0: Internal Constrast Control off(POR) X_0=1: Internal Constrast Control on Internal contrast circuits can be disabled if external contrast circuits is preferred.

COMMAND TABLE

Bit Pattern	Command	Comment
$0011001X_0$	Set Display Mode	X_0=0 : normal display mode (POR) X_0=1 : icon display mode
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
00110110	Master Clear GDDRAM	Master clear page 1 and 2 of GDDRAM, dummy write is required after this command.
00110111	Master Clear Icons	Master Clear of GDDRAM page 3. GDDRAM page 3 should be selected and dummy write is required
$0011100X_0$	Set Display Frequency	X_0=0: normal display frequency X_0=1: slow display mode
$0011101X_0$	Reserved.	X_0=0: normal operation (POR) X_0=1: test mode (Note: Make sure to set X_0=0 during application)
$0100X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_3X_2X_1X_0$ as number of lines to scroll. Scroll value = 0 upon POR
$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00: select annunciator 1 (POR) A_1A_0=01: select annunciator 2 A_1A_0=10: select annunciator 3 A_1A_0=11: select annunciator 4 X_0=0: turn selected annunciator off (POR) X_0=1: turn selected annunciator on
01101000	Set Horizontal Scrolling	Set horizontal scrolling mode. The next input from D0~D7 will be interpreted as the horizontal shift value.
$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=00: 0.00% (POR) X_1X_0=01: -0.18% X_1X_0=10: -0.22% X_1X_0=11: -0.35%
$0111000X_0$	Increase / Decrease Contrast Value	X_0=0: Decrease by one level X_0=1: Increase by one level (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.
$0111001X_0$	Reserved	
$0111010X_0$	Reserved	
$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Make sure to set X_0=0 during application)
$0111100X_0$	Reserved	
$0111101X_0$	Set External / Internal Oscillator	X_0=0: External oscillator (POR) X_0=1: Internal oscillator. For internal oscillator place a resistor between OSC1 and OSC2. For external oscillator mode, feed clock input to OSC2.
$0111110X_0$	Reserved	
$0111111X_0$	Set Oscillator Enable / Disable	X_0=0: oscillator master disable (POR) X_0=1: oscillator master enable. This is the master control fro oscillator circuitry. This command should be issued after the “External / Internal Oscillator” command.
$1X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits.
$X_7X_6X_5X_4X_3X_2X_1X_0$	Set Horizontal Scroll Value	To set the amount of Horizontal scroll

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$ pin and D/$\overline{C}$ pin. Data is valid at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increasd by one automatically.

To write data to the GDDRAM, input Low to R/$\overline{W}$ pin and High to D/$\overline{C}$ pin. Data is latched at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increasd by one automatically.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the “Commands Required for R/W Actions on RAM” Table)

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Command	No	*1
1	0	Write Data	Yes	*2
1	1	Read Data	Yes	

Address Increment is done automatically data read write. The column address pointer of GDDRAM[*3] is affected.

Remarks : *1. Refer to the command “Read Contrast Vaule”.

*2. If write data is issued after Command Clear RAM, Address increse is not applied.

*3. Column Address will be wrapped round when overflow.

Commmands Required for Display Mode Setup

Display Mode	Commands Required	
Normal Display Mode	Set External / Internal Oscillator Set Oscillator Enable, Set Display Mode (Normal Display) Set Display On.	(0111101X_0)* (01111111)* (00110010)* (00101001)*
Icon Display Mode	Set External / Internal Oscillator Set Oscillator Enable, Set Display Mode (Icon Display) Set Display On.	(0111101X_0)* (01111111)* (00110011)* (00101001)*
Annunciator Display	Set External / Internal Oscillator Set Oscillator Enable, Set Annunciator On/Off.	(0111101X_0)* (01111111)* (01100$A_1A_0X_0$)*
Standby Mode 1.	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*
Standby Mode 2.	Set External Oscillator Set Display Off, Set Oscillator Enable. Set Annunciator On / Off,	(01111011)* (00101000)* (01111111)* (01100$A_1A_0X_0$)*
Standby Mode 3.	Set Internal Oscillator Set Display Off, Set Oscillator Enable. Set Annunciator On / Off,	(01111010)* (00101000)* (01111111)* (01100$A_1A_0X_0$)*

Other Related Command with Display Mode : Set Segment Mapping, Set Common Mapping, Set Vertical Scroll Value.

Commands Related to Voltage Generator :

Set Oscillator Enable / Disable, Set Internal Regulator On/Off, Set Temperature Coefficient, Set Internal Constrast Control On/Off, Increase / Decrease Contrast Level, Set Internal Voltage Divider On/Off, Set Display On/Off, Set Reference Voltage Generator, Set Contrast Level, Set Voltage Doubler / Tripler

Commands Required for R/W Actions on RAM

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set MSB of GDDRAM Column Address Set GDDRAM Column Address Read/Write Data	(000000X_1X_0)* (0010011X_0)* (1$X_6X_5X_4X_3X_2X_1X_0$)* ($X_7X_6X_5X_4X_3X_2X_1X_0$)
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	(0011010X_0)
Increase GDDRAM Address.	Dummy Read Data Set GDDRAM Column Address	($X_7X_6X_5X_4X_3X_2X_1X_0$) (1$X_6X_5X_4X_3X_2X_1X_0$)
Master Clear GDDRAM	Master Clear GDDRAM Dummy Write Data	(00110110) ($X_7X_6X_5X_4X_3X_2X_1X_0$)
Master Clear Icons	Set Clear Page 3 of GDDRAM Master Clear Icons Dummy Write Data	(00000010)* (00110111) ($X_7X_6X_5X_4X_3X_2X_1X_0$)
Horizontal Scrolling with Writing GDDRAM	Set GDDRAM Page 1 Set MSB of GDDRAM Column Address Set GDDRAM Column Address Write Data Set GDDRAM Page 1 Set MSB of GDDRAM Column Address Set GDDRAM Column Address Write Data Set Horizontal Scroll Set Scroll Value	(00000000)* (0010011X_0)* (1$X_6X_5X_4X_3X_2X_1X_0$)* ($X_7X_6X_5X_4X_3X_2X_1X_0$) (00000001)* (0010011X_0)* (1$X_6X_5X_4X_3X_2X_1X_0$)* ($X_7X_6X_5X_4X_3X_2X_1X_0$) (01101000) (00000001)

* No need to resend the command again if it is set previously.
The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed.

Display Output Description by Working Example

This is an example of output pattern on the LCD panel. The following table is a description of what is inside the CDDRAM, CGRAM and GDDRAM. Figure 9b and 9c are the output pattern on the LCD display with different command enabled.

(Display Mode, Page Swapping, Scrolling, Column Re-map and Row Re-map)

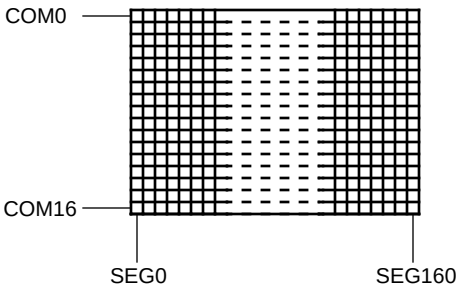
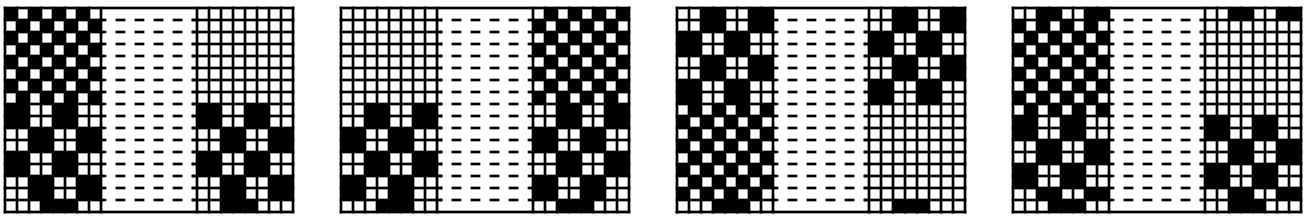


Figure 9a

Content of GDDRAM

PAGE 1	5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - - 0 0 0 0 0 0 0 0 5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - - 0 0 0 0 0 0 0 0
PAGE 2	3 3 C C 3 3 C C - - - - - - - - - - - - - - - - 3 3 C C 3 3 C C 3 3 C C 3 3 C C - - - - - - - - - - - - - - - - 3 3 C C 3 3 C C
PAGE 3	0 0 0 0 0 0 0 0 - - - - - - - - - - - - - - - - 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 - - - - - - - - - - - - - - - - 0 0 1 1 1 0 0 0

Figure 9b

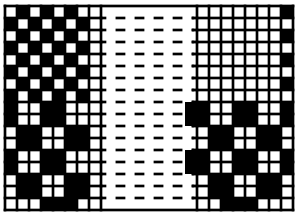


Column remap disable
Row re-map disable

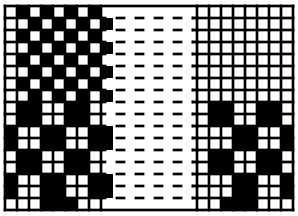
Column remap enable
Row re-map disable

Column remap disable
Row re-map enable

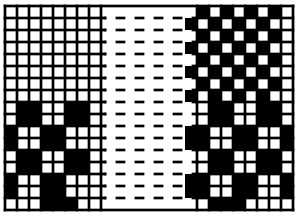
Column remap disable
Row re-map disable
Scroll Value = 0Fh



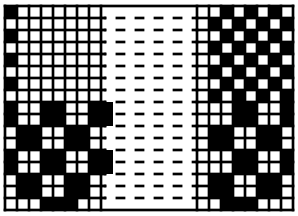
Column remap disable
Row re-map disable
Horizontal scroll = 1



Column remap disable
Row re-map disable
Horizontal scroll = 160



Column remap enable
Row re-map disable
Horizontal scroll = 1

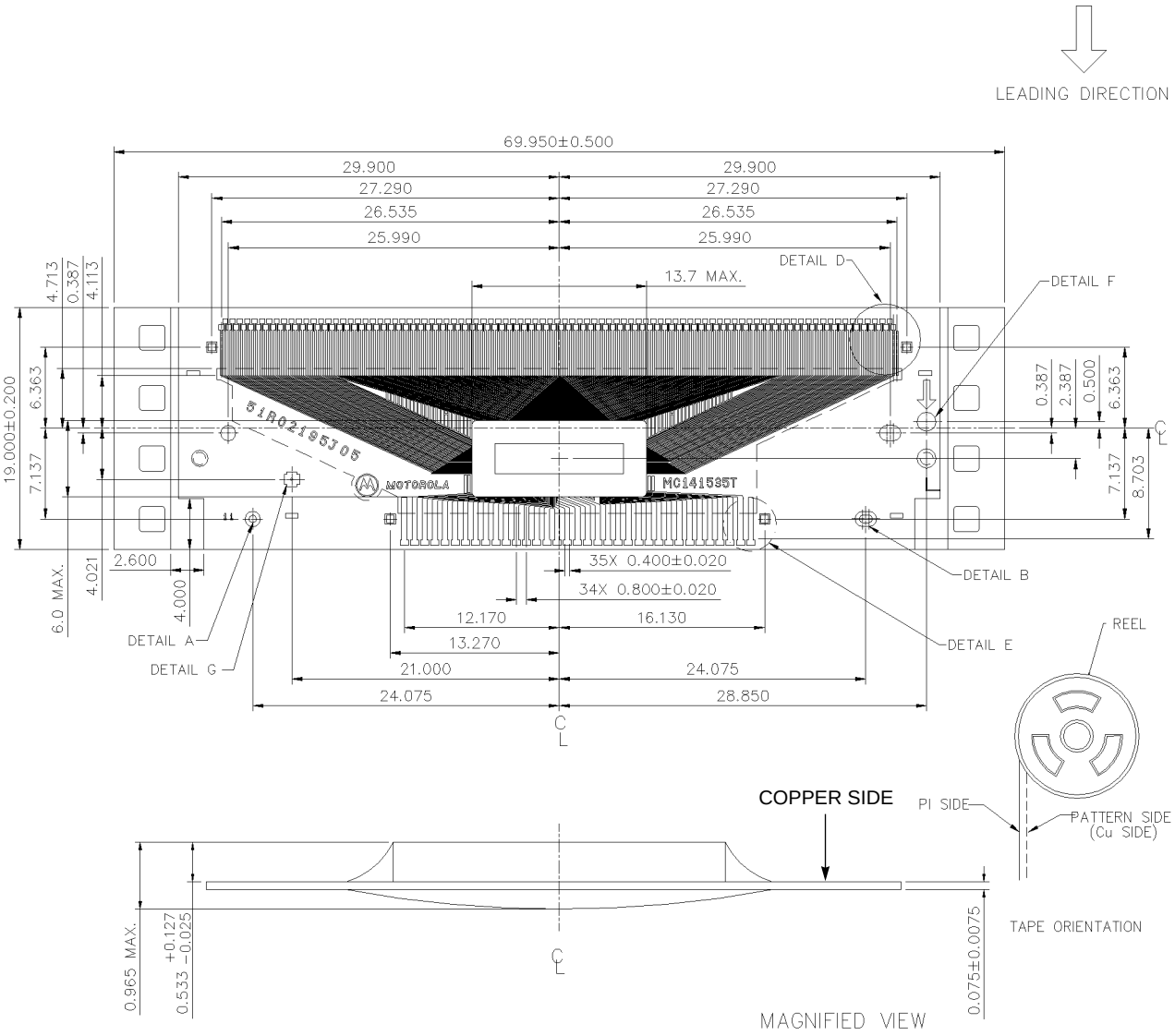


Column remap enable
Row re-map disable
Horizontal scroll = 160

Figure 9c. Examples of LCD display with different command enabled

MC141535T TAB PACKAGE DIMENSION (1 OF 2)
98ASL00248A ISSUE A

DO NOT SCALE THIS DRAWING

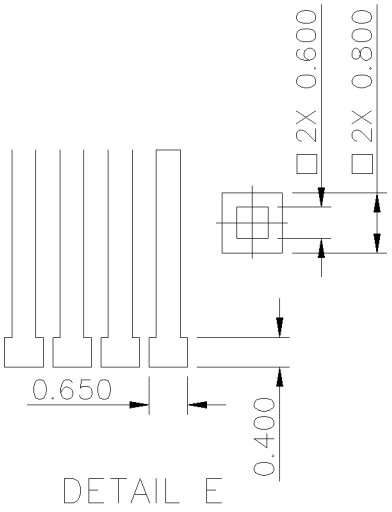


NOTES FOR ALL PAGES

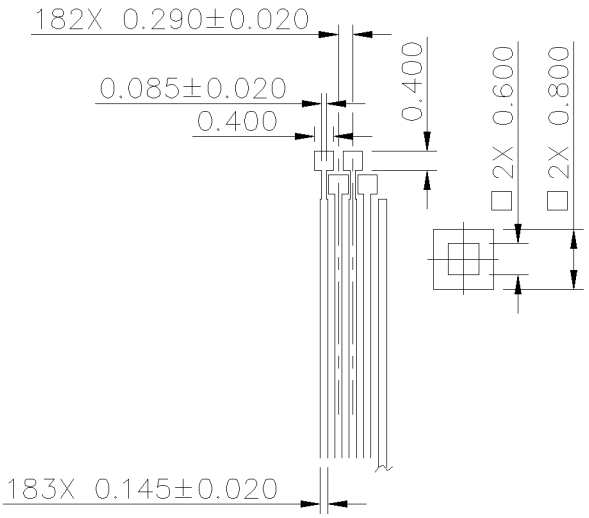
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX−S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø 2.0 MM HOLE.
7. 4 SPROCKET HOLES DEVICE

MC141535T TAB PACKAGE DIMENSION (2 OF 2)
98ASL00248A ISSUE A

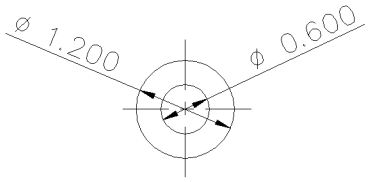
DO NOT SCALE THIS DRAWING



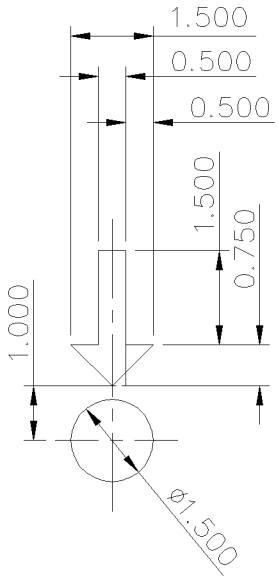
DETAIL E



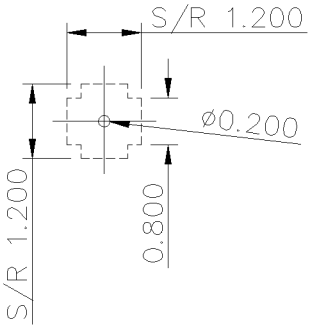
DETAIL D



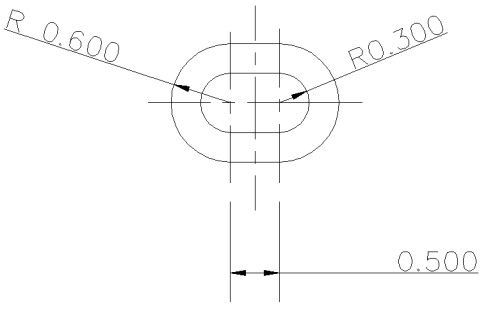
DETAIL A



DETAIL F



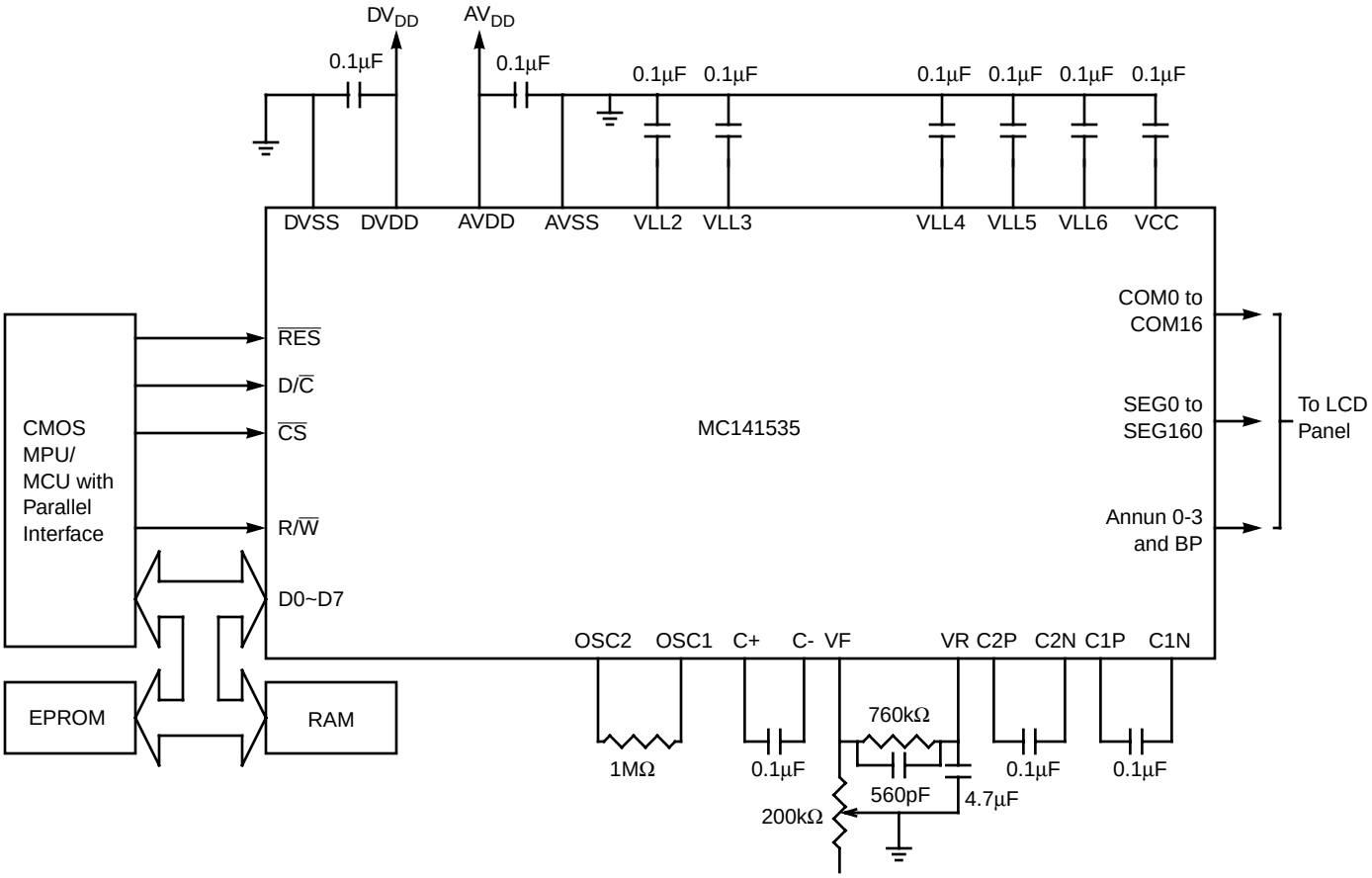
DETAIL G



DETAIL B

Application Circuit

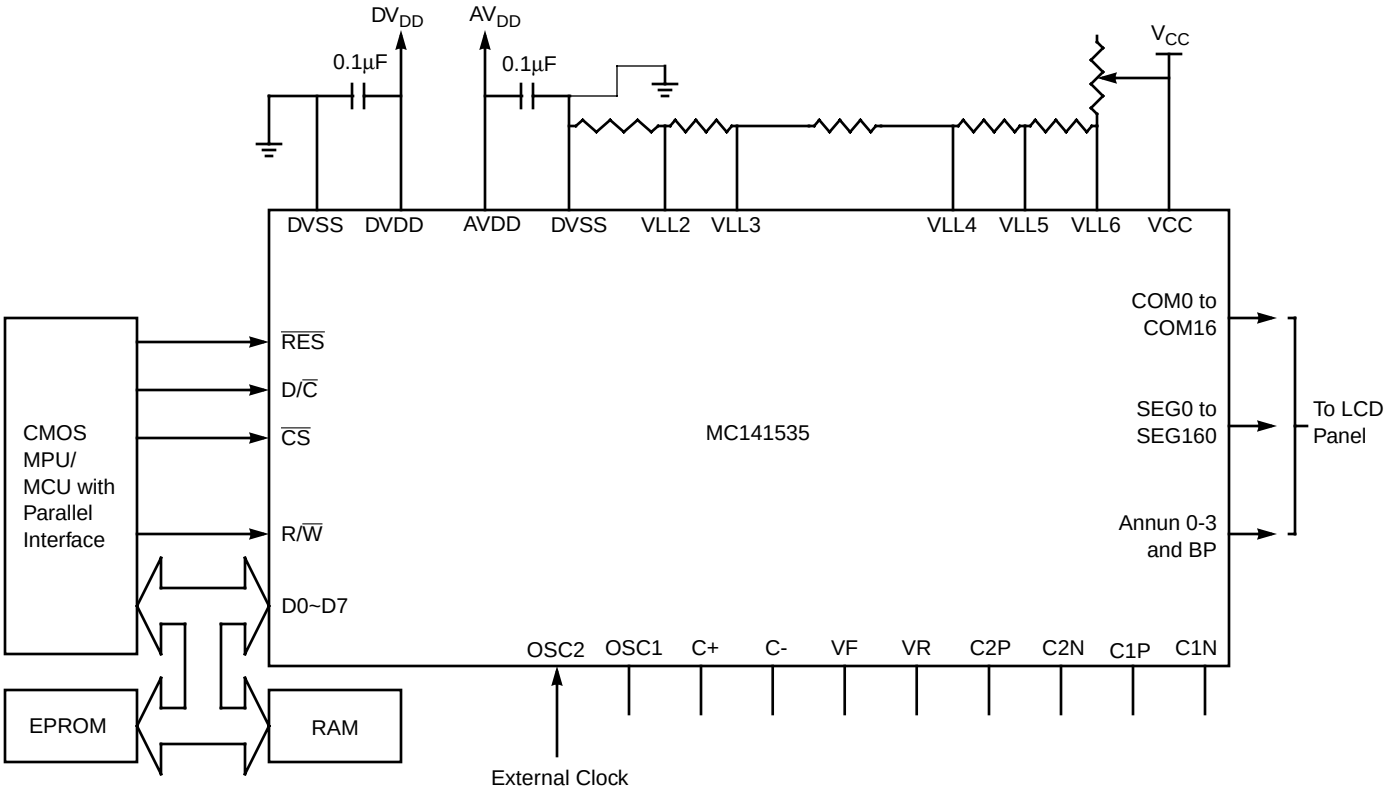
16/17 MUX Dispaly with Analog Circuitry enabled, Tripler enabled and 1:5 bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Application Circuit

16/17 MUX Display with Analog Circuit disabled, External Bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

MC141535 Die Pad Co-ordinate

Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)
1	N/C	-5151.88	-1390.83	71	OSC2	2038.33	-1288.71	141	SEG28	3931.25	1275.76	211	SEG98	-1404.15	1275.76
2	N/C	-5050.13	-1390.83	72	AVDD	2140.08	-1288.71	142	SEG29	3855.03	1275.76	212	SEG99	-1480.37	1275.76
3	N/C	-4948.38	-1390.83	73	N/C	2269.58	-1390.83	143	SEG30	3778.81	1275.76	213	SEG100	-1556.59	1275.76
4	N/C	-4846.63	-1390.83	74	N/C	2371.33	-1390.83	144	SEG31	3702.59	1275.76	214	SEG101	-1632.81	1275.76
5	N/C	-4744.88	-1390.83	75	N/C	2473.08	-1390.83	145	SEG32	3626.37	1275.76	215	SEG102	-1709.03	1275.76
6	N/C	-4643.13	-1390.83	76	N/C	2574.83	-1390.83	146	SEG33	3550.15	1275.76	216	SEG103	-1785.25	1275.76
7	N/C	-4541.38	-1390.83	77	N/C	2676.58	-1390.83	147	SEG34	3473.93	1275.76	217	SEG104	-1861.47	1275.76
8	DVDD	-4264.62	-1307.21	78	N/C	2778.33	-1390.83	148	SEG35	3397.71	1275.76	218	SEG105	-1937.69	1275.76
9	RES	-4183.22	-1307.21	79	N/C	2880.08	-1390.83	149	SEG36	3321.49	1275.76	219	SEG106	-2013.91	1275.76
10	D/C	-4101.82	-1307.21	80	N/C	2981.83	-1390.83	150	SEG37	3245.27	1275.76	220	SEG107	-2090.13	1275.76
11	R/W	-4020.42	-1307.21	81	N/C	3083.58	-1390.83	151	SEG38	3169.05	1275.76	221	SEG108	-2166.35	1275.76
12	CS	-3939.02	-1307.21	82	N/C	3185.33	-1390.83	152	SEG39	3092.83	1275.76	222	SEG109	-2242.57	1275.76
13	DVSS	-3857.62	-1307.21	83	N/C	3287.08	-1390.83	153	SEG40	3016.61	1275.76	223	SEG110	-2318.79	1275.76
14	D0	-3776.22	-1307.21	84	N/C	3388.83	-1390.83	154	SEG41	2940.39	1275.76	224	SEG111	-2395.01	1275.76
15	D1	-3694.82	-1307.21	85	N/C	3490.58	-1390.83	155	SEG42	2864.17	1275.76	225	SEG112	-2471.23	1275.76
16	D2	-3613.42	-1307.21	86	N/C	3592.33	-1390.83	156	SEG43	2787.95	1275.76	226	SEG113	-2547.45	1275.76
17	D3	-3532.02	-1307.21	87	N/C	3694.08	-1390.83	157	SEG44	2711.73	1275.76	227	SEG114	-2623.67	1275.76
18	D4	-3450.62	-1307.21	88	N/C	3795.83	-1390.83	158	SEG45	2635.51	1275.76	228	SEG115	-2699.89	1275.76
19	D5	-3369.22	-1307.21	89	N/C	3897.58	-1390.83	159	SEG46	2559.29	1275.76	229	SEG116	-2776.11	1275.76
20	D6	-3287.82	-1307.21	90	N/C	3999.33	-1390.83	160	SEG47	2483.07	1275.76	230	SEG117	-2852.33	1275.76
21	D7	-3206.42	-1307.21	91	N/C	4101.08	-1390.83	161	SEG48	2406.85	1275.76	231	SEG118	-2928.55	1275.76
22	N/C	-3054.72	-1390.83	92	N/C	4202.83	-1390.83	162	SEG49	2330.63	1275.76	232	SEG119	-3004.77	1275.76
23	N/C	-2952.97	-1390.83	93	N/C	4304.58	-1390.83	163	SEG50	2254.41	1275.76	233	SEG120	-3080.99	1275.76
24	N/C	-2851.22	-1390.83	94	N/C	4406.33	-1390.83	164	SEG51	2178.19	1275.76	234	SEG121	-3157.21	1275.76
25	N/C	-2749.47	-1390.83	95	N/C	4508.08	-1390.83	165	SEG52	2101.97	1275.76	235	SEG122	-3233.43	1275.76
26	N/C	-2647.72	-1390.83	96	N/C	4609.83	-1390.83	166	SEG53	2025.75	1275.76	236	SEG123	-3309.65	1275.76
27	N/C	-2545.97	-1390.83	97	N/C	4711.58	-1390.83	167	SEG54	1949.53	1275.76	237	SEG124	-3385.87	1275.76
28	N/C	-2444.22	-1390.83	98	N/C	4813.33	-1390.83	168	SEG55	1873.31	1275.76	238	SEG125	-3462.09	1275.76
29	N/C	-2342.47	-1390.83	99	N/C	4915.08	-1390.83	169	SEG56	1797.09	1275.76	239	SEG126	-3538.31	1275.76
30	N/C	-2240.72	-1390.83	100	N/C	5016.83	-1390.83	170	SEG57	1720.87	1275.76	240	SEG127	-3614.53	1275.76
31	N/C	-2138.97	-1390.83	101	BP	5163.35	-1160.69	171	SEG58	1644.65	1275.76	241	SEG128	-3690.75	1275.76
32	N/C	-2037.22	-1390.83	102	ANN2	5163.35	-1084.47	172	SEG59	1568.43	1275.76	242	SEG129	-3766.97	1275.76
33	N/C	-1935.47	-1390.83	103	ANN3	5163.35	-1008.25	173	SEG60	1492.21	1275.76	243	SEG130	-3843.19	1275.76
34	N/C	-1833.72	-1390.83	104	COM16	5163.35	-932.03	174	SEG61	1415.99	1275.76	244	SEG131	-3919.41	1275.76
35	N/C	-1731.97	-1390.83	105	COM15	5163.35	-855.81	175	SEG62	1339.77	1275.76	245	SEG132	-3995.63	1275.76
36	N/C	-1630.22	-1390.83	106	COM14	5163.35	-779.59	176	SEG63	1263.55	1275.76	246	SEG133	-4071.85	1275.76
37	N/C	-1528.47	-1390.83	107	COM13	5163.35	-703.37	177	SEG64	1187.33	1275.76	247	SEG134	-4148.07	1275.76
38	N/C	-1426.72	-1390.83	108	COM12	5163.35	-627.15	178	SEG65	1111.11	1275.76	248	SEG135	-4224.29	1275.76
39	N/C	-1324.97	-1390.83	109	COM11	5163.35	-550.93	179	SEG66	1034.89	1275.76	249	SEG136	-4300.51	1275.76
40	N/C	-1223.22	-1390.83	110	COM10	5163.35	-474.71	180	SEG67	958.67	1275.76	250	SEG137	-4376.73	1275.76
41	N/C	-1121.47	-1390.83	111	COM9	5163.35	-398.49	181	SEG68	882.45	1275.76	251	SEG138	-4452.95	1275.76
42	N/C	-1019.72	-1390.83	112	COM8	5163.35	-322.27	182	SEG69	806.23	1275.76	252	SEG139	-4529.17	1275.76
43	N/C	-917.97	-1390.83	113	SEG0	5163.35	-206.09	183	SEG70	730.01	1275.76	253	SEG140	-4605.39	1275.76
44	N/C	-816.22	-1390.83	114	SEG1	5163.35	-129.87	184	SEG71	653.79	1275.76	254	SEG141	-5163.35	1242.09
45	N/C	-714.47	-1390.83	115	SEG2	5163.35	-53.65	185	SEG72	577.57	1275.76	255	SEG142	-5163.35	1165.87
46	N/C	-612.72	-1390.83	116	SEG3	5163.35	22.57	186	SEG73	501.35	1275.76	256	SEG143	-5163.35	1089.65
47	N/C	-510.97	-1390.83	117	SEG4	5163.35	98.79	187	SEG74	425.13	1275.76	257	SEG144	-5163.35	1013.43
48	N/C	-409.22	-1390.83	118	SEG5	5163.35	175.01	188	SEG75	348.91	1275.76	258	SEG145	-5163.35	937.21
49	N/C	-307.47	-1390.83	119	SEG6	5163.35	251.23	189	SEG76	272.69	1275.76	259	SEG146	-5163.35	860.99
50	N/C	-205.72	-1390.83	120	SEG7	5163.35	327.45	190	SEG77	196.47	1275.76	260	SEG147	-5163.35	784.77
51	AVSS	-57.72	-1288.71	121	SEG8	5163.35	403.67	191	SEG78	120.25	1275.76	261	SEG148	-5163.35	708.55
52	VF	44.03	-1288.71	122	SEG9	5163.35	479.89	192	SEG79	44.03	1275.76	262	SEG149	-5163.35	632.33
53	AVSS	145.78	-1288.71	123	SEG10	5163.35	556.11	193	SEG80	-32.19	1275.76	263	SEG150	-5163.35	556.11
54	C2P	247.53	-1288.71	124	SEG11	5163.35	632.33	194	SEG81	-108.41	1275.76	264	SEG151	-5163.35	479.89
55	C2N	349.28	-1288.71	125	SEG12	5163.35	708.55	195	SEG82	-184.63	1275.76	265	SEG152	-5163.35	403.67
56	C2N	451.03	-1288.71	126	SEG13	5163.35	784.77	196	SEG83	-260.85	1275.76	266	SEG153	-5163.35	327.45
57	C1P	552.78	-1288.71	127	SEG14	5163.35	860.99	197	SEG84	-337.07	1275.76	267	SEG154	-5163.35	251.23
58	C1N	654.53	-1288.71	128	SEG15	5163.35	937.21	198	SEG85	-413.29	1275.76	268	SEG155	-5163.35	175.01
59	C1N	756.28	-1288.71	129	SEG16	5163.35	1013.43	199	SEG86	-489.51	1275.76	269	SEG156	-5163.35	98.79
60	C+	858.03	-1288.71	130	SEG17	5163.35	1089.65	200	SEG87	-565.73	1275.76	270	SEG157	-5163.35	22.57
61	C-	959.78	-1288.71	131	SEG18	5163.35	1165.87	201	SEG88	-641.95	1275.76	271	SEG158	-5163.35	-53.65
62	VR	1122.58	-1288.71	132	SEG19	5163.35	1242.09	202	SEG89	-718.17	1275.76	272	SEG159	-5163.35	-129.87
63	VLL2	1224.33	-1288.71	133	SEG20	4541.01	1275.76	203	SEG90	-794.39	1275.76	273	SEG160	-5163.35	-206.09
64	VLL3	1326.08	-1288.71	134	SEG21	4464.79	1275.76	204	SEG91	-870.61	1275.76	274	COM16	-5163.35	-322.27
65	VLL4	1427.83	-1288.71	135	SEG22	4388.57	1275.76	205	SEG92	-946.83	1275.76	275	COM0	-5163.35	-398.49
66	VLL5	1529.58	-1288.71	136	SEG23	4312.35	1275.76	206	SEG93	-1023.05	1275.76	276	COM1	-5163.35	-474.71
67	VLL6	1631.33	-1288.71	137	SEG24	4236.13	1275.76	207	SEG94	-1099.27	1275.76	277	COM2	-5163.35	-550.93
68	OSC1	1733.08	-1288.71	138	SEG25	4159.91	1275.76	208	SEG95	-1175.49	1275.76	278	COM3	-5163.35	-627.15
69	VCC	1834.83	-1288.71	139	SEG26	4083.69	1275.76	209	SEG96	-1251.71	1275.76	279	COM4	-5163.35	-703.37
70	OSC2	1936.58	-1288.71	140	SEG27	4007.47	1275.76	210	SEG97	-1327.93	1275.76	280	COM5	-5163.35	-779.59
												281	COM6	-5163.35	-855.81
												282	COM7	-5163.35	-932.03
												283	ANN1	-5163.35	-1008.25
												284	ANN0	-5163.35	-1084.47
												285	BP	-5163.35	-1160.69

Die Size : 431.5 mil x 129.53 mil

Note : Do not connect the NC pin to external circuit

Pad No.	Pad Size	Unit	Pad No.	Pad Size	Unit
1-7	62x62	µm	101-132	107x50	µm
8-21	50x107	µm	133-253	50x107	µm
21-100	62x62	µm	254-285	107x50	µm