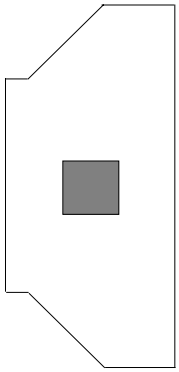
MC141539

LCD Segment / Common Driver with Controller
CMOS



ORDERING INFORMATION

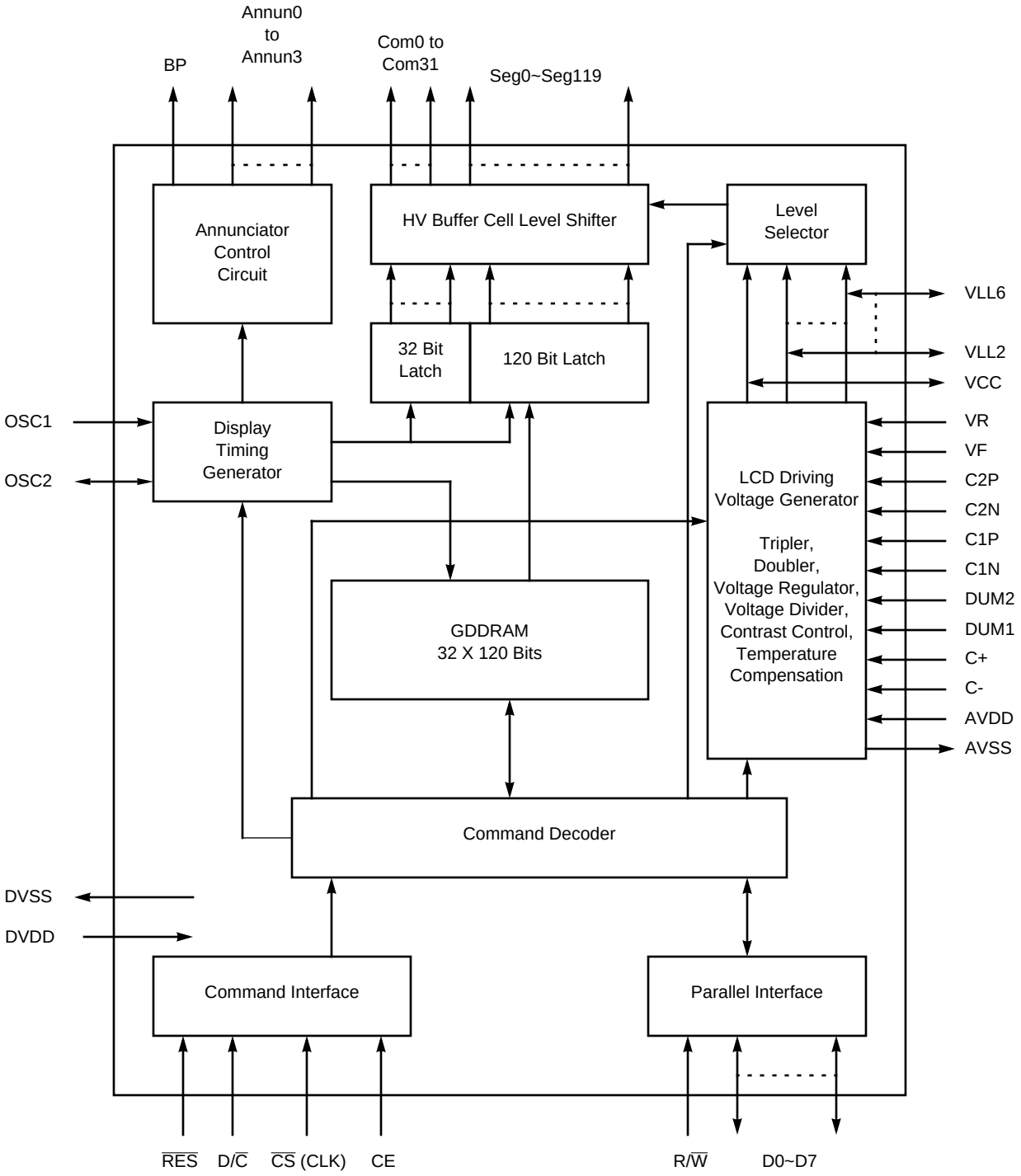
MC141539T1R	TAB
MC141539T2R	TAB

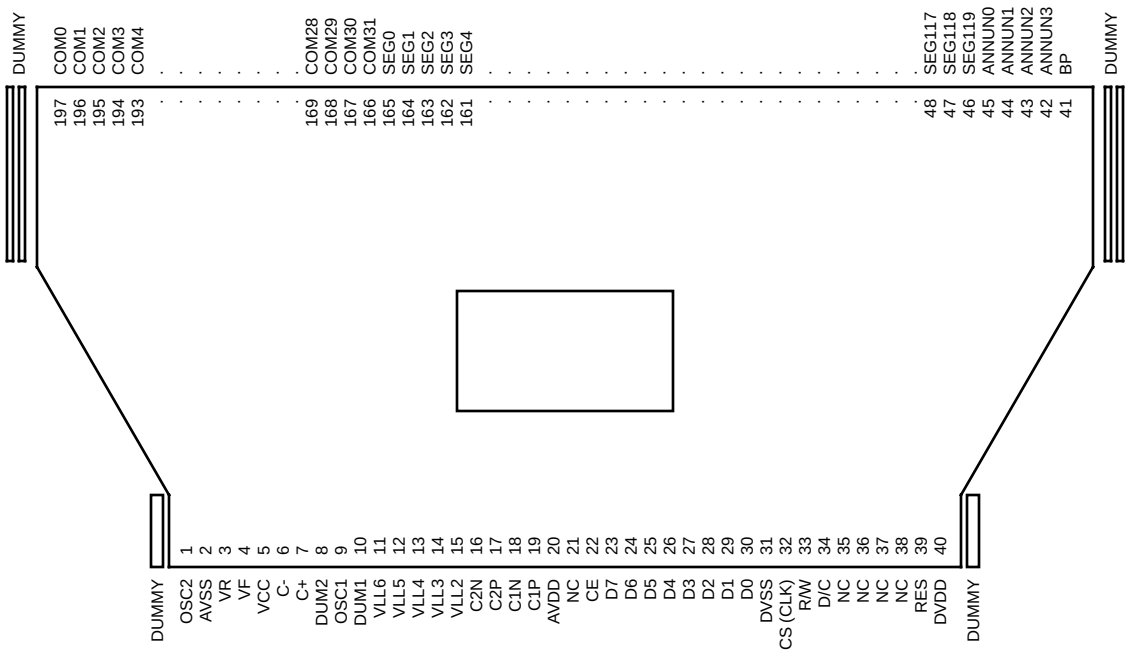
MC141539 is a CMOS LCD Driver which consists of 4 annunciator outputs and 152 high voltage LCD driving signals (32 commons and 120 segments). It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD bias voltage generator circuit such that fewer external components are required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Operating Temperature Range : -30 to 85°C
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 Bit Parallel Interface
- Graphic Mode Operation
- On Chip 480 Byte Graphic Display Data RAM
- 120 Segment Drivers, 32 Common Drivers
- Selectable 1/16 or 1/32 Multiplex Ratio
- Selectable on Chip Voltage Doubler and Tripler
- Selectable 1:5 or 1:7 Bias Ratio
- Re-mapping of Row and Column Drivers
- Four Stand Alone Annunciator Driver Circuits
- Selectable LCD Driving Voltage Temperature Coefficients
- 16 Level Internal Contrast Control
- External Contrast Control Provided
- Master Clear RAM
- Standard TAB Package

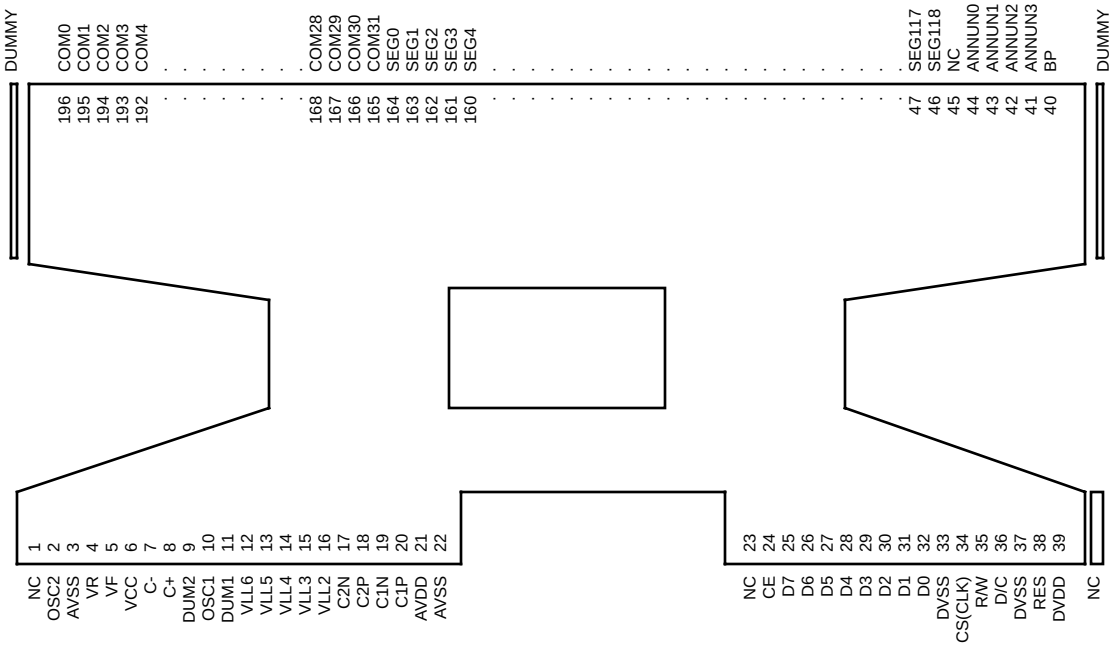
REV 7
2/98

Block Diagram





MC141539T1 PIN ASSIGNMENT
(COPPER VIEW)



MC141539T2 PIN ASSIGNMENT
(COPPER VIEW)

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MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_{A1} T_{A2}	Operating Temperature For Using Internal Oscillator For Using External Oscillator	 -25 to +85 -30 to +85	 ˚C ˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
V_{SS} = AV_{SS} = DV_{SS} (DV_{SS} = V_{SS} of Digital circuit, AV_{SS} = V_{SS} of Analogue Circuit)
V_{DD} = AV_{DD} = DV_{DD} (DV_{DD} = V_{DD} of Digital circuit, AV_{DD} = V_{DD} of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Supply voltage (Absolute value Referenced to V_{SS})					
DV_{DD}	Operating Range of Logic Circuit Supply DV_{DD}		2.4	3.15	3.5	V
AV_{DD}	Operating Range of Voltage Generator Circuit Supply AV_{DD}		DV_{DD}	3.15	3.5	V
	Supply Current (Measure with V_{DD} fixed at 2.8V)					
I_{AC}	Access Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Accessing, T_{cyc}=1MHz, Osc. Freq.=50kHz, 1/32 Duty Cycle,1/7 Bias.	0	200	300	µA
I_{DP1}	Display Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=50kHz, 1/32 Duty Cycle,1/7 Bias.	0	76	115	µA
I_{DP2}	Display Mode Supply Current Drain from Pin AVDD and DVDD	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz, 1/32 Duty Cycle,1/7 Bias.	0	55	75	µA
I_{SB1}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD	Display Off, Oscillator Disabled, R/W Halt	0	300	500	nA
I_{SB2}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, External Oscillator and Frequency = 50kHz.	0	2.5	5	µA
I_{SB3}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 50kHz.	0	5	10	µA
	VLCD Voltage (Absolute Value Refer to V_{SS})					
V_{CC1}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Tripler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100µA	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Doubler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100µA	-	2*AV_{DD}	7	V
V_{LCD}	LCD Driving Voltage input at pin V_{CC}.	Internal DC/DC Converter Disabled.	AV_{DD}	-	10.5	V
	Output Voltage					
V_{OH1}	Output High Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0.8*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0	-	0.2*V_{DD}	V
V_{R1}	LCD Driving Voltage Source at Pin VR	Regulator Enabled, I_{out}=50µA	0	-	V_{CC}	V
V_{R2}	LCD Driving Voltage Source at Pin VR	Regulator Disabled, I_{out}=50µA.	-	Floating	-	V
	Input Voltage					
V_{IH1}	Input High Voltage at Pins, $\overline{RES}$, CE, $\overline{CS}$, D0-D7, $\overline{R}$/W, D/C, OSC1 and OSC2.		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage at Pins, $\overline{RES}$, CE, $\overline{CS}$, D0-D7, $\overline{R}$/W, D/C, OSC1 and OSC2.		0	-	0.2*V_{DD}	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, DV_{DD}=2.4-3.15V, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	LCD Display Voltage. (LCD Driving Voltage Output from Pins VLL6, VLL5, VLL4, VLL3 and VLL2.)	1/5 Bias Ratio, Voltage Divider Enabled, Regulator Enabled.				
V_{LL6}			-	V_R	-	V
V_{LL5}			-	0.8*V_R	-	V
V_{LL4}			-	0.6*V_R	-	V
V_{LL3}			-	0.4*V_R	-	V
V_{LL2}			-	0.2*V_R	-	V
		1/7 Bias Ratio, Voltage Divider Enabled, Regulator Enabled				
V_{LL6}			-	V_R	-	V
V_{LL5}			-	6/7*V_R	-	V
V_{LL4}			-	5/7*V_R	-	V
DUM2			-	4/7*V_R	-	V
DUM1			-	3/7*V_R	-	V
V_{LL3}			-	2/7*V_R	-	V
V_{LL2}			-	1/7*V_R	-	V
		External Voltage Generator, Voltage Divider Disable				
V_{LL6}			0.5V_{CC}	-	V_{CC}	V
V_{LL5}			0.5V_{CC}	-	V_{CC}	V
V_{LL4}			0.5V_{CC}	-	V_{CC}	V
V_{LL3}			V_{SS}	-	0.5V_{CC}	V
V_{LL2}			V_{SS}	-	0.5V_{CC}	V
	Output Current					
I_{OH}	Output High Current Source from Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=VDD-0.4V	100	-	-	µA
I_{OL}	Output Low Current Drain by Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=0.4V	-	-	-100	µA
I_{OZ}	Output Tri-state Current Drain Source at pins D0-D7 and OSC2		-1	-	1	µA
I_{IL}/I_{IH}	Input Current at pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$ OSC1 and OSC2.		-1	-	1	µA
Ron	On Resistance Channel Resistance between LCD Driving Signal Pins (SEG and COM) and Driving Voltage Input Pins (V_{LL2} to V_{LL6}).	During Display on, 0.1V Apply between Two Terminals, V_{CC} within Operating Voltage Range	-	-	10	kΩ
V_{SB}	Memory Retention Voltage (DV_{DD}) Standby Mode, Retained All Internal Configuration and RAM Data		1.8	-	-	V
C_{IN}	Input Capacitance OSC1, OSC2 and All Control Pins		-	5	7.5	pF
	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled	-	-0.35	-	%
V_{CN}	Internal Contrast Control VR Output Voltage with Internal Contrast Control Selected. 16 Voltage Levels Controlled by Software. Each Level is Typical of 2.25% of the Regulator Output Voltage.	Regulator Enabled, Internal Contrast Control Enabled	-	±18	-	%

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{VR \text{ at } 50^{\circ}C - VR \text{ at } 0^{\circ}C}{50^{\circ}C - 0^{\circ}C} \times \frac{1}{VR \text{ at } 25^{\circ}C} \times 100\%$$

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, AV_{DD}=DV_{DD}=2.4 to 3.5V, T_A=25˚C)

Total variation of VR ΔV_{RT} is affected by the following factors :

Process variation of Regulator ΔV_R

External V_{DD} Variation contributed to Regulator ΔV_{VDD}

External resistor pair Ra/Rf contributed to Regulator ΔV_{res}

where $\Delta V_{RT} = \sqrt{(\Delta V_R)^2 + (\Delta V_{V_{DD}})^2 + (\Delta V_{res})^2}$

Assume external V_{DD} variation is +/-6% at 3.15V and 1% variation resistor used at application

	TC Level	ΔV_{VDD} (%)	ΔV_R (%)	ΔV_{res} (%)	ΔV_{RT} (%)
Reference Generator	TC0	±6.0	±2.5	±1.414	±6.652
	TC1	±4.0			±4.924
	TC2	±2.5			±3.805
	TC3	±1.4			±3.195

AC ELECTRICAL CHARACTERISTICS (T_A=25˚C, Voltage referenced to V_{SS}, V_{DD}=2.4 to 3.15V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Oscillation Frequency.	Set Clock Frequency to Low				
F_{OSC1}	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	38.4	-	kHz
F_{ANN1}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP		-	18.75	-	Hz
F_{FRM1}	LCD Driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, Either 1/32 or 1/16 Duty Cycle, Graphic Display Mode	-	66	-	Hz
	Oscillation Freq.	Set Clock Frequency to High				
$Fosc_2$	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	50	-	kHz
F_{ANN2}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP		-	24.4	-	Hz
F_{FRM2}	LCD driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, Either 1/32 Duty Cycle	-	65	-	Hz
OSC	Internal Oscillation Frequency					
	Internal OSC Oscillation Frequency with Different Value of Feedback Resistor.	Internal Oscillator Enabled. V_{DD} within Operation Range	See Figure 1 for the relationship			

Set Clock Frequency to Slow : F_{FRM1}=F_{OSC1}/576

Set Clock Frequency to Normal : F_{FRM2}=F_{OSC2}/768

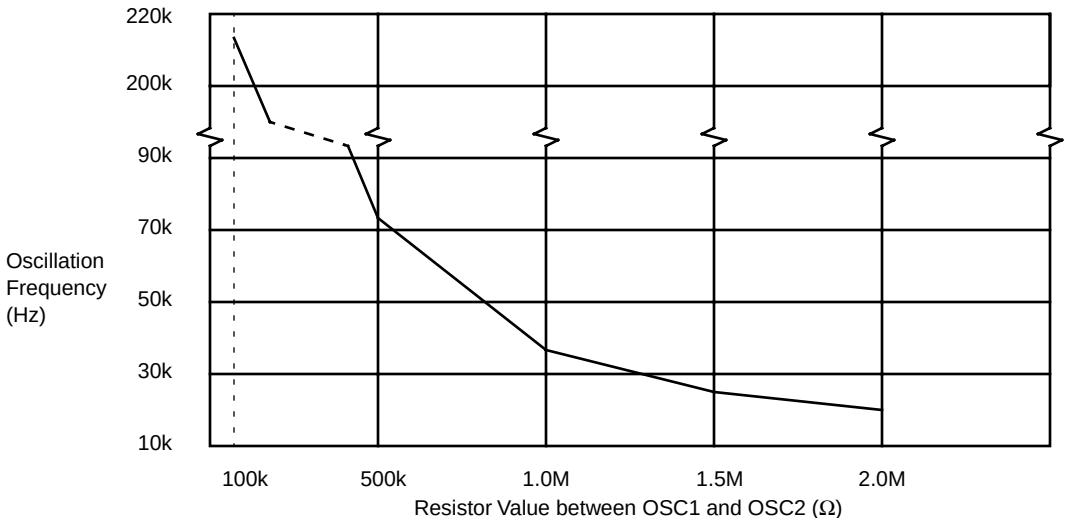


Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value

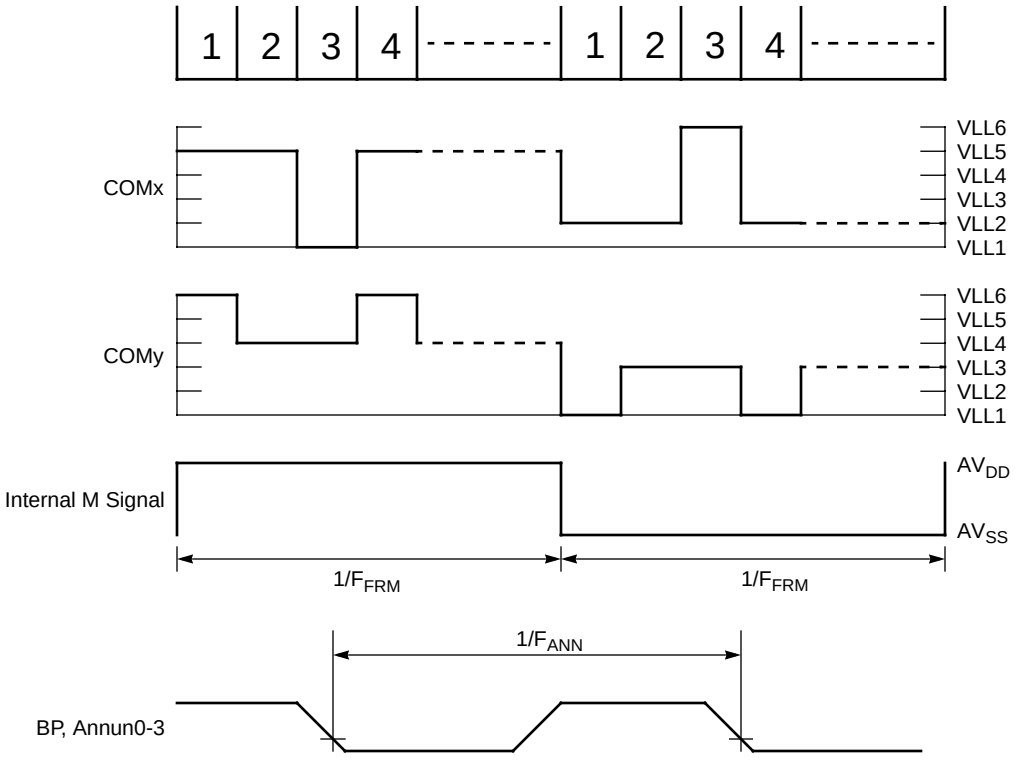


Figure 2. LCD Driving Signal Timing Diagram

TABLE 2a. Parallel Timing Characteristics (Write Cycle) (T_A=-10 to 60˚C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DS}	Data Setup Time	290	-	-	ns
t_{DH}	Data Hold Time	0	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns

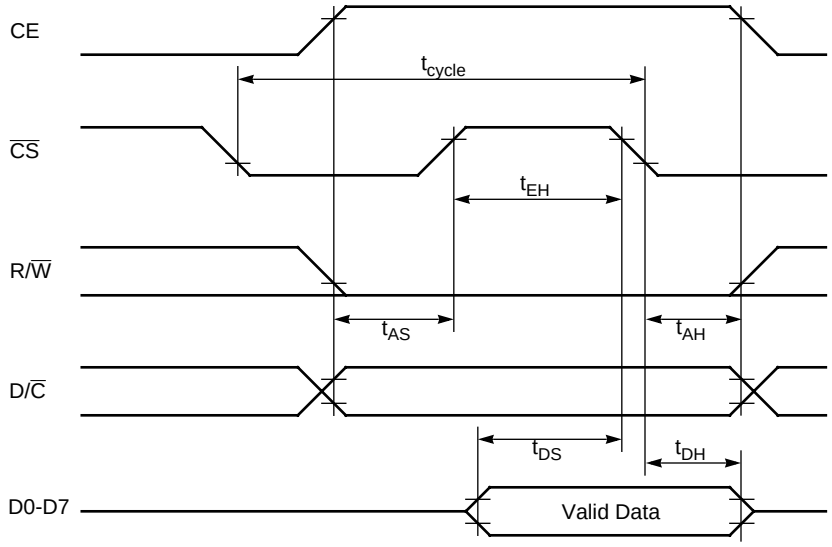


Figure 3. Timing Characteristics (Write Cycle)

TABLE 2b. Parallel Timing Characteristics (Read Cycle) (T_A=-10 to 60˚C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	375	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DS}	Data Setup Time	-	-	350	ns
t_{DH}	Data Hold Time	7	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns

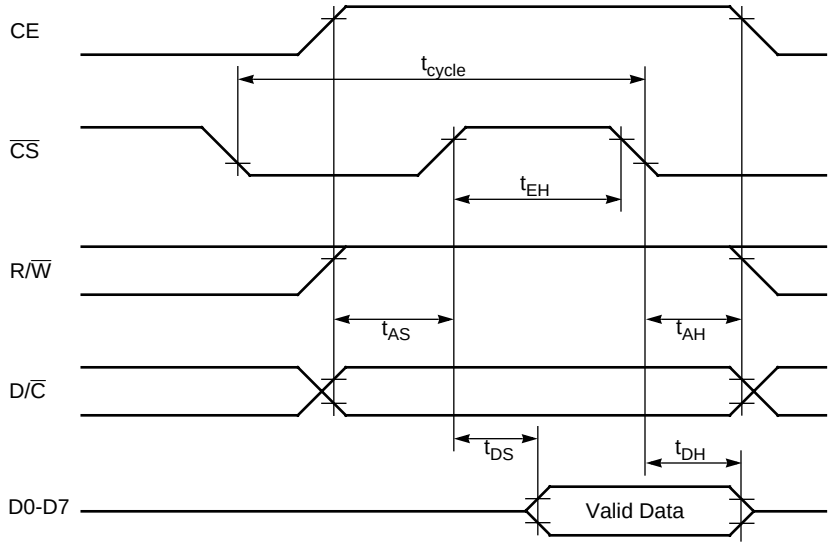


Figure 4. Timing Characteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)

This input pin acknowledge the driver the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Input Clock)

This pin is normal Low clock input. Data on D0-D7 is latched at the falling edge of CS.

$\overline{RES}$ (Reset)

An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 μs.

CE (Chip Enable)

HIGH input to this pin to enable the control pins on the driver.

D0-D7

This bi-directional bus is used for data / command transferring.

R/$\overline{W}$ (Read/Write)

This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/W input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)

For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value is placed between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)

This is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2

Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit. For internal Voltage Divider enabled, a capacitor to AV_{SS} is required on each pin.

DUM1 and DUM2

If internal Voltage Divider is enabled with 1/7 bias selected, a capacitor to AV_{SS} is required on each pin. Otherwise, pull these two pin to AV_{SS}

C1N and C1P

If Internal DC/DC Converter is enabled, a capacitor is required to connect these two pins.

C2N and C2P

If 32 Mux is selected and Internal DC/DC Converter is enabled, a capacitor is required between these two pins. Otherwise, leave these pin open.

C+ and C-

If internal divider circuit is enabled, a capacitor is required to connect between these two pins.

VR and VF

This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 μF capacitor placed between VR and AVSS. (Refer to the Application Circuit Section)

COM0-COM31 (Row Drivers)

These pins provide the row driving signal to LCD panel. Com0-Com31 are used in 32 mux configuration. Com0-Com15 are used in 16 mux and no row remap configuration while Com16-Com31 are used in 16 mux with row remap configuration. They output 0V during display off.

SEG0-SEG119 (Column Drivers)

These 120 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)

This pin combines with Annun0-Annun3 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of F_{ANNn} Hz. It outputs low when oscillator is disabled.

Annun0 - Annun3 (Annunciator Frontplanes)

These pins are four independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a F_{ANNn} Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When oscillator is disabled, all these pins output 0V.

AVDD and AVSS

AVDD is the positive supply to the LCD bias voltage generator. AVSS is ground.

VCC

For using the Internal DC/DC Converter, a 0.1 μF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Positive power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS

Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command.

Data is directed to this module based upon the input of the D/C pin. If D/C high, data is written to Graphic Display Data RAM (GDDRAM). D/C low indicates that the input at D0-D7 is interpreted as a Command.

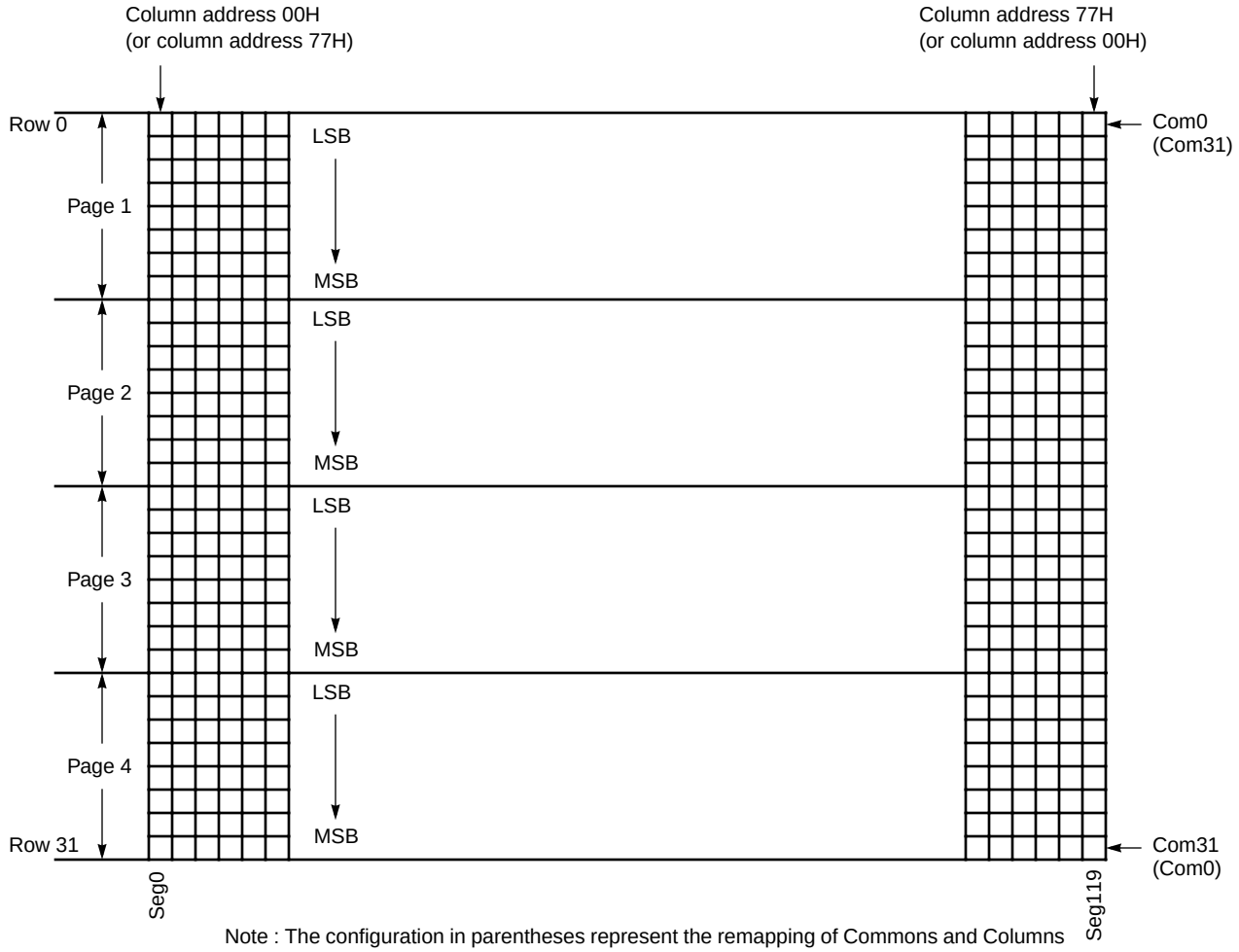
CE is the master chip selection signal. A High input enable the input lines ready to sample signals. Reset is of same function as Power ON Reset (POR). Once RES received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7), R/W, and the CS. The R/W input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/W input Low indicates a write to Display Data RAM or Internal Command Registers depending on the status of D/C input. The CS input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (120x32 = 3840 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.



Note : The configuration in parentheses represent the remapping of Commons and Columns

Figure 5. Graphic Display Data RAM (GDDRAM) Address Map

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 15 kHz to 50 kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 4 annunciators and BP are generated by this module. The 4 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit too. the annunciators pins output 0V when oscillator is disabled. Annunciator output waveform shown in Figure 7.

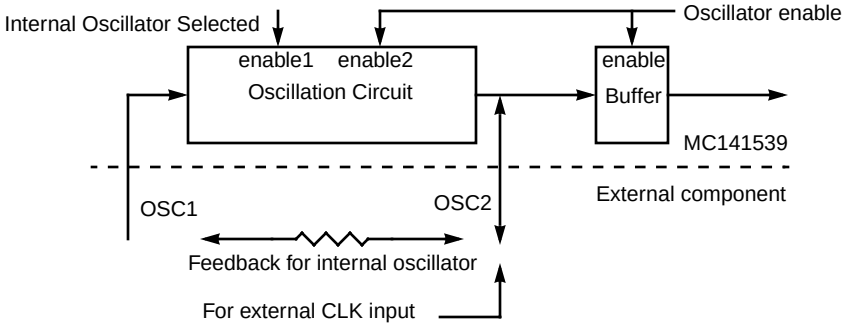


Figure 6. Oscillator Circuitry

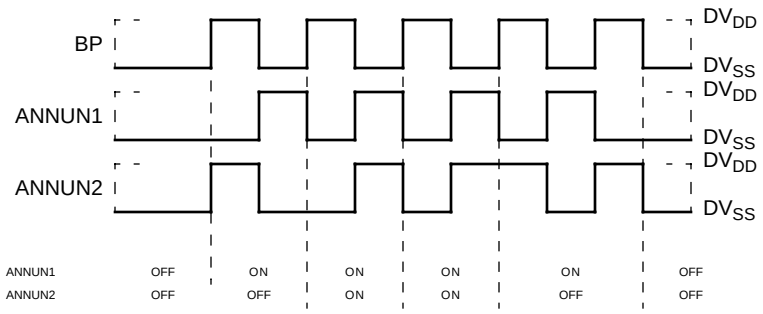


Figure 7. Annunciators and BP Display Waveform

LCD Driving Voltage Generator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Either Doubler or Tripler can be enabled.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. It can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.
4. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
5. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.
6. Bias Ratio Selection circuitry
   Software control of 1/5 and 1/7 bias ratio to match the characteristic of LCD panel.

All blocks can be individually turned off if external voltage generator is employed

32 Bit Latch / 120 Bit Latch

A 152 bit long register which carries the display signal information. First 32 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shift-er)

HV Buffer Cell works as a level shift-er which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Reference Generator

Two reference generators on chip to provide reference voltage to the regulator circuitry. The VR (LCD driving voltage) stability is affected by the performance of the reference voltage. For details on it's performance, please refer to electrical characteristic.

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 8a, 8b and 8c illustrate the desired multiplex scheme.

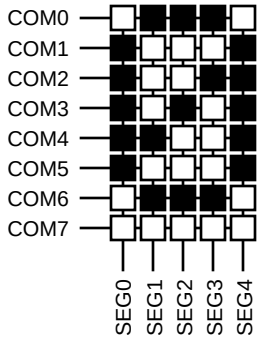


Figure 8a. LCD Display Example “0”

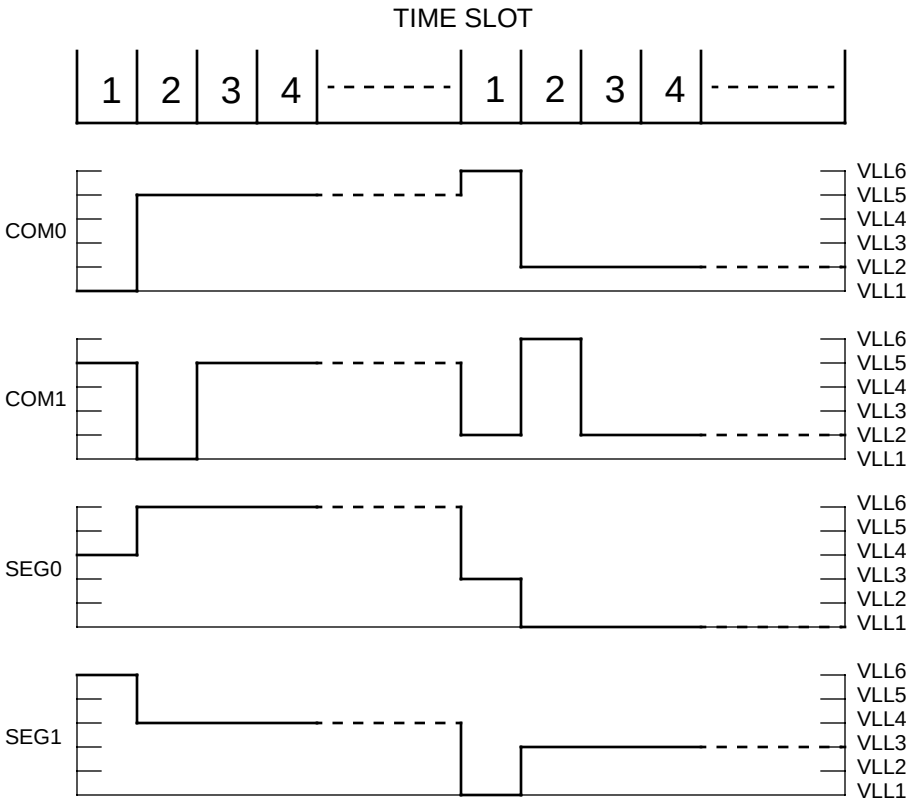


Figure 8b. LCD Driving Signal from MC141539

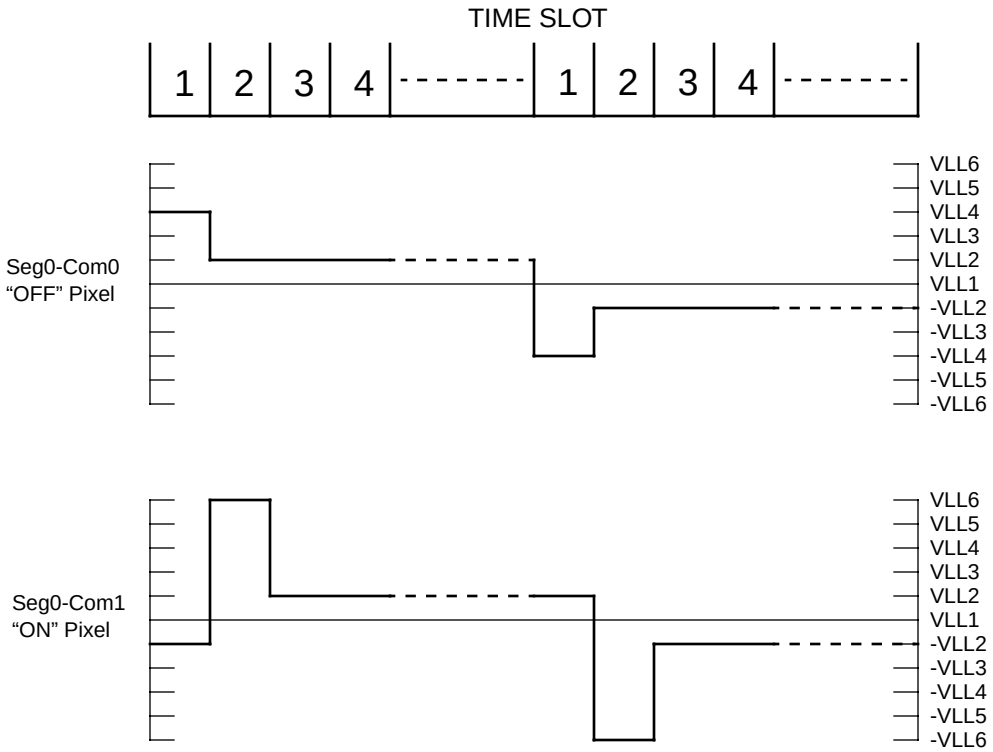


Figure 8c. Effective LCD waveform on LCD pixel

Command Description

Display On/Off (Display Mode / Stand-by Mode)

The Dispaly On command turns the LCD Common and Segment outputs on and has no effect to the annunciator output. This command causes the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note : “Oscillator On” command should be sent before “Display On” is selected)

The Display Off command turns the display off and the states of the LCD driver are as follow during display off :

1. The Common and Segment outputs are fixed at V_{LL1} (V_{SS}).
2. The bias Voltage Generator is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The status of the Annunciators and Oscillator are not affected by this command.

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-77H (120 columns). The column address will be increased by one automatically after a read or write operation. Refer “Address Enlacement Table” and command “Set GDDRAM Page Address”.

Set GDDRAM Page Address

This command positions the row address to 1 of 4 possible positions in GDDRAM. Refer to figure 5.

Master Clear GDDRAM

This command is to clear the 480 byte Display Data RAM by setting the RAM data to zero. Issue this command followed by a dummy write command.

Set Vertical Scroll Value

This command is used to scroll the screen vertically with scroll value 0 to 31. With scroll value equals to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 31 are mapped to Com1 through Com31 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 31 will be mapped to Com1 through Com30 respectively and Row 0 will be mapped to Com31.

Save / Restore Column Address

With bit option = 1 in this command, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With bit option = 0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 119 of GDDRAM mapped to Seg0-Seg119 respectively;
2. Column 0 - Column 119 of GDDRAM mapped to Seg119-Seg0 respectively.

Detail information please refer to section “Display Output Description”.

Set Row Mapping

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row 31 of GDDRAM to Com0 - Com31 respectively;
2. Row 0 - Row 31 of GDDRAM to Com31 - Com0 respectively.

See section “Display Output Description” for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 4 stand alone annunciator drivers.

Set Oscillator Enable / Disable

This command is used to either turn on / off Oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command “Set Display On/Off” and “Set Annunciator On/Off”. See command “Ext/Int Oscillator” for more information

Set External / Internal Oscillator

This command is used to select either internal or external oscillator. When internal oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Set Clock Frequency

Use this command to choose from two different oscillation frequencies (50kHz or 38.4kHz) to get the 60 Hz frame frequency. With frequency high, 50 kHz clock frequency is preferred. 38.4kHz clock frequency (low frequency) enable for power saving purpose.

Set Internal DC/DC Converter On/Off

Use this command to select the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Disable the Internal DC/DC Converter if external Vcc is provided.

Set Voltage Doubler / Tripler

Use this command to choose Voltage Doubler or Tripler when the Internal DC/DC Converter is enabled.

Set Internal Regulator On/Off

Choose bit option 0 to disable the Internal Regulator. Choose bit option 1 to enable Internal Regulator which consists of the internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltage Divider is disabled, external bias can be used for V_{LL6} to V_{LL2}. If the Internal Voltage Divider is enabled, the internal circuit will automatically select the correct bias level according to the number of multiplex. Refer to command “Set Bias Ratio ”.

Set Duty Cycle

This command is to select 16 mux or 32 mux display. When 16 mux is enabled, the unused 16 common outputs will be swinging between VLL2 and VLL5 for dummy scan purpose and doubler will be used.

Set Bias Ratio

This command sets the 1/5 bias or 1/7 bias for the divider output. The selection should match the characteristic of LCD Panel.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to

increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from lowest value after POR.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use.

Read Contrast Value

This command allows the user to read the current contrast level value. With R/$\overline{W}$ input high (READ), D/$\overline{C}$ input low (COMMAND) and D7 D6 D5 D4 are equal to 0 0 0 1, the value of the internal contrast value can be read on D0-D3 at the falling edge of CS.

Set Temperature Coefficient

A temperature gradient selector circuit controlled by two control bits TC1 and TC2. This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

COMMAND TABLE

Bit Pattern	Command	Comment
$000000X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using X_1X_0 as address bits. X_1X_0=00 : page 1 (POR) X_1X_0=01 : page 2 X_1X_0=10 : page 3 X_1X_0=11 : page 4
$0001X_3X_2X_1X_0$	Set Contrast Level	Set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR.
$0001X_3X_2X_1X_0$	Read Contrast Value	With D/$\overline{C}$ pin input Low, R/$\overline{W}$ pin input high, and D7 D6 D5 D4 pins equal to 0001 at the rising edge of $\overline{CS}$, the value of the internal contrast register will be latched out at D3 D2 D1 D0 pins, i.e. $X_3X_2X_1X_0$, at the rising edge of $\overline{CS}$.
$0010000X_0$	Set Voltage Doubler / Tripler	X_0=0: Select Voltage Tripler (POR) X_0=1: Select Voltage Doubler
$0010001X_0$	Set Column Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg119
$0010010X_0$	Set Row Mapping	With duty cycle is 1/32 X_0=0 : Row0 to Com0 (POR) X_0=1: Row0 to Com31
$0010011X_0$	Reserved	
$0010100X_0$	Set Display On/Off	X_0=0: display off (POR) X_0=1: display on
$0010101X_0$	Set Internal DC/DC Converter On/Off	X_0=0: Internal DC/DC Converter off (POR) X_0=1: Internal DC/DC Converter on
$0010110X_0$	Set Internal Regulator On/Off	X_0=0: Internal Regulator off (POR) X_0=1: Internal Regulator on When the application employs external contrast control, the internal contrast control, temperature compensation and the Regulator must be enabled.
$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: Internal Voltage Divider off (POR) X_0=1: Internal Voltage Divider on When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0: Internal Contrast Control off (POR) X_0=1: Internal Contrast Control on Internal contrast circuits can be disabled if external contrast circuits is preferred.
$0011001X_0$	Set Clock Frequency	X_0=0 : low frequency (38.4kHz) (POR) X_0=1 : high frequency (50kHz)
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
$0011011X_0$	Master Clear GDDRAM	Master clear entire GDDRAM
$0011100X_0$	Set Bias Ratio	X_0=0: set 1/7 bias (POR) X_0=1: set 1/5 bias
$0011101X_0$	Reserved.	X_0=0: normal operation (POR) X_0=1: test mode (Note: Make sure to set X_0=0 during application)
$010X_4X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_4X_3X_2X_1X_0$ as number of lines to scroll. Scroll value = 0 upon POR
$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00: select annunciator 1 (POR) A_1A_0=01: select annunciator 2 A_1A_0=10: select annunciator 3 A_1A_0=11: select annunciator 4 X_0=0: turn selected annunciator off (POR) X_0=1: turn selected annunciator on

Bit Pattern	Command	Comment
$0110100X_0$	Set Duty Cycle	X_0=0: 1/32 duty and tripler enabled (POR) X_0=1: 1/16 duty and doubler enabled
$0110101X_0$	Reserved	X_0=0: Reserved X_0=1: Reserved
$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=00: 0.00% (POR) X_1X_0=01: -0.18% X_1X_0=10: -0.22% X_1X_0=11: -0.35%
$0111000X_0$	Increase / Decrease Contrast Value	X_0=0: Decrease by one level X_0=1: Increase by one level (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.
$0111001X_0$	Reserved	
$0111010X_0$	Reserved	
$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Make sure to set X_0=0 during application)
$0111100X_0$	Reserved	
$0111101X_0$	Set Internal / External Oscillator	X_0=0: internal oscillator(POR) X_0=1: external oscillator Internal oscillator circuit is automatically enabled if resistors are placed at OSC1 and OSC2. For external oscillator, simply feed clock in OSC2.
$0111110X_0$	Reserved	
$0111111X_0$	Set Oscillator Disable / Enable	X_0=0: disable oscillator (POR) X_0=1: enable oscillator. This is the master control fro oscillator circuitry. This command should be issued after the “Set External / Internal Oscillator” command.
$1X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits.

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$ pin and D/$\overline{C}$ pin. Data is valid at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to R/$\overline{W}$ pin and High to D/$\overline{C}$ pin. Data is latched at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the “Commands Required for R/W Actions on RAM” Table)

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Command	No	*1
1	0	Write Data	Yes	*2
1	1	Read Data	Yes	

Address Increment is done automatically data read write. The column address pointer of GDDRAM[*3] is affected.

Remarks : *1. Refer to the command “Read Contrast Value”.
*2. If write data is issued after Command Clear RAM, Address increase is not applied.
*3. Column Address will be wrapped round when overflow.

Power Up Sequence (Commands Required)

Command Required	POR Status	Remarks
Set Clock Frequency	Low	*1
Set Oscillator Enable	Disable	
Set Annunciator Control Signals	All annuciators off	*1
Set Duty Cycle	1/32 duty	*1
Set Bias Ratio	1/7 bias	*1
Set DC/DC Converter On	Off	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast Control On	Off	*1, *3
Increase Contrast Value	Contrast Value = 0	*1, *2, *3
Set Internal Voltage Divider On	Off	
Set Segment Mapping	Seg. 0 = Col. 0	
Set Common Mapping	Com. 0 = Row 0	
Set Vertical Scroll Value	Scroll Value = 0	
Set Display On	Off	

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Regulator is enabled.

Commands Required for Display Mode Setup

Display Mode	Commands Required	
Display Mode	Set External / Internal Oscillator, Set Oscillator Enable, Set Display On.	($0111101X_0$)* (01111111)* (00101001)*
Annunciator Display	Set External / Internal Oscillator, Set Oscillator Enable, Set Annunciator Control Signals.	($0111101X_0$)* (01111111)* ($01100A_1A_0X_0$)*
Standby Mode 1.	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*
Standby Mode 2.	Set External Oscillator, Set Annunciator Control Signals, Set Display Off, Set Oscillator Enable.	(01111101)* ($01100A_1A_0X_0$)* (00101000)* (01111111)*
Standby Mode 3.	Set Internal Oscillator, Set Annunciator Control Signals, Set Display Off, Set Oscillator Enable.	(01111100)* ($01100A_1A_0X_0$)* (00101000)* (01111111)*

Other Related Command with Display Mode : Set Duty Cycle, Set Column Mapping, Set Row Mapping, Set Vertical Scroll Value.

Commands Related to Voltage Generator :
Set Oscillator Disable/Enable, Set Internal Regulator On/Off, Set Duty Cycle, Set Temperature Coefficient, Set Internal Contrast Control On/Off, Increase/Decrease Contrast Level, Set Internal Voltage Divider On/Off, Set Bias Ratio, Set Display On/Off, Set Reference Voltage Generator, Set VDD Reference, Set Contrast Level

* No need to resend the command again if it is set previously

Commands Required for R/W Actions on RAM

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	(000000X_1X_0)* (1$X_6X_5X_4X_3X_2X_1X_0$)* ($X_7X_6X_5X_4X_3X_2X_1X_0$)
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	(0011010X_0)
Increase GDDRAM Address.	Dummy Read Data	($X_7X_6X_5X_4X_3X_2X_1X_0$)
Master Clear GDDRAM	Master Clear GDDRAM Dummy Write Data	(00110110) ($X_7X_6X_5X_4X_3X_2X_1X_0$)

* No need to resend the command again if it is set previously .

Display Output Description by Working Example

This is an example of output pattern on the LCD panel. Figure 9b and 9c are data map of GDDRAM and the output pattern on the LCD display with different command enable.

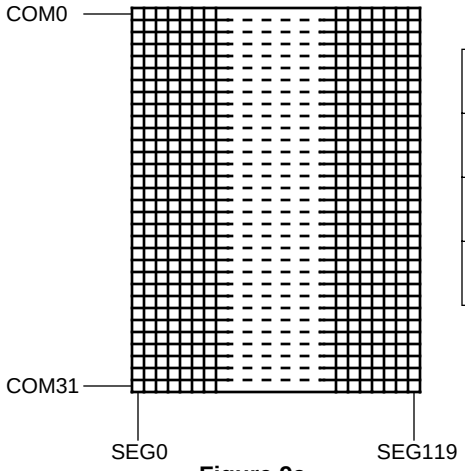
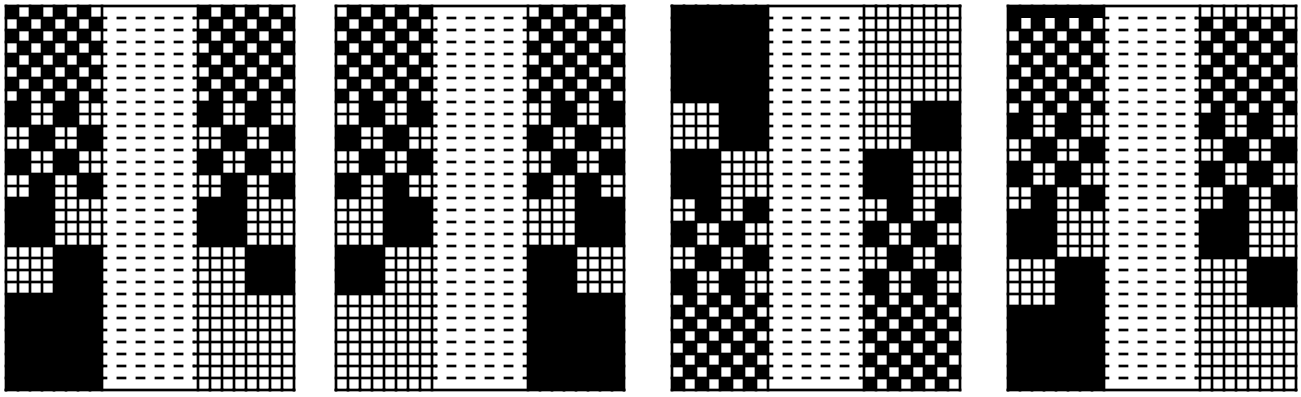


Figure 9a

		Content of GDDRAM
PAGE 1	Upper Nibble	5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
	Lower Nibble	5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
PAGE 2	Upper Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - - - - - C C 3 3 C C 3 3 C C
	Lower Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - - - - - C C 3 3 C C 3 3 C C
PAGE 3	Upper Nibble	0 0 0 0 F F F F 0 0 - - - - - - - - - - - - - F F 0 0 0 0 F F F F
	Lower Nibble	F F F F 0 0 0 0 F F - - - - - - - - - - - - - 0 0 F F F F 0 0 0 0
PAGE 4	Upper Nibble	F F F F F F F F 0 0 - - - - - - - - - - - - - F F 0 0 0 0 0 0 0 0
	Lower Nibble	F F F F F F F F 0 0 - - - - - - - - - - - - - F F 0 0 0 0 0 0 0 0

Figure 9b



Column remap disable
Row re-map disable

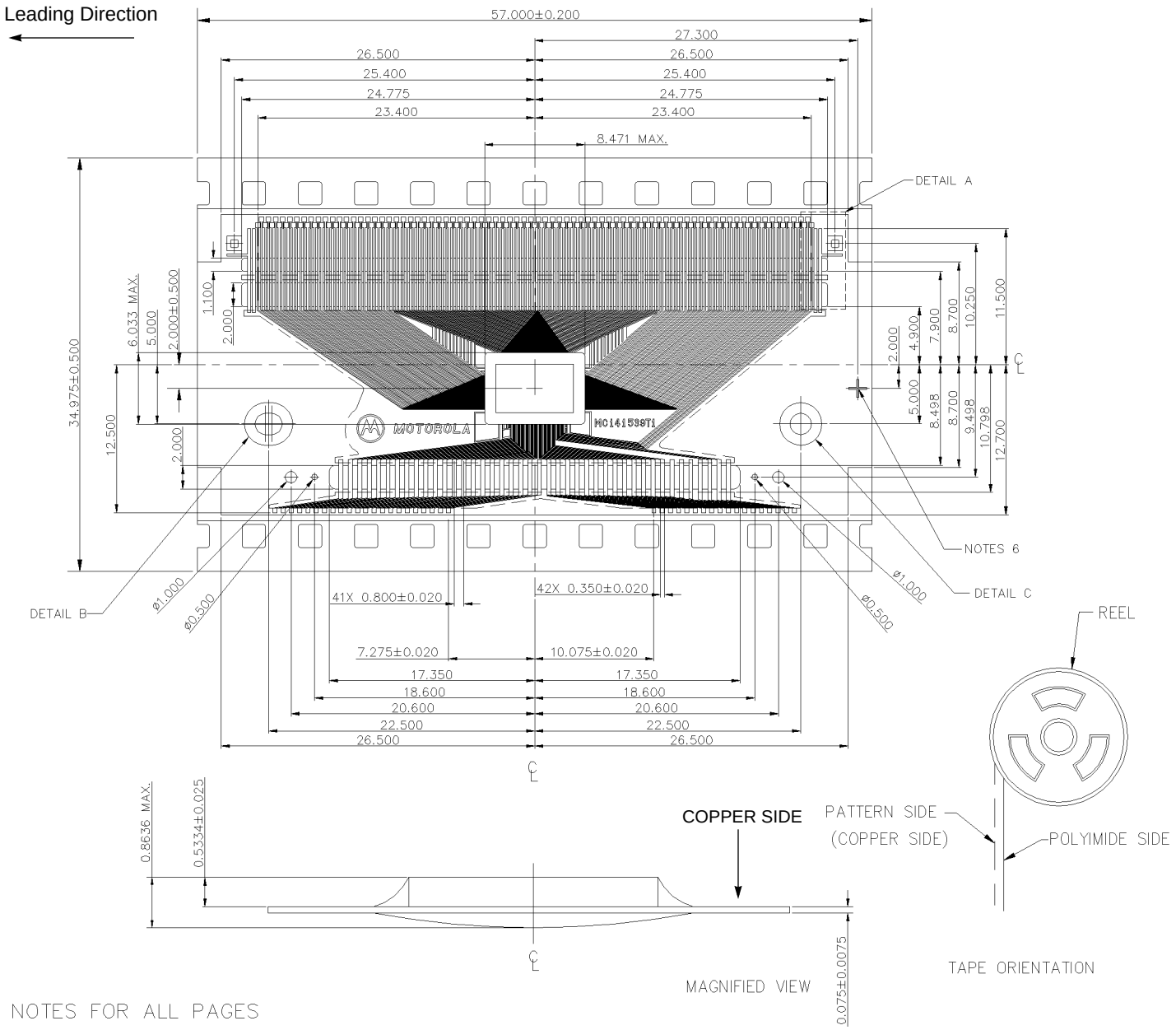
Column remap enable
Row re-map disable

Column remap disable
Row re-map enable

Column remap disable
Row re-map disable
Scroll Value = 31

Figure 9c. Examples of LCD display with different command enabled

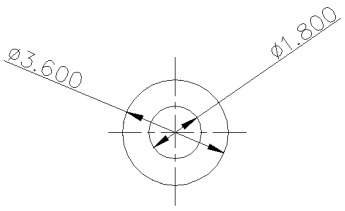
MC141539T1 TAB PACKAGE DIMENSION (1 OF 2)
98ASL00251A ISSUE 0
DO NOT SCALE THIS DRAWING



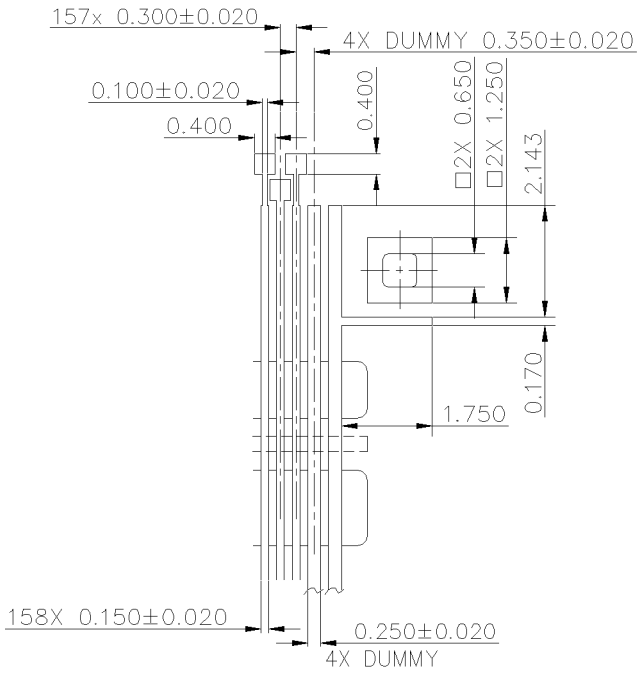
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø 2.0 MM HOLE.
7. 12 SPROCKET HOLES DEVICE

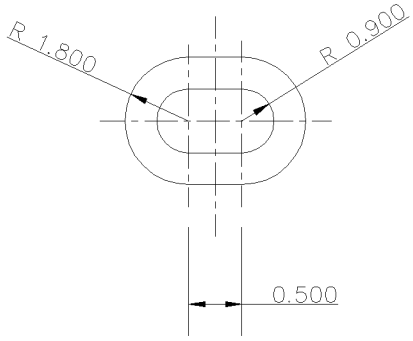
MC141539T1 TAB PACKAGE DIMENSION (2 OF 2)
98ASL00251A ISSUE 0
DO NOT SCALE THIS DRAWING



DETAIL C

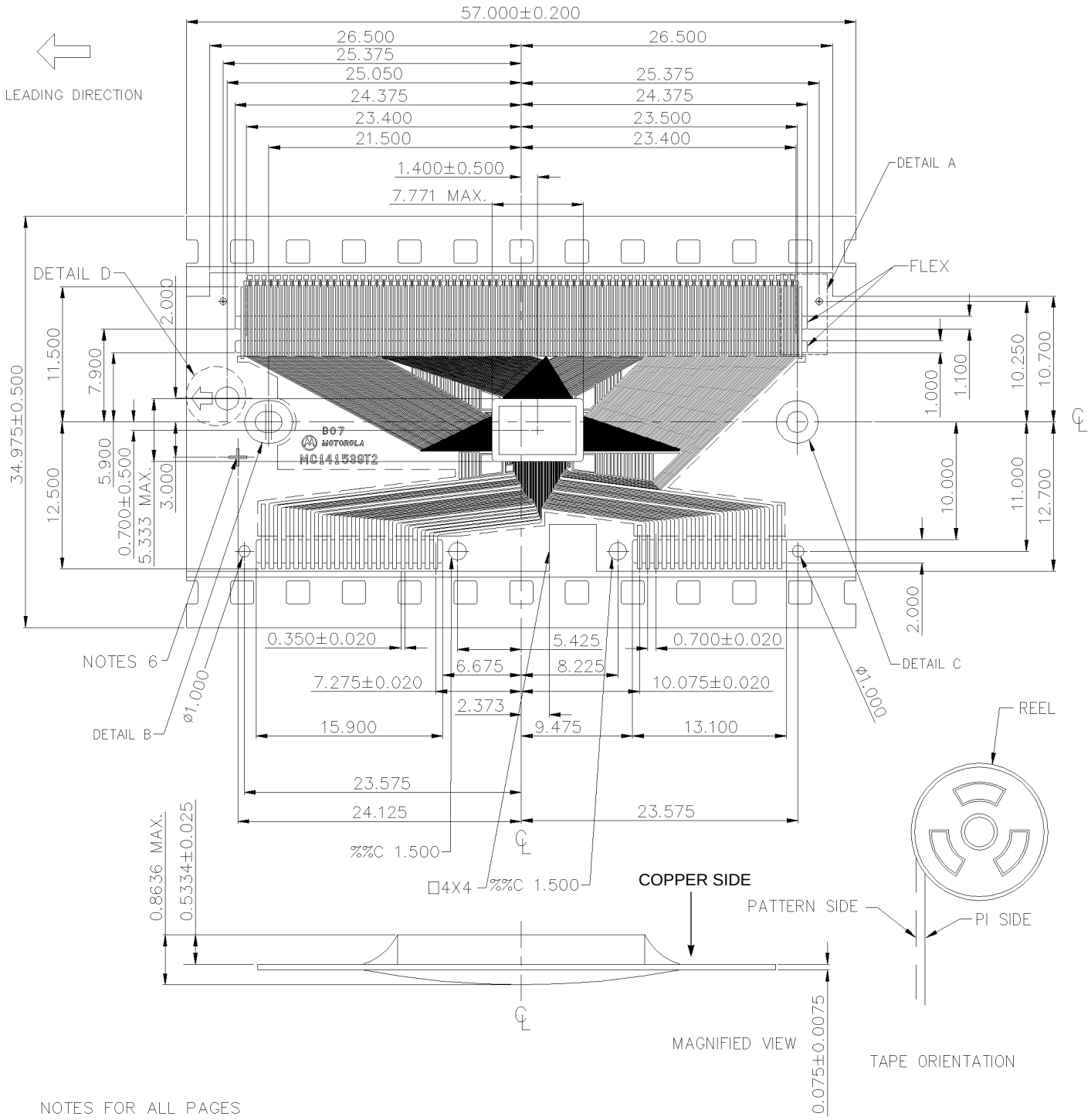


DETAIL A



DETAIL B

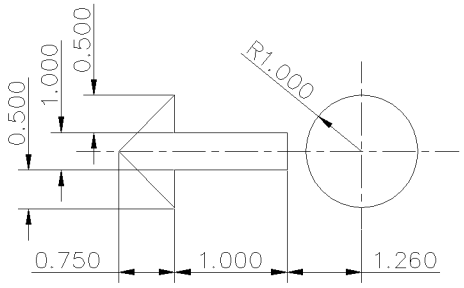
MC141539T2 TAB PACKAGE DIMENSION (1 OF 2)
98ASL00244A ISSUE 0
DO NOT SCALE THIS DRAWING



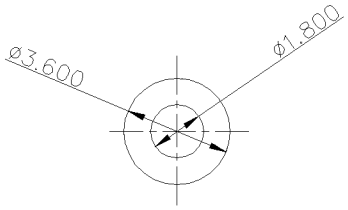
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø 2.0 MM HOLE.
7. 12 SPROCKET HOLES DEVICE

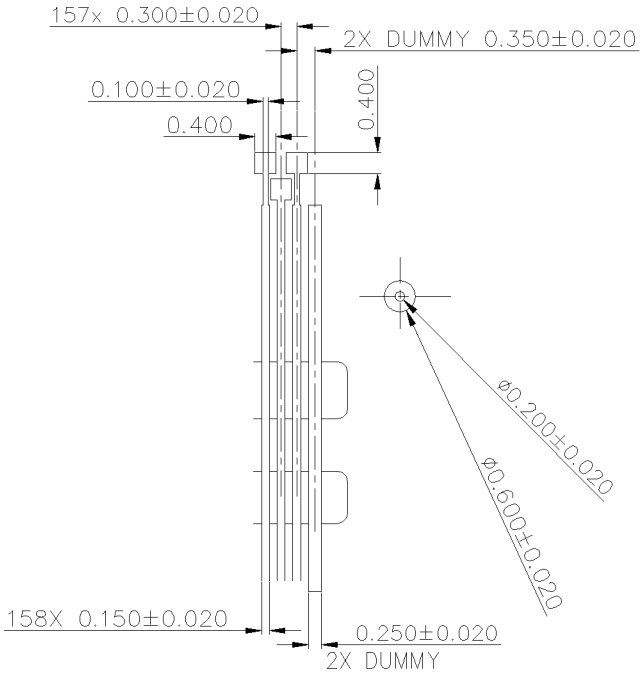
MC141539T2 TAB PACKAGE DIMENSION (2 OF 2)
98ASL00244A ISSUE 0
DO NOT SCALE THIS DRAWING



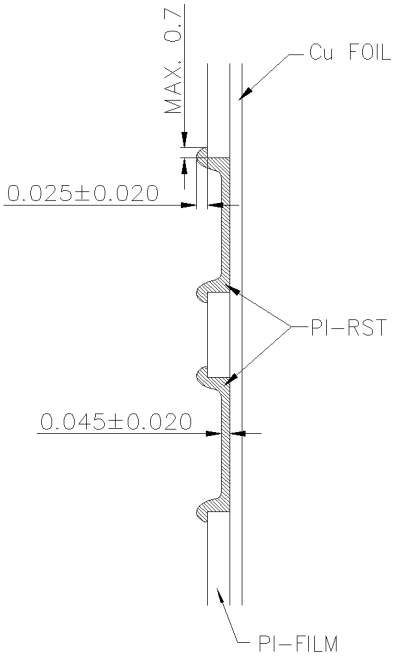
DETAIL D

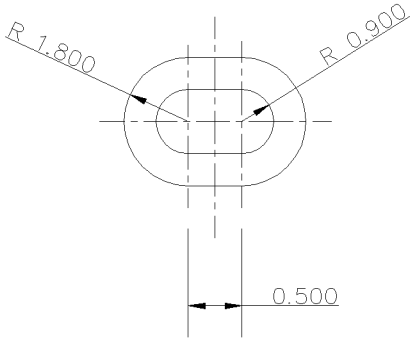


DETAIL C



DETAIL A



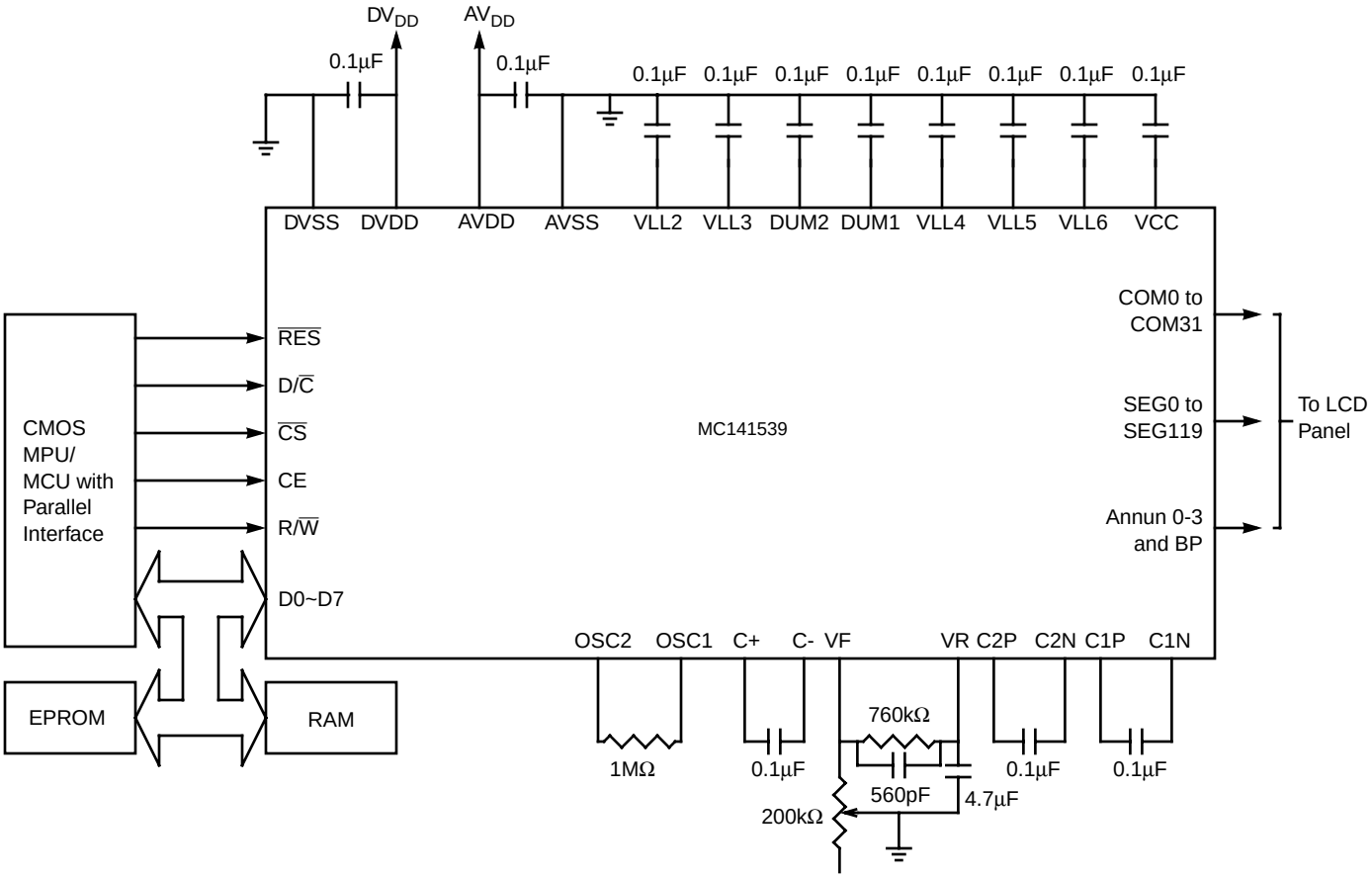


DETAIL B

FLEX MATERIAL DETAIL

Application Circuit

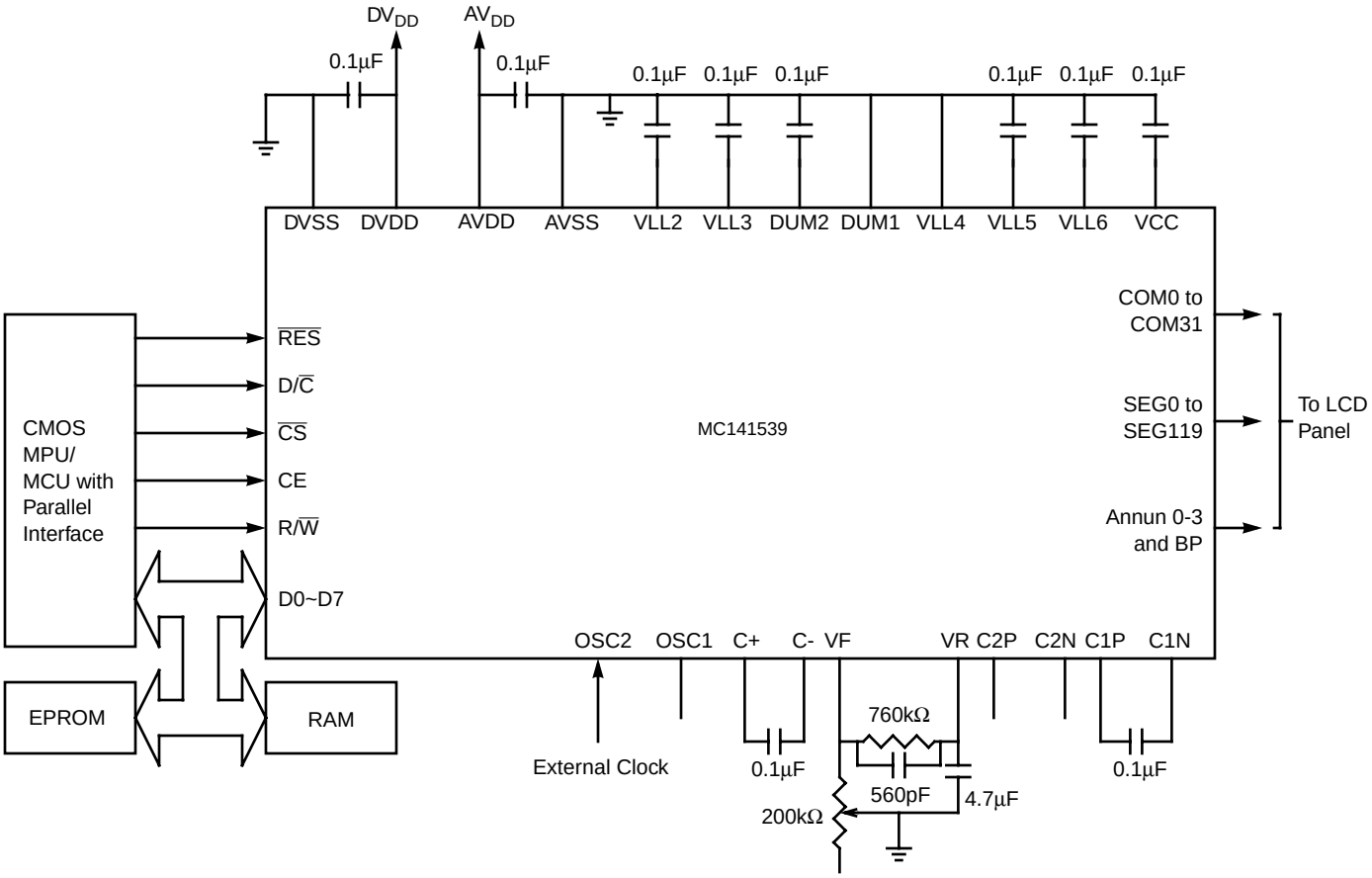
32 MUX Display with Analog Circuitry enabled, Tripler enabled and 1/7 bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Application Circuit

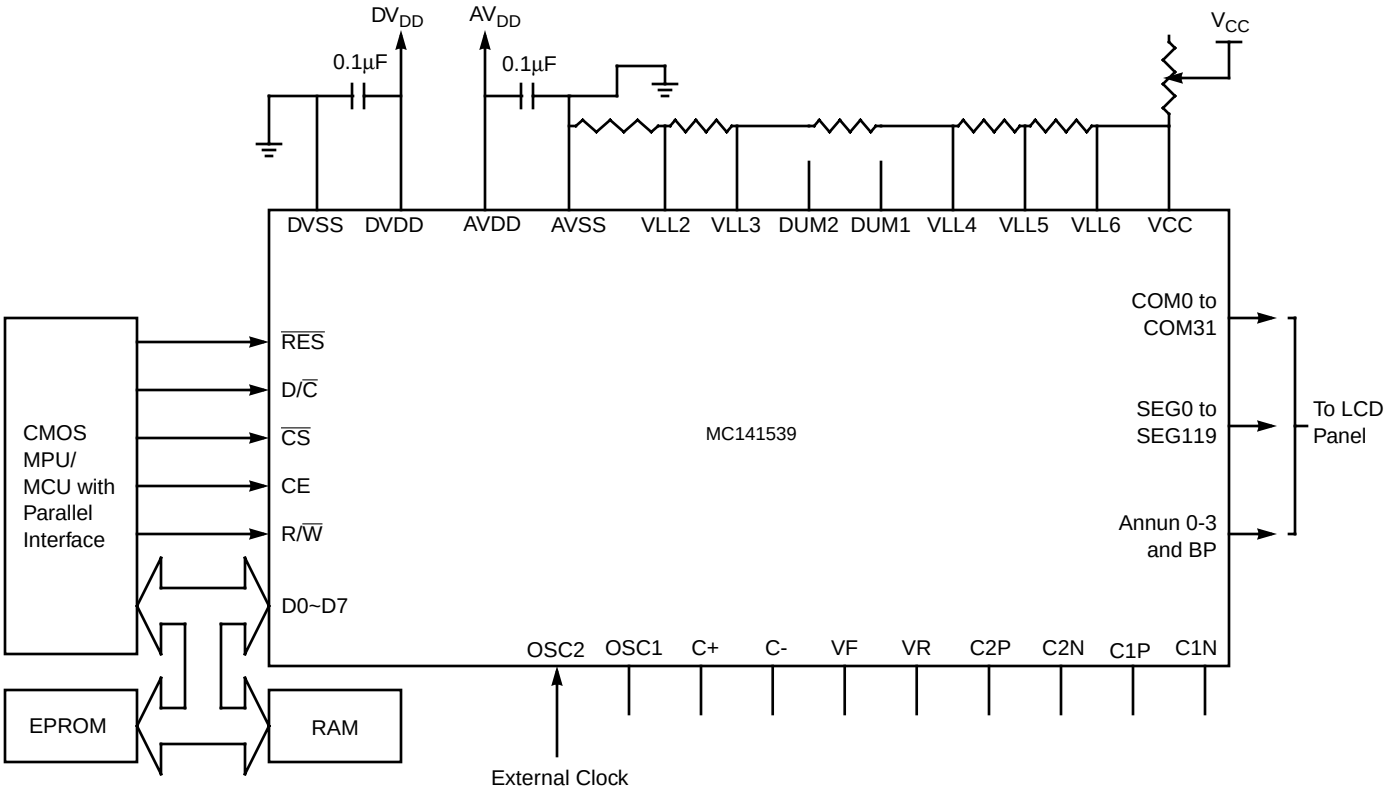
16 MUX Display with Analog Circuitry enabled, Tripler disabled and 1/5 bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Application Circuit

16/32 MUX Display with Analog Circuitry disabled



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.