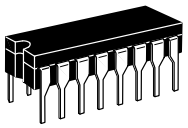
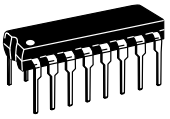
MC14569B

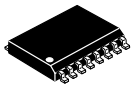
Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

T_A = – 55° to 125°C for all packages.

The MC14569B is a programmable divide–by–N dual 4–bit binary or BCD down counter constructed with MOS P–channel and N–channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase–locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

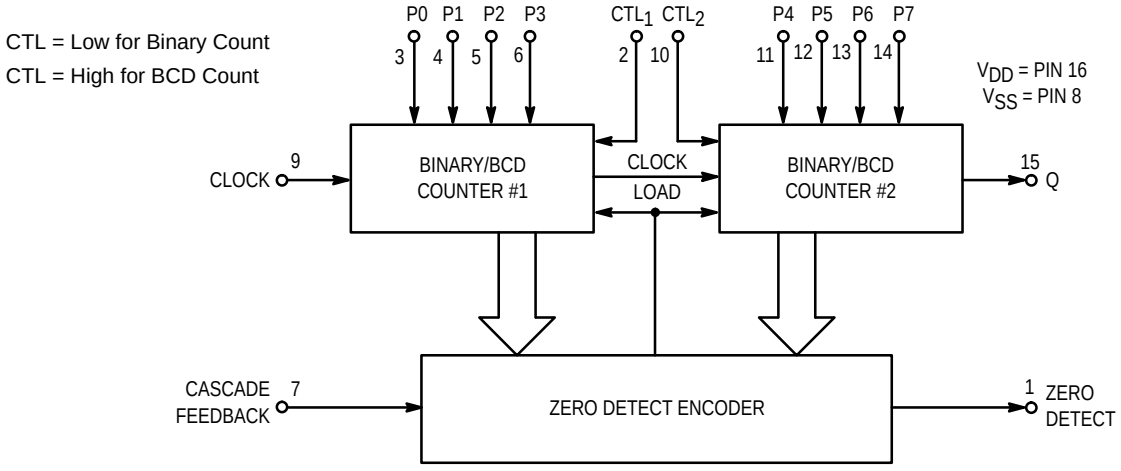
- Speed–up Circuitry for Zero Detection
- Each 4–Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14568B, MC14522B or MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.20 µA/kHz) f + I_{DD}							
		15	I_T = (1.95 µA/kHz) f + I_{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise Time	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn–On Delay Time Zero Detect Output	t_{PLH}	5.0 10 15	— — —	420 175 125	700 300 250	ns
Q Output		5.0 10 15	— — —	675 285 200	1200 500 400	ns
Turn–Off Delay Time Zero Detect Output	t_{PHL}	5.0 10 15	— — —	380 150 100	600 300 200	ns
Q Output		5.0 10 15	— — —	530 225 155	1000 400 300	ns
Clock Pulse Width	t_{WH}	5.0 10 15	300 150 115	100 45 30	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.5 9.5 13.0	2.1 5.1 7.8	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	NO LIMIT			µs

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

SWITCHING WAVEFORMS

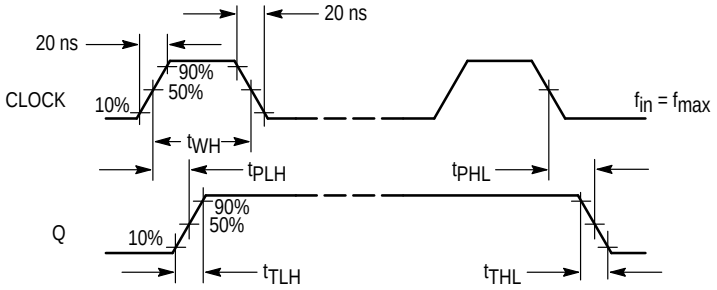


Figure 1.

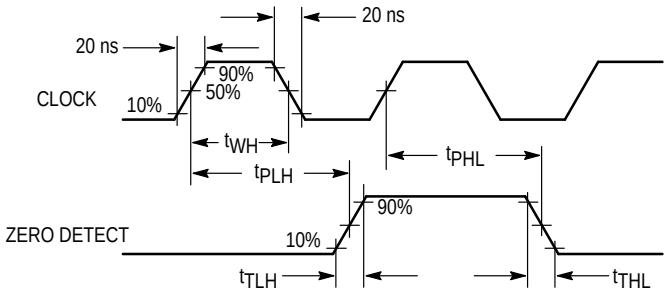


Figure 2.

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) — Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are “don’t cares.” Refer to Table 1 for output characteristics.

CTL_1 (Pin 2) — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL_2 (Pin 10) — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

V_{SS} (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

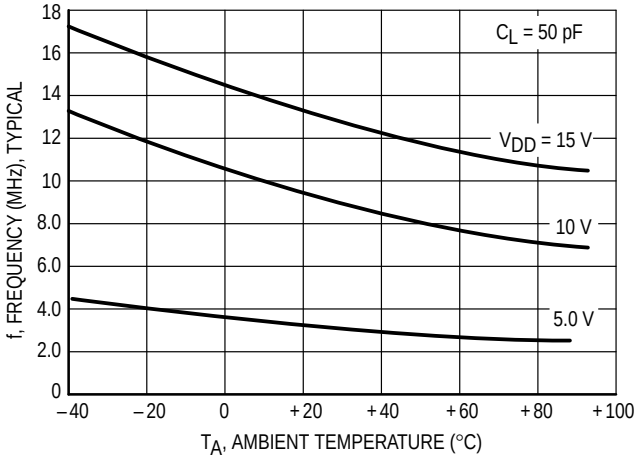
V_{DD} (Pin 16) — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

OPERATING CHARACTERISTICS

The MC14569B is a programmable divide–by–N dual 4–bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL_1 and CTL_2.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14568B, MC14522B or the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to “0”, Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V_{DD}.



PIN ASSIGNMENT

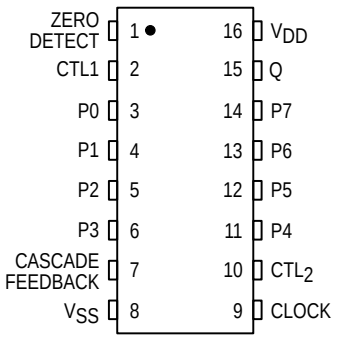


Table 1. Mode Controls (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL_1	CTL_2	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

NOTE: Data Preset Inputs (P0–P7) are “Don’t Cares” while Cascade Feedback is Low.

Table 2. Mode Controls (CTL_1 = Low, CTL_2 = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	1	0	0	0	136	136	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	1	1	1	255	255	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
128	64	32	16	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

Table 3. Mode Controls (CTL_1 = High, CTL_2 = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		
P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**Zero Detect**	**Q**	**Comments**
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	0	0	1	19	X	
0	0	1	0	0	0	0	0	20	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	0	0	0	0	0	60	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	0	0	0	0	150	150	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	0	0	1	159	159	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)

Table 4. Mode Controls (CTL_1 = Low, CTL_2 = High, Cascade Feedback = High)

Preset Values								Divide Ratio		
P7	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	**Zero Detect**	**Q**	**Comments**
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	48	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	1	0	0	0	0	80	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	1	1	0	0	0	0	112	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	144	144	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	1	1	1	159	159	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
128	64	32	16	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

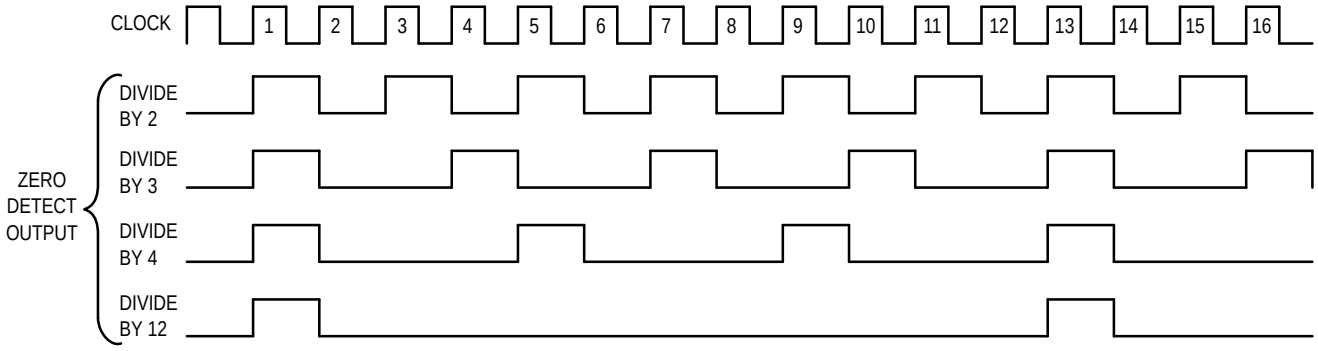
X = No Output (Always Low)

Table 5. Mode Controls (CTL_1 = High, CTL_2 = High, Cascade Feedback = High)

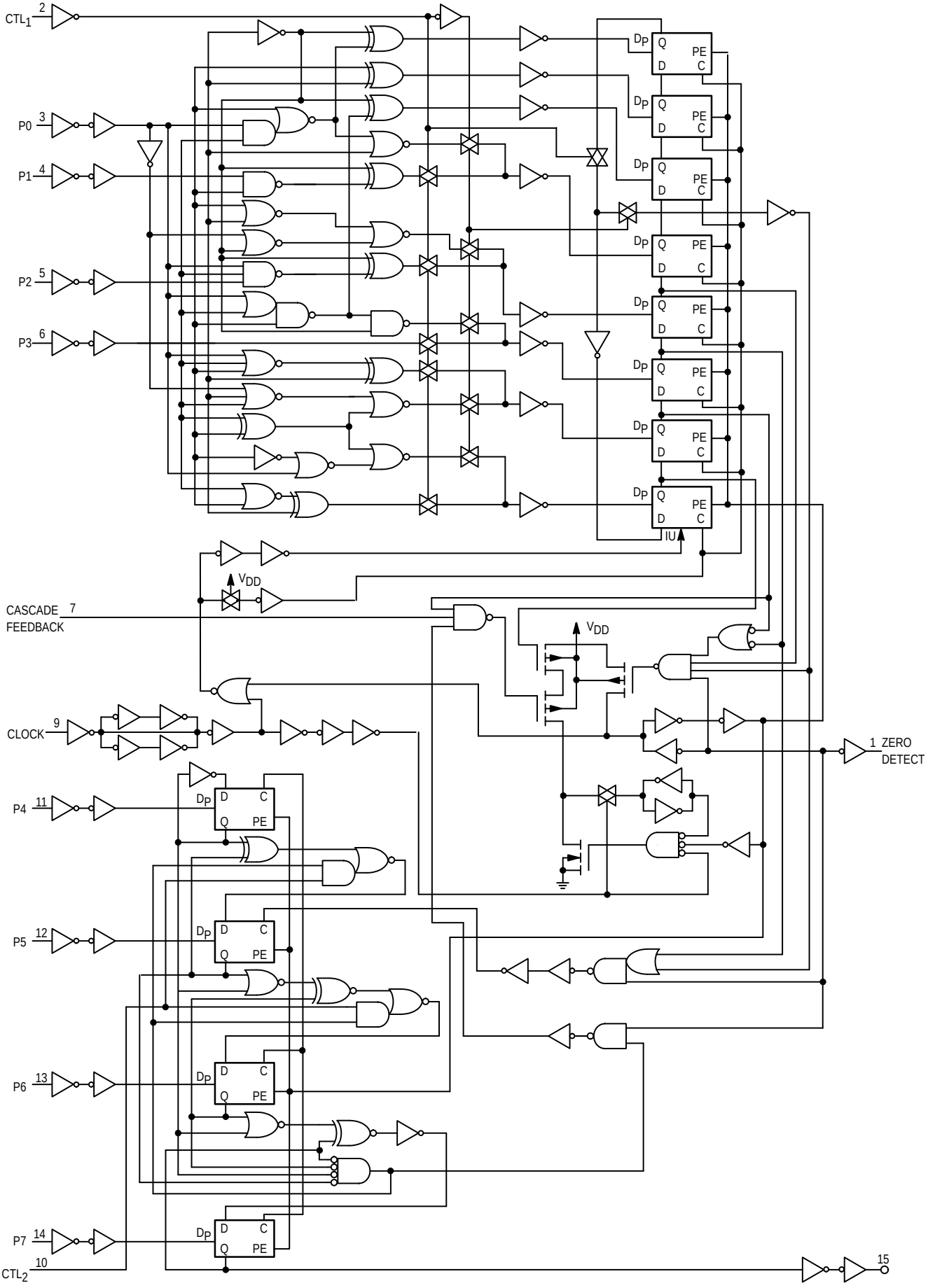
Preset Values								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	100	100	Max Count
0	0	0	0	0	0	0	1	X	X	illegal state
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	0	0	1	99	99	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)

TIMING DIAGRAM MC14569B



LOGIC DIAGRAM



TYPICAL APPLICATIONS

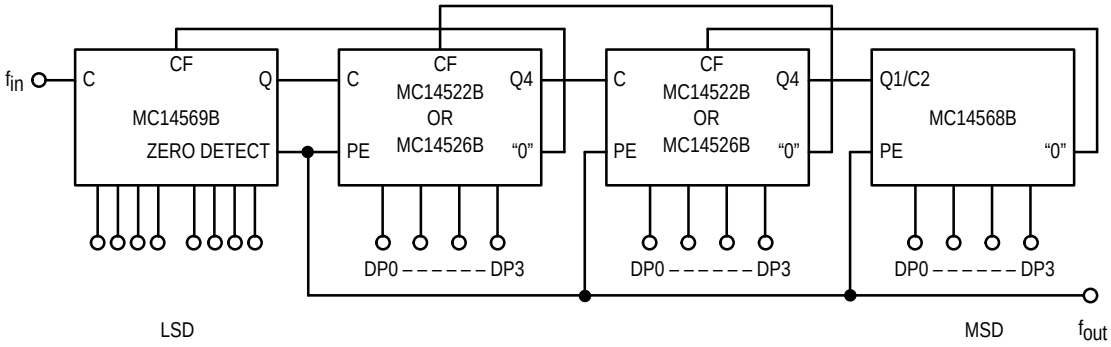


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

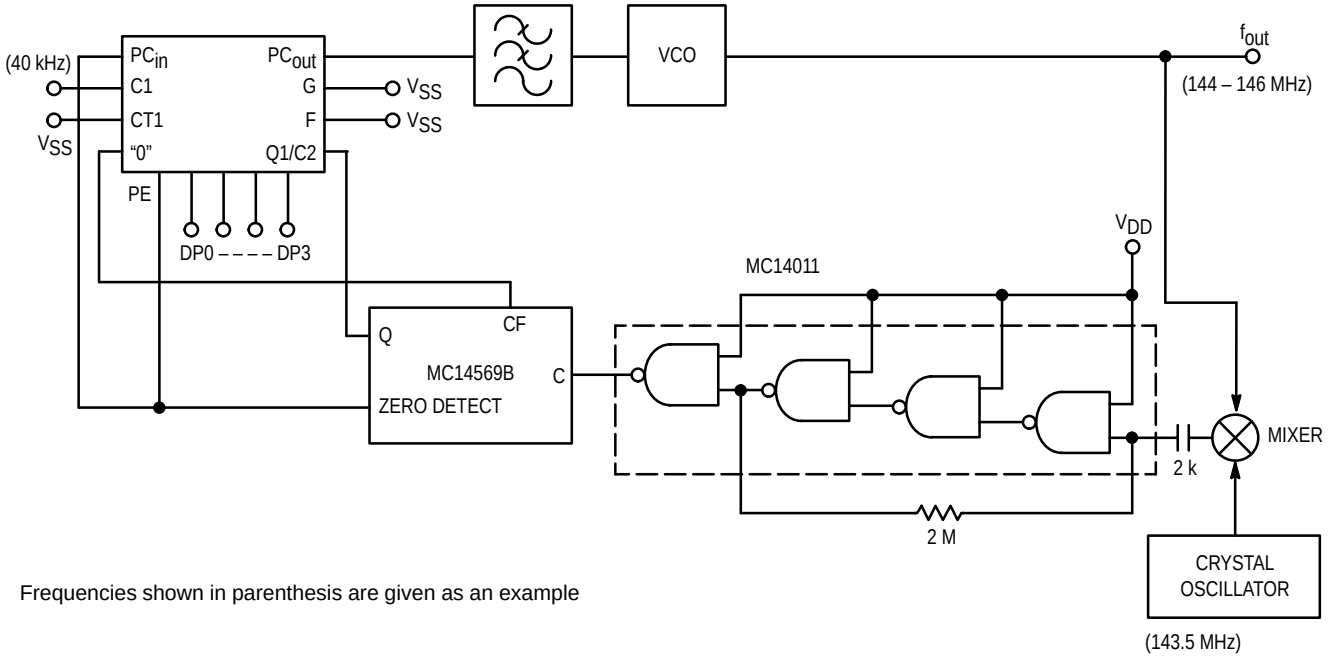
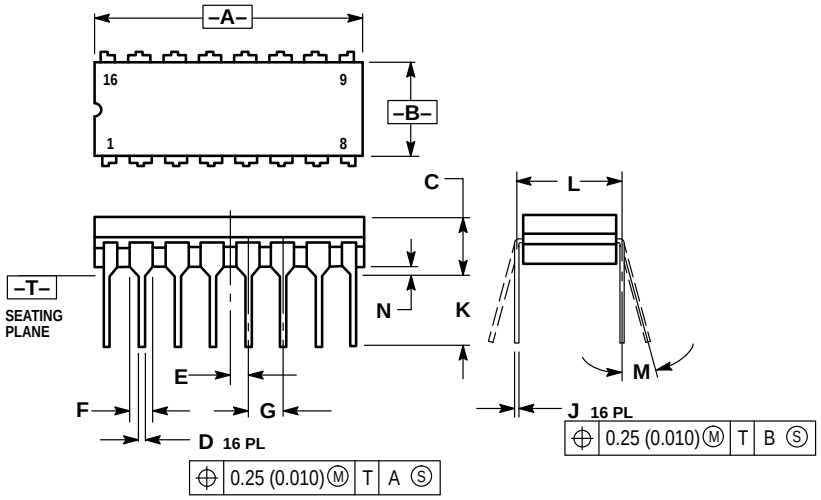


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

OUTLINE DIMENSIONS

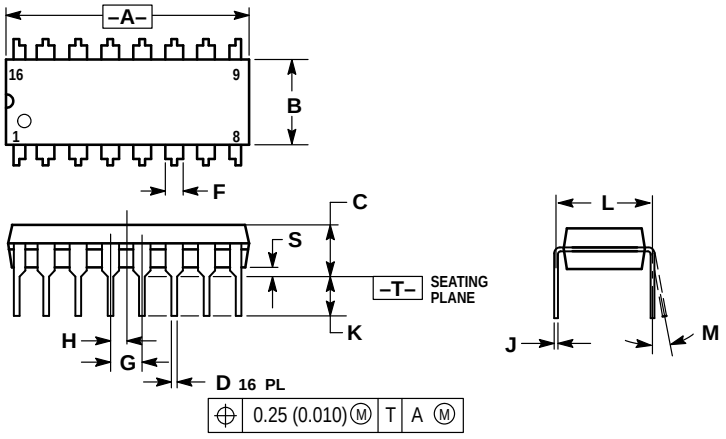
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

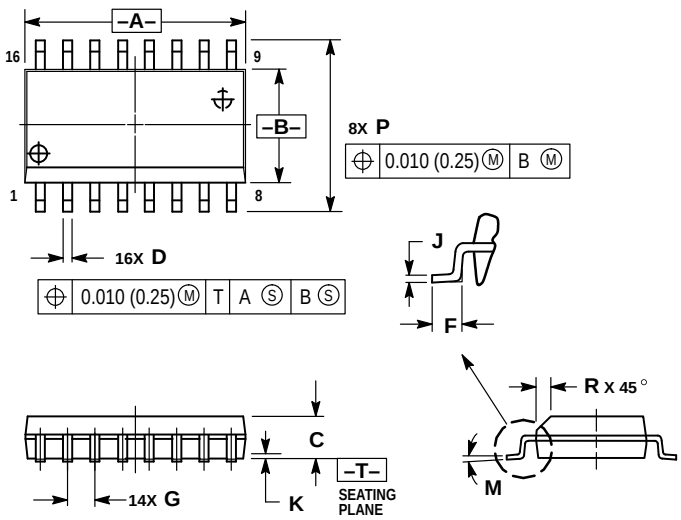


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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