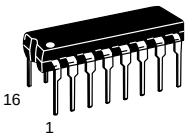
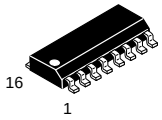
MC26C32

Product Preview

Quad EIA-422-A Line Receiver
CMOS



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC26C32P	Plastic DIP
MC26C32D	SOG Package

The MC26C32 is a quad differential line receiver designed for digital data transmission over balanced lines. The MC26C32 meets all the requirements of standard EIA–422–A while retaining the low–power characteristics of CMOS.

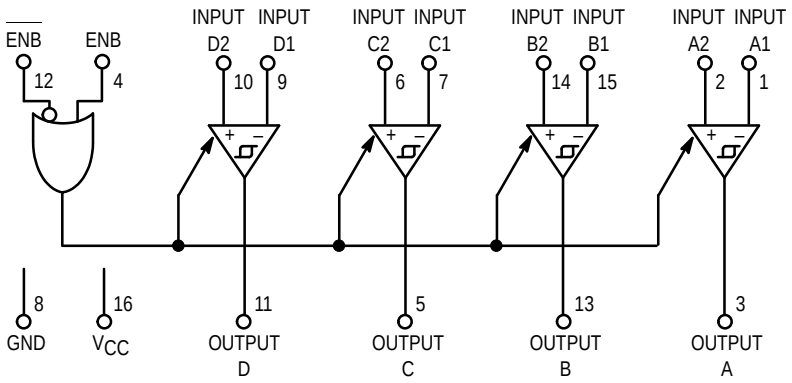
The MC26C32 has an input sensitivity of 200 mV over the common mode input voltage range of ± 7 V. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The MC26C32 is pin compatible with the AM26LS32.

All pins are protected against damage due to electrostatic discharges.

- Typical Power Supply Current: 6 mA
- 2000 V ESD Protection on the Inputs and Outputs
- Typical Propagation Delay: 18 ns
- Typical Input Hysteresis: 75 mV
- Meets the Requirements of Standard EIA–422–A
- Operation from Single 5 V Supply
- High Impedance Mode for Outputs Connected to System Buses
- TTL/CMOS Compatible Outputs

BLOCK DIAGRAM



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REV 4
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TRUTH TABLE

Control Inputs E/$\overline{E}$	Input	Output
L/H	X	Z
All other combinations of enable inputs	$V_{ID} \geq V_{TH}$ (max)	1
	$V_{ID} \geq V_{TH}$ (min)	0
	Open	1

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	± 10	V
Input Differential Voltage	V_{ID}	± 14	V
Enable Control Input Voltage	V_{in}	V_{CC} + 0.5	V
Storage Temperature	T_{stg}	– 65 to + 150	°C
Maximum Current per Output	I_O	± 25	mA
ESD (Human Body Model)		2000	V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
Operating Temperature Range	T_A	– 40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated) (See Note 1)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current, $V_{CC} \geq$ Max		I_{CC}	—	6	12	mA
Enable Input Current, $V_{in} = V_{CC}$ or GND		L_I	—	—	± 1.0	µA
Input Voltage — Low Logic State (Enable Control)		V_{IL}	—	—	0.8	V
Input Voltage — High Logic State (Enable Control)		V_{IH}	2	—	—	V
Differential Input Voltage, – 7 V < V_{LCM} < 7 V	$V_{out} = V_{OH}$ $V_{out} = V_{OL}$	V_{TH}	0.2 —	— —	— – 0.2	V
Input Hysteresis, V_{LCM} = 0 V		V_{hys}	—	75	—	mV
Comparator Input Current	V_{in} = + 10 V, Other Input = GND V_{in} = – 10 V, Other Input = GND	I_{in}	— —	1.4 – 2.5	— —	mA
Comparator Input Resistance, – 10 V < V_{LCM} < + 10 V		R_{in}	4	4.8	—	kΩ
Output Voltage (Low Logic State) V_{ID} = – 1 V, I_{out} = 6 mA (Note 2)		V_{OL}	—	0.13	0.33	V
Output Voltage (High Logic State) V_{ID} = + 1 V, I_{out} = – 6 mA (Note 2)		V_{OH}	3.8	4.8	—	V
Output Leakage Current (High Logic State) $V_{out} = V_{CC}$ or GND		I_{OZ}	– 5	—	5	µA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. See EIA specifications EIA–422–A for exact test conditions.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output, C_L = 50 pF, V_{DIFF} = 2.5 V	t_{PLH} t_{PHL}	—	18	30	ns
Skew = $\lvert t_{PHL} - t_{PLH} \rvert$	Skew	—	1	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PLZ} t_{PHZ}	—	12	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PZL} t_{PZH}	—	14	—	ns

* Skew: difference in propagation delays between complementary outputs.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

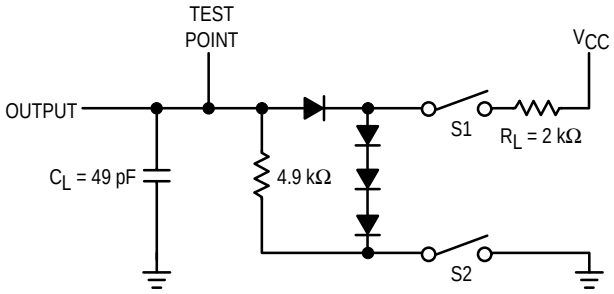


Figure 1. Test Circuit

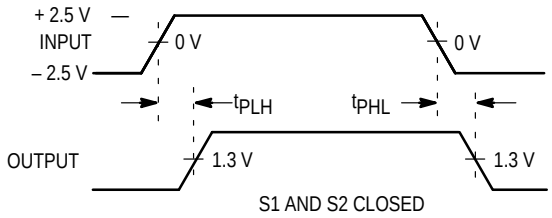


Figure 2. Propagation Delays

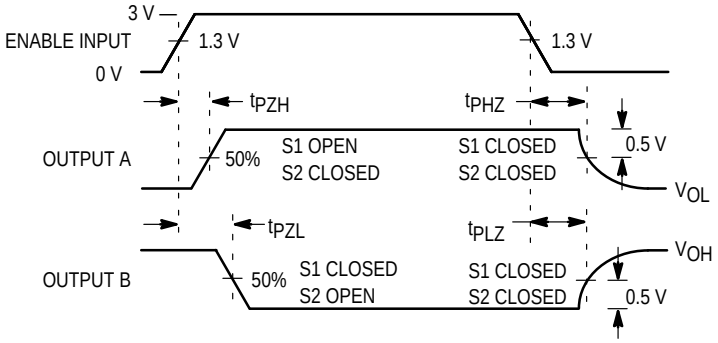


Figure 3. Enable and Disable Times

TYPICAL APPLICATIONS

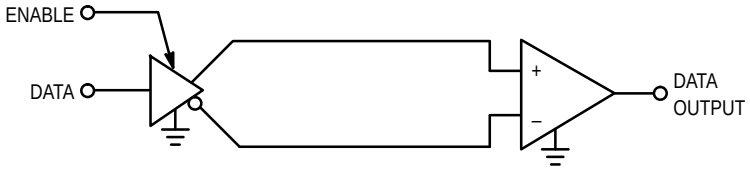
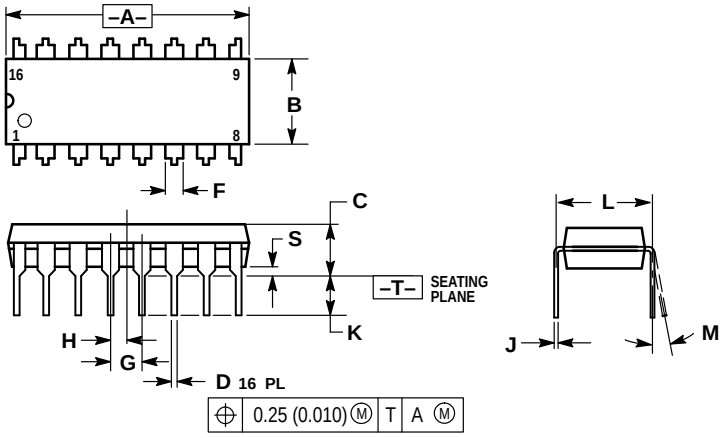


Figure 4. Two–Wire Balanced Systems (EIA–422–A)

PACKAGE DIMENSIONS

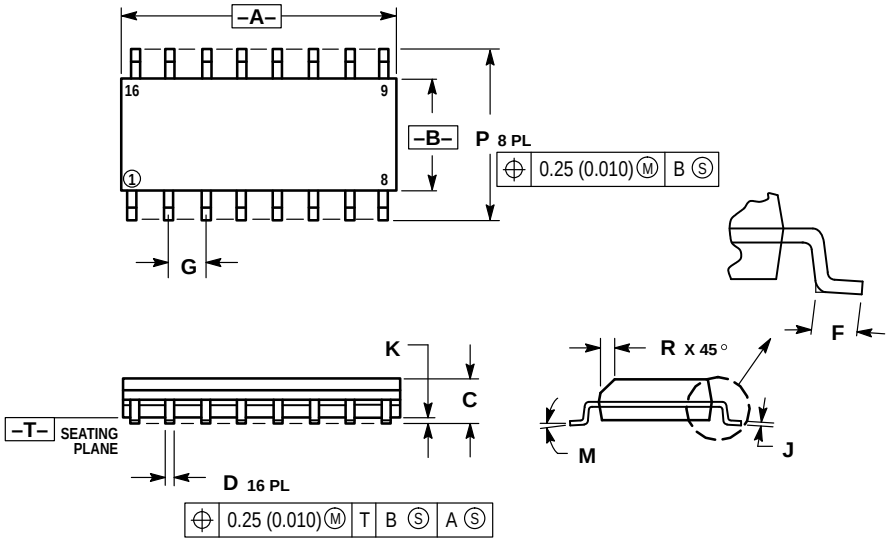
P SUFFIX
PLASTIC DIP
CASE 648–08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

D SUFFIX
SOG PACKAGE
CASE 751B–05



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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